

HA19209, HA19210

8-Bit Flash Type Analog-to-Digital Converter

Description

The HA19209/210 monolithic bipolar LSIs feature high speed 8-bit A/D conversion with low power dissipation. Digital data output and clock input terminals are compatible with TTL and CMOS. The device is designed for video signal processing applications.

Features

- 8-Bit resolution including overflow
- Low power dissipation: 250mW (typ)
- High speed
- Maximum conversion rate: 30MSPS (million samples per second)
- Single power supply: +5V
- Input clock level and digital output signal level compatible with TTL and CMOS (can drive one LS TTL IC)
- Needs no sample and hold circuit
- 28-pin package.

Applications

- Digital television set, digital video tape recorder
- High speed measuring instrumentation
- Industrial equipment with pattern recognition computer

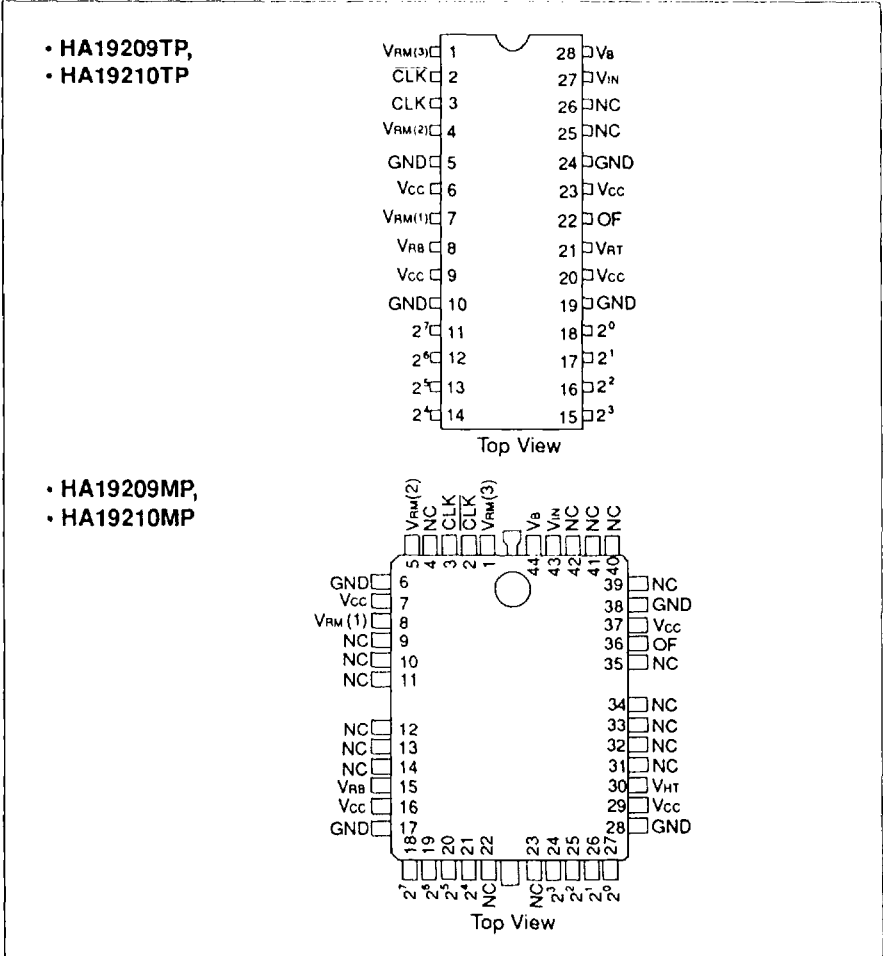
Table 1 shows the difference between HA19209 and HA19210.

Ordering Information

Type No.	Package
HA19209TP	600mil 28-pin plastic DIP (DP-28)
HA19209MP	44-pin plastic QFI (MP-44)
HA19210TP	600mil 28-pin plastic DIP (DP-28)
HA19210MP	44-pin plastic QFI (MP-44)



Pin Arrangement



Block Diagram

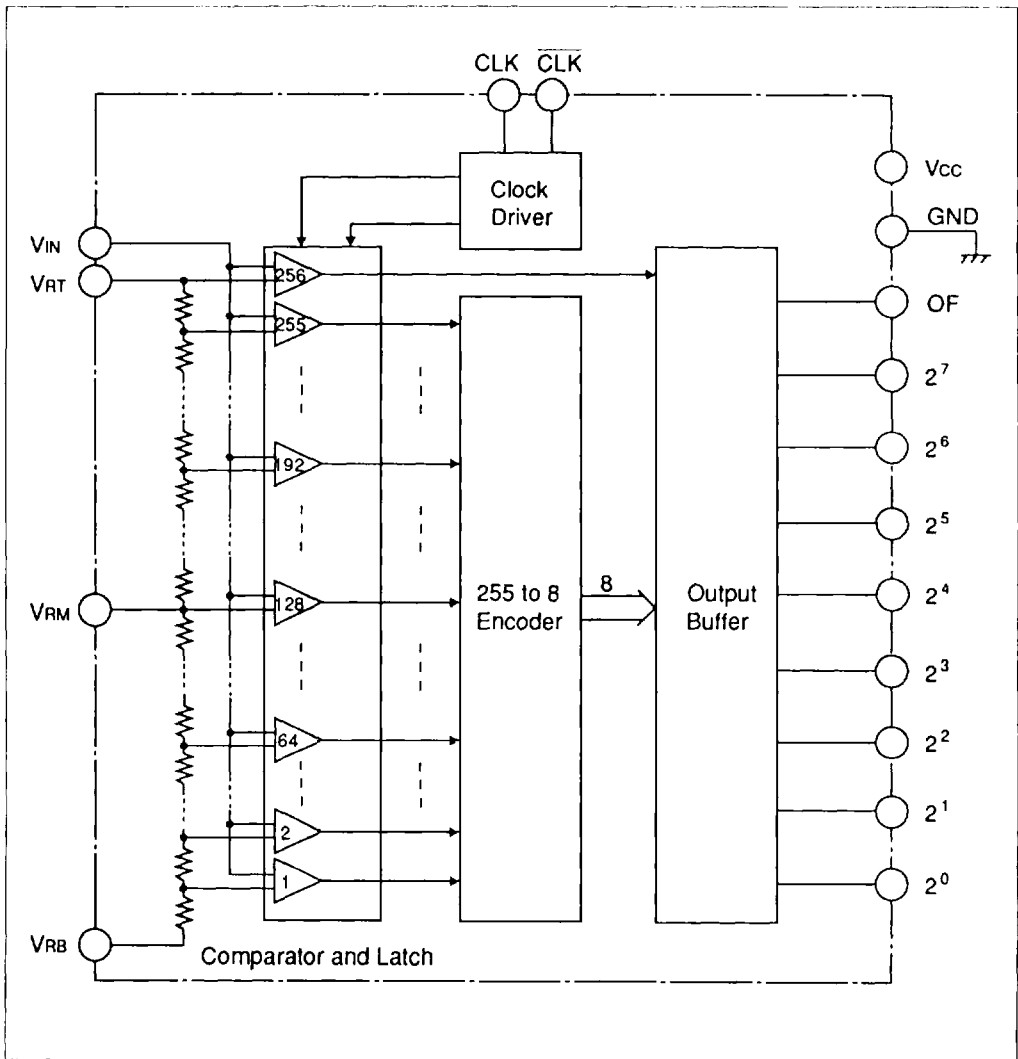


Table 1 Output Code Table

Input Voltage	HA19209						HA19210					
	OF	2 ⁷	2 ⁶	...	2 ¹	2 ⁰	OF	2 ⁷	2 ⁶	...	2 ¹	2 ⁰
V _{RB}	0	0	0	...	0	0	0	0	0	...	0	0
V _{RB} + 1 LSB	0	0	0	...	0	1	0	0	0	...	0	1
V _{RB} + 2 LSB	0	0	0	...	1	0	0	0	0	...	1	0
⋮	⋮	⋮	⋮	...	⋮	⋮	⋮	⋮	⋮	...	⋮	⋮
V _{RB} + 127 LSB	0	0	1	...	1	1	0	0	1	...	1	1
V _{RB} + 128 LSB	0	1	0	...	0	0	0	1	0	...	0	0
⋮	⋮	⋮	⋮	...	⋮	⋮	⋮	⋮	⋮	...	⋮	⋮
V _{RT} - 2 LSB	0	1	1	...	1	0	0	1	1	...	1	0
V _{RT} - 1 LSB	0	1	1	...	1	1	0	1	1	...	1	1
V _{RT}	1	1	1	...	1	1	1	0	0	...	0	0



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Pin Description (HA19209TP/HA19210TP)

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	$V_{RM}(3)$	Reference Voltage Correcting Input	15	2^3	Digital Output Pin
2	\overline{CLK}	Clock Input Pin Inversed Phase	16	2^2	Digital Output Pin
3	CLK	Clock Input Pin	17	2^1	Digital Output Pin
4	$V_{RM}(2)$	Reference Voltage Correcting Input	18	2^0	Digital Output (LSB) Pin
5	GND	Ground Pin	19	GND	Ground Pin
6	Vcc	Power Supply Pin (+5V)	20	Vcc	Power Supply (+5V)
7	$V_{RM}(1)$	Reference Voltage Correcting input	21	V_{RT}	High level Reference Input Pin
8	V_{RB}	Low Level Reference Input Pin	22	OF	Overflow Output Pin
9	Vcc	Power Supply Pin (+5V)	23	Vcc	Power Supply Pin (+5V)
10	GND	Ground Pin	24	GND	Ground Pin
11	2^7	Digital Output (MSB) Pin	25	NC	Non Connection Pin
12	2^6	Digital Output Pin	26	NC	Non Connection Pin
13	2^5	Digital Output Pin	27	V_{IN}	Analog Input Pin
14	2^4	Digital Output Pin	28	V_B	Connected to Vcc with 100k Ω



Pin Description (HA19209MP/HA19210MP)

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	V _{RM(3)}	Reference Voltage Correcting Input	23	NC	Non Connection Pin
2	$\overline{\text{CLK}}$	Clock Input Pin Inversed Phase	24	2 ³	Digital Output Pin
3	CLK	Clock Input Pin	25	2 ²	Digital Output Pin
4	NC	Non Connection Pin	26	2 ¹	Digital Output Pin
5	V _{RM(2)}	Reference Voltage Correcting input	27	2 ⁰	Digital Output (LSB) Pin
6	GND	Ground Pin	28	GND	Ground Pin
7	V _{CC}	Power Supply Pin (+5V)	29	V _{CC}	Power Supply Pin (+5V)
8	V _{RM(1)}	Reference Voltage Correcting Input	30	V _{RT}	High Level Reference Input Pin
9	NC	Non Connection Pin	31	NC	Non Connection Pin
10	NC	Non Connection Pin	32	NC	Non Connection Pin
11	NC	Non Connection Pin	33	NC	Non Connection Pin
12	NC	Non Connection Pin	34	NC	Non Connection Pin
13	NC	Non Connection Pin	35	NC	Non Connection Pin
14	NC	Non Connection Pin	36	OF	Overflow Output Pin
15	V _{RB}	Low Level Reference Input Pin	37	V _{CC}	Power Supply Pin (+5V)
16	V _{CC}	Power Supply Pin (+5V)	38	GND	Ground Pin
17	GND	Ground Pin	39	NC	Non Connection Pin
18	2 ⁷	Digital Output (MSB) Pin	40	NC	Non Connection Pin
19	2 ⁶	Digital Output Pin	41	NC	Non Connection Pin
20	2 ⁵	Digital Output Pin	42	NC	Non Connection Pin
21	2 ⁴	Digital Output Pin	43	V _{IN}	Analog Input Pin
22	NC	Non Connection Pin	44	V _B	Connected to V _{CC} with 100kΩ



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Absolute Maximum Ratings (Ta=25°C, unless otherwise specified)

Item	Symbol	Rating	Unit
Supply Voltage	V _{CC}	+7.0	V
Input Signal Voltage *1	V _{in}	0 to V _{CC}	V
Reference Input Terminal Voltage *1	V _R	0 to V _{CC}	V
Clock Input Voltage *2	V _{CLK}	0 to V _{CC}	V
Power Dissipation	P _T	800	mW
Operating Temperature Range	T _{opr}	0 to +70	°C
Storage Temperature Range	T _{stg}	-55 to +125	°C

Notes: *1. V_{in} and V_R should not be lower than 1.2V at the same time.

*2. V_{CLK} and $\overline{V_{CLK}}$ should not be lower than 1.5V at the same time.

Electrical Characteristics (Ta=25°C, V_{CC}=5V, V_{RT}=3.5V, V_{RB}=1.5V, unless otherwise specified)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	
Resolution		8	8	8	bits	V _{CC} =5.0V	
Supply Voltage Range	V _{CC}	4.75	5.0	5.25	V		
Reference Terminal	RT	V _{RT}	V _{RB}	3.5	V _{CC} - 0.9	V	V _{CC} =5.0V
Voltage Range	RB	V _{RB}	1.2	1.5	V _{RT}	V	V _{CC} =5.0V
	RM	V _{RM}	2.4	2.5	2.6	V	Only for Reference Voltage Correction
Input Signal Voltage Range	V _{in}	V _{RB} - 0.1	—	V _{RT} - 0.1	V	V _{CC} =5.0V	
Input Dynamic Range	V _{RT} - V _{RB}	—	2.0	2.1	V _{p-p}		
Supply Current	I _{CC}	—	50	90	mA	V _{CC} =5.0V, f _{CLK} =20Msps	
Reference Terminal	RT	I _{RT}	—	11	16.6	mA	
Voltage Range	RB	I _{RB}	-16.6	-11	—	mA	
Input Current	I _{in}	—	70	200	μA	V _{in} =4.1V	
Input Capacitance	C _{in}	—	40	—	pF	f _{IN} =1MHz, V _{RB} <V _{in} <V _{RT}	
High Level Digital Output Voltage	V _{OH1}	3.8	4.2	—	V	I _{OH} =-400μA	
	V _{OH2}	3.5	4.0	—	V	I _{OH} =-5mA	
Low Level Digital Output Voltage	V _{OL}	—	0.6	0.75	V	I _{OL} =400μA	
Clock Input Current	I _i	-100	—	100	μA	V _{CLK} : 0V to 2.7V	



Electrical Characteristics (Ta=25°C, VCC=5V, VRT=3.5V, VRB=1.5V, unless otherwise specified) (cont)

High Level Clock Input Voltage	V _{IH}	2.0	—	V _{CC}	V	
Low Level Clock Input Voltage	V _{IL}	0	—	0.8	V	
Static Linearity	Differential	D.N.L.	-0.5	—	+0.5	LSB Figure 3-5
Error	Integral	I.N.L	—	—	2.0	LSB _{p-p}
Maximum Conversion Rate	f _{CLK max.}	20	30	—	Msp/s	f _{in} =3.58MHz (figure 3-5)
Differential Gain	DG	—	1.0	—	%	f _{CLK} =20Msp/s,
Differential Phase	DP	—	0.5	—	Degree	NTSC, 40IRE Unlocked (figure 3-5)
Clock Pulse Width	t _{WH}	30	35	—	ns	f _{CLK} =20Msp/s
	t _{WL}	10	15	—	ns	
Digital Output Propagation Delay	t _{PD}	23	28	33	ns	
Digital Output Rise Time	t _{TLH}	—	8	10	ns	R _L =2kΩ, C _L =10pF
Digital Output Fall Time	t _{THL}	—	20	24	ns	

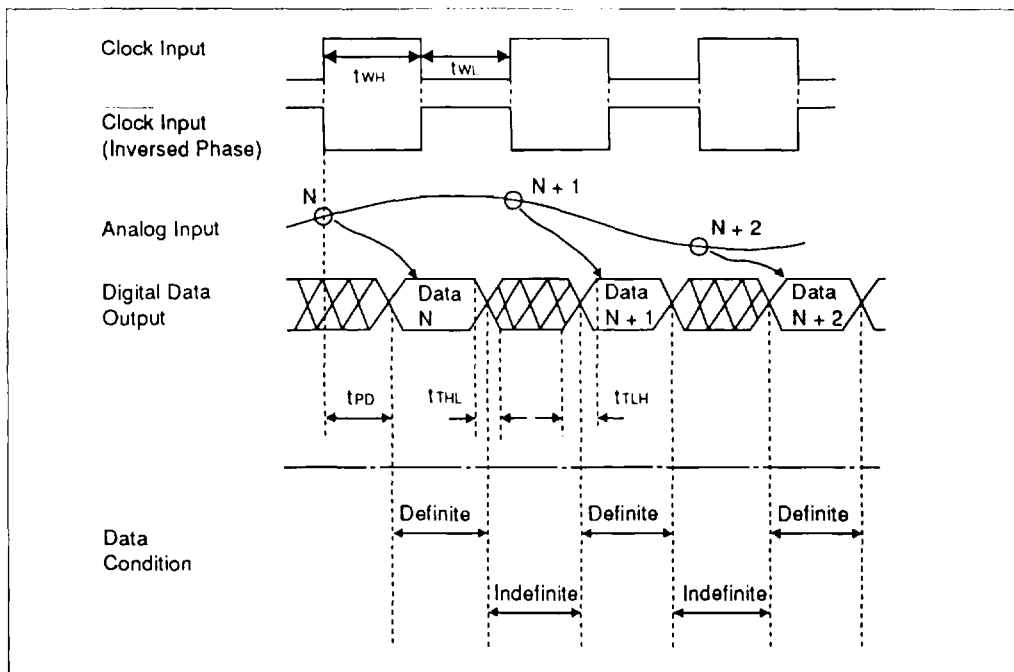


Figure 1 Sample Timing



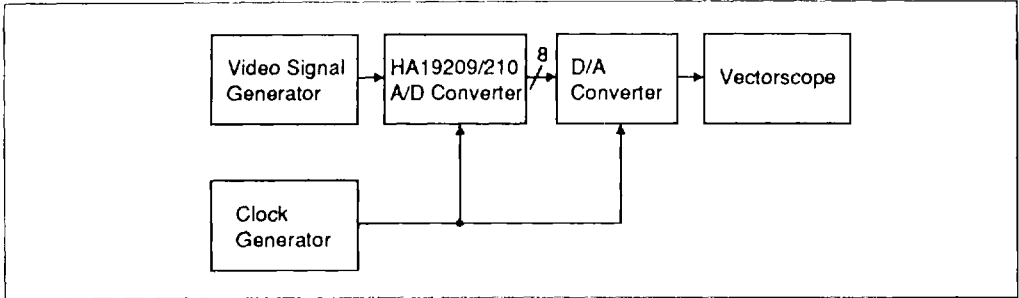


Figure 2 Test Circuit Block Diagram
Differential Gain (DG), Differential Phase (DP)

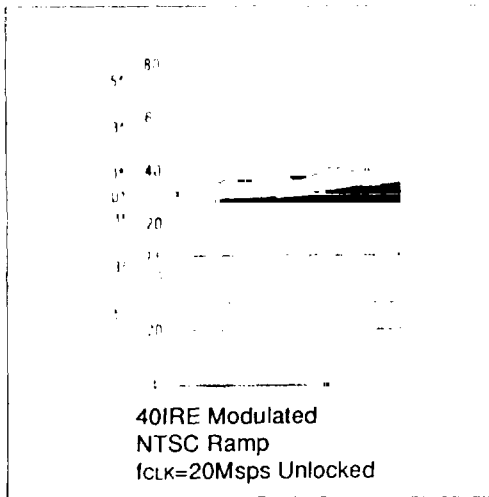


Figure 3 Differential Phase (DP)

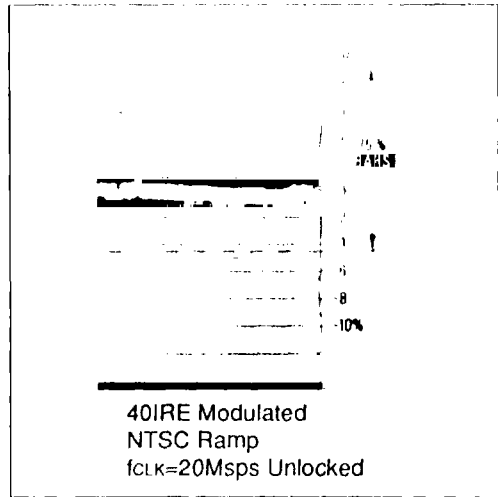


Figure 4 Differential Gain (DG)

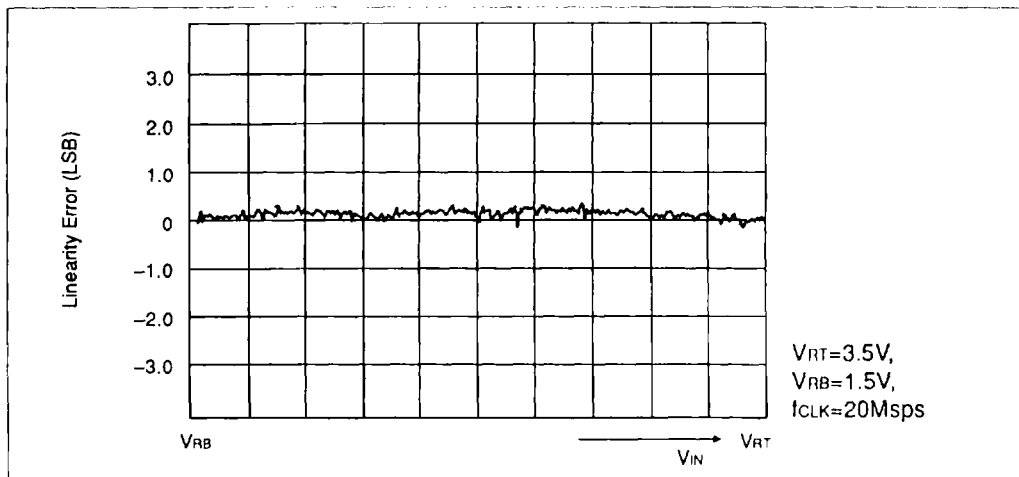


Figure 5 Static Linearity (N.L.)



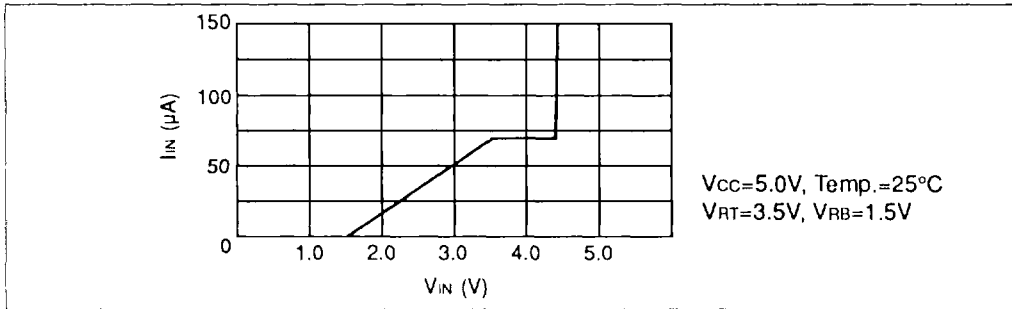


Figure 6 Analog Input Terminal DC Characteristic

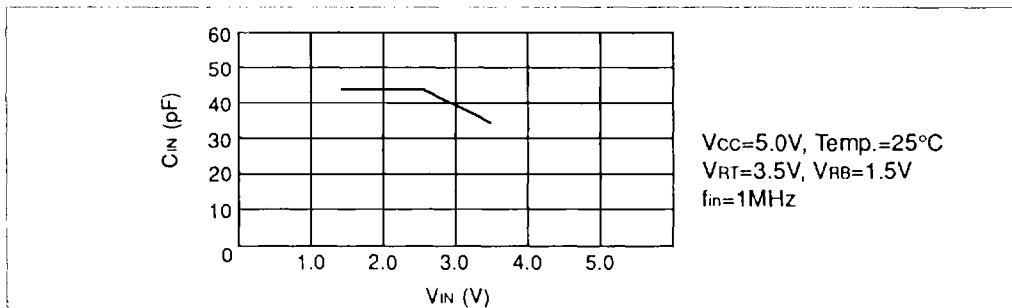


Figure 7 Input Capacitance vs. Input DC Level

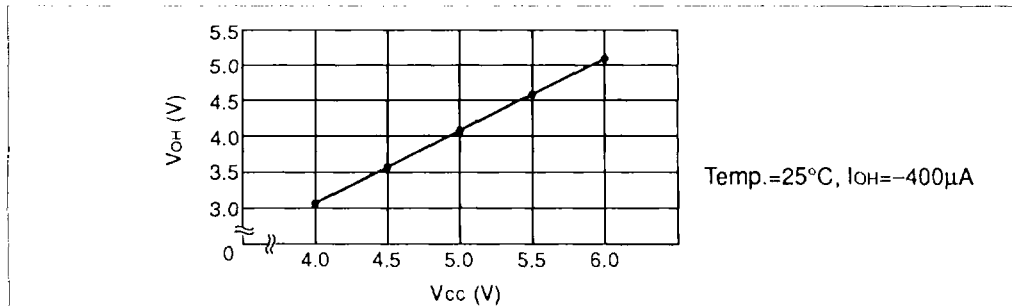


Figure 8 High Level Digital Output vs. Supply Voltage

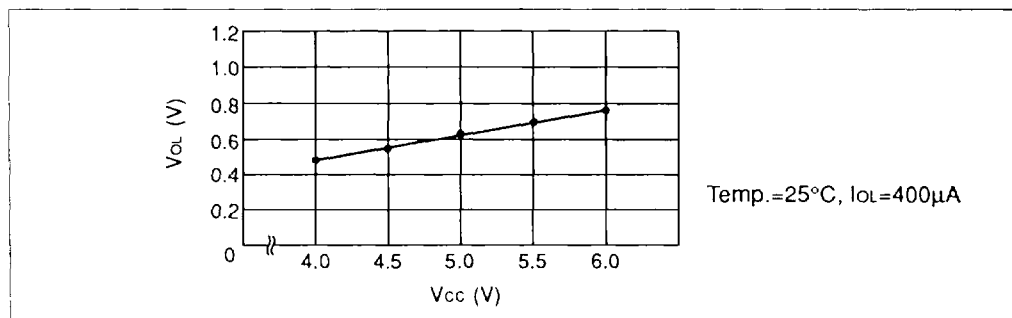


Figure 9 Low Level Digital Output vs. Supply Voltage



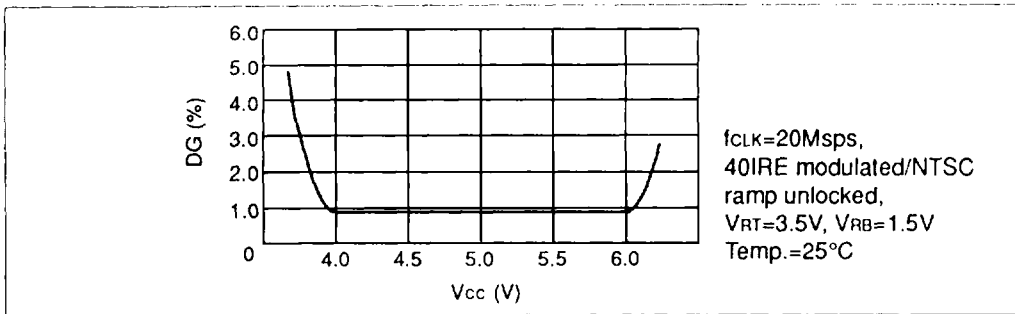


Figure 10 Differential Gain vs. Supply Voltage

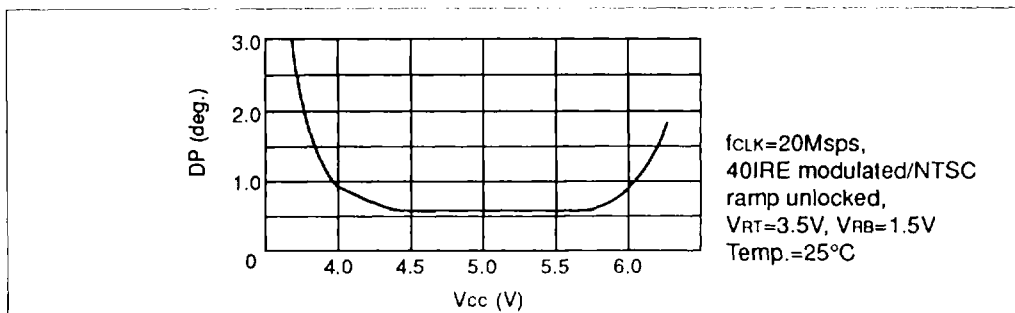


Figure 11 Differential Phase vs. Supply Voltage

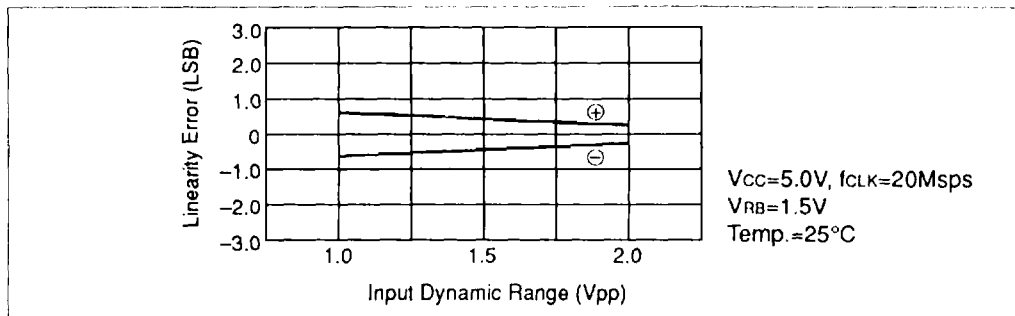


Figure 12 Static Linearity Error vs. Input Dynamic Range

