HD49428F

QAM Cable Demodulator

HITACHI

November 1996

Description

The HD49428F is a complete 256/64 QAM demodulator implementation suitable for use in Cable set-top applications. It can operate in systems using symbol rates up to 5.5 Mbauds.

The HD49428F uses a fully digital state of the art QAM Demodulator architecture which combines high performance with low overall system cost. The architecture uses 8-bit samples of the incoming analog signal, thus requiring an inexpensive analog-to-digital coverter. The Demodulator is designed to handle 256 or 64 QAM signals and automatically recognizes the QAM type of the incoming signal.

The HD49428F also integrates a number of peripheral functions which help to optimize System cost and performance. These include a general purpose Microprocessor Port, a Serial Port and timing generation for FEC system. The chip allows the System Designer to choose between these various capabilities through hardwiring of external pins.

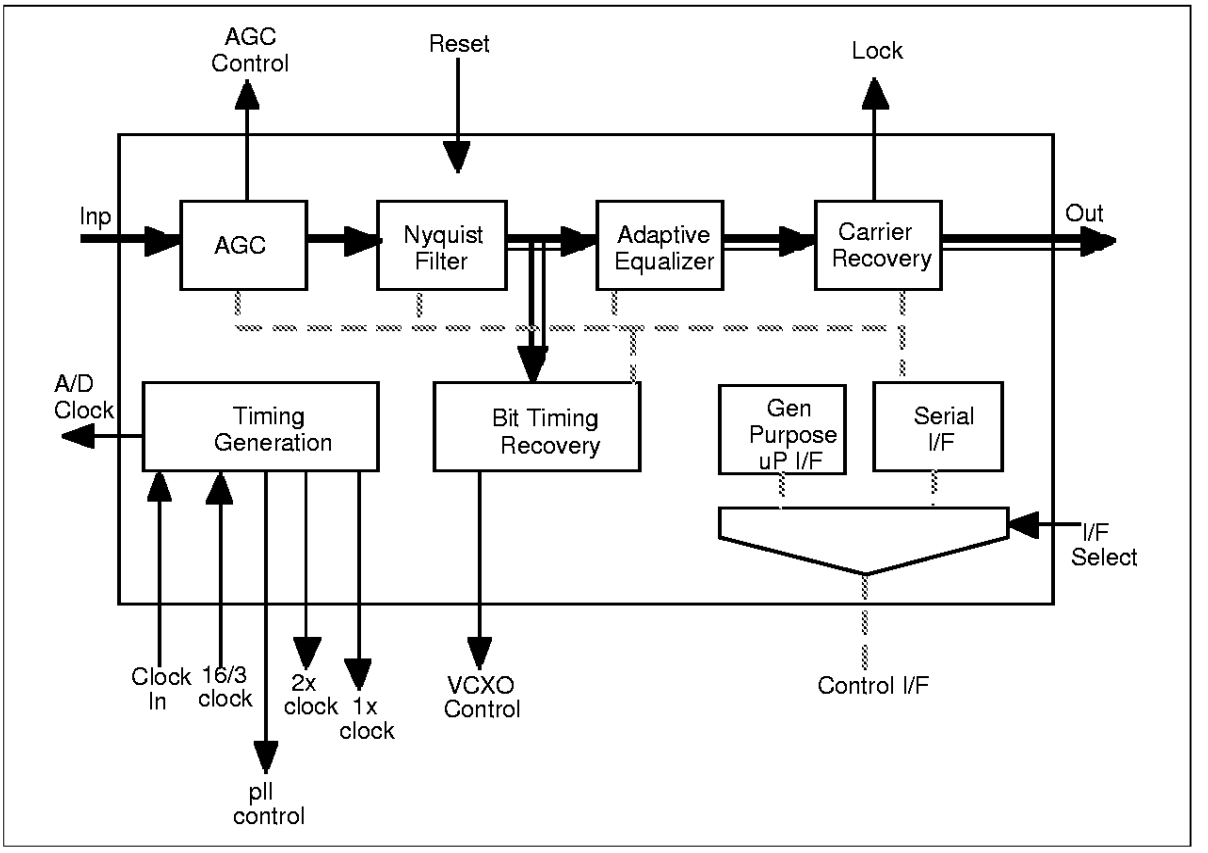
The various parameters of the QAM demodulator sytem are programmable by the user via the microprocessor port or the serial port. These can be programmed to fine-tune the performance of the QAM demodulator system. However, the chip can also function in a stand-alone mode using default parameters resulting in a low cost system.

Features

- Single Chip 256/64 QAM Cable Demodulator
  - — Supports up to 5.5 MBaud rates, fully synchronous design
- Fully Digital Implementation includes
  - — AGC
  - — Nyquist Filter
  - — Symbol Timing Recovery
  - — Adaptive Equalizer
  - — Carrier Recovery
  - — Automatic QAM type detection
- Onchip Peripheral functions include
  - — General Purpose Microprocessor Port
  - — I^2C (TM) Compatible Serial Port
  - — Timing Generation for FEC System

- Standalone or microcontroller assisted operation
- Optimal System Implementation
  — Requires only one 8 bit A/D
- Standard 80 Pin PQFP Package

Block Diagram



64 QAM Performance Specification

Guidelines forInterpreting QAM Performance Specification

1. The specified impaired signal conditions are for single impairments only, unless otherwise noted.
2. In order to state a threshold Signal/Noise ratio vs. BER performance for the complete system including error correction, we assume a nominal FEC performance. We assume that the FEC provides 5.8 dB coding gain at an error rate of 10-8 after error correction. This means that the Signal/Noise at the demodulator output can be 5.8 dB below the theoretical Signal/Noise required for an uncoded error rate of 10-8.
3. Consistent with our assumption that these specifications are single-impairment unless noted, our performance specifications are referenced to the input of the demodulator IC. This is equivalent to assuming a perfect 8-bit A/D converter. If the actual A/D converter has less than eight effective bits,

this quantization represents an additional noise source which degrades performance. (Examples: an A/D of 7.5 effective bits degrades 64-QAM performance by less than 0l1 dB: an A/D of 7 effective bits degrades performance by about 0.2 dB.)

Table 1. 64 QAM Performance Specification

Parameter	Specification	
Frequency	+/- 125 kHz	
Phase noise:	-73 dBc/Hz at 10 kHz from carrier	
CNR	23 dB signal power to noise power in 5 MHz for corrected BER of 10-8. See Guidelines above on FEC.	
Hum (120 Hz Modulation)	10% peak to peak Square hum (infinite bandwidth)	
	20% peak to peak Sinusoidal hum2	
	6% peak to peak Triangular hum	
Residual FM	50-kHz peak to peak deviation when modulated by 120 Hz sine wave.	
Discrete RF Interference	Single tone -15 dBc	
Multipath	**Delay Amplitude**	**(Reflection/signal ratio)**
(when reference tap is ~1/3 of total delay range of equalizer taps)	0-300ns	10db
	300-700 ns	10 dB
	700-1400 ns	15 dB
Spectral Tilt	+/- 5 dB	
Saw Filter Ripple	< +/-0.50 dB	
Saw Filter Group Delay Variation	< +/- 75 ns	
Acquisition Time:	< 100 ms	Operating Condition is –11 dB, 600 ns multipath, 26 dB SNR
Acquisition Time	< 100 ms	Operating Condition is –73 dBc @10 kHz phase noise, 26 dB SNR
Dynamic multipath	Single multipath at 1 µs:	
	-20 dBc, phase rotation = 5 Hz.	
AGC Voltage	0–5 Volts	

64 QAM Soft Decision Levels

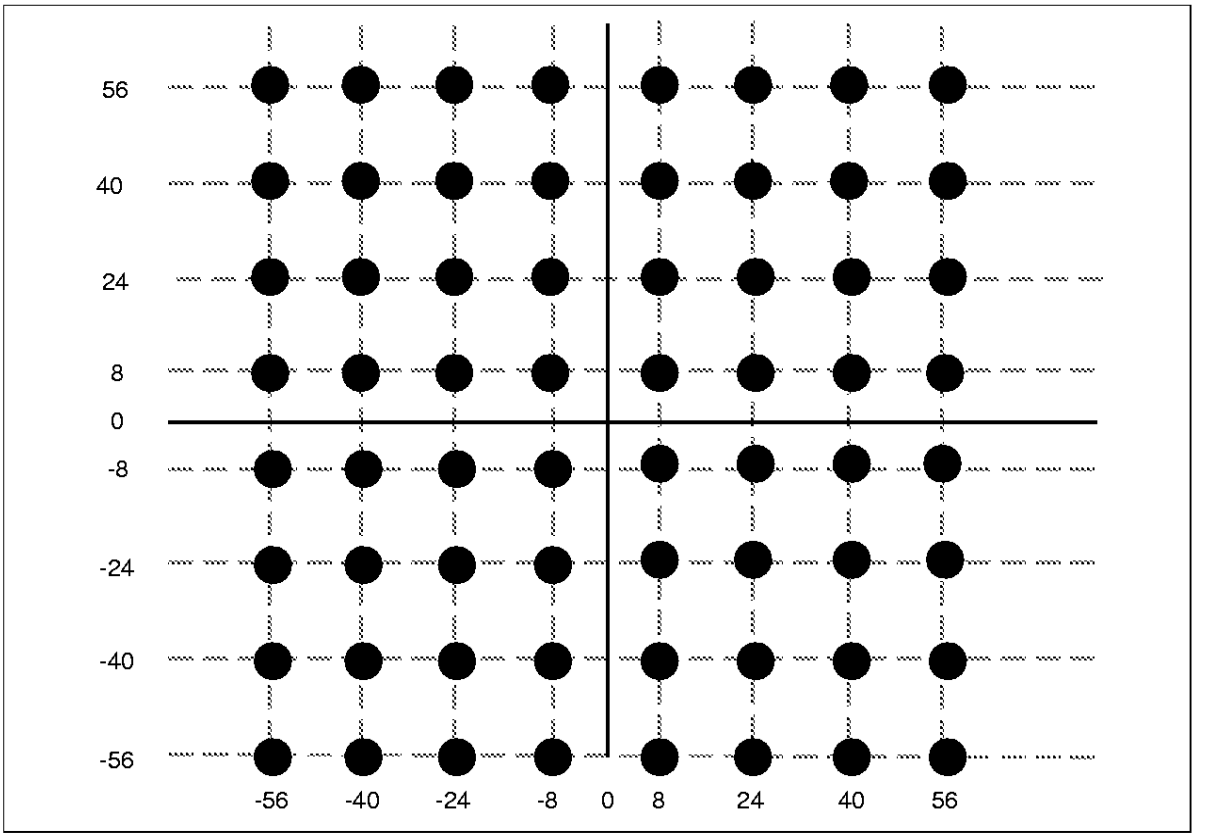


Figure 2 64 QAM Soft Decision Levels

The 64 QAM soft decisions are available as 7 bit outputs for each I and Q and are available on ports ISYM[7:1] and QSYM[7:1] in the non-mux mode. The QAM constellation is shown in the figure above. This assumes that the 7 bit symbols are interpreted as signed 2's complement numbers.

256 QAM Performance Specifications

Guidelines for the Interpretation of These Specifications

1. The specified impaired signal conditions are for single impairments only, unless otherwise noted.
2. In order to state a threshold Signal/Noise ratio vs. BER performance for the complete system including error correction, we assume a nominal FEC performance. We assume that the FEC provides 5.8 dB coding gain at an error rate of 10-8 after error correction. This means that the Signal/Noise at the demodulator output can be 5.8 dB below the theoretical Signal/Noise required for an uncoded error rate of 10-8.
3. Consistent with our assumption that these specifications are single-impaired unless noted, our performance specifications are referenced to the input of the demodulator IC. This is equivalent to assuming a perfect 8-bit A/D converter. If the actual A/D converter has less than eight effective bits, this quantization represents an additional noise source which degrades performance. (Examples:an A/D

of 7.5 effective bits degrades 256-QAM performance by less than 0.1 dB; an A/D of 7effective bits degrades performance by about 0.5 dB.)

Table 2. 256 QAM Specification

Parameter	Specification	
Frequency	+/-125 kHz	
Phase noise:	-77 dBc/Hz at 10 kHz from carrier	
CNR	30 dB for corrected BER of 10-8. See Guidelines above on FEC.	
Hum (120 Hz Modulation)	7% peak to peak Square hum (infinite bandwidth) 18% peak to peak Sinusoidal hum 23% peak to peak Triangular hum	
Residual FM	50 kHz peak to peak deviation when modulated by 120 Hz sine wave.	
Discrete RF Interference	Single tone -21 dBc	
Multipath (when reference tap is ~1/3 of total delay range of equalizer taps)	Delay Amplitude 0-300 ns 300-700 ns 700-1400 ns	(reflection/signal ratio) -10db -13 dB -15 dB
Spectral Tilt	+/- 3dB	
Saw Filter Ripple	< +/- 0.2 dB	
Preferred SAW Filter Shape	0.1 dB Bandwidth > 40 dB Rejection	5 Mhz 6 Mhz
Saw Filter Group Delay Variation	< +/-20ns	
Acquisition Time:	<150 ms	Operating Condition is -15 dB, 600 ns multipath, 33dB SNR
Acquisition Time:	<100 ms	Operating Condition is -77 dBc @10 kHz phase noise, 33dB SNR
Dynamic multipath	Single multipath at 1 μs: -20 dBc, phase rotation = 5 Hz.	
AGC Voltage	0-5 Volts	

256 QAM Soft Decision Levels

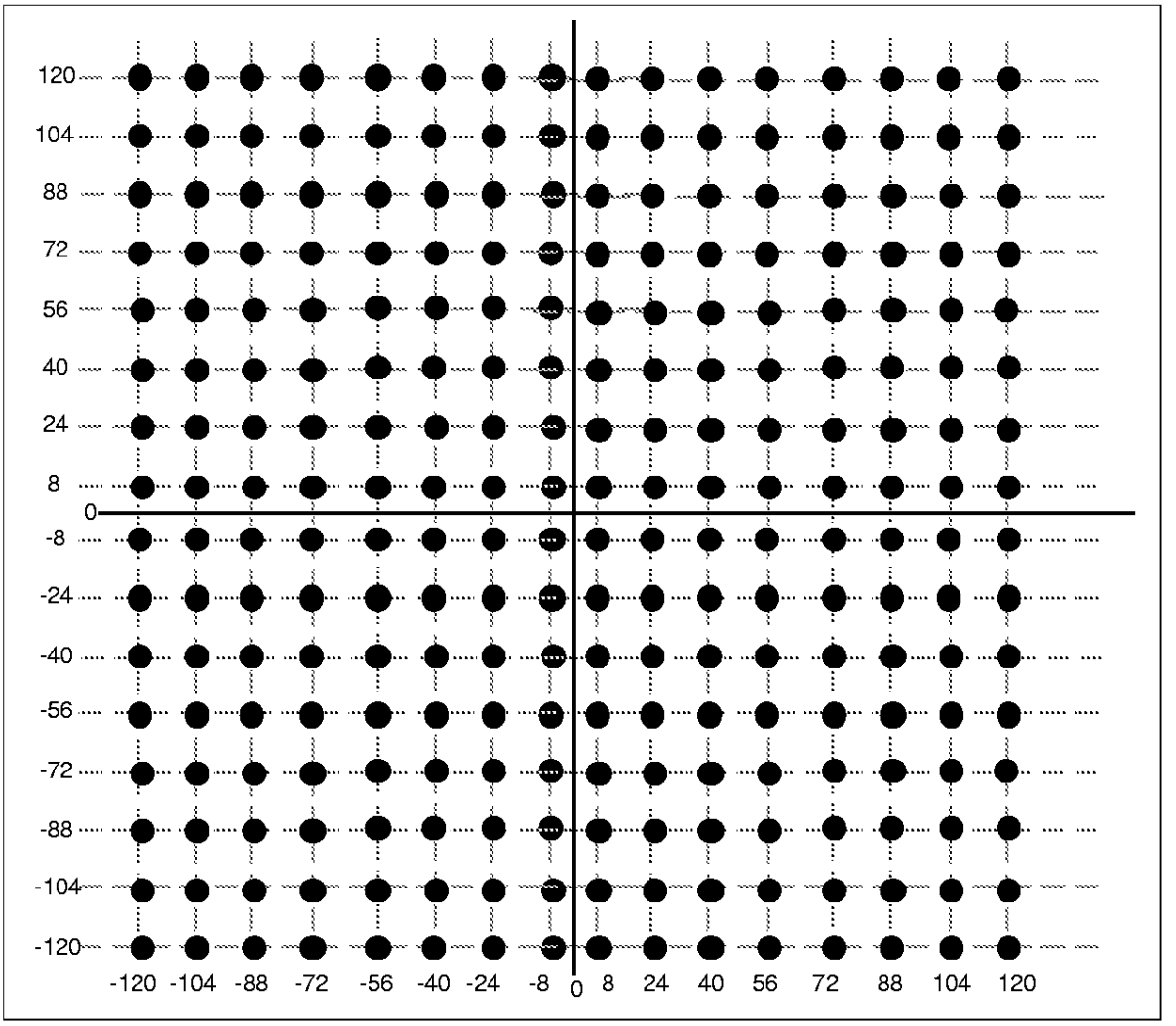


Figure 3 256 QAM Soft Decision Levels

The 256 QAM soft decisions are available as 8 bit outputs for each I and Q and are available on ports ISYM[7:0] and QSYM[7:0] in the non-multiplexed mode. The QAM constellation is shown in the figure above. This assumes that the 8 bit symbols are interpreted as signed 2's complement numbers.

Detailed I/O Description

Table 3. Detailed Pin Description

Pin Name	Type	Description	Number of Pins
SIG[7:0]	I	Sampled input signal (From A/DConverter.) Can be signed or unsigned	8
AGCCNTRL	O	Sigma-Delta modulated control output. This signal is externally low-pass filtered and then used to control gain of an analog AGC amplifier or attenuator.	1
VCXOCNTRL	O	Sigma-Delta modulated control output. This signal is externally low pass filtered and then used to control the frequency of a VCXO.	1
ISYM[7:0]	O	In-phase soft decision output .	8
QSYM[7:0]	O	Quadrature-phase soft decision output	8
LOCK	O	Carrier Recovery Lock Indicator	1
CLK4XIN	I	The clock input is 4x Symbol rate.	1
CLK27IN	I	TTL clock input for 27Mhz clock	1
CLK4X	O	A/D sampling clock at 4x Symbol rate	1
PLL27CNTRL	O	Control output for controlling external VCO which produces the 27m clock	1
CLK2X	O	2x symbol rate clock suitable for FEC.	1
CLK1X	O	Symbol rate clock	1
$\overline{CS}$/SCL	I	Chip Select Input for general purposer µP interface. SCL (clk) input for -I^{2}C interface.	1
R/$\overline{W}$	I	Read/$\overline{Write}$ indicator for general purpose µP I/F	1
WAIT	O	Open Drain Output for general purpose µP I/F. Deassertion (low) of this signal after start of a transaction indicates to the master that the slave chip is ready to complete the transaction.	1
ADDR/$\overline{DATA}$	I	Chooses accessing of internal address pointer register or the register pointed to for general purpose µP I/F	1
SEL-I2C	I	Selects -I^{2}C or µP Interface	1
D[0]/SDA	Bi	SELI2C = 0: Bidirectional Data pin D[0] for µP I/F SELI2C=1: -I^{2}C I/O data pin.	1
D[7:1]	Bi	SELI2C = 0: General Purpose µP Interface bidiractional Data bus. When SEL12C= 1µP: -I^{2}C Device Address input	6
$\overline{RESET}$	I	Master Reset. This resest initializes all the internal circuits to their default states.	1
$\overline{SCAN}$	I	For Test Purposes only	1
$\overline{Test}$	I	For Test Purposes only	1

Table 3. Detailed Pin Description (cont)

Pin Name	Type	Description	Number of Pins
NC		Not connected	3
VSS	P	Ground Pins	16
VDD	P	5 V Supply Pins	12

Programming

The HD49428F contains a number of on-chip registers which can be programmed to optimize the performance of the QAM demodulation System. It also contains a number of on-chip status registers which can be read by the system for diagnostic purposes. The chip can also function in a stand-alone mode using no external programming. This stand-alone mode uses default register values and is suitable for a low cost system implementation.

Program Registers

Table 4. Program Registers

Register Name	Addr	Pos	Description	
EQUALIZER CENTER TAP	24	[3:0]	**d7**	Equalizer center tap location
AGC POWER REFERENCE	25	[7:0]	**d64**	Power Reference for AGC
BIT SYNC LOCK THRESHOLD	26	[7:0]	**d32**	Lock Threshold for Bit Timing Recovery Loop
AGC INVERT	27	[0:0]	**0**	Pos. External AGC gain slope
			1	Neg. External AGC gain slope
AGC LOCK ENABLE	27	[1:1]	0	Updating of Equalizer is always done regardless of AGC lock.
			1	Updating of Equalizer is done only when AGC lock is achieved.
AGC GAIN	27	[3:2]	00	Fast AGC loop gain
			01	Medium fast
			10	Medium slow
			11	Slow AGC Loop Gain
VCXO POLARITY	27	[4:4]	0	Neg. xfer function VCXO slope
			1	Pos. xfer function VCXO slope
BIT SYNC LOCK_ENABLE	27	[5:5]	0	Constant timing loop gain
			1	Lowered loop gain in lock mode.

Table 4. Program Registers (cont)

Register Name	Addr	Pos	Description	
BIT SYNC GAIN	27	[7:6]	00	High VCXO loop gain
			01	Medium high
			10	Medium low
			11	Low VCXO loop gain
INPUT SIGNAL TYPE	28	[0:0]	**0**	input is unsigned (0 to 255)
			1	input is signed(-128 to 127)
AUTOMATIC QAM DETECTION	29	[1:0]	00	Automatic QAM detection. Initialized to 64 QAM
			10	Automatic QAM detection. Initialized to 256 QAM
			01	Force 64 QAM Acquisition
			11	Force 256 QAM Acquisition
SWAP IQ OUTPUT	29	[2:2]	**0**	I and Q outputs not swapped
			1	I and Q outputs swapped
OUTPUT TYPE	29	[3:3]	0	Outputs are unsigned (0 to 255)
			1	Outputs are signed (-128 to 127)
TONE CANCELER	29	[4:4]	**0**	Enable Tone Canceler
			1	Disable Tone Canceler
IMPULSE BLANKER CONTROL	29	[5:5]	0	Disable Impulse blanker
			1	Enable Impulse blanker
TONE CANCELER PREFILTER QUADRANT	29	[7:6]	**00**	-1.75 MHz w.r.t Carrier Freq (NTSC co-channel quadrant)
			01	+2.0 Mhz w.r.t. Carrier Freq
			10	-0.5 Mhz w.r.t. Carrier Freq
			11	0.75 Mhz w.r.t Carrier Freq
Q256 DECISION DIRECTED AGC LIMIT	30	[7:0]	**d112**	Absolute value limit below which symbols are used to update decision directed AGC circuit in 256 QAM mode.
Q64 ACQUISITION MODULUS	31	[7:0]	**d84**	Radius square size of constellation, below which during acquisition, no carrier updating occurs.
Q256 ACQUISITION MODULUS.	32	[7:0]	**d84**	Radius square size of constellation, below which during acquisition, no carrier updating occurs.

Table 4. Program Registers (cont)

Register Name	Addr	Pos	Description	
Carrier Recovery lock mode PLL 1st order gain	33	[7:6]	**00**	High gain
			01	Medium high
			10	Medium low
			11	Low gain
Carrier Recovery lock mode PLL 2nd order gain	33	[5:4]	00	High gain
			01	Medium high
			10	Medium low
			11	Low gain
Carrier Recovery Acq. mode PLL 1st order gain	33	[3:2]	**00**	High gain
			01	Medium high
			10	Medium low
			11	Low gain
Carrier Recovery Acq. mode PLL 2nd order gain	33	[1:0]	00	High gain
			01	Medium high
			10	Medium low
			11	Low gain
Q64 MSE lock/nolock Threshold	34	[7:0]	**d92**	Mean square sliced error compared to this value for 64 QAM. lock condition is set if average error is below this limit.
Q256 MSE lock/nolock Threshold	35	[7:0]	**d38**	Mean square sliced error compared to this value for 256 QAM. lock condition is set if average error is below this limit.
Constellation magnitude Threshold	36	[7:0]	**d136**	Constellation magnitude (size) is compared to this value. Magnitude lock is set if average magnitude is above this limit.
Tilt Detection Threshold	37	[7:0]	**d64**	Tilt error magnitude is compared to this value. Tilt lock is set if average tilt is below this limit.
Carrier Lock hysteresis	38	[1:0]	**d1**	This value determines the number of consecutive averaging periods for which carrier lock has been lost to change to acquisition mode.
Impulse Count	38	[5:2]	**d10**	This value determines the number of consecutive symbols to ignore once an impulse has been detected.
Tone Cancel Prefilter	38	[6:6]	**0**	Tone canceler Prefilter enabled
			1	Tone Canceler Prefilter disabled
auto_reset	38	[7:7]	**0**	Auto reset is enabled
			1	Auto reset is disabled System will automatically perform a soft reset if carrier lock is not achieved in about 4 seconds

Table 4. Program Registers

Register Name	Addr	Pos	Description	
Impulse detection Multiplies	39	[7:6]		Scale factor used for dynamic impulse detection circuit.
			00	Large multiplier
			01	medium large
			10	medium low
			11	Low multiplier
Impulse detection Threshold limit (256 QAM)	39	[5:4]	00	Large limit
			01	Medium large
			10	Medium small
			11	Small limit
Impulse detection Threshold limit (64 QAM)	39	[3:2]	00	Large limit
			01	Medium large
			10	Medium small
			11	Small limit
Output Mux	45	[0:0]	**0**	Non-Mux Mode
			1	Mux mode
VCO slope	45	[1:1]	**0**	Negative slope
			1	Positive slope

Status Registers

Table 5. Status Registers

Register Name	Addr	Position	Description
ITAP[1]	0	[7:0]	In-Phase tap weight of Adaptive Equalizer (tap [1])
QTAP[1]	1	[7:0]	Quadrature tap weight of Adaptive equalizer (tap [1])
ITAP[2]	2	[7:0]	Quadrature tap weight of Adaptive equalizer (tap [1])
QTAP[2]	3	[7:0]	Quadrature tap weight of Adaptive equalizer (tap [1])
ITAP[3]	4	[7:0]	Quadrature tap weight of Adaptive equalizer (tap [1])
QTAP[3]	5	[7:0]	Quadrature tap weight of Adaptive equalizer (tap [1])
ITAP[4]	6	[7:0]	Quadrature tap weight of Adaptive equalizer (tap [1])
QTAP[4]	7	[7:0]	Quadrature tap weight of Adaptive equalizer (tap [1])
ITAP[5]	8	[7:0]	Quadrature tap weight of Adaptive equalizer (tap [1])
QTAP[5]	9	[7:0]	Quadrature tap weight of Adaptive equalizer (tap [1])
ITAP[6]	10	[7:0]	Quadrature tap weight of Adaptive equalizer (tap [1])
QTAP[6]	11	[7:0]	Quadrature tap weight of Adaptive equalizer (tap [1])

Table 5. Status Registers (cont)

Register Name	Addr	Position	Description
ITAP[7]	12	[7:0]	Quadrature tap weight of Adaptive equalizer (tap [1])
QTAP[7]	13	[7:0]	Quadrature tap weight of Adaptive equalizer (tap [1])
ITAP[8]	14	[7:0]	Quadrature tap weight of Adaptive equalizer (tap [1])
QTAP[8]	15	[7:0]	Quadrature tap weight of Adaptive equalizer (tap [1])
ITAP[9]	16	[7:0]	Quadrature tap weight of Adaptive equalizer (tap [1])
QTAP[9]	17	[7:0]	Quadrature tap weight of Adaptive equalizer (tap [1])
ITAP[10]	18	[7:0]	Quadrature tap weight of Adaptive equalizer (tap [1])
QTAP[10]	19	[7:0]	Quadrature tap weight of Adaptive equalizer (tap [1])
ITAP[11]	20	[7:0]	Quadrature tap weight of Adaptive equalizer (tap [1])
QTAP[11]	21	[7:0]	Quadrature tap weight of Adaptive equalizer (tap [1])
ITAP[12]	22	[7:0]	Quadrature tap weight of Adaptive equalizer (tap [1]).....(tap[12])
QTAP[12]	23	[7:0]	Quadrature tap weight of Adaptive equalizer (tap [1]).....(tap[12])
AGC LOCK	28	[1:1]	AGC lock (0=F, 1=T)
BIT SYNC LOCK	28	[2:2]	Bitsync Lock (0=F, 1=T)
CARRIER LOCK	39	[0:0]	Carrier recovery lock (0=F, 1=T)
QAM TYPE FOUND	39	[1:1]	Automatic QAM detection circuit results, 0=64, 1=256
AVG ERROR LSB	40	[7:0]	This 16 bit register contains the sliced error value summed over 4096 symbols (used for SNR estimation)
AVG ERROR MSB	41	[7:0]	
FREQ OFFSET	42	[7:0]	Frequency offset of carrier recovery loop.
VCXO CONTROL	43	[7:0]	VCXO control signal, used for monitoring bit timing circuit
AGC CONTROL	44	[7:0]	AGC control signal, used for monitoring AGC circuit
REV NUMBER	46	[7:0]	QAM demod chip rev number

Control Interfaces

The programming and status registers can be accessed via the chip's control interface. For maximum System flexibility, a general purpose Microprocessor Interface and an -I^2C (TM) compatible serial interface are available on the chip. The two interfaces share I/O pins, and only one Interface can be selected in a system implementation by hardwiring the SELI2C input appropriately. Details of each interface are given below.

General Purpose µP Interface

The following I/O pins constitute the µP Interface. The µP interface is available when the SELI2C pin is low. The following table gives a detailed description of the I/O pins involved.

Table 6. General Purpose µP Interface

Pin Name	Type	Description
$\overline{CS}$	I	The chip select input activates a transaction. The type of the transaction is determined by the state of the R/$\overline{W}$ and ADDR/$\overline{DATA}$ pins. The WAIT output deasserts itself when the chip is ready to complete the transaction. The external microcontroller then finishes the transaction by de-asserting the $\overline{CS}$ pin.
R/$\overline{W}$	I	This input indicates whether a transaction will be read or write transaction. In a read transaction, data from an on-chip register will be read by the external controller. In a write transaction, data will be written into one of the chip's on-chip registers.
ADDR/$\overline{DATA}$	I	When this input is asserted during a write, data from the D[7:0] bus is written into the on-chip address pointer register. When this input is de-asserted, an on-chip register pointed to by the address pointer register is read or written.
D[7:0]	Bi	This bidirectional parallel bus is used to read and write on-chip registers.
WAIT	O	This is a tristate output. It is driven only when the chip is selected (by asserting $\overline{CS}$ input). The chip indicates that it is ready to complete the transaction by deasserting this pin. The transaction is formally complete when the external controller de-asserts $\overline{CS}$ input.

This interface uses an indirect addressing mode for accessing the on-chip registers. The Address Pointer Register acts as the pointer. Hence, a random register access typically will require 2 I/F transactions. During the first transaction, addr_mode input is asserted, and the address of the register that needs to be accessed is written to the Address Pointer Register. During the next transaction, the appropriate register is accessed. However, if registers are to be accessed sequentially, then an autoincrement feature will allow one access per transaction for all subsequent sequential accesses.

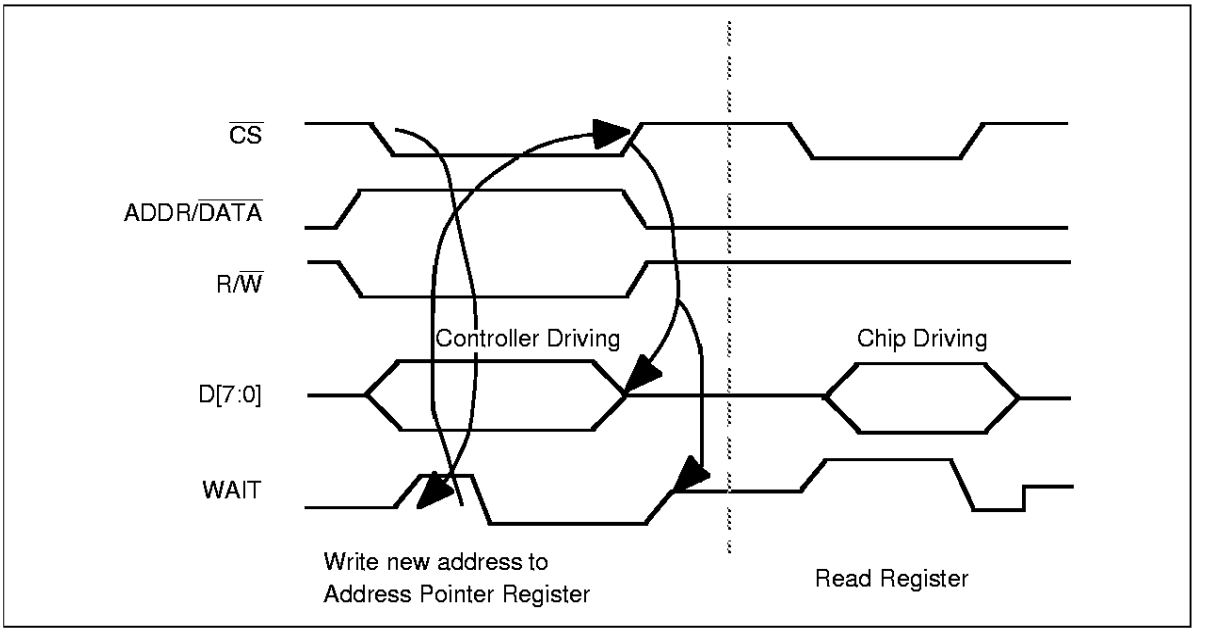


Figure 4 µP Interface Protocol

Serial Interface

The Serial interface is active when the SELI2Cinput pin is wired high. The serial interface is -I²C (TM) compatible and involves the following I/O pins.

Table 7. Serial Interface

Pin Name	Type	Description
SDA (D[0])	I/O	This is the bidirectional data pin of the -I²C (TM) compatible serial interface.
SCL ($\overline{CS}$)	I	This is the clock pin of the -I²C (TM) compatible interface. Since the chip is programmed to be a slave only, this is an input pin.

The -I²C compatible serial interface is configured to be a slave.

-I²C Protocol

The following figure describes the -I2C protocol that is implemented and timing relationship between various pins in a serial transfer. As shown, the SDA pin can change state during the low period of the SCL pin. The two exceptions to this rule occur during the start and stop conditions. During the "start" condition, SDA pin makes a high to low transition while the SCL pin is high. A low to high transition of SDA pin while SCL is high represents a "stop" condition. -I2C (TM) specification requires that each transaction is in multiples of 8 serial clocks with the MSB bit transmitted first. Each 8-bit transaction is ended by the receiver sending an acknowledgement by driving the SDA pin low as shown.

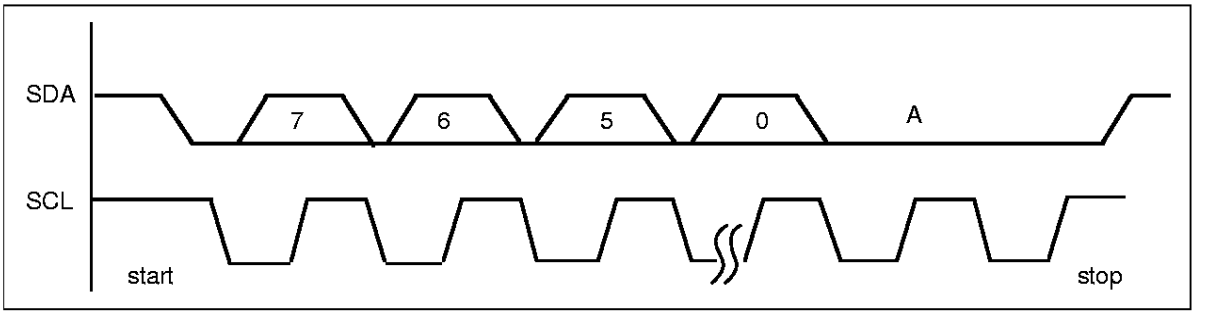


Figure 5 I²C Address and Data Protocol

An -I2C serial transfer begins with a -I2C master (usually a micro-controller) starting a new transaction. Each such transaction is composed of multiple transfers, each of which involves a 8-bit serial transfer followed by an acknowledgement from the receiver, as described in the previous paragraph. The first serial transfer in a transaction involves the I2C master broadcasting a 7-bit I2C device address over the bus. The 8th bit of this transfer indicates the direction of subsequent transfers. A "1" indicates that the -I2C master wants to read from a slave device and a "0" indicates that the -I2C master wants to write to a slave device. The addresssed device sends an acknowledgement if it is available. A typical transaction is shown in figure 4. The address byte (7 bits of address and read/write bit) is referred to as byte A. Subsequent data bytes are referred to as D0 to Dn. This terminology is used in all subsequent discussions.

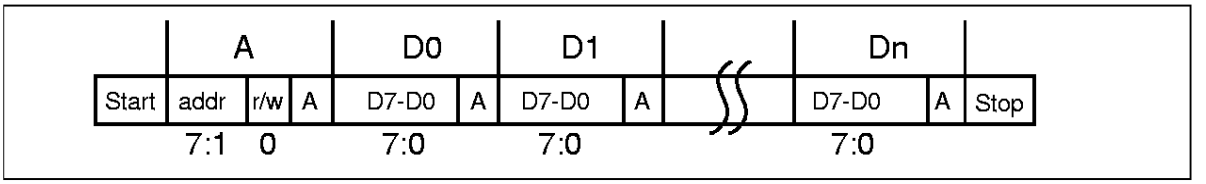


Figure 6 I²C Address and Data Protocol

Programming Protocol

-I2C is a serial transfer protocol that specifies how bytes of data are transferred over a serial interface. However the interpretation of what these bytes mean and the specification of the order in which they are sent is unique to each system.

The HD49428F uses the -I2C bus to allow an external controller to access its on-chip registers. The on-chip registers are accessed using the address pointer register. A transaction can contain an arbitrary number of byte transfers. The direction of the transfer is set by the read/write bit (bit 0 in byte A).

Write Transactions: A transaction is determined to be a write transaction when bit A[0] equals "0". During a write transaction, data is written to HD49428F on-chip registers by the -I2C master. The 6 LSBs of the 1st data byte (D0) are written to the address pointer register. We will refer to this address as A0. Byte D1 is written to register A0, byte D2 is written to register A0 + 1 and so on.

Read Transactions: A transaction is determined to be a read transaction when bit A[0] equals "1". During a read transaction, data is read from HD49428Fx on-chip registers by the I2C master. During the first data transaction, the 6 LSBs of data byte D1 read from HD49428F represent the contents of the address pointer

register. We will refer to this address location as A0. Byte D1 represents data from register at location A0, byte D2 represents data from location A0 + 1 and so on.

The following table specifies the semantics.

Table 8. HD49428F Serial Protocol Specification

Byte Name	Specification (Write)	Specification (read)
A	This is the address byte with following specification: A[7:1]: I^2C slave address	
	A[0] = 0	A[0] = 1
D0	Byte is written to address pointer register and points to register A0.	Byte is read from address pointer register and points to register A0
D1	Byte is written to register at address A0	Byte is read fromregister at address A0
D2	Byte is written to register at address (A0 + 1)	Byte is read fromregister at address (A0 + 1)
D3	Byte is written to register at address (A0 + 2)	Byte is read fromregister at address (A0 + 2)
Dn	Byte is written to register at address (A0 + n - 1)	Byte is read fromregister at address (A0 + n - 1)

Timing Generation

The HD49428F accepts a master clock input which is 4x Symbol rate. The HD49428F provides a 4x Symbol rate clock for A/D trigger, and 2x and 1x symbol rate clocks for FEC system. The chip provides a VCO control output which can be used to implement a high performance phase-locked loop (PLL) using an inexpensive external VCO. This allows the generation of a phase locked 16/3x clock which can be used for the FEC system.

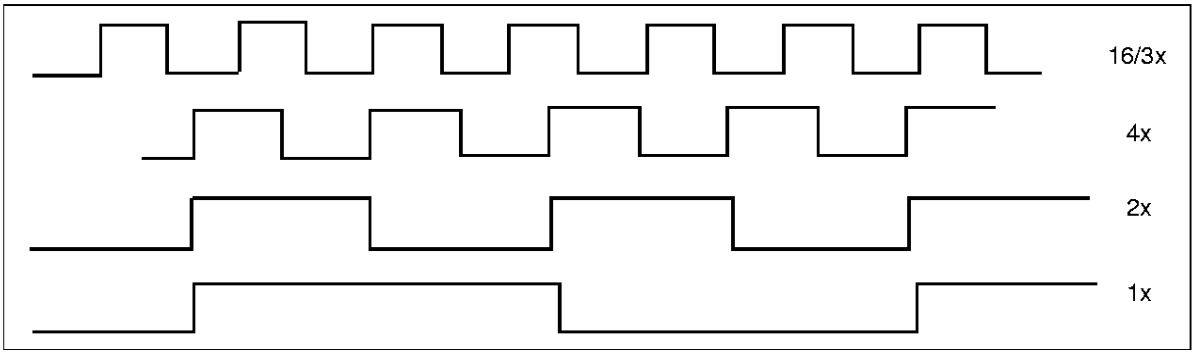


Figure 7 Timing Generation

Pinout

Table 9. Pin Assignment

Pin No	Name	Type	Type Sym	Notes
1	VSS	P	G	
2	VSS	P	G	
3	CLK4XIN	I	IC	
4	NC			
5	CLK27IN	I	IC	
6	NC			
7	PLL27CNTRL	O	O2	
8	VCXOCNTRL	O	O4	
9	AGCCNTRL	O	O4	
10	VDD	P	V	
11	SIG7	I	IT	
12	SIG6	I	IT	
13	SIG5	I	IT	
14	SIG4	I	IT	
15	SIG3	I	IT	
16	SIG2	I	IT	
17	SIG1	I	IT	
18	SIG0	I	IT	
19	VSS	P	G	
20	VSS	P	G	
21	VSS	P	G	
22	VSS	P	G	
23	VDD	P	V	
24	VDD	P	V	
25	QSYM0	O	O2	
26	QSYM1	O	O2	
27	QSYM2	O	O2	
28	QSYM3	O	O2	
29	QSYM4	O	O2	
30	QSYM5	O	O2	
31	VDD	P	V	
32	QSYM6	O	O2	
33	QSYM7	O	O2	

Table 9. Pin Assignment (cont)

Pin No	Name	Type	Type Sym	Notes
34	LOCK	O	O4	
35	ISYM0	O	O2	
36	ISYM0	O	O2	
37	VDD	P	V	
38	VDD	P	V	
39	VSS	P	G	
40	VSS	P	G	
41	VSS	P	G	
42	VSS	P	G	
43	ISYM2	O	O2	
44	ISYM3	O	O2	
45	ISYM4	O	O2	
46	ISYM5	O	O2	
47	ISYM6	O	O2	
48	ISYM7	O	O2	
49	NC			
50	VDD	P	V	
51	ADDR/$\overline{\text{DATA}}$	I	IT	
52	$\overline{\text{CS}}$	I	IT	
53	$\overline{\text{RESET}}$	I	IT	
54	WAIT	O	OZ8	
55	D0	O	B8	
56	D1	O	B8	
57	D2	O	B8	
58	D3	O	B8	
59	VSS	P	G	
60	VSS	P	G	
61	VSS	P	G	
62	VSS	P	G	
63	VDD	P	V	
64	VDD	P	V	
65	CLK1X	O	O2	
66	D4	BiDir	B8	
67	D5	BiDir	B8	
68	D6	BiDir	B8	

Table 9. Pin Assignment (cont)

Pin No	Name	Type	Type Sym	Notes
69	D7	BiDir	B8	
70	R/$\overline{W}$	I	IT	
71	VDD	P	V	
72	CLK2X	O	O2	
73	$\overline{TEST}$	I	ITP	
74	CLK4X	O	O2	
75	$\overline{SCAN}$	O	ITP	
76	SELI2C	I	ITP	
77	VDD	P	V	
78	VDD	P	V	
78	VSS	P	G	
80	VSS	P	G	

DC Characteristics

Table 10. Absolute Maximum Ratings

Parameter	Abs Maximum
Supply Voltage	6.5 V.
Input Voltage	-0.3 ~ VDD+0.3 V.
Operating Temperature	0 ~70 degrees C
Storage Temperature	125 degrees C

Table 11. DC Characteristics (Refer to table 9 to reference Pin Type Sym)

Sym	Pin Type Sym	Min	Typ	Max	Units	Test Conditions	Description
VDD	V	4.5	5	5.5	V		Operating Power Supply Voltage
IDD	V		180		mA	Vdd=5.0V Fclk=20.25Mhz VIH = Vdd - 0.5V VIL = 0.5V	Operating Supply Current
VOH1	O2	3.5			V	IOH = -2 mA VDD=4.5V	Output High Level for 2 mA Drivers
VOH2	O4	3.5			V	IOH = -4 mA VDD=4.5V	Output High Level for 4 mA Drivers

Table 11. DC Characteristics (cont) (Refer to table 9 to reference Pin Type Sym)

Sym	Pin Type Sym	Min	Typ	Max	Units	Test Conditions	Description
VOH3	B8,OZ8	3.5			V	IOH = -8 mA VDD=4.5V	Output High Level for 8 mA Drivers
VOL1	O2			0.4	V	IOL = 2 mA VDD=4.5V	Output Low Level for 2 mA Drivers
VOL2	O4			0.4	V	IOL = 4 mA VDD=4.5V	Output Low Level for 4 mA Drivers
VOL3	B8,OZ8			0.4	V	IOL = 8 mA VDD=4.5V	Output Low Level for 8 mA Drivers
VIH1	IC	0.7xVdd		Vdd	V		Input high level for CMOS level input pins
VIH2	IT,ITP	2.0		Vdd	V		Input high level for TTL level input pins.
VIL1	IC	-0.3		0.3xVdd	V		Input low level for CMOS level input pins
VIL2	IT,ITP	-0.3		0.8	V		Input low level for TTL level input pins.
IIN	IC,IT	-1		1	uA	Vdd=5.5V VIN = 5.5V or VIN= 0 V.	Input Current for non-pullup inputs
IIH	ITP	-10		+10	uA	Vdd=5.5V VIN = 5.5V	Input current for inputs with Pullups when input is high
IIL	ITP	-500			uA	Vdd=5.5V VIN = 0.0 v	Input current for inputs with Pullups when input is low.
IOZ	OZ8,B8	-10		+10	uA	Output = HIZ Vdd=5.5V VIN = 5.5V or VIN = 0.0V	Input current for bidirectional pins when pin is in high impedence state.
RH1	vcxocntrl						Output Resistance of P driver
RL1	vcxocntrl						Output Resistance of N driver
RH2	pll27cntrl				K		Output Resistance of P driver
RL2	pll27cntrl				K		Output Resistance of N driver
RH3	agccntrl				K		Output Resistance of P driver
RL3	agccntrl				K		Output Resistance of N driver

12. AC Characteristic

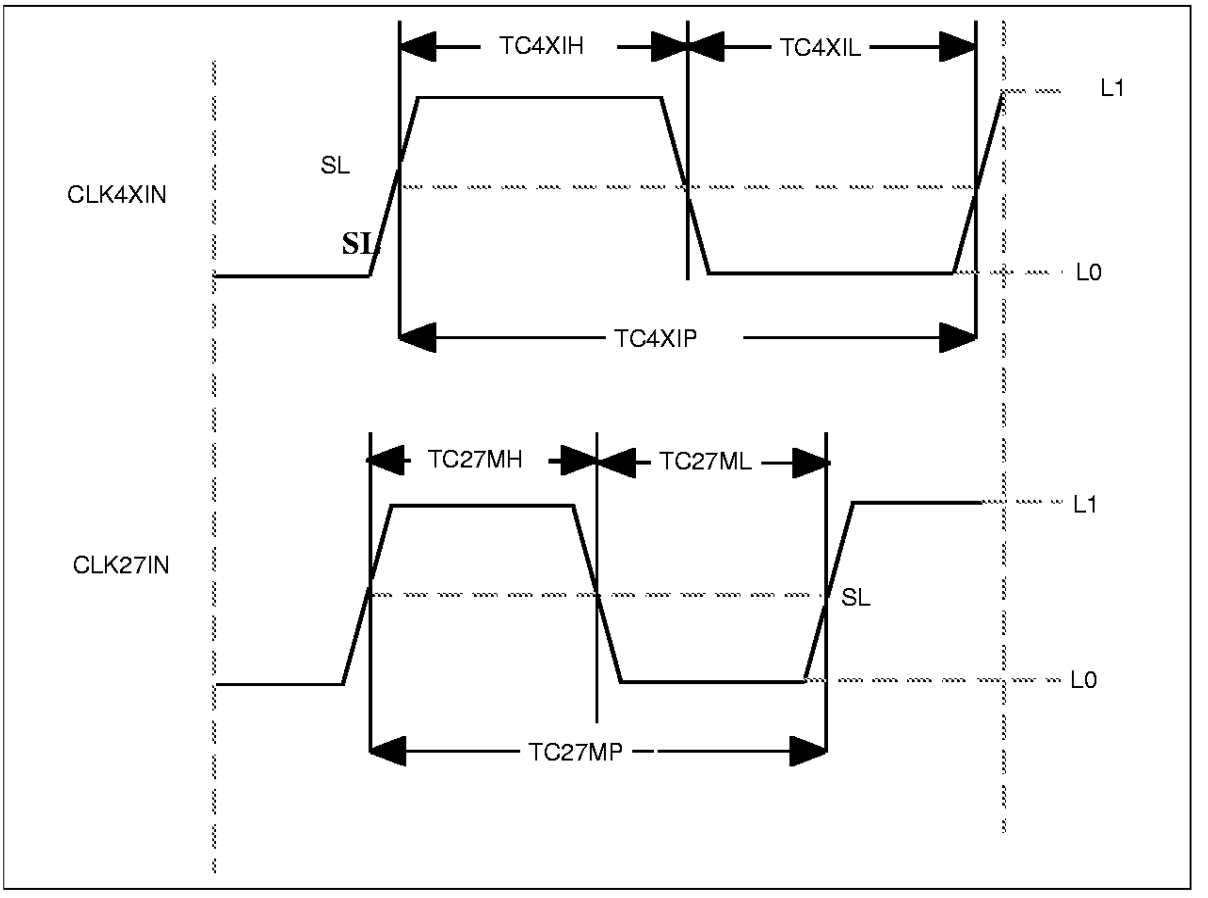


Figure 8 Clock Inputs

Table 12. Clock Inputs

Sym	Pin	Min	Typ	Max	Units	Test Conditions	Description
TC4XIP	CLK4XIN	46.29	49.43		ns	SL= 0.5Vdd L1 = 0.7Vdd	CLK4XIN Period
TC4XIH	CLK4XIN	15			ns	L0 = 0.3Vdd	CLK4XIN HighTime
TC4XIL	CLK4XIN	15			ns		CLK4XIN LowTime
TC27MP	CLK27IN	25	37		ns		CLK27IN Period
TC27MH	CLK27IN	0.4 x TC27MP		0.6 x TC27MP	ns		CLK27IN High Time
TC27ML	CLK27IN	0.4 x TC27MP		0.6 x TC27MP	ns		CLK27IN LowTime

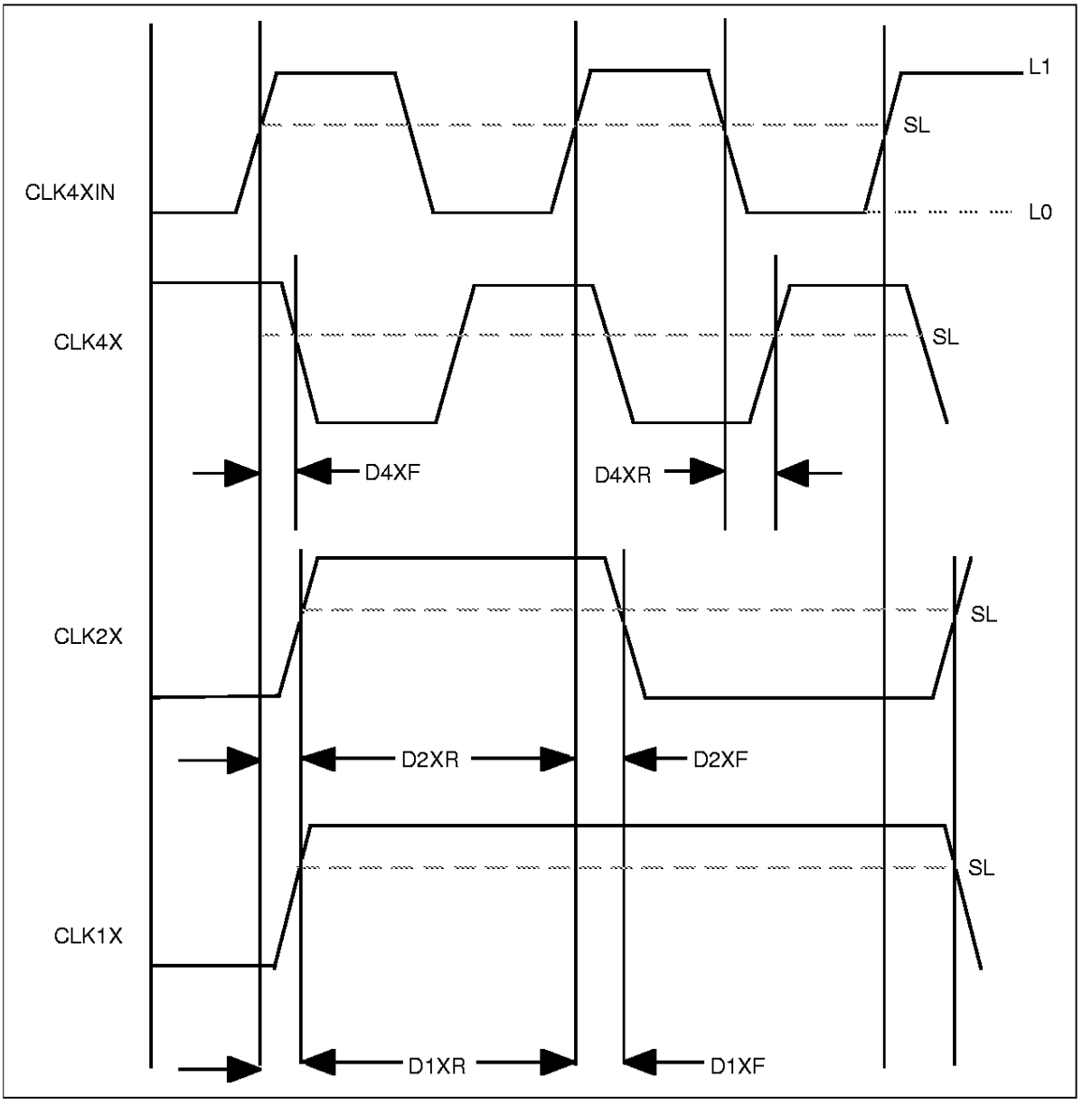


Figure 9 Clock Inputs

Table 13. Clock Outputs

Sym	PIN	Min	Typ	Max	Units	Test Conditions	Description
D4XF	CLK4X			28	ns	SL= 0.5Vdd Cload=30pf	Delay from rising edge of clk4xin to falling edge of clk4x.
D4XR	CLK4X			28	ns	SL+0.5Vdd Cload=30pf	Delay from rising edge of clk4xin to falling edge of clk4x.
D4XM	CLK4X	0		10	ns		Difference between D4XF and D4XR
D2XF	CLK2X			18	ns	SL=0.5Vdd Cload=30pf	Delay from rising edge of clk4xin to falling edge of clk2x.
D2XR	CLK2X			18	ns	SL=0.5Vdd Cload=30pf	Delay from rising edge of clk4xin to rising edge of clk2x.
D1XF	CLK1X			18	ns	SL= 0.5Vdd Cload=30pf	Delay from rising edge of clk4xin to falling edge of clk1x.
D1XR	CLK1X			18	ns	SL= 0.5Vdd Cload=30pf	Delay from rising edge of clk4xin to rising edge of clk1x.

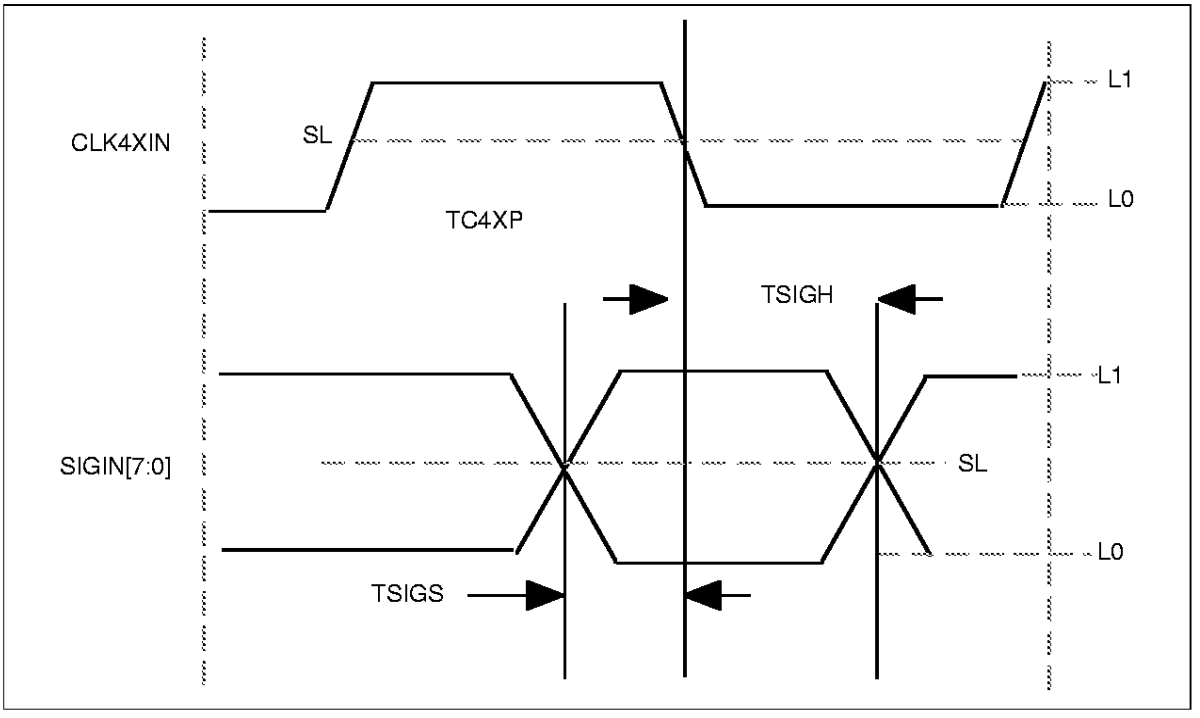


Figure 10 Input QAM Signal

Table 14. Input QAM Signal

Sym	PIN	Min	Typ	Max	U	Test Conditions	Description
TSIGS	SIGIN[7:0]	0			ns	SL= 0.5Vdd L1 = 0.7Vdd L0 = 0.3Vdd	Setup time of SIGIN[[7:0] wrt Falling edge of CLK4XIN
TSIGH	SIGIN[7:0]	D4XR			ns		Hold time of SIGIN[[7:0] wrt Falling edge of CLK4XIN

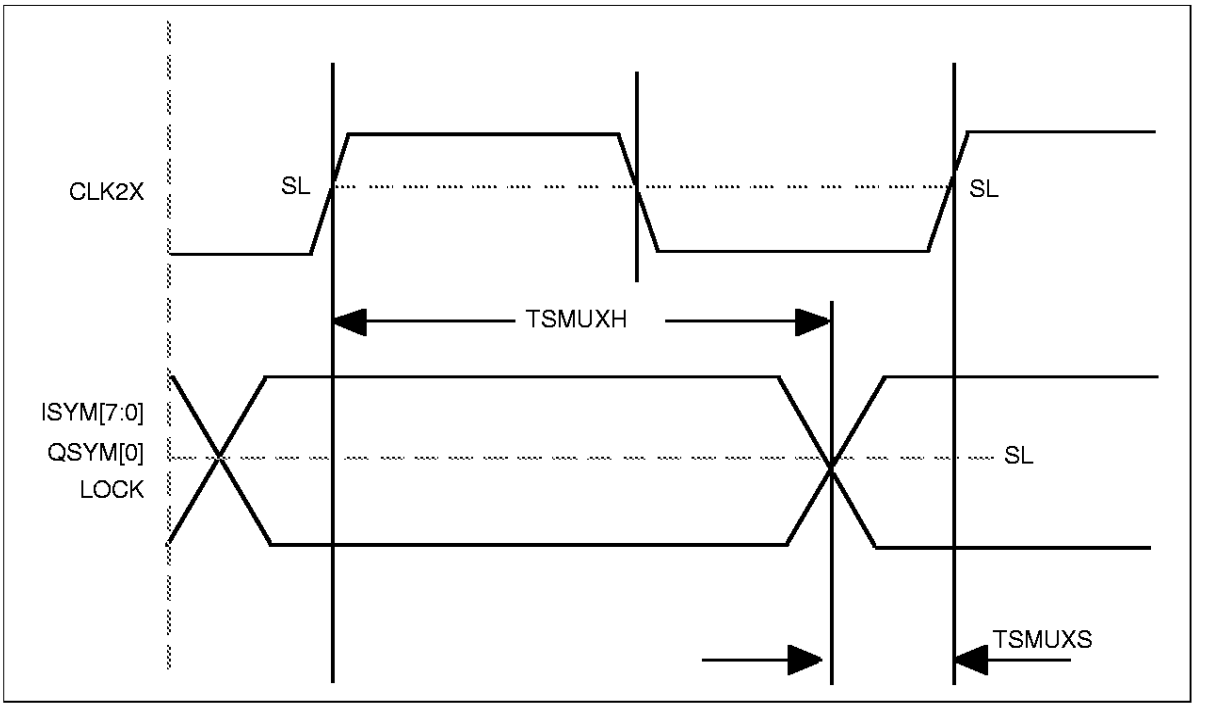


Figure 11 QAM Outputs in Multiplex Mode

Table 15. QAM Outputs in Multiplex Mode

Sym	PIN	Min	Typ	Max	U	Test Conditions	Description
TSMUXS	ISYM[7:0] QSYM[0] LOCK	20			ns	SL= 0.5Vdd Cload=30pf	Setup time of ISYM[7:0], QSYM[0] and LOCK wrt rising edge of CLK2X when output MUX mode is selected.
TSMUXH	ISYM[7:0] QSYM[0] LOCK	20			ns		Hold time of ISYM[7:0], QSYM[0] and LOCK wrt rising edge of CLK2X when output MUX mode is selected

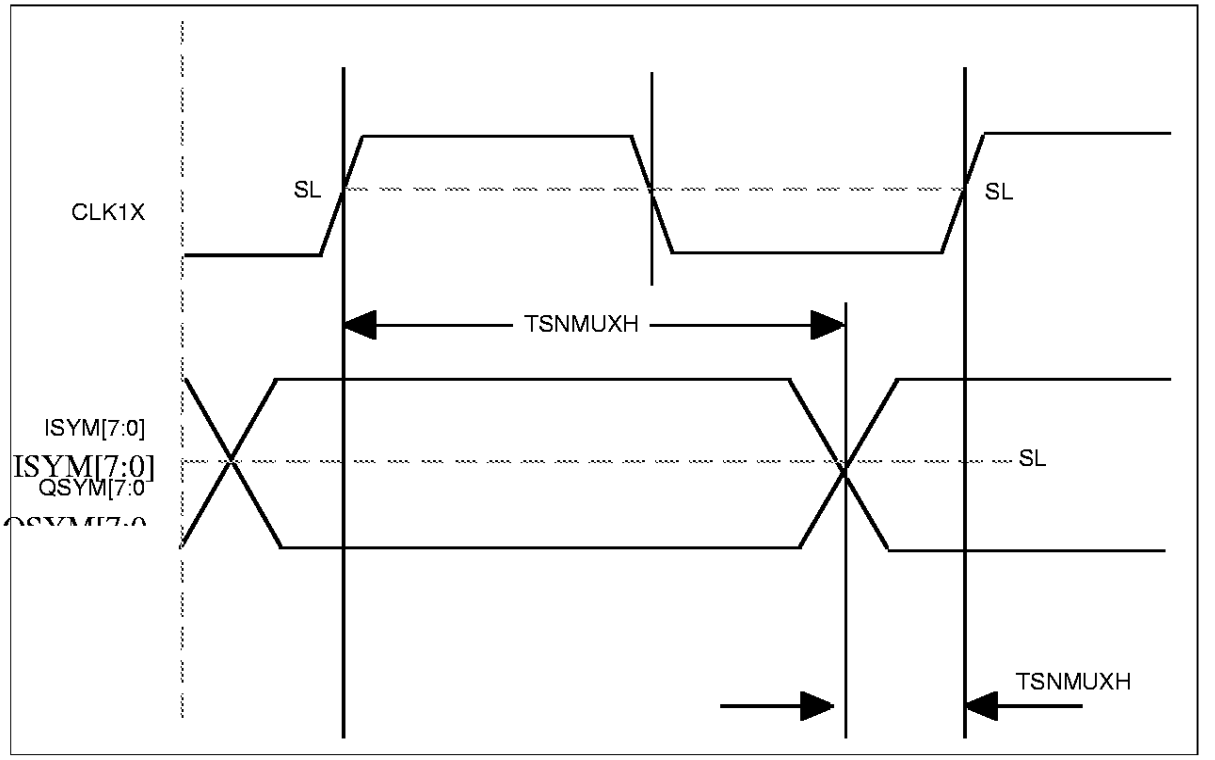


Figure 12 QAM Outputs in Nonmultiplex Mode

Table 16. QAM Outputs in Multiplex Mode

Sym	Pin	Min	Typ	Max	Units	Test Conditions	Description
TSNMUXS	ISYM[7:0] QSYM[7:0]	20			ns	SL= 0.5Vdd Cload=30pf	Setup time of ISYM[7:0], QSYM[7:0] wrt rising edge of CLK1X when output NON-MUX mode is selected.
TSNMUXH	ISYM[7:0] QSYM[7:0]	20			ns	SL= 0.5Vdd Cload=30pf	Hold time of ISYM[7:0], QSYM[7:0] wrt rising edge of CLK1X when output NON-MUX mode is selected.

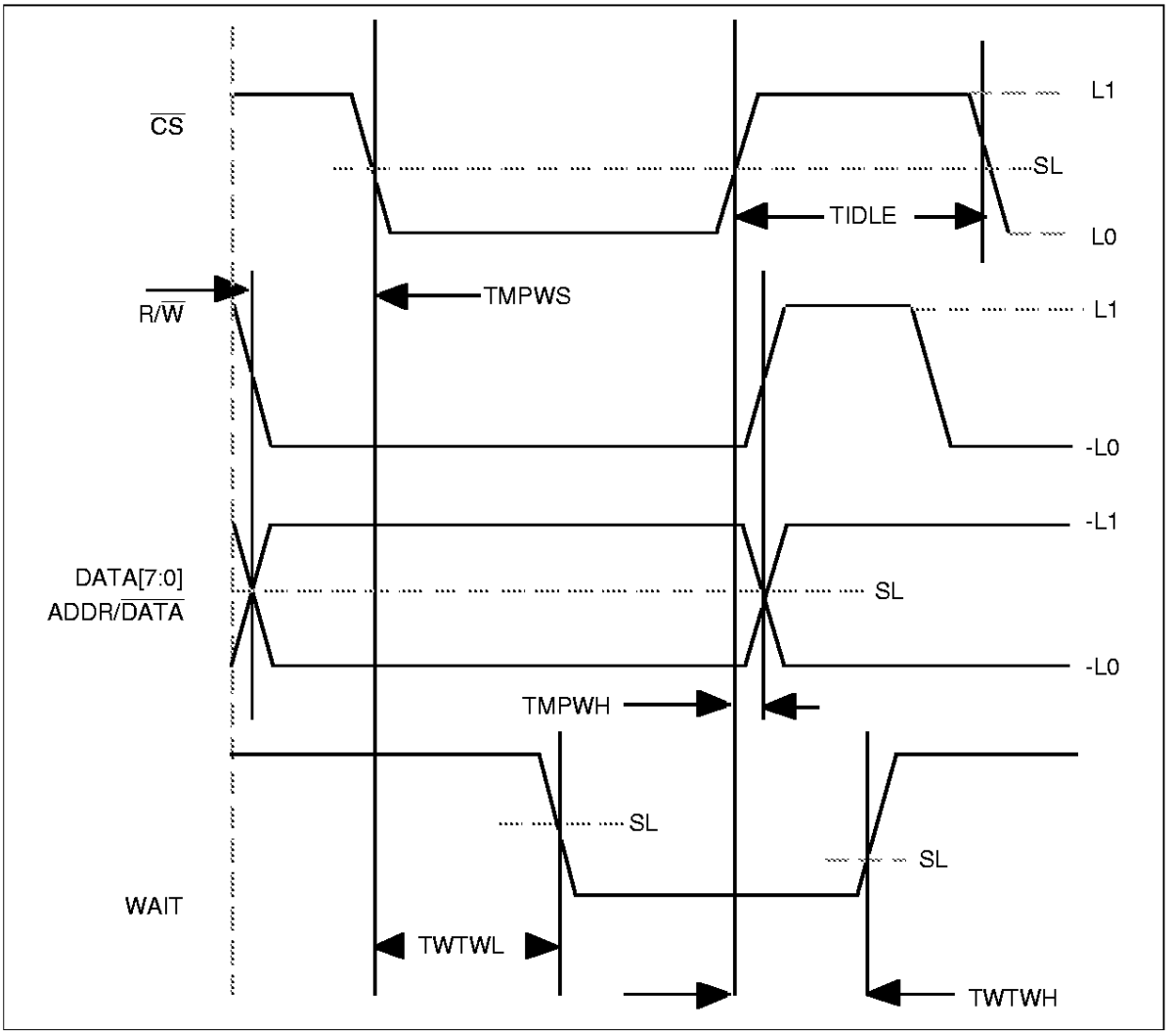


Figure 13 Microprocessor Write Cycle

Table 17. Microprocessor Write Cycle

Sym	Pin	Min	Typ	Max	Units	Test Conditions	Description
TMPWS	Data[7:0] ADDR/$\overline{DAT}$ $\overline{A}$ R/$\overline{W}$	TC4XIP			ns	SL= 0.5Vdd L1 = 0.7Vdd L0=0.3Vdd	Setup Time of R/$\overline{W}$,ADDR/$\overline{DATA}$, and DATA[7:0] wrt $\overline{CS}$.
TMPWH	Data[7:0] ADDR/$\overline{DAT}$ $\overline{A}$ R/$\overline{W}$	TC4XIP			ns		Hold Time of R/$\overline{W}$,ADDR/$\overline{DATA}$, and DATA[7:0] wrt $\overline{CS}$.
TWTWL	WAIT			TC4XIP *2 + 18	ns	SL=0.5Vdd Cload=100pf Rpullp = 1K	Delay from falling edge of $\overline{CS}$ to falling edge of WAIT.
TWTWH	WAIT			10	ns	Rpullup = 1K	Delay from rising edge of $\overline{CS}$ to rising edge of WAIT.
TIDLE	$\overline{CS}$	TC4XIP *2			ns	SL= 0.5Vdd L1 = 0.7Vdd L0=0.3Vdd	Delay between consecutive microprocessor transactions.

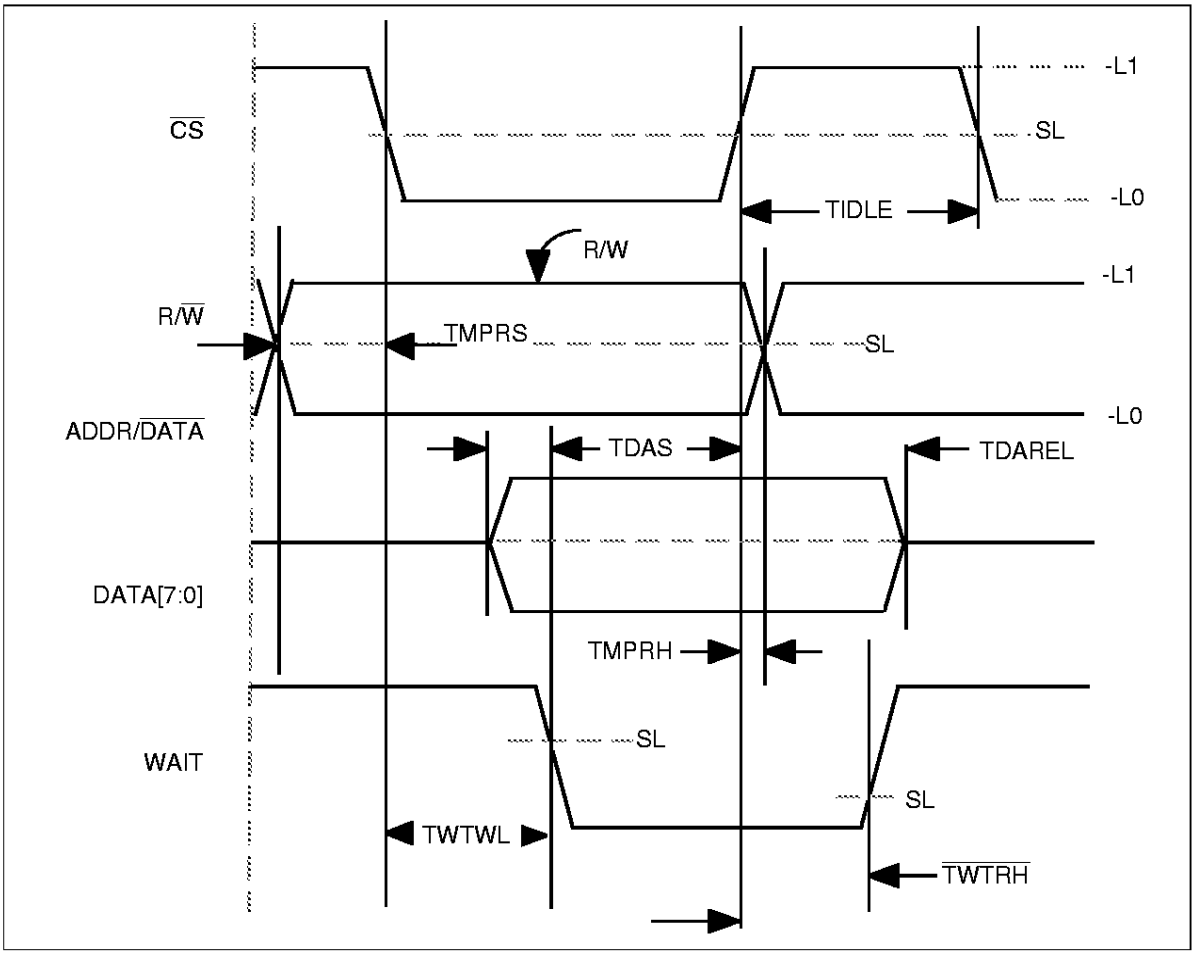


Figure 14 Microprocessor Read Cycle

Table 18. Microprocessor Read Cycle

Sym	Pin	Min	Typ	Max	Units	Test Conditions	Description
TMPRS	ADDR/$\overline{DATA}$ R/$\overline{W}$	TC4XIP			ns	SL= 0.5Vdd L1=0.7Vdd L0=0.3Vdd	Setup Time of R/$\overline{W}$,ADDR/$\overline{DATA}$, and DATA[7:0] wrt $\overline{CS}$.
TMPRH	ADDR/$\overline{DATA}$ R/$\overline{W}$	TC4XIP			ns	SL= 0.5Vdd L1=0.7Vdd L0=0.3Vdd	Hold Time of R/$\overline{W}$,ADDR/$\overline{DATA}$, and DATA[7:0] wrt $\overline{CS}$.
TWTRL	WAIT			TC4XIP *6+ 18	ns	SL=0.5Vdd Cload=100pf Rpullup=1K	Delay from falling edge of $\overline{CS}$ to falling edge of WAIT.
TWTRH	WAIT			10	ns	SL=0.5V Cload=100pf Rpullup=1K	Delay from rising edge of $\overline{CS}$ to rising edge of WAIT.
TDAS	DATA[7:0]	0			ns	SL=0.5V Cload=100pf	Setup time of DATA[7:0] wrt falling edge of WAIT.
TDAREL	DATA[7:0]	10			ns	SL=0.5V Cload=100pf	Delay between rising edge of $\overline{CS}$ and tristating of DATA
TIDLE	$\overline{CS}$	TC4XIP *2			ns	SL= 0.5Vdd L1=0.7Vdd L0=0.3Vdd	Delay between consecutive microprocessor transactions.

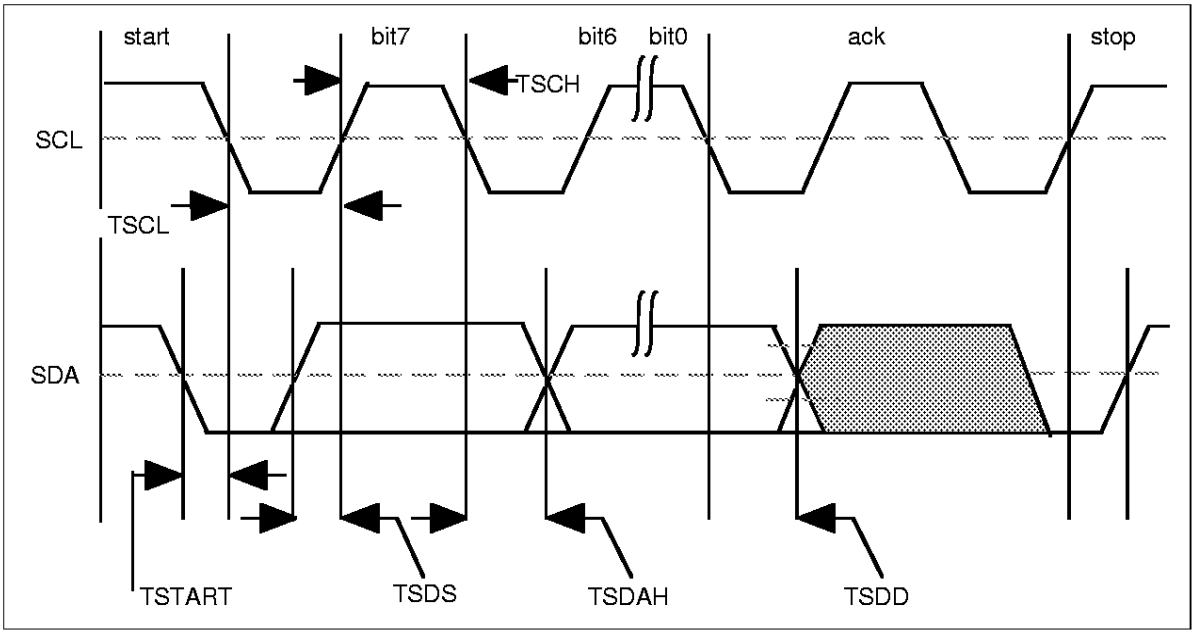


Figure 15 Microprocessor Read Cycle

Table 19. Microprocessor Read Cycle

Sym	PIN	Min	Typ	Max	Units	Test Conditions	Description
TSTART	SCL ($\overline{CS}$)	0.6			us	SL= 0.5Vdd L1=0.7Vdd L0=0.3Vdd	Setup time of SDA falling edge(start) with respect to falling edge of SCL.
TSTOP	SDA (DATA(0))	0.6			us		Setup time of SCL rising edge wrt rising edge of SDA(stop).
TSCL	SCL ($\overline{CS}$)	1.3			us		Low time of SCL clock pulse.
TSCH	SCL ($\overline{CS}$)	0.6			us		High time of SCL clock pulse.
TSDS	SDA (DATA(0))	TC4XIP			ns		Setup time of SDA wrt rising edge of SCL.
TSDH	SDA (DATA(0))	TC4XIP			ns		Hold time of SDA wrt falling edge of SCL.
TSDD	SDA (DATA(0))				ns	SL=0.5V (0-1 Transition) SL+0.5Vdd (1-0 Transition) Rpullup=1K CLoad=100pf	Delay from falling edge of SCL to SDA valid when HD49428F is driving SDA (eg acknowledge on write).

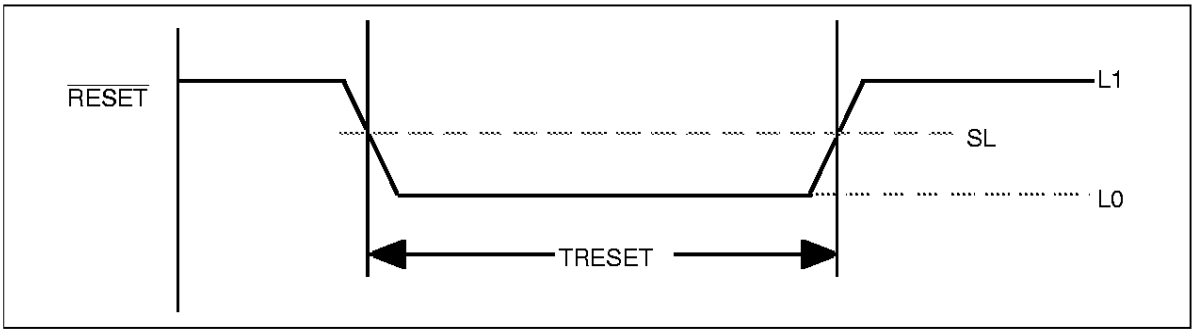


Figure 16 Reset

Table 20. Reset

Sym	PIN	Min	Typ	Max	Units	Test Conditions	Description
$\overline{TRESET}$	$\overline{RESET}$	TC4XIP	*10		ns	SL=0.5Vdd L1=0.7Vdd L0= 0.3Vdd	Low time of $\overline{RESET}$ signal

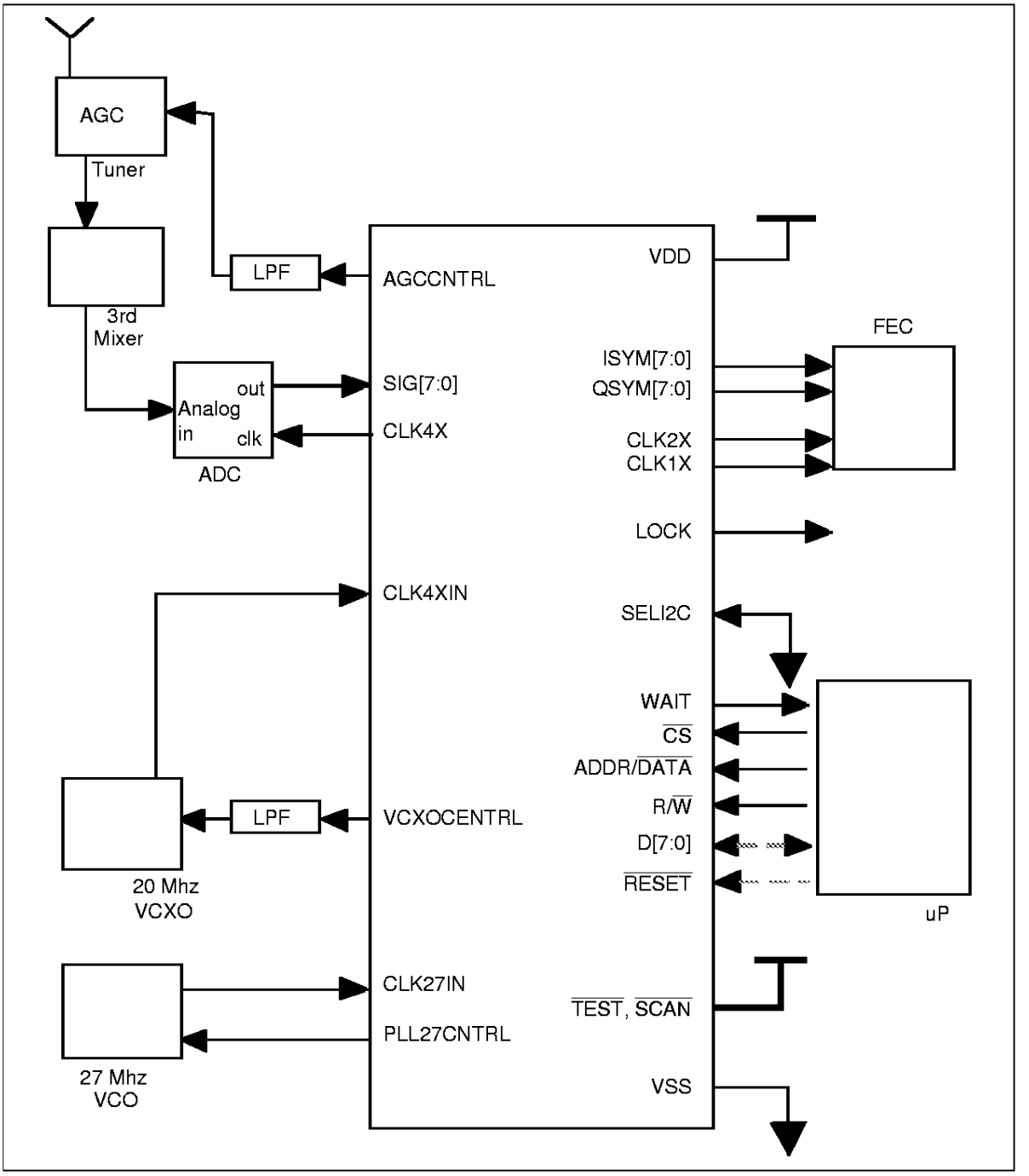


Figure 17 General Purpose µP Controller

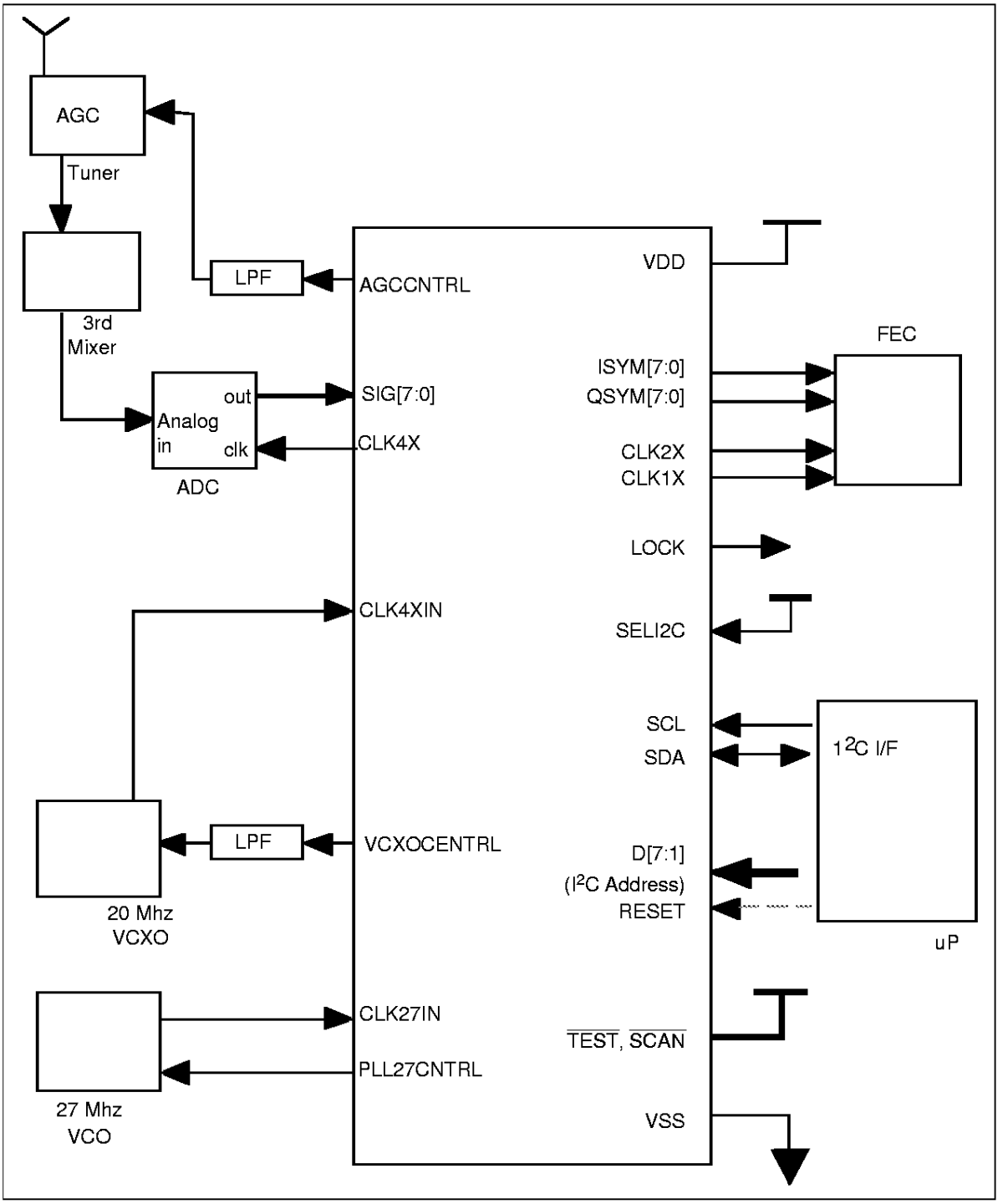


Figure 18 I²C Serial Controller

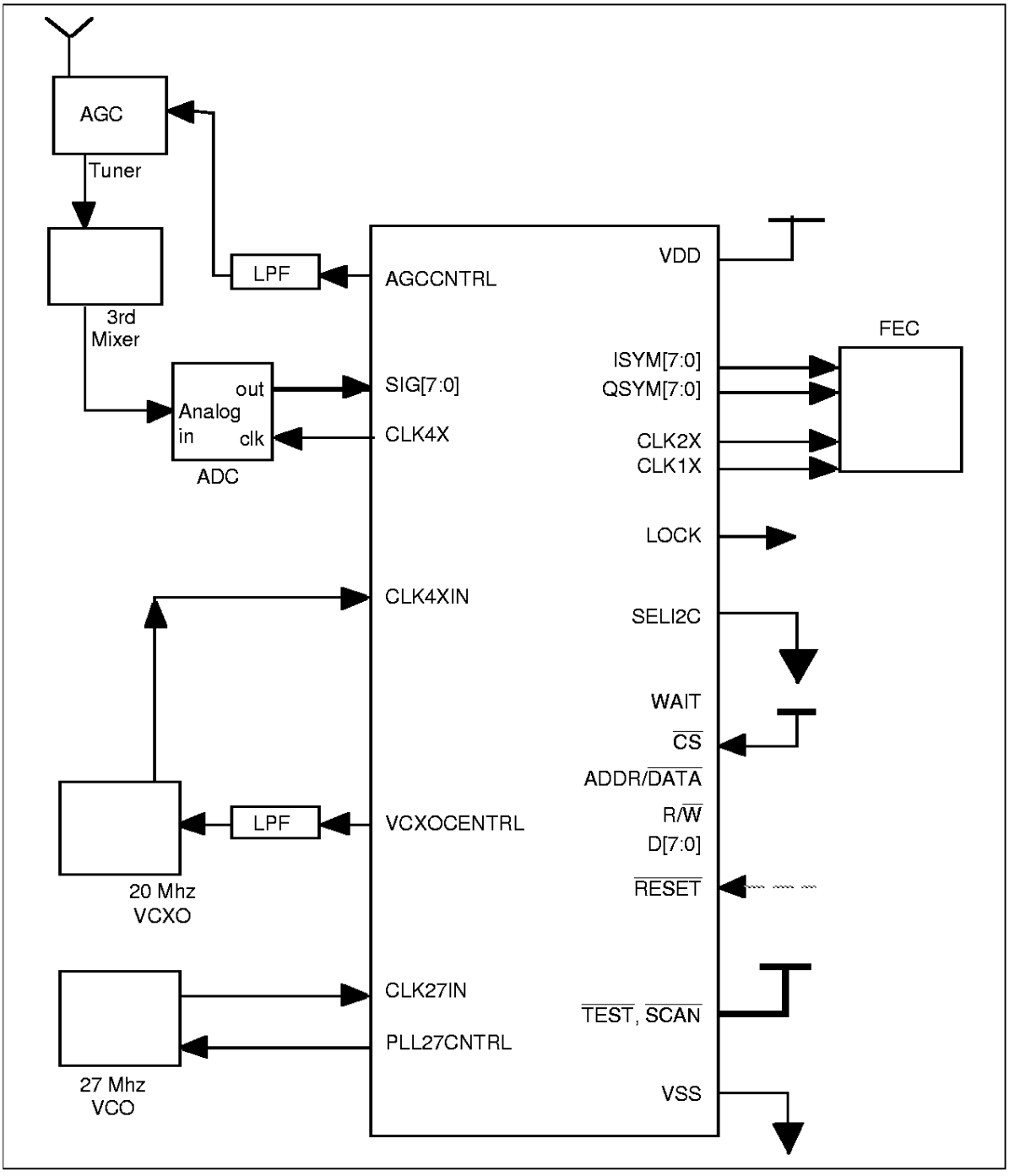


Figure 19 Stand-Alone Operation