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001682

# Digital Signal Processor

T1682

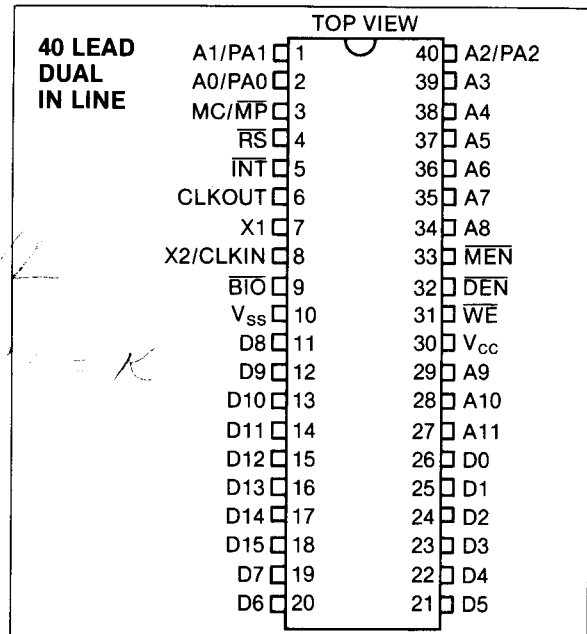
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## FEATURES:

- 160ns instruction cycle (max)
- 144 word on-chip data RAM
- ROMless version-DSP320C10
- 1.5K word on-chip program ROM – DSP320CM10
- External memory expansion to a total of 4K words at full speed
- 16-bit instruction/data word
- 32-bit ALU/Accumulator
- 16 x 16-bit multiply in 160ns (max)
- 0 to 15-bit barrel shifter
- Eight input and eight output channels
- 16-bit bidirectional data bus with 50-megabits-per-second transfer rate
- Interrupt with full context save
- Signed two's complement fixed-point arithmetic
- CMOS technology
- Single 5-V supply
- Two versions available:
  - DSP320C10 . . . . .20.5MHz Clock
  - DSP320C10-25 . . . . .25MHz Clock

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PLAC  
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## PIN CONFIGURATION



## DESCRIPTION

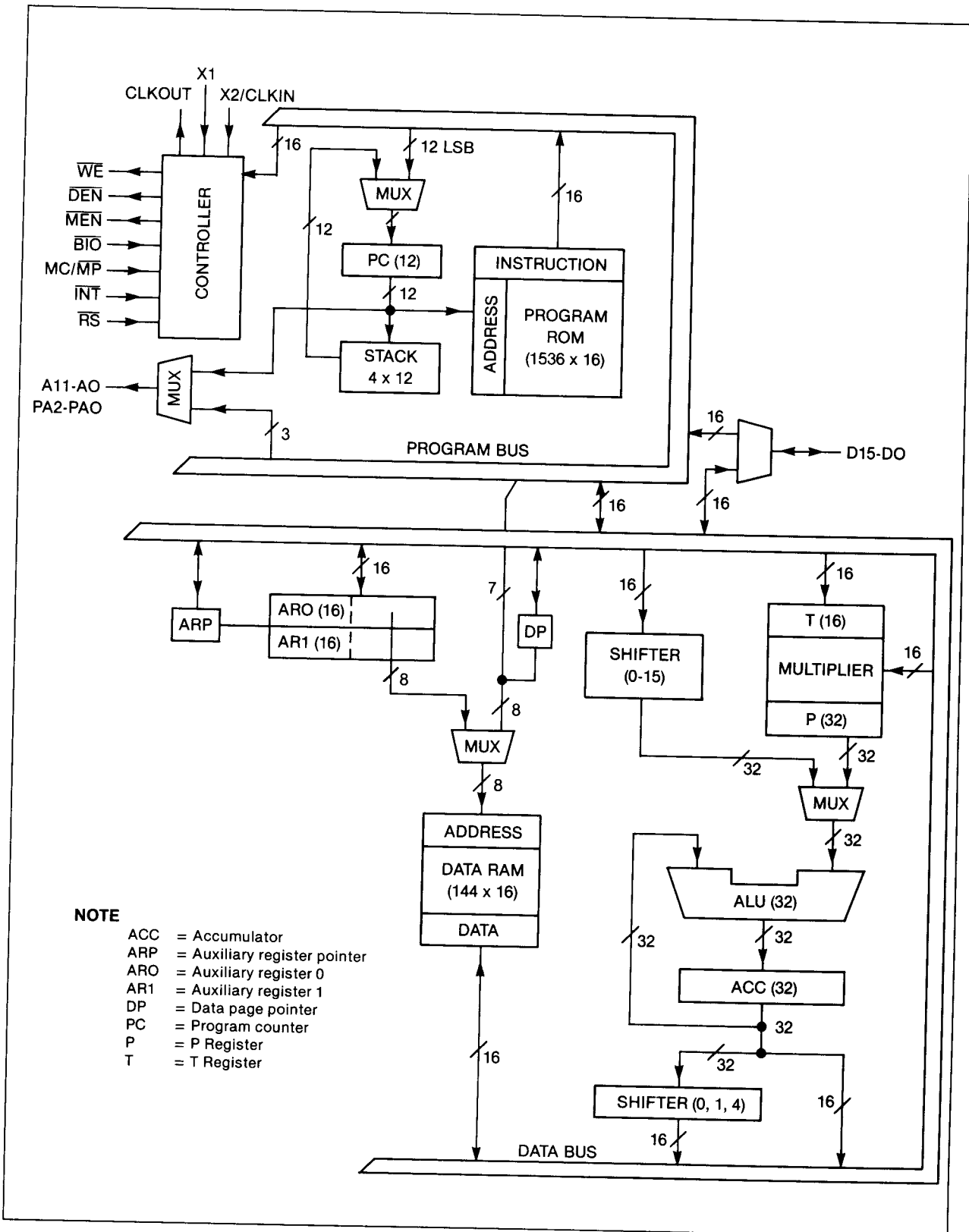
The DSP320C10 is the first low power CMOS member of the General Instrument DSP320 family of digital signal processors, designed to support a wide range of high-speed or numeric-intensive applications. This device is a CMOS pin-for-pin compatible version of the industry standard DSP32010 digital signal processor. The 16/32-bit single-chip microcomputer combines the flexibility of a high-speed controller with the numerical capability of an array processor, thereby offering an inexpensive alternative to multichip bit-slice processors. The DSP320 family contains MOS microcomputers capable of executing six million instructions per second. This high throughput is the result of the comprehensive, efficient, and easily programmed instruction set and of the highly pipelined architecture. Special instructions have been incorporated to speed the execution of digital signal processing (DSP) algorithms.

The DSP320 family's unique versatility and power give the design engineer solutions to a variety of complicated applications. In addition, these microcomputers are capable of providing the multiple functions often required for a single application. For example, the DSP320 family can enable an industrial robot to synthesize and recognize speech, sense objects with radar or optical intelligence, and perform mechanical operations through digital servo loop computations.

## PIN NOMENCLATURE

SIGNATURE	I/O	DEFINITION
A11-AO/ PA2-PAO	OUT	External address bus. I/O port address multiplexed over PA2-PA0.
BTO	IN	External polling input for bit test and jump operations.
CLKOUT	OUT	System clock output, 1/4 crystal/CLKIN frequency.
D15-D0	I/O	16-bit data bus.
DEN	OUT	Data enable indicates the processor accepting input data on D15-D0.
INT	IN	Interrupt.
MC/MP	IN	Memory mode select pin. High selects microcomputer mode. Low selects microprocessor mode.
MEN	OUT	Memory enable indicates that D15-D0 will accept external memory instruction.
RS	IN	Reset used to initialize the device.
V <sub>CC</sub>	IN	Power.
V <sub>SS</sub>	IN	Ground.
WE	OUT	Write enable indicates valid data on D15-D0.
X1	IN	Crystal input.
X2/CLKIN	IN	Crystal input or external clock input.

FUNCTIONAL BLOCK DIAGRAM



## ARCHITECTURE

The DSP320 family utilizes a modified Harvard architecture for speed and flexibility. In a strict Harvard architecture, program and data memory lie in two separate spaces, permitting a full overlap of the instruction fetch and execution. The DSP320 family's modification of the Harvard architecture allows transfers between program and data spaces, thereby increasing the flexibility of the device. This modification permits coefficients stored in program memory to be read into the RAM, eliminating the need for a separate coefficient ROM. It also makes available immediate instructions and subroutines based on computed values.

The DSP320C10 utilizes hardware to implement functions that other processors typically perform in software. For example, this device contains a hardware multiplier to perform a multiplication in a single 160-ns cycle. There is also a hardware barrel shifter for shifting data on its way into the ALU. Finally, extra hardware has been included so that auxiliary registers, which provide indirect data RAM addresses, can be configured in an autoincrement/decrement mode for single-cycle manipulation of data tables. This hardware-intensive approach gives the design engineer the type of power previously unavailable on a single chip.

### 32-bit ALU/accumulator

The DSP320C10 contains a 32-bit ALU and accumulator that support double-precision arithmetic. The ALU operates on 16-bit words taken from the data RAM or derived from immediate instructions. Besides the usual arithmetic instructions, the ALU can perform Boolean operations, providing the bit manipulation ability required of a high-speed controller.

### Shifters

A barrel shifter is available for left-shifting data 0 to 15 places before it is loaded into, subtracted from, or added to the accumulator. This shifter extends the high-order bit of the data word and zero-fills the low-order bits for two's complement arithmetic. A second shifter left-shifts the upper half of the accumulator 0, 1, or 4 places while it is being stored in the data RAM. Both shifters are very useful for scaling and bit extraction.

### 16 x 16-bit parallel multiplier

The DSP320C10's multiplier performs a 16 x 16-bit, two's complement multiplication in one 160-ns instruction cycle. The 16-bit T Register temporarily stores the multiplicand; the P Register stores the 32-bit result. Multiplier values either come from the data memory or are derived immediately from the MPYK (multiply immediate) instruction word. The fast on-chip multiplier allows the DSP320C10 to perform such fundamental operations as convolution, correlation, and filtering at the rate of 3 million samples per second.

### Program Memory Expansion

The DSP320C10 is equipped with a 1536-word ROM which can be mask-programmed at the factory with a customer's program. It can also execute from an additional 2560 words of off-chip program memory at full speed. This memory expansion capability is especially useful for those situations where a customer has a number of different applications that share the same subroutines. In this case, the common subroutines can be stored on-chip while the application specific code is stored off-chip.

The DSP320C10 can operate in either of the following memory modes via the MC/MP pin:

Microcomputer Mode (MC) — Instruction addresses 0-1535 fetched from on-chip ROM. Those with addresses 1536-4095 fetched from off-chip memory at full speed.

Microprocessor Mode (MP) — Full speed execution from all 4096 off-chip instruction addresses.

*Handwritten notes:*  
1536-4095  
Microprocessor Mode (MP) — Full speed execution from all 4096 off-chip instruction addresses.

The ability of the DSP320C10 to execute at full speed from off-chip memory provides the following important benefits:

- Easier prototyping and development work than is possible with a device that can address only on-chip ROM
- Purchase of a standard off-the-shelf product rather than a semi-custom mask-programmed device
- Ease of updating code
- Execution from external RAM
- Downloading of code from another microprocessor
- Use of off-chip RAM to expand data storage capability

**Input/output**

The DSP320C10's 16-bit parallel data bus can be utilized to perform I/O functions at burst rates of 50 million bits per second. Available for interfacing to peripheral devices are 128 input and 128 output bits consisting of eight 16-bit multiplexed input ports and eight 16-bit multiplexed output ports. In addition, a polling input for bit test and jump operations (BIO) and an interrupt pin (INT) have been incorporated for multi-tasking.

**Interrupts and subroutines**

The DSP320C10 contains a four-level hardware stack for saving the contents of the program counter during interrupts and subroutine calls. Instructions are available for saving the DSP320C10's complete context. The instructions, PUSH stack from accumulator, and POP stack to accumulator permit a level of nesting restricted only by the amount of available RAM. The interrupts used in the DSP320C10 are maskable.

**INSTRUCTION SET**

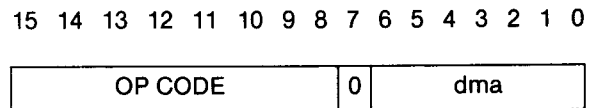
The DSP320C10's comprehensive instruction set supports both numeric-intensive operations, such as signal processing, and general purpose operations, such as high-speed control. The instruction set, explained in Tables 1 and 2, consists primarily of single-cycle single-word instructions, permitting execution rates of up to six million instructions per second. Only infrequently used branch and I/O instructions are multicycle.

The DSP320C10 also contains a number of instructions that shift data as part of an arithmetic operation. These all execute in a single cycle and are very useful for scaling data in parallel with other operations.

Three main addressing modes are available with the DSP320C10 instruction set: direct, indirect, and immediate addressing.

**Direct Addressing**

In direct addressing, seven bits of the instruction word concatenated with the data page pointer form the data memory address. This implements a paging scheme in which the first page contains 128 words and the second page contains 16 words. In a typical application, infrequently accessed variables, such as those used for servicing an interrupt, are stored on the second page. The instruction format for direct addressing is shown below.



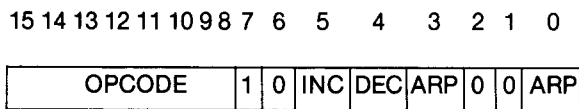
Bit 7 = 0 defines direct addressing mode. The opcode is contained in bits 15 through 8. Bits 6 through 0 contain data memory address.

The seven bits of the data memory address (dma) field can directly address up to 128 words (1 page) of data memory. Use of the data memory page pointer is required to address the full 144 words of data memory.

Direct addressing can be used with all instructions requiring data operands except for the immediate operand instructions.

**Indirect addressing**

Indirect addressing forms the data memory from the least significant eight bits of one of two auxiliary registers, AR0 and AR1. The auxiliary register pointer (ARP) selects the current auxiliary register. The auxiliary registers can be automatically incremented or decremented in parallel with the execution of any indirect instruction to permit single-cycle manipulation of data tables. The instruction format for indirect addressing is as follows:



Bit 7 = 1 defines indirect addressing mode. The opcode is contained in bits 15 through 8. Bits 7 through 0 contain indirect addressing control bits.

Bit 3 and bit 0 control the Auxiliary Register Pointer (ARP). If bit 3 = 0, then the content of bit 0 is loaded into the ARP. If bit 3 = 1, then content of ARP remain unchanged. ARP = 0 defines the contents of ARO as memory address. ARP = 1 defines the contents of AR1 as memory address.

Bit 5 and bit 4 control the auxiliary registers. If bit 5 = 1, then the ARP defines which auxiliary register is to be incremented by 1. If bit 4 = 1, then the ARP defines which auxiliary register is to be decremented by 1. If bit 5 or bit 4 are zero, then neither auxiliary register is incremented or decremented. Bits 6, 2, and 1 are reserved and should always be programmed to zero.

Indirect addressing can be used with all instructions requiring data operands, except for the immediate operand instructions.

**Immediate Addressing**

The DSP320C10 instruction set contains special "immediate" instructions. These instructions derive data from part of the instruction word rather than from the data RAM. Some very useful immediate instructions are multiply immediate (MPYK), load accumulator immediate (LACK), and load auxiliary register immediate (LARK).

**TABLE 1 – INSTRUCTION SYMBOLS**

SYMBOL	MEANING
ACC	Accumulator
D	Data memory address field
I	Addressing mode bit
K	Immediate operand field
PA	3-bit port address field
R	1-bit operand field specifying auxiliary register
S	4-bit left-shift code
X	3-bit accumulator left-shift field

**TABLE 2 – DSP320C10 INSTRUCTION SET SUMMARY**

Accumulator Instructions (See Table 1 for symbol explanations)

MNEMONIC	DESCRIPTION	NO. CYCLES	NO. WORDS	OPCODE INSTRUCTION REGISTER															
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ABS	Absolute value of accumulator	1	1	0	1	1	1	1	1	1	1	1	0	0	0	1	0	0	0
ADD	Add to accumulator with shift	1	1	0	0	0	0	← S →	I	← D →									
ADDH	Add to high-order accumulator bits	1	1	0	1	1	0	0	0	0	0	I	← D →						
ADDS	Add to accumulator with no sign extension	1	1	0	1	1	0	0	0	0	0	I	← D →						
AND	AND with accumulator	1	1	0	1	1	1	1	0	0	1	I	← D →						
LAC	Load accumulator with shift	1	1	0	0	1	0	← S →	I	← D →									
LACK	Load accumulator immediate	1	1	0	1	1	1	1	1	1	0	← K →							
OR	OR with accumulator	1	1	0	1	1	1	1	0	1	0	I	← D →						
SACH	Store high-order accumulator bits with shift	1	1	0	1	0	1	1	← X →	I	← D →								
SACL	Store low-order accumulator bits	1	1	0	1	0	1	0	0	0	0	I	← D →						
SUB	Subtract from accumulator with shift	1	1	0	0	0	1	← S →	I	← D →									
SUBC	Conditional subtract (for divide)	1	1	0	1	1	0	0	1	0	0	I	← D →						
SUBH	Subtract from high-order accumulator bits	1	1	0	1	1	0	0	0	1	0	I	← D →						
SUBS	Subtract from accumulator with no sign extension	1	1	0	1	1	0	0	0	0	1	I	← D →						
XOR	Exclusive OR with accumulator	1	1	0	1	1	1	1	0	0	0	I	← D →						
ZAC	Zero accumulator	1	1	0	1	1	1	1	1	1	1	1	0	0	0	1	0	0	1
ZALH	Zero accumulator and load high-order bits	1	1	0	1	1	0	0	1	0	1	I	← D →						
ZALS	Zero accumulator and load low-order bits with no sign extension	1	1	0	1	1	0	0	1	1	0	I	← D →						

**Auxiliary Register and Data Page Pointer Instructions**

MNEMONIC	DESCRIPTION	NO. CYCLES	NO. WORDS	OPCODE INSTRUCTION REGISTER															
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LAR	Load auxiliary register	1	1	0	0	1	1	1	0	0	R	I	← D →						
LARK	Load auxiliary register immediate	1	1	0	1	1	1	0	0	0	R	← K →							
LARP	Load auxiliary register pointer immediate	1	1	0	1	1	0	1	0	0	0	1	0	0	0	0	0	0	K
LDP	Load data memory page pointer	1	1	0	1	1	0	1	1	1	1	I	← D →						
LDPK	Load data memory page pointer immediate	1	1	0	1	1	0	1	1	1	0	0	0	0	0	0	0	0	K
MAR	Modify auxiliary register and pointer	1	1	0	1	1	0	1	0	0	0	I	← D →						
SAR	Store auxiliary register	1	1	0	0	1	1	0	0	0	R	I	← D →						

**TABLE 2 – DSP320C10 INSTRUCTION SET SUMMARY (continued)**

**Branch Instructions**

MNEMONIC	DESCRIPTION	NO. CYCLES	NO. WORDS	OPCODE INSTRUCTION REGISTER															
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
B	Branch unconditionally	2	2	1	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0
				0	0	0	0	← BRANCH ADDRESS →								0	0	0	0
BANZ	Branch on auxiliary register not zero	2	2	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0
BGEZ	Branch if accumulator ≥ 0	2	2	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
				0	0	0	0	← BRANCH ADDRESS →								0	0	0	0
BGZ	Branch if accumulator > 0	2	2	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
				0	0	0	0	← BRANCH ADDRESS →								0	0	0	0
BIOZ	Branch on $\overline{BIO} = 0$	2	2	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0
				0	0	0	0	← BRANCH ADDRESS →								0	0	0	0
BLEZ	Branch if accumulator ≤ 0	2	2	1	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0
				0	0	0	0	← BRANCH ADDRESS →								0	0	0	0
BLZ	Branch if accumulator < 0	2	2	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0
				0	0	0	0	← BRANCH ADDRESS →								0	0	0	0
BNZ	Branch if accumulator ≠ 0	2	2	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
				0	0	0	0	← BRANCH ADDRESS →								0	0	0	0
BV	Branch on overflow	2	2	1	1	1	1	0	1	0	1	0	0	0	0	0	0	0	0
				0	0	0	0	← BRANCH ADDRESS →								0	0	0	0
BZ	Branch if accumulator = 0	2	2	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
				0	0	0	0	← BRANCH ADDRESS →								0	0	0	0
CALA	Call subroutine from accumulator	2	1	0	1	1	1	1	1	1	1	1	0	0	0	1	1	0	0
CALL	Call subroutine immediately	2	2	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
				0	0	0	0	← BRANCH ADDRESS →								0	0	0	0
RET	Return from subroutine or interrupt routine	2	1	0	1	1	1	1	1	1	1	1	0	0	0	1	1	0	1

**T Register, P Register, and Multiply Instructions**

MNEMONIC	DESCRIPTION	NO. CYCLES	NO. WORDS	OPCODE INSTRUCTION REGISTER																
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
APAC	Add P register to accumulator	1	1	0	1	1	1	1	1	1	1	1	0	0	0	1	1	1	1	
LT	Load T register	1	1	0	1	1	0	1	0	1	0	1	← D →							
LTA	LTA combines LT and APAC into one instruction	1	1	0	1	1	0	1	1	0	0	1	← D →							
LTD	LTD combines LT, APAC, and DMOV into one instruction	1	1	0	1	1	0	1	0	1	1	1	← D →							
MPY	Multiply with T register, store product in P register	1	1	0	1	1	0	1	1	0	1	1	← D →							
MPYK	Multiply T register with immediate operand; store product in P register	1	1	1	0	0	← K →													
PAC	Load accumulator from P register	1	1	0	1	1	1	1	1	1	1	1	1	0	0	0	1	1	1	
SPAO	Subtract P register from accumulator	1	1	0	1	1	1	1	1	1	1	1	1	0	0	1	0	0	0	

**TABLE 2 – DSP320C10 INSTRUCTION SET SUMMARY (concluded)**

**Control Instructions**

MNEMONIC	DESCRIPTION	NO. CYCLES	NO. WORDS	OPCODE INSTRUCTION REGISTER																	
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
DINT	Disable interrupt	1	1	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1
EINT	Enable interrupt	1	1	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	0
LST	Load status register	1	1	0	1	1	1	1	0	1	1	1	1	←	D	→					
NOP	No operation	1	1	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
POP	POP stack to accumulator	2	1	0	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1	0	1
PUSH	PUSH stack from accumulator	2	1	0	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1	0	0
ROVM	Reset overflow mode	1	1	0	1	1	1	1	1	1	1	1	1	0	0	0	1	0	1	0	
SOVM	Set overflow mode	1	1	0	1	1	1	1	1	1	1	1	1	0	0	0	1	0	1	1	
SST	Store status register	1	1	0	1	1	1	1	1	0	0	1	1	←	D	→					

**I/O and Data Memory Operations**

MNEMONIC	DESCRIPTION	NO. CYCLES	NO. WORDS	OPCODE INSTRUCTION REGISTER																	
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
DMOV	Copy contents of data memory location into next location	1	1	0	1	1	0	1	0	0	1	1	1	←	D	→					
IN	Input data from port	2	1	0	1	0	0	0	←	PA	→	1	1	←	D	→					
OUT	Output data to port	2	1	0	1	0	0	1	←	PA	→	1	1	←	D	→					
TBLR	Table read from program memory to data RAM	3	1	0	1	1	0	0	1	1	1	1	1	←	D	→					
TBLW	Table write from data RAM to program	3	1	0	1	1	1	1	1	0	1	1	1	←	D	→					

**DEVELOPMENT SYSTEMS AND SOFTWARE SUPPORT**

XDS/320 is a complete line of development support tools for the DSP320 family. Since it consists of host-independent hardware along with software that runs on a variety of host computers (e.g., TI990, VAX (VMS), IBM370), XDS/320 is an inexpensive solution to development support.

XDS/320 supports all phases of developing an application with the DSP320 family. In the initial phase, the DSP320C10 evaluation module is used to characterize the performance of the DSP320C10. Once this evaluation phase is com-

plete, sophisticated development operations are performed with the TMS32010 Evaluation Module (EVM), the XDS/320 macro assembler, linker, simulator, and emulator. The XDS/320 macro assembler and linker are used to translate program modules into object code and link them together. This puts the program modules into a form which can be loaded into the XDS/320 simulator or emulator. The simulator provides a quick means for initially debugging DSP320C10 software while the XDS/320 emulator, using the self-emulation capability of the DSP320C10, provides the in-circuit emulation necessary to perform system level debug efficiently.

**Absolute maximum ratings over specified temperature range (unless otherwise noted)\*\***

Supply voltage,  $V_{CC}$  ..... - 0.3V to 7V  
 All input voltages ..... - 0.3V to 15V  
 Output voltage ..... - 0.3V to 15V  
 DSP320C10 continuous power dissipation . . . . .3W  
 DSP320C10-25 continuous power dissipation .35W  
 Air temperature range above  
     operating device ..... 0°C to 70°C  
 Storage temperature range . . . . - 55°C to + 150°C

Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied – operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.  
 Data labeled “typical” is presented for design guidance only and is not guaranteed.

**D.C. CHARACTERISTICS**

Characteristics	DSP320C10			DSP320C10-25			Unit	Conditions
	Min	Nom	Max	Min	Nom	Max		
Supply voltage, VCC	4.5	5	5.5	4.75	5	5.25	V	
Supply voltage, VSS	–	0	–	–	0	–	V	
High-level input voltage, VIH All inputs except CLKIN CLKIN	2.0	–	–	2.0	–	–	V	
	.56V <sub>CC</sub>	–	–	.56V <sub>CC</sub>	–	–	V	
Low-level input voltage, VIL (all inputs)	–	–	.8	–	–	.8	V	
High-level output voltage VOH	VCC – .4	–	–	VCC – .4	–	–	V	IOH = 20uA
	2.4	–	–	2.4	–	–	V	IOH = 300uA
Low-level output voltage VOL	–	–	0.4	–	–	0.4	V	IOL = 2mA
Off-state output current IOZ	–	–	20	–	–	20	uA	DSP320C10: VCC = 5.5V, VO = VCC – .4V DSP320C10-25: VCC = 5.25V, VO = VCC – .4V DSP320C10: VCC = 5.5V, VO = 0.4V DSP320C10-25: VCC = 5.25V, VO = 0.4V
	–	–	– 20	–	–	– 20	uA	
Input current I <sub>I</sub>	–	–	± 50	–	–	± 50	uA	VI = VSS to VCC
Supply current ICC Tested with Clocks running.	–	–	50	–	–	65	mA	DSP320C10: VCC = 5.5V, fx = 6.7 to 20.5MHz DSP320C10-25: VCC = 5.25V, fx = 15.0 to 25MHz
Input capacitance C <sub>i</sub> Data bus All others	–	25	–	–	25	–	pF	f = 1MHz, all other pins OV
	–	15	–	–	15	–	pF	
Output capacitance C <sub>o</sub> Data bus All others	–	25	–	–	25	–	pF	
	–	10	–	–	10	–	pF	

\*\*All typical values are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

### CLOCK CHARACTERISTICS AND TIMING

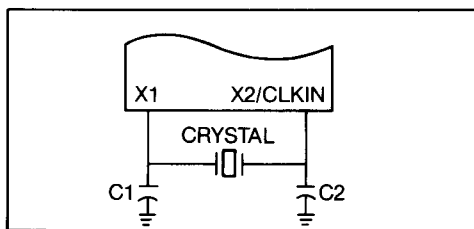
The DSP320C10 can use either its internal oscillator or an external frequency source for a clock.

#### Internal clock option

The internal oscillator is enabled by connecting a crystal across X1 and X2/CLKIN (see Figure 1). The frequency of CLKOUT is one-fourth the crystal fundamental frequency. The crystal should be fundamental mode, and parallel resonant, with an effective series resistance of 30 ohms, a power dissipation of 1mW, and be specified at a load capacitance of 20pF.

Characteristics	Sym	Min	Nom	Max	Unit	Conditions
DSP320C10 Crystal frequency	$f_x$	6.7	—	20.5	MHz	0°C to 70°C
DSP320C10-25 Crystal frequency	$f_x$	15.0	—	25.0	MHz	0°C to 70°C
C1, C2		—	10	—	pF	0°C to 70°C

FIGURE 1 – INTERNAL CLOCK OPTION



#### External clock option

An external frequency source can be used by injecting the frequency directly into X2/CLKIN with X1 left unconnected. The external frequency injected must conform to the specifications listed in the table below.

### A.C. CHARACTERISTICS

[TA = 0°C to 70°C, Vcc = 5V ± 10% (for DSP320C10); 5V ± 5% (for DSP320C10-25); VSS = 0V]

Characteristics	Sym	DSP320C10			DSP320C10-25			Unit	Test cond.
		Min	Nom	Max	Min	Nom	Max		
Master clock cycle time	$t_c(MC)$	48.78	—	150	40	—	66.67	ns	
Rise time master clock input	$t_r(MC)$	—	5	10	—	5	10	ns	
Fall time master clock input	$t_f(MC)$	—	5	10	—	5	10	ns	
Pulse duration master clock low, $t_c(MC) = 50ns$	$t_w(MCL)$	—	20	—	—	18	—	ns	
Pulse duration master clock high, $t_c(MC) = 50ns$	$t_w(MCH)$	—	20	—	—	18	—	ns	
Pulse duration master clock	$t_w(MCP)$	$0.475 t_c(C)$	—	$0.525 t_c(C)$	$0.475 t_c(C)$	—	$0.525 t_c(C)$	ns	
CLKOUT cycle time	$t_c(C)$	195.12	—	—	160	—	—	ns	
CLKOUT rise time	$t_r(C)$	—	10	—	—	10	—	ns	
CLKOUT fall time	$t_f(C)$	—	8	—	—	8	—	ns	
Pulse duration, CLKOUT low	$t_w(CL)$	—	92	—	—	74	—	ns	
Pulse duration, CLKOUT high	$t_w(CH)$	—	90	—	—	72	—	ns	See Fig. 2.
Delay time to CLKIN† to CLKOUT†*	$t_d(MCC)$	25	—	60	25	—	60	ns	

NOTE:  $t_c(C)$  is the cycle time of CLKOUT, i.e.,  $4 * t_c(MC)$  (4 time CLKIN cycle time if an external oscillator is used).

\*These values were derived from characterization data and are not tested or guaranteed.

**Absolute maximum ratings over specified temperature range (unless otherwise noted)\*\***

Supply voltage,  $V_{CC}$  ..... - 0.3V to 7V  
 All input voltages ..... - 0.3V to 15V  
 Output voltage ..... - 0.3V to 15V  
 DSP320C10I continuous power dissipation .. .36W  
 DSP320C10I-25 continuous power dissipation .40W  
 Air temperature range above  
     operating device ..... - 40°C to + 85°C  
 Storage temperature range ..... - 55°C to + 150°C

Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied – operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled “typical” is presented for design guidance only and is not guaranteed.

**D.C. CHARACTERISTICS**

Characteristics	DSP320C10I			DSP320C10I-25			Unit	Conditions
	Min	Nom	Max	Min	Nom	Max		
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V	
Supply voltage, $V_{SS}$	–	0	–	–	0	–	V	
High-level input voltage, $V_{IH}$ All inputs except CLKIN CLKIN	2.0 .56V <sub>cc</sub>	– –	– –	2.0 .56V <sub>cc</sub>	– –	– –	V V	
Low-level input voltage, $V_{IL}$ (all inputs)	–	–	.8	–	–	.8	V	
High-level output voltage $V_{OH}$	$V_{CC} - .4$	–	–	$V_{CC} - .4$	–	–		$I_{OH} = 20\mu A$
	2.4	–	–	2.4	–	–	V	$I_{OH} = 300\mu A$
Low-level output voltage $V_{OL}$	–	–	0.4	–	–	0.4	V	$I_{OL} = 2mA$
Off-state output current $I_{OZ}$	–	–	20	–	–	20	$\mu A$	DSP320C10I: $V_{CC} = 5.5V$ , $V_O = V_{CC} - .4V$ DSP320C10I-25: $V_{CC} = 5.25V$ , $V_O = V_{CC} - .4V$ DSP320C10I: $V_{CC} = 5.5V$ , $V_O = 0.4V$ DSP320C10I-25: $V_{CC} = 5.25V$ , $V_O = 0.4V$
	–	–	-20	–	–	-20	$\mu A$	
Input current $I_i$	–	–	$\pm 50$	–	–	$\pm 50$	$\mu A$	$V_I = V_{SS} \text{ to } V_{CC}$
Supply current $I_{CC}$ Tested with Clocks running.	–	–	65	–	–	75	mA	DSP320C10I: $V_{CC} = 5.5V$ , $f_x = 6.7 \text{ to } 20.5Hz$ DSP320C10I-25: $V_{CC} = 5.25V$ , $f_x = 15.0 \text{ to } 25MHz$
Input capacitance $C_i$ Data bus All others	–	25	–	–	25	–	pF	
	–	15	–	–	15	–	pF	
Output capacitance $C_o$ Data bus All others	–	25	–	–	25	–	pF	$f = 1MHz$ , all other pins OV
	–	10	–	–	10	–	pF	

\*\*All typical values are at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ .

### CLOCK CHARACTERISTICS AND TIMING

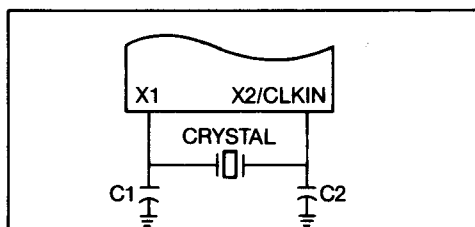
The DSP320C10I can use either its internal oscillator or an external frequency source for a clock.

#### Internal clock option

The internal oscillator is enabled by connecting a crystal across X1 and X2/CLKIN (see Figure 1). The frequency of CLKOUT is one-fourth the crystal fundamental frequency. The crystal should be fundamental mode, and parallel resonant, with an effective series resistance of 30 ohms, a power dissipation of 1mW, and be specified at a load capacitance of 20pF.

Characteristics	Sym	Min	Nom	Max	Unit	Conditions
DSP320C10I Crystal frequency	$f_x$	6.7	—	20.5	MHz	–40°C to 85°C
DSP320C10I-25 Crystal frequency	$f_x$	15.0	—	25.0	MHz	–40°C to 85°C
C1, C2		—	10	—	pf	–40°C to 85°C

FIGURE 1 – INTERNAL CLOCK OPTION



#### External clock option

An external frequency source can be used by injecting the frequency directly into X2/CLKIN with X1 left unconnected. The external frequency injected must conform to the specifications listed in the table below.

### A.C. CHARACTERISTICS

[TA = –40°C to 85°C, Vcc = 5V ± 10% (for DSP320C10I); 5V ± 5% (for DSP320C10I-25); VSS = 0V]

Characteristics	Sym	DSP320C10I			DSP320C10I-25			Unit	Test cond.
		Min	Nom	Max	Min	Nom	Max		
Master clock cycle time	$t_c(MC)$	48.78	—	150	40	—	66.67	ns	See Fig. 2.
Rise time master clock input	$t_r(MC)$	—	5	10	—	5	10	ns	
Fall time master clock input	$t_f(MC)$	—	5	10	—	5	10	ns	
Pulse duration master clock low, $t_c(MC) = 50ns$	$t_w(MCL)$	—	20	—	—	18	—	ns	
Pulse duration master clock high, $t_c(MC) = 50ns$	$t_w(MCH)$	—	20	—	—	18	—	ns	
Pulse duration master clock	$t_w(MCP)$	$0.475 t_c(C)$	—	$0.525 t_c(C)$	$0.475 t_c(C)$	—	$0.525 t_c(C)$	ns	
CLKOUT cycle time	$t_c(C)$	195.12	—	—	160	—	—	ns	
CLKOUT rise time	$t_r(C)$	—	10	—	—	10	—	ns	
CLKOUT fall time	$t_f(C)$	—	8	—	—	8	—	ns	
Pulse duration, CLKOUT low	$t_w(CL)$	—	92	—	—	74	—	ns	
Pulse duration, CLKOUT high	$t_w(CH)$	—	90	—	—	72	—	ns	
Delay time to CLKIN† to CLKOUT↓*	$t_d(MCC)$	25	—	60	25	—	60	ns	

NOTE:  $t_c(C)$  is the cycle time of CLKOUT, i.e.,  $4 * t_c(MC)$  (4 time CLKIN cycle time if an external oscillator is used).

\*These values were derived from characterization data and are not tested or guaranteed.

**Absolute maximum ratings over specified temperature range (unless otherwise noted)\*\***

Supply voltage,  $V_{CC}$  ..... - 0.3V to 7V  
 All input voltages ..... - 0.3V to 15V  
 Output voltage ..... - 0.3V to 15V  
 DSP320C10M continuous power dissipation ... .36W  
 DSP320C10M-25 continuous power  
 dissipation ..... .42W  
 Air temperature range above  
 operating device ..... - 55°C to + 125°C  
 Storage temperature range .... - 55°C to + 150°C

Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied – operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled “typical” is presented for design guidance only and is not guaranteed.

**D.C. CHARACTERISTICS**

Characteristics	DSP320C10M			DSP320C10M-25			Unit	Conditions
	Min	Nom	Max	Min	Nom	Max		
Supply voltage, VCC	4.5	5	5.5	4.5	5	5.5	V	
Supply voltage, VSS	-	0	-	-	0	-	V	
High-level input voltage, VIH All inputs except CLKIN CLKIN	2.0	-	-	2.0	-	-	V	
	.56Vcc	-	-	.56Vcc	-	-	V	
Low-level input voltage, VIL (all inputs)	-	-	0.8	-	-	.8	V	
High-level output voltage VOH	VCC - .4	-	-	VCC - .4	-	-		IOH = 20uA
	2.4	-	-	2.4	-	-	V	IOH = 300uA
Low-level output voltage VOL	-	-	0.4	-	-	0.4	V	IOL = 2mA
Off-state output current IOZ	-	-	20	-	-	20	uA	VCC = 5.5V, VO = VCC - .4V
	-	-	-20	-	-	-20	uA	VCC = 5.5V, VO = 0.4V
Input current I <sub>i</sub>	-	-	± 50	-	-	± 50	uA	VI = VSS to VCC
Supply current ICC Tested with Clocks running.	-	-	65	-	-	75	mA	DSP320C10M: VCC = 5.5V, fx = 6.7 to 20.5Hz DSP320C10M-25: VCC = 5.5V, fx = 15.0 to 25MHz
Input capacitance C <sub>i</sub> Data bus All others	-	25	-	-	25	-	pF	
	-	15	-	-	15	-	pF	
Output capacitance C <sub>O</sub> Data bus All others	-	25	-	-	25	-	pF	f = 1MHz, all other pins OV
	-	10	-	-	10	-	pF	

\*\*All typical values are at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ .

### CLOCK CHARACTERISTICS AND TIMING

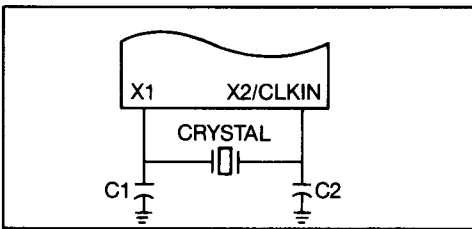
The DSP320C10M can use either its internal oscillator or an external frequency source for a clock.

#### Internal clock option

The internal oscillator is enabled by connecting a crystal across X1 and X2/CLKIN (see Figure 1). The frequency of CLKOUT is one-fourth the crystal fundamental frequency. The crystal should be fundamental mode, and parallel resonant, with an effective series resistance of 30 ohms, a power dissipation of 1mW, and be specified at a load capacitance of 20pF.

Characteristics	Sym	Min	Nom	Max	Unit	Conditions
DSP320C10M Crystal frequency	$f_x$	6.7	—	20.5	MHz	– 55°C to 125°C
DPS320C10M-25 Crystal frequency	$f_x$	15.0	—	25.0	MHz	– 55°C to 125°C
C1, C2	—	—	10	—	pf	– 55°C to 125°C

FIGURE 1 – INTERNAL CLOCK OPTION



#### External clock option

An external frequency source can be used by injecting the frequency directly into X2/CLKIN with X1 left unconnected. The external frequency injected must conform to the specifications listed in the table below.

### A.C. CHARACTERISTICS

[TA = – 55°C to 125°C, Vcc = 5V ± 10% (for DSP320C10M); 5V ± 10% (for DSP320C10M-25); VSS = OV]

Characteristics	Sym	DSP320C10M			DSP320C10M-25			Unit	Test cond.
		Min	Nom	Max	Min	Nom	Max		
Master clock cycle time	$t_c(\text{MC})$	48.78	—	150	40	—	66.67	ns	See Fig. 2.
Rise time master clock input	$t_r(\text{MC})$	—	5	10	—	5	10	ns	
Fall time master clock input	$t_f(\text{MC})$	—	5	10	—	5	10	ns	
Pulse duration master clock low, $t_c(\text{MC}) = 50\text{ns}$	$t_w(\text{MCL})$	—	20	—	—	18	—	ns	
Pulse duration master clock high, $t_c(\text{MC}) = 50\text{ns}$	$t_w(\text{MCH})$	—	20	—	—	18	—	ns	
Pulse duration master clock	$t_w(\text{MCP})$	$0.475t_c(\text{C})$	—	$0.525t_c(\text{C})$	$0.475t_c(\text{C})$	—	$0.525t_c(\text{C})$	ns	
CLKOUT cycle time	$t_c(\text{C})$	195.12	—	—	160	—	—	ns	
CLKOUT rise time	$t_r(\text{C})$	—	10	—	—	10	—	ns	
CLKOUT fall time	$t_f(\text{C})$	—	8	—	—	8	—	ns	
Pulse duration, CLKOUT low	$t_w(\text{CL})$	—	92	—	—	74	—	ns	
Pulse duration, CLKOUT high	$t_w(\text{CH})$	—	90	—	—	72	—	ns	
Delay time to CLKIN to CLKOUT*	$t_d(\text{MCC})$	25	—	60	25	—	60	ns	

NOTE:  $t_c(\text{C})$  is the cycle time of CLKOUT, i.e.,  $4 * t_c(\text{MC})$  (4 time CLKIN cycle time if an external oscillator is used).

\*These values were derived from characterization data and are not tested or guaranteed.

PARAMETER MEASUREMENT INFORMATION

FIGURE 2 – TEST LOAD CIRCUIT

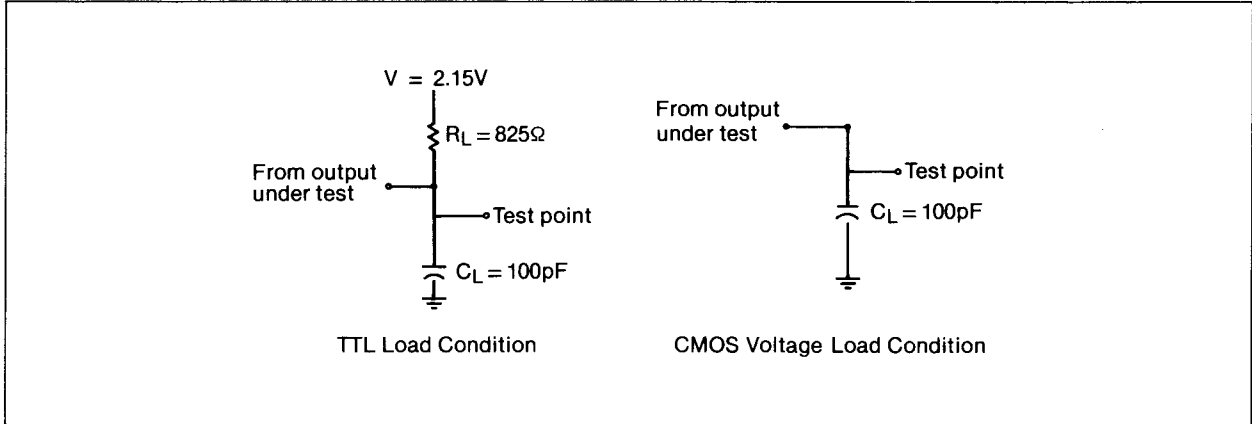
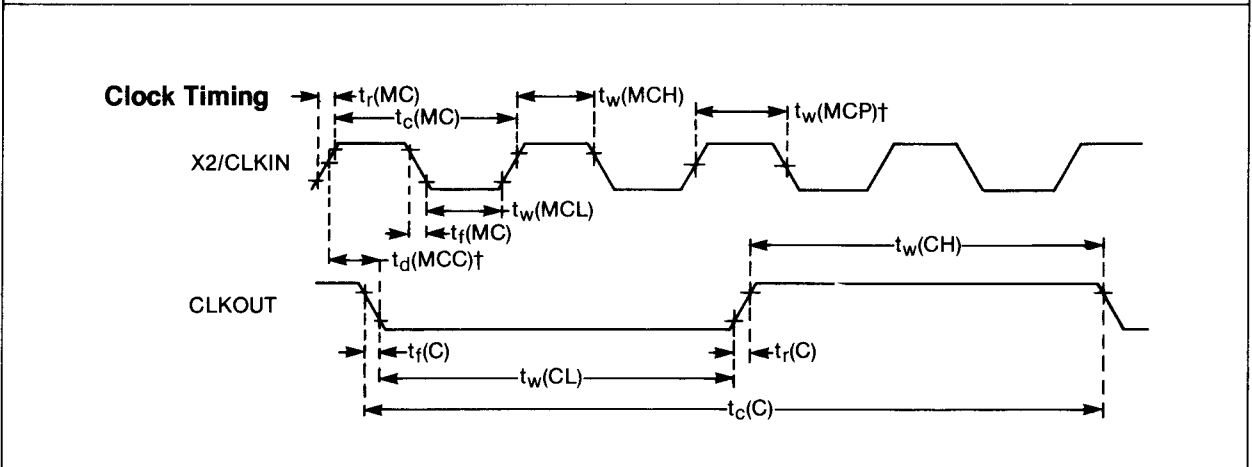
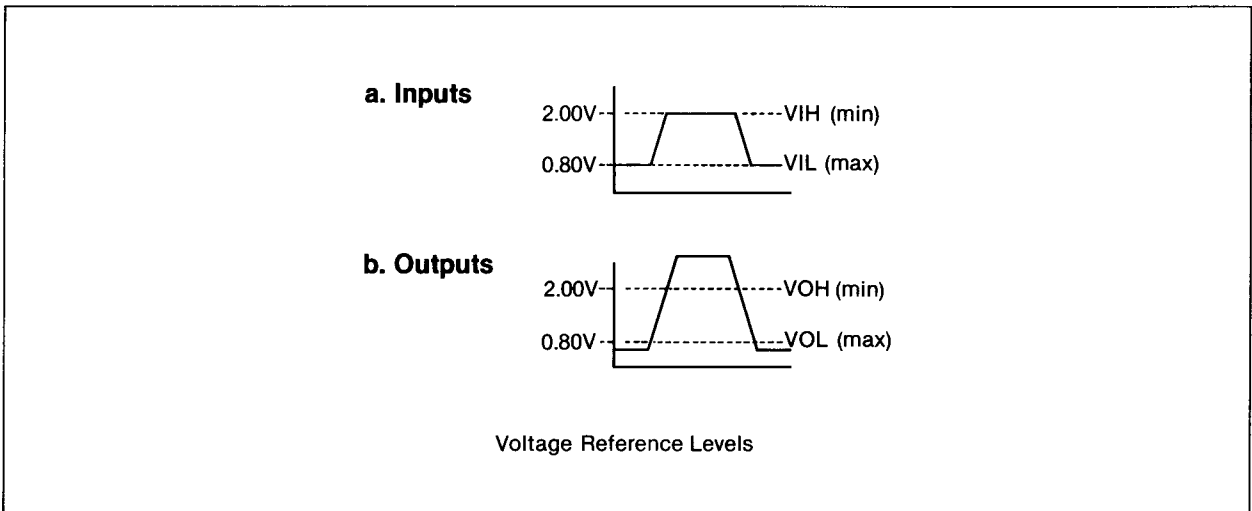


FIGURE 3 – A.C. TIMING VOLTAGE REFERENCE LEVELS



$\dagger t_d(\text{MCC})$  and  $t_w(\text{MCP})$  are referenced to an intermediate level of 1.5 volts on the CLKIN waveform.  
NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

## MEMORY AND PERIPHERAL INTERFACE TIMING

### Switching characteristics over recommended operating conditions

Characteristics	Sym	Min	Typ	Max	Unit	Conditions
Delay time CLKOUT↓ to address bus valid (See Note)	$t_{d1}$	10*	—	50	ns	See Figure 2.
Delay time CLKOUT↓ to $\overline{MEN}$ ↓	$t_{d2}$	$\frac{1}{4} t_C(C) - 5^*$	—	$\frac{1}{4} t_C(C) + 15$	ns	
Delay time CLKOUT↓ to $\overline{MEN}$ ↑	$t_{d3}$	- 10*	—	15	ns	
Delay time CLKOUT↓ to $\overline{DEN}$ ↓	$t_{d4}$	$\frac{1}{4} t_C(C) - 5^*$	—	$\frac{1}{4} t_C(C) + 15$	ns	
Delay time CLKOUT↓ to $\overline{DEN}$ ↑	$t_{d5}$	- 10*	—	15	ns	
Delay time CLKOUT↓ to $\overline{WE}$ ↓	$t_{d6}$	$\frac{1}{2} t_C(C) - 5^*$	—	$\frac{1}{2} t_C(C) + 15$	ns	
Delay time CLKOUT↓ to $\overline{WE}$ ↑	$t_{d7}$	- 10*	—	15	ns	
Delay time CLKOUT↓ to data bus OUT valid	$t_{d8}$	—	—	$\frac{1}{4} t_C(C) + 65$	ns	
Time after CLKOUT↓ that data bus starts to be driven	$t_{d9}$	$\frac{1}{4} t_C(C) - 5^*$	—	—	ns	
Time after CLKOUT↓ that data bus stops being driven	$t_{d10}$	—	—	$\frac{1}{4} t_C(C) + 30^*$	ns	
Data bus OUT valid after CLKOUT↓	$t_v$	$\frac{1}{4} t_C(C) - 10$ - 10	—	—	ns	

NOTE: Address bus will be valid upon  $\overline{WE}$ ↑,  $\overline{DEN}$ ↑, or  $\overline{MEN}$ ↑.

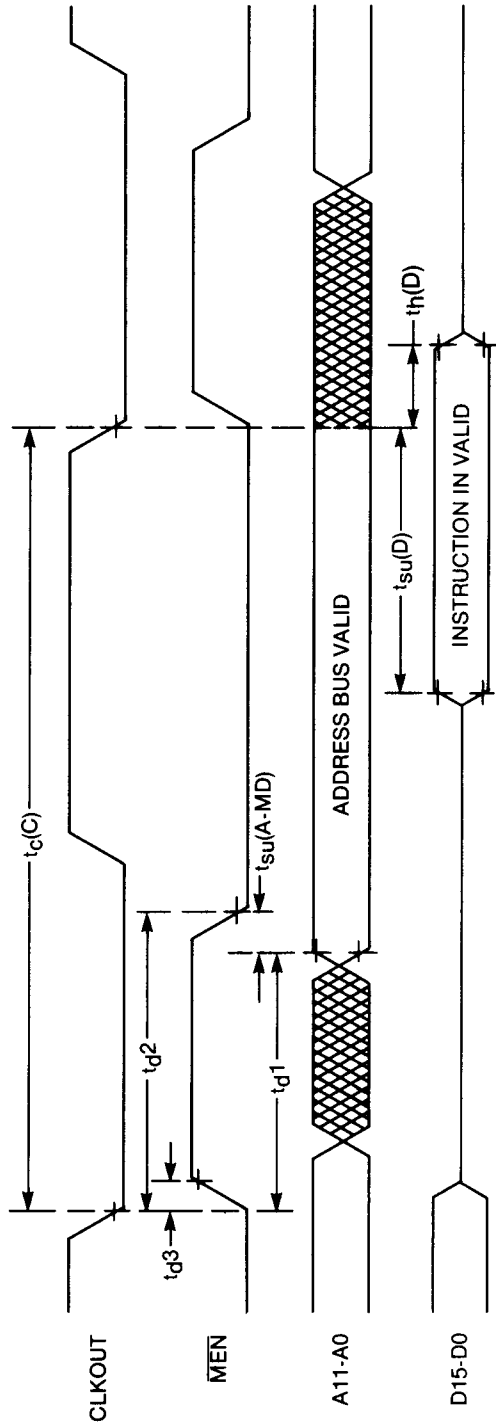
\*These values were derived from characterization data and are not tested.

### Timing requirements over recommended operating conditions

Characteristics	Sym	Min	Typ	Max	Unit	Conditions
Setup time data bus valid prior to CLKOUT↓	$t_{su}(D)$	50	—	—	ns	See Figure 2.
Hold time data bus held valid after CLKOUT↓	$t_h(D)$	0	—	—	ns	
Address bus setup time prior to $\overline{MEN}$ ↓ or $\overline{DEN}$ ↓	$t_{su}(A-MD)$	$\frac{1}{4} t_C(C) - 45$	—	—	ns	

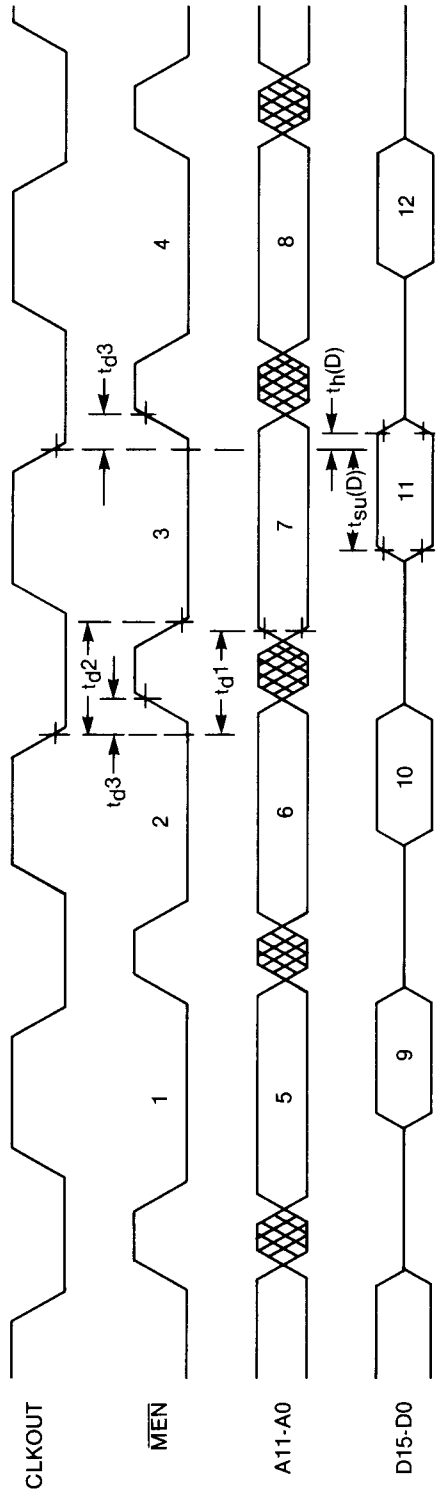
NOTE: Data may be removed from the data bus upon  $\overline{MEN}$ ↑ or  $\overline{DEN}$ ↑ preceding CLKOUT↓.

MEMORY READ



NOTE Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted

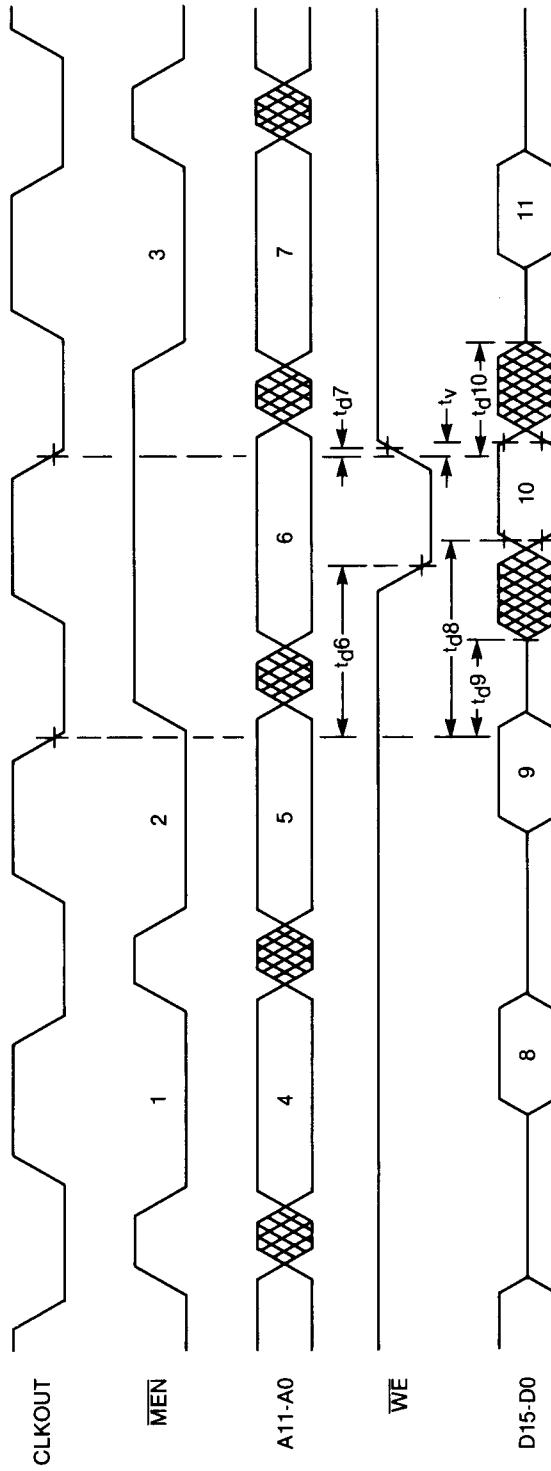
TBLR INSTRUCTION TIMING



- LEGEND
- 1. TBLR INSTRUCTION PREFETCH
  - 2. DUMMY PREFETCH
  - 3. DATA FETCH
  - 4. NEXT INSTRUCTION PREFETCH
  - 5. ADDRESS BUS VALID
  - 6. ADDRESS BUS VALID
  - 7. ADDRESS BUS VALID
  - 8. ADDRESS BUS VALID
  - 9. INSTRUCTION IN VALID
  - 10. INSTRUCTION IN VALID
  - 11. DATA IN VALID
  - 12. INSTRUCTION IN VALID

NOTE Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted

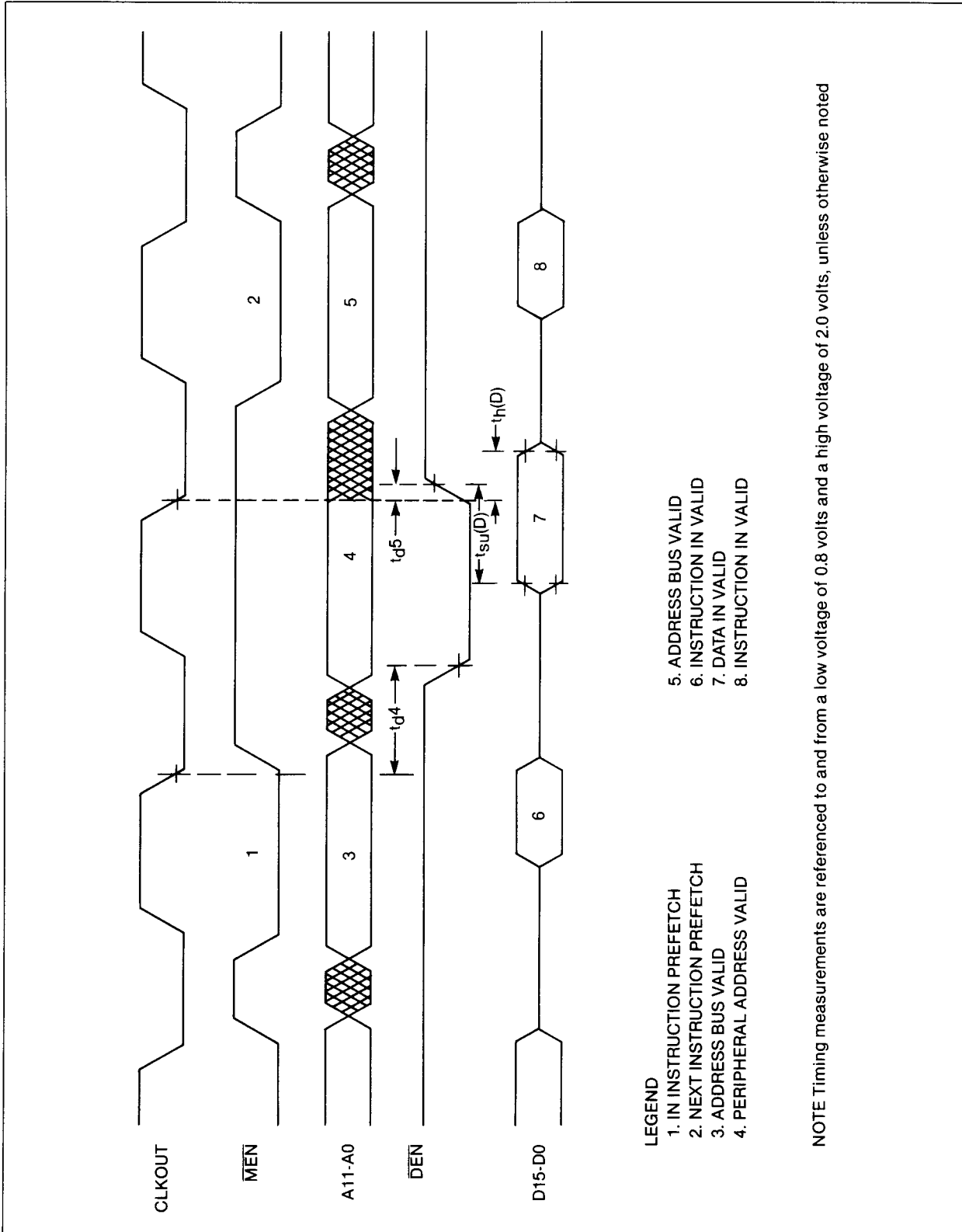
TBLW INSTRUCTION TIMING



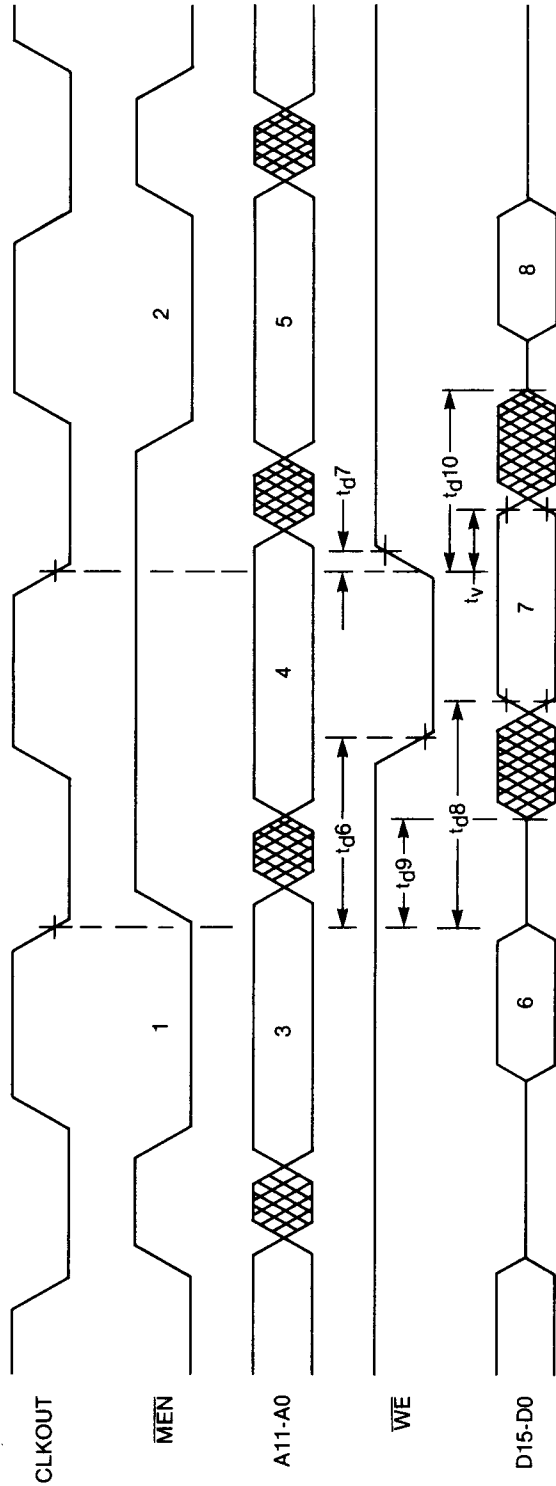
- LEGEND
- 1. TBLW INSTRUCTION PREFETCH
  - 2. DUMMY PREFETCH
  - 3. NEXT INSTRUCTION PREFETCH
  - 4. ADDRESS BUS VALID
  - 5. ADDRESS BUS VALID
  - 6. ADDRESS BUS VALID
  - 7. ADDRESS BUS VALID
  - 8. INSTRUCTION IN VALID
  - 9. INSTRUCTION IN VALID
  - 10. DATA OUT VALID
  - 11. INSTRUCTION IN VALID

NOTE Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted

IN INSTRUCTION TIMING



OUT INSTRUCTION TIMING



- LEGEND
- 1. OUT INSTRUCTION PREFETCH
  - 2. NEXT INSTRUCTION PREFETCH
  - 3. ADDRESS BUS VALID
  - 4. PERIPHERAL ADDRESS VALID
  - 5. ADDRESS BUS VALID
  - 6. INSTRUCTION IN VALID
  - 7. DATA OUT VALID
  - 8. INSTRUCTION IN VALID

NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

## RESET ( $\overline{RS}$ ) TIMING

### Timing requirements over recommended operating conditions

Characteristics	Sym	Min	Nom	Max	Unit
Reset ( $\overline{RS}$ ) setup time prior to CLKOUT. See Notes 1-4.	$t_{su}(R)$	50	—	—	ns
$\overline{RS}$ pulse duration	$t_w(R)$	$5t_C(C)$	—	—	ns

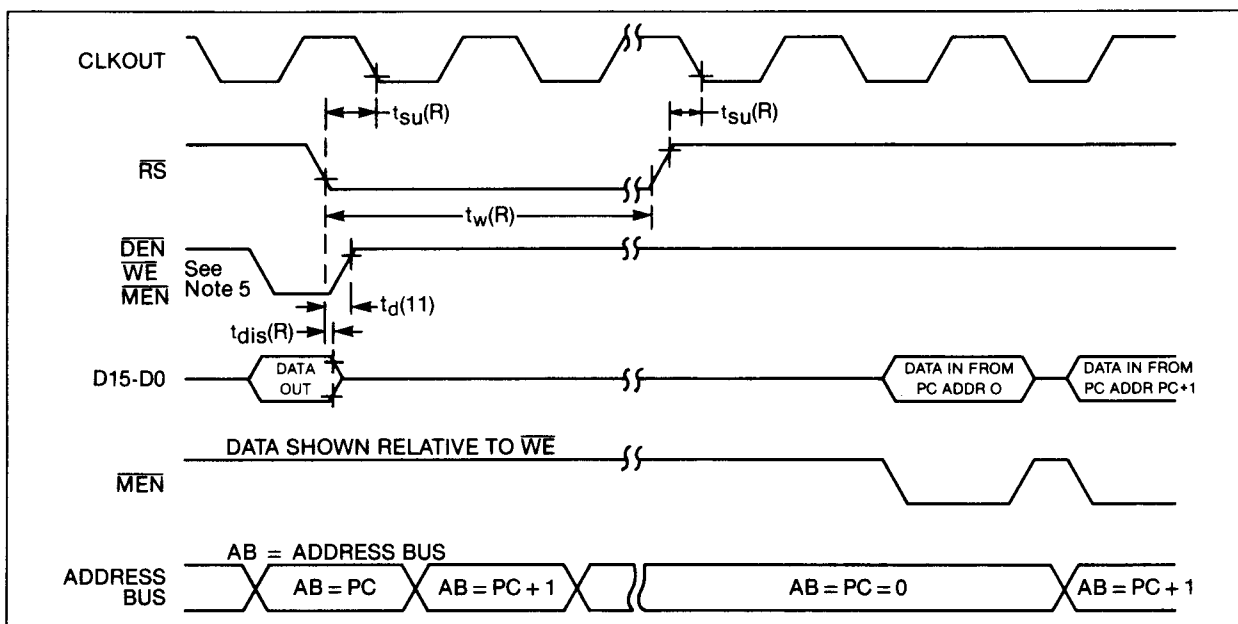
NOTE: To insure correct recognition of power on reset, the  $\overline{RS}$  pin must be kept low during the power up and released high only 3 machine cycles after the power is stable. To avoid problems due to slow rising reset signal, it is recommended that the reset signal be passed through a schmitt trigger before presenting it at the pin.

### Switching characteristics over recommended operating conditions

Characteristics	Sym	Min	Typ	Max	Unit	Conditions
Delay time $\overline{DEN}t$ , $\overline{WE}t$ , and $\overline{MEN}t$ from $\overline{RS}$	$t_{d11}$	—	—	$\frac{1}{2}t_C(C)+50^*$	ns	See Figure 2
Data bus disable time after $\overline{RS}$	$t_{dis}(R)$	—	—	$\frac{1}{4}t_C(C)+50^*$	ns	

NOTE:  $\overline{RS}$  can occur anytime during a clock cycle. Time given is minimum to ensure synchronous operation.  
\*These values were derived from characterization data and are not tested or guaranteed.

## RESET TIMING



### NOTES:

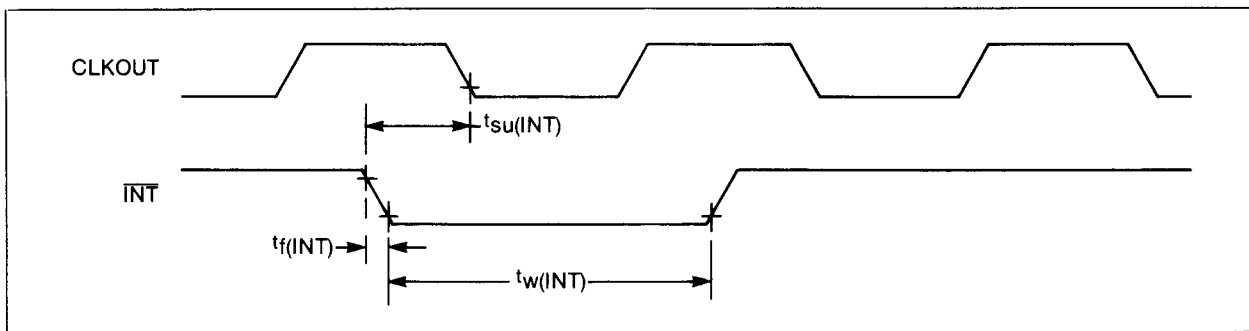
- $\overline{RS}$  forces  $\overline{DEN}$ ,  $\overline{WE}$ , and  $\overline{MEN}$  high and tristates data bus DO through D15. AB outputs (and program counter) are synchronously cleared to zero after the next complete CLK cycle from  $\downarrow\overline{RS}$ .
- $\overline{RS}$  must be maintained active low for a minimum of five clock cycles to be recognized.
- Resumption of normal program will commence after one complete CLK cycle from  $\uparrow\overline{RS}$ .
- Due to the synchronizing action on  $\overline{RS}$ , time to execute the function can vary dependent upon when  $\uparrow\overline{RS}$  or  $\downarrow\overline{RS}$  occur in the CLK cycle.
- Diagram shown is for definition purpose only.  $\overline{DEN}$ ,  $\overline{WE}$ , and  $\overline{MEN}$  are mutually exclusive.
- Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.
- During a write cycle,  $\overline{RS}$  may produce an invalid write address.

**INTERRUPT ( $\overline{\text{INT}}$ ) TIMING**

Timing requirements over recommended operating conditions

Characteristics	Sym	Min	Typ	Max	Unit
Fall time $\overline{\text{INT}}$	$t_f(\text{INT})$	—	—	15	ns
Pulse duration $\overline{\text{INT}}$	$t_w(\text{INT})$	$t_c(\text{C})$	—	—	ns
Setup time $\overline{\text{INT}}\downarrow$ before $\text{CLKOUT}\downarrow$	$t_{su}(\text{INT})$	50	—	—	ns

**INTERRUPT TIMING**



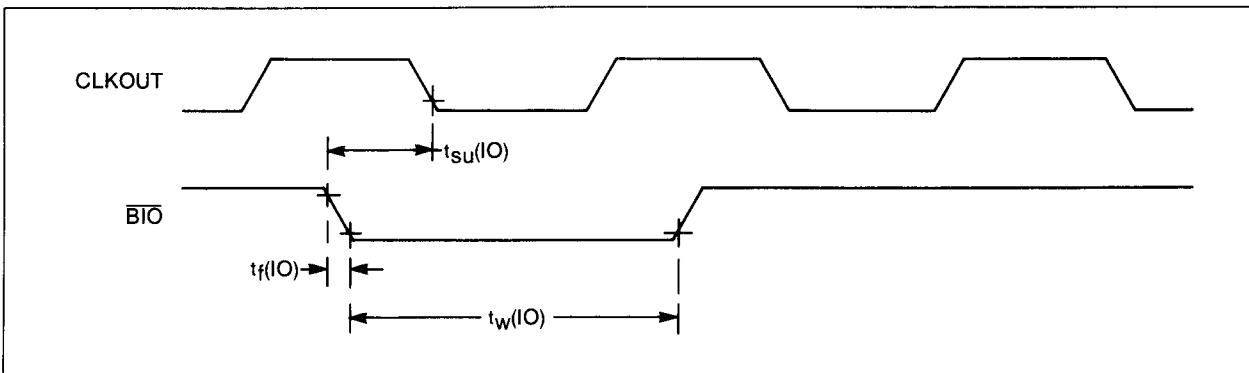
NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

**I/O ( $\overline{\text{BIO}}$ ) TIMING**

Timing requirements over recommended operating conditions

Characteristics	Sym	Min	Typ	Max	Unit
Fall time $\overline{\text{BIO}}$	$t_f(\text{IO})$	—	—	15	ns
Pulse duration $\overline{\text{BIO}}$	$t_w(\text{IO})$	$t_c(\text{C})$	—	—	ns
Setup Time $\overline{\text{BIO}}\downarrow$ before $\text{CLKOUT}\downarrow$	$t_{su}(\text{IO})$	50	—	—	ns

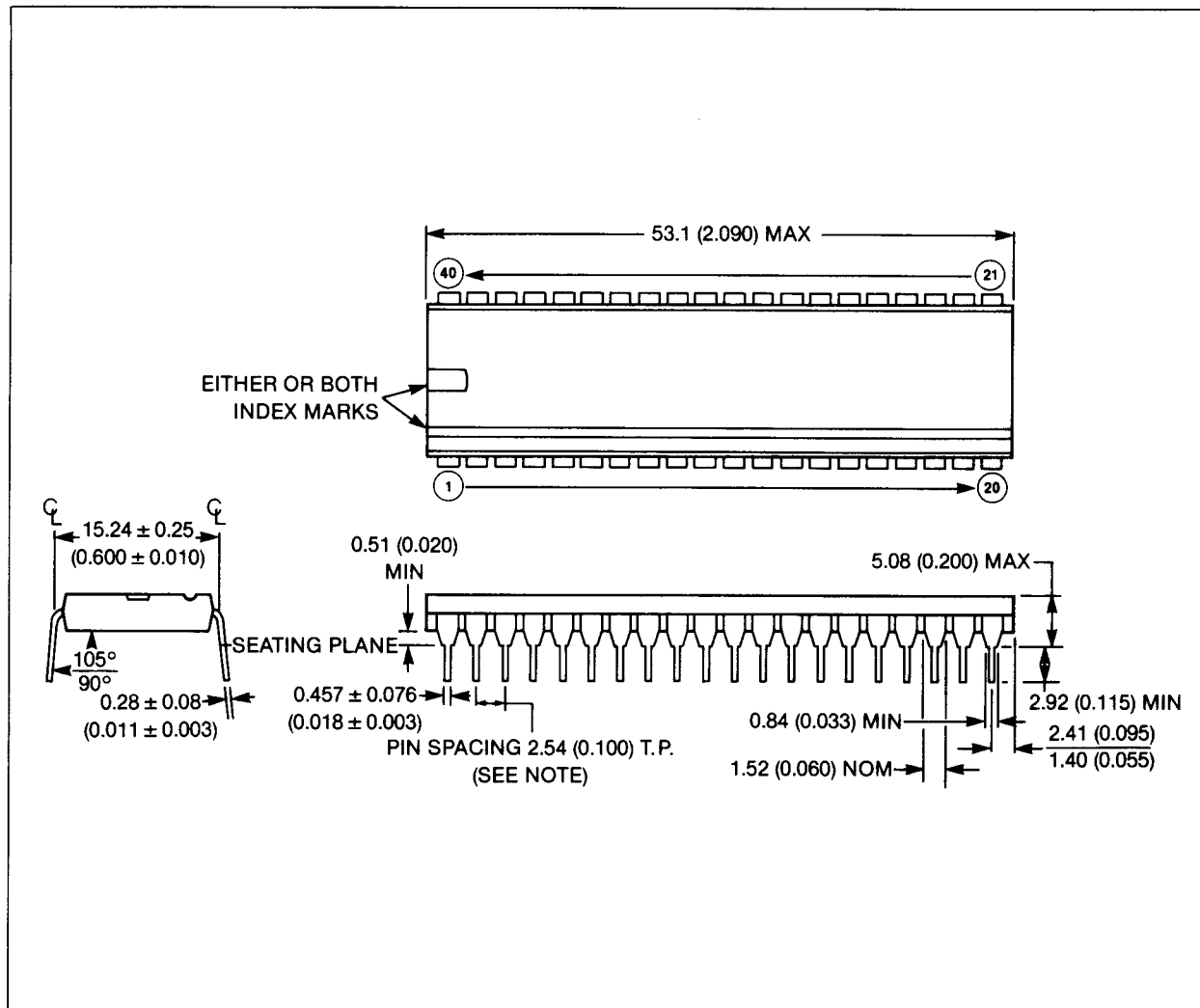
**BIO TIMING**



NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

**MECHANICAL DATA**

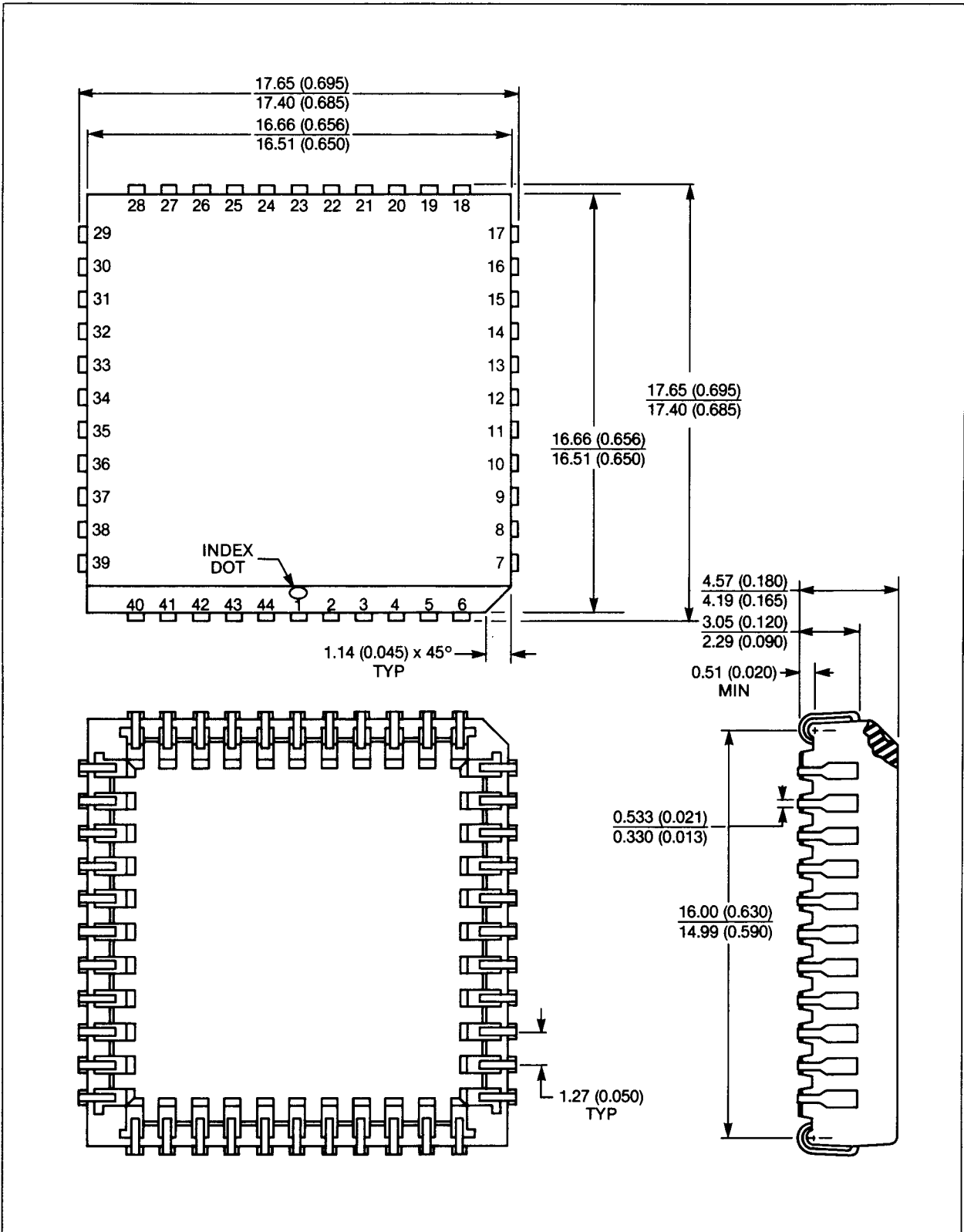
**40-pin plastic dual-in-line package**



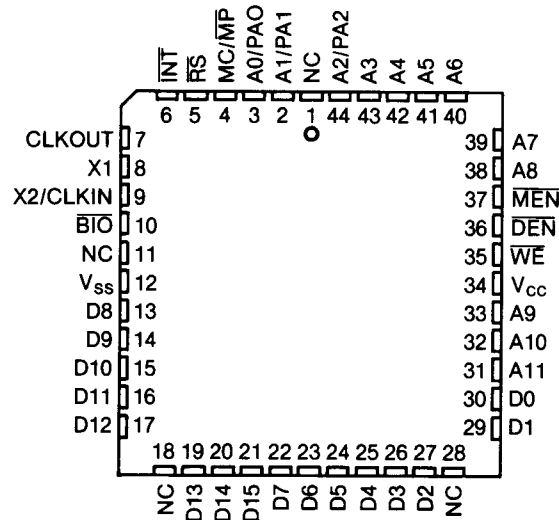
**NOTES:**

1. Each pin centerline is located within 0.254 (0.010) of its true longitudinal position.
2. All linear dimensions are in millimeters and parenthetically in inches. Inch dimensions govern.

44-PIN PLASTIC CHIP CARRIER



44-PIN PLASTIC CHIP CARRIER PIN CONFIGURATION



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