Section 7

Electrical Characteristics

Absolute Maximum Ratings

Table 7-1. **Absolute Maximum Ratings**

Parameter	Symbol	Min	Max	Units
Supply Voltage	V_{CC}	-	7.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{OP}	-25°	85°	C
Storage Temperature	T_{STG}	-40°	125°	C

Note Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

Operating Conditions

Table 7-2. **Operating Conditions**

Parameter	Symbol	Min	Max	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0°	70°	C

DC Characteristics

Table 7-3. DC Characteristics

Parameter	Type	Symbol	Min	Max	Units	Condition
Input Low Voltage	All	V_{IL}		0.8	V	
Input High Voltage	C0,C2,C4, C8,OSC2	V_{IH}	3.5		V	
Input High Voltage	T0,T4,T8, T24	V_{IH}	2.4			
Output Low Voltage	C2	V_{OL}		0.4	V	I_{OL}=2 ma
	C4	V_{OL}		0.4	V	I_{OL}=4 ma
	C8	V_{OL}		0.4	V	I_{OL}=8 ma
	T4	V_{OL}		0.45	V	I_{OL}=4 ma
	T8	V_{OL}		0.45	V	I_{OL}=8 ma
	T24	V_{OL}		0.45	V	I_{OL}=24 ma
Output High Voltage	C2	V_{OH}	3.5		V	I_{OH}=-2 ma
	C4	V_{OH}	3.5		V	I_{OH}=-4 ma
	C8	V_{OH}	3.5		V	I_{OH}=-8ma
Output High Voltage	T4, T8, T24	V_{OH}	2.4		V	I_{OH}=-4 ma
Input Current		I_{IN}	-	±10	µA	
Power Supply Current @ 32 MHz		I_{CC}		150	mA	VCC=5.25
High-Z Leakage Current		I_{OZ}	-	±10	µA	
Static Power Supply Current		I_{CCSB}		2	mA	VCC=5.25

AC Characteristics

Note: All timing parameters are specified under capacitive load of 50 pF and temperature of 70 degree C, unless otherwise stated. Timing units are in nanoseconds. All specifications are subject to change.

Local Bus Interface

Figure 7-1. **Local Bus Master Mode Timing Diagram**

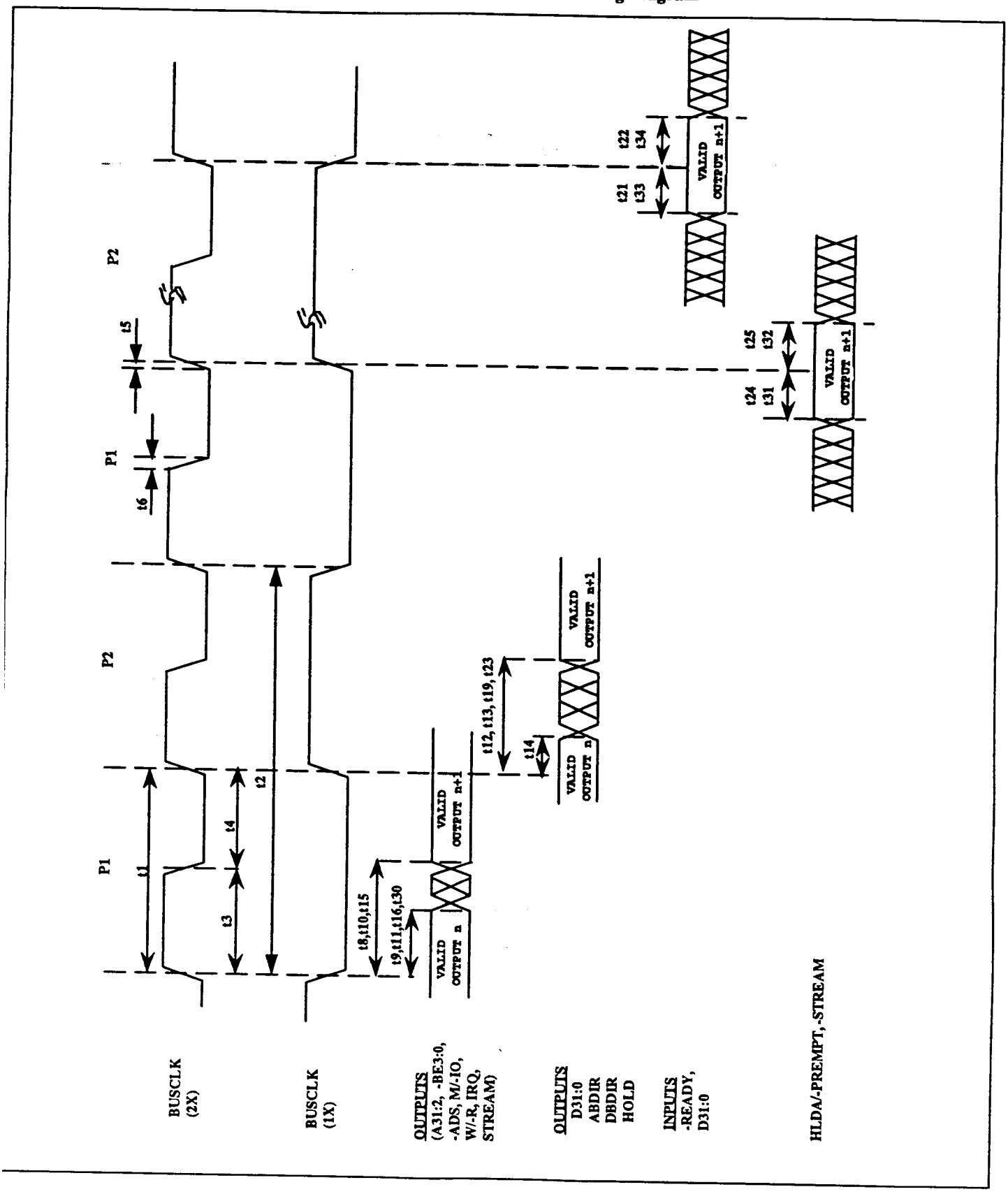


Figure 7-2. **Local Bus Slave Mode Timing Diagram**

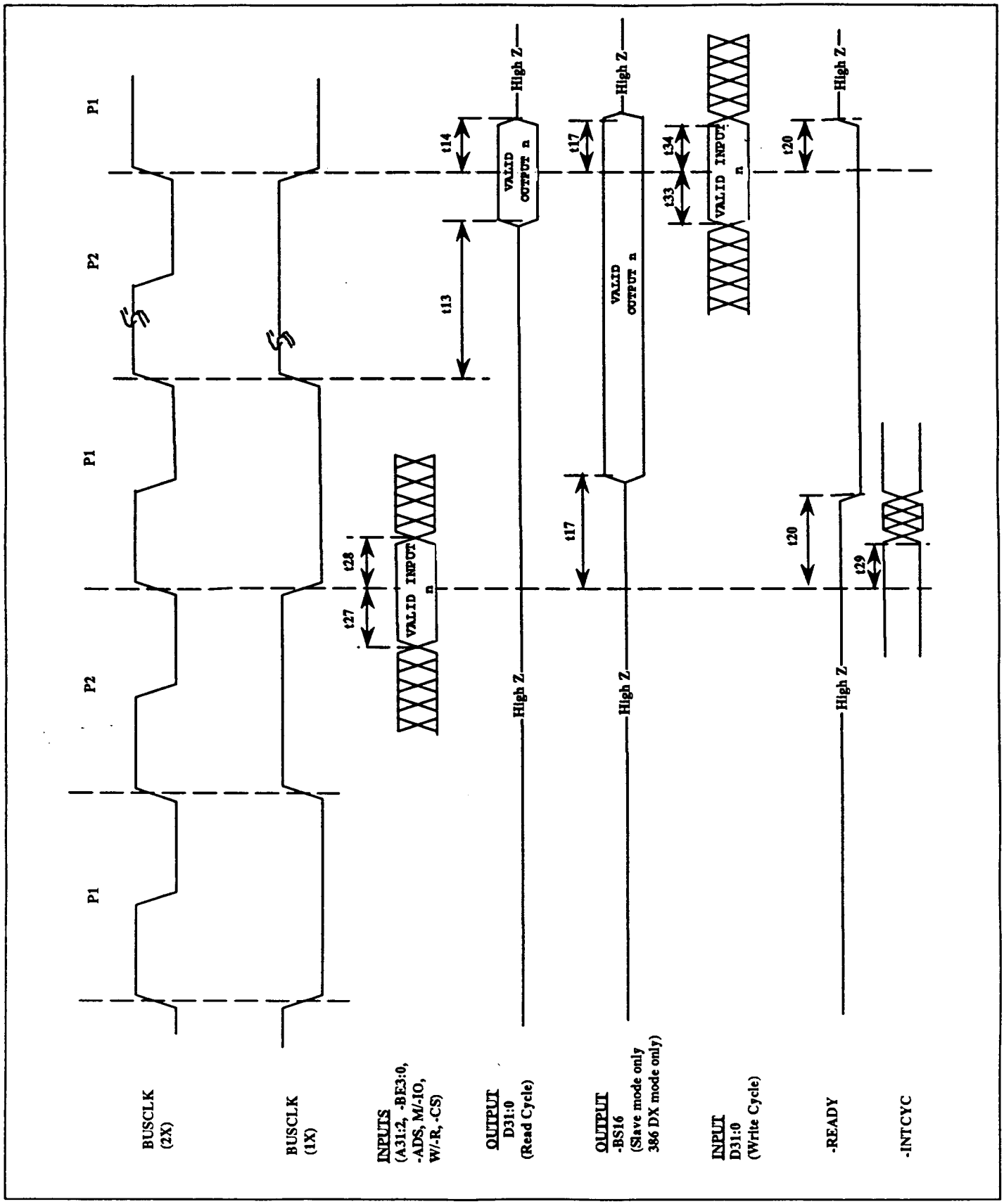


Table 7-4. **Local Bus Timing Table**

Symbol	Parameter	Min	Typ.	Max	Figure	Notes
t1	2X Clock Period	20		125	7-1	
t2	P1 and P2 Clock Period	40		250	7-1	
t3	2X Clock High time	7			7-1	
t4	2X Clock Low time	7			7-1	
t5	2X Clock rise time			7		
t6	2XClock fall time			7		
t8	Address A32:2 Valid Delay			20	7-1	
t9	Address A32:2 Float Delay			20	7-1	
t10	-ADS,M/-IO, W/-R Valid Delay			15	7-1	
t11	-ADS,M/-IO, W/-R Float Delay			20	7-1	
t12	ABDIR Valid Delay	2		13	7-1	
t13	D31:0 Valid Delay (slave mode)			24	7-1, 7-2	
t14	D31:0 Float Delay (slave mode)			17	7-1, 7-2	
t15	BE3:0 Valid Delay			15	7-1	
t16	BE3:0 Float Delay			20	7-1	
t17	-BS16 Valid and Float Delay (slave mode)	5		10	7-2	
t19	DBDIR Valid Delay	2		16	7-1	
t20	-READY Valid and Float Delay (slave mode)	7		15	7-2	
t21	-READY Setup time (master mode)	7			7-1	
t22	-READY Hold time (master mode)	4			7-1	
t23	HOLD Valid Delay	2		13	7-1	
t24	HLDA/-PREMPT Setup time	15			7-1	
t25	HLDA/-PREMPT Hold time	4			7-1	
t27	-CS setup, A31:2, BE3:0, -ADS, M/-IO	15			7-2	
t28	-CS hold, A31:2, BE3:0, -ADS, M/-IO	4			7-2	
t29	-INTCYC Valid Delay	9		14	7-2	
t30	STREAM Valid Delay			22	7-1	
t31	STREAM setup	20			7-1	
t32	STREAM hold	20			7-1	
t33	D31:0 Read setup (master mode)	5			7-1	
t34	D31:0 Read hold (master mode)	3			7-1	

Figure 7-3. **Local Bus Master Write Functional Timing**

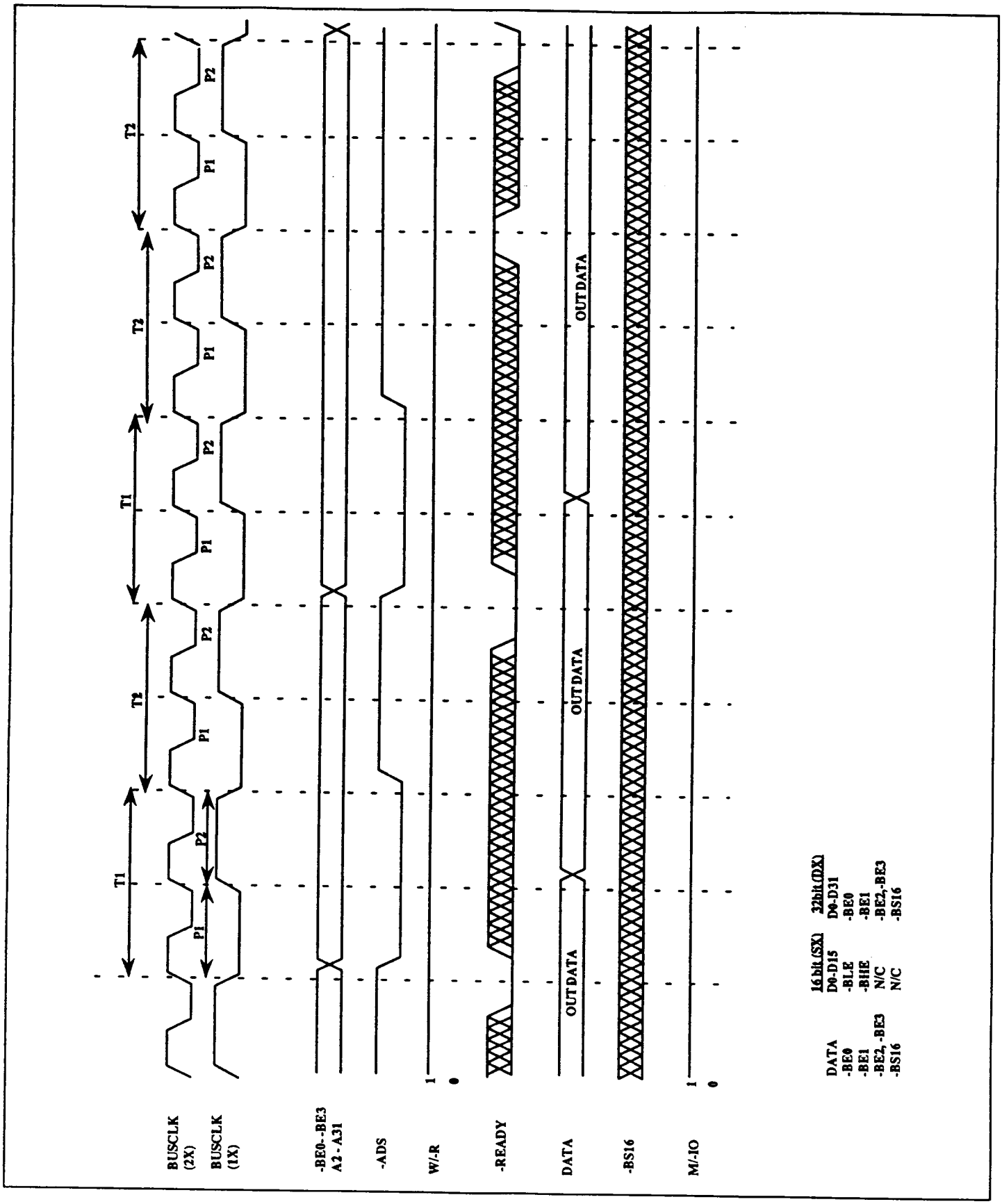


Figure 7-4. **Local Bus Master Read Functional Timing**

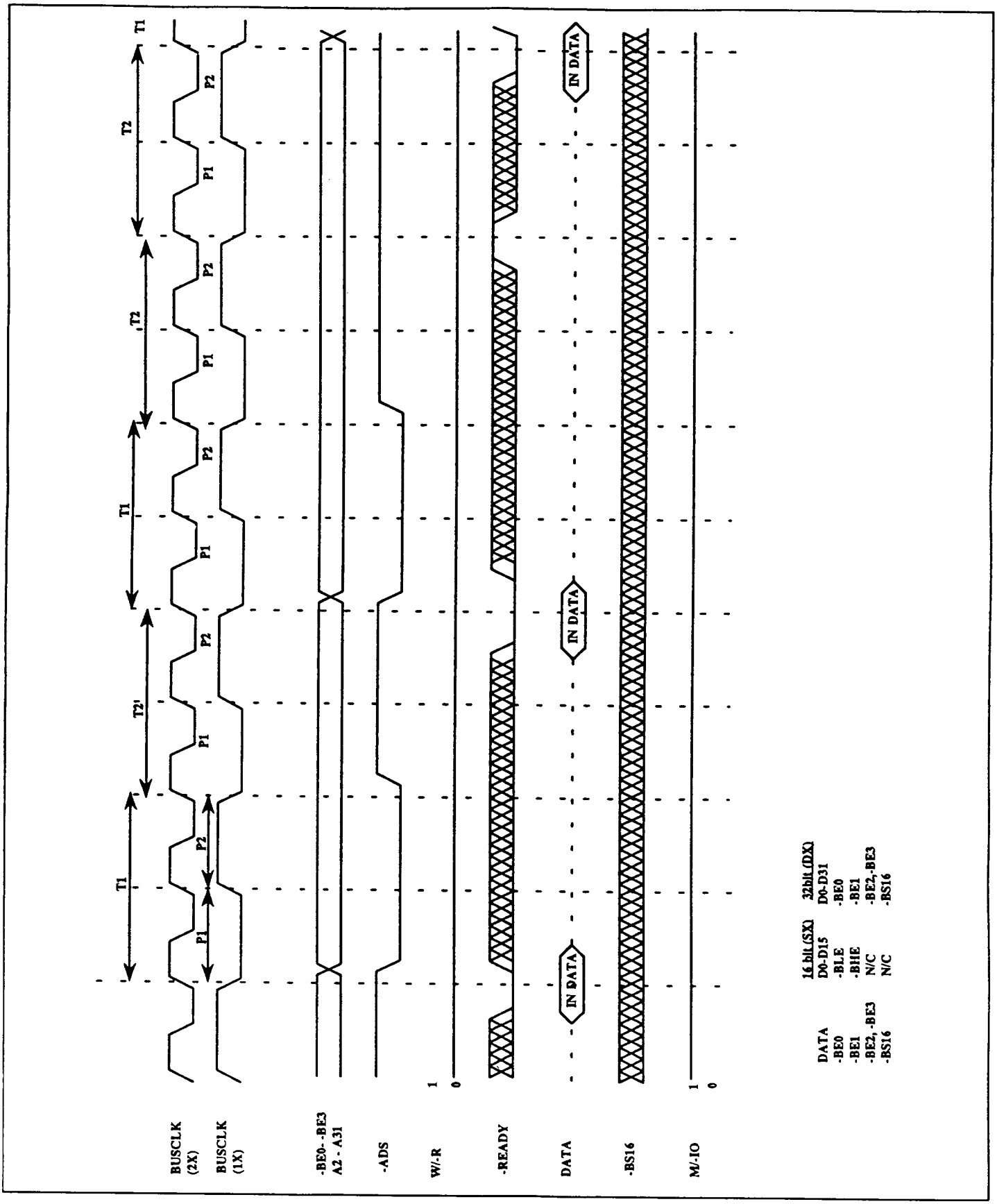


Figure 7-5. **Local Bus Acquisition, Release and Pre-empt Functional Timing**

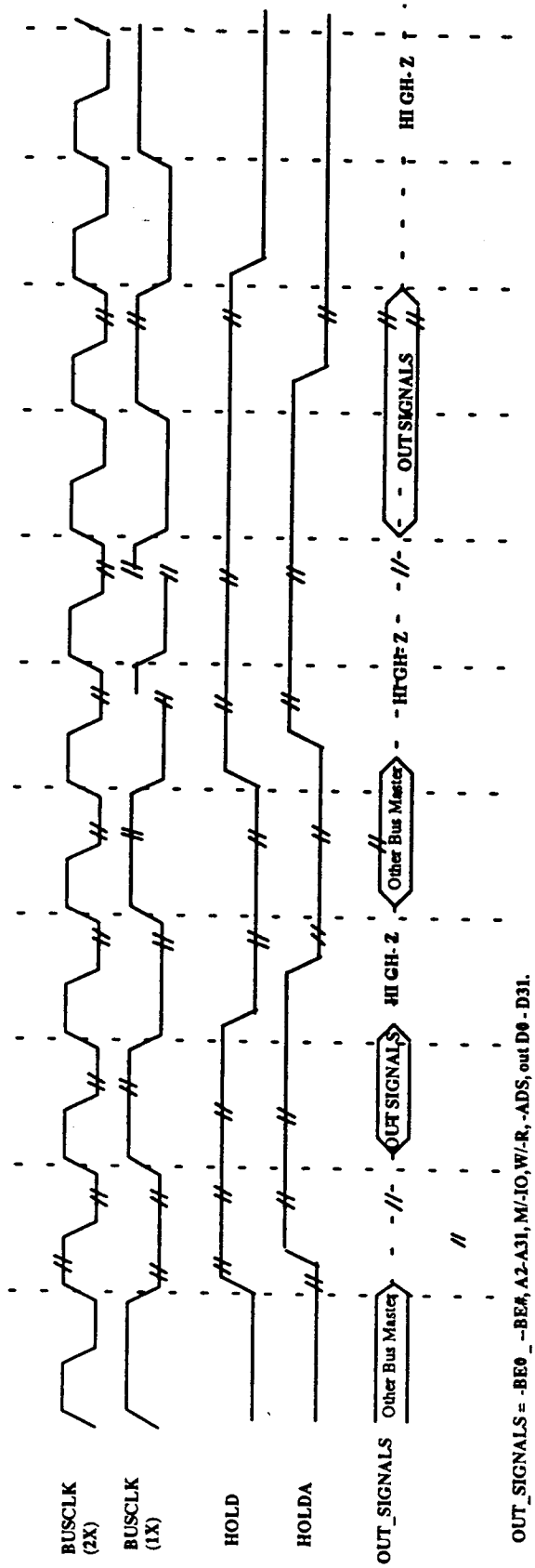


Figure 7-6. **Local Bus Slave Memory Read/Write Functional Timing**

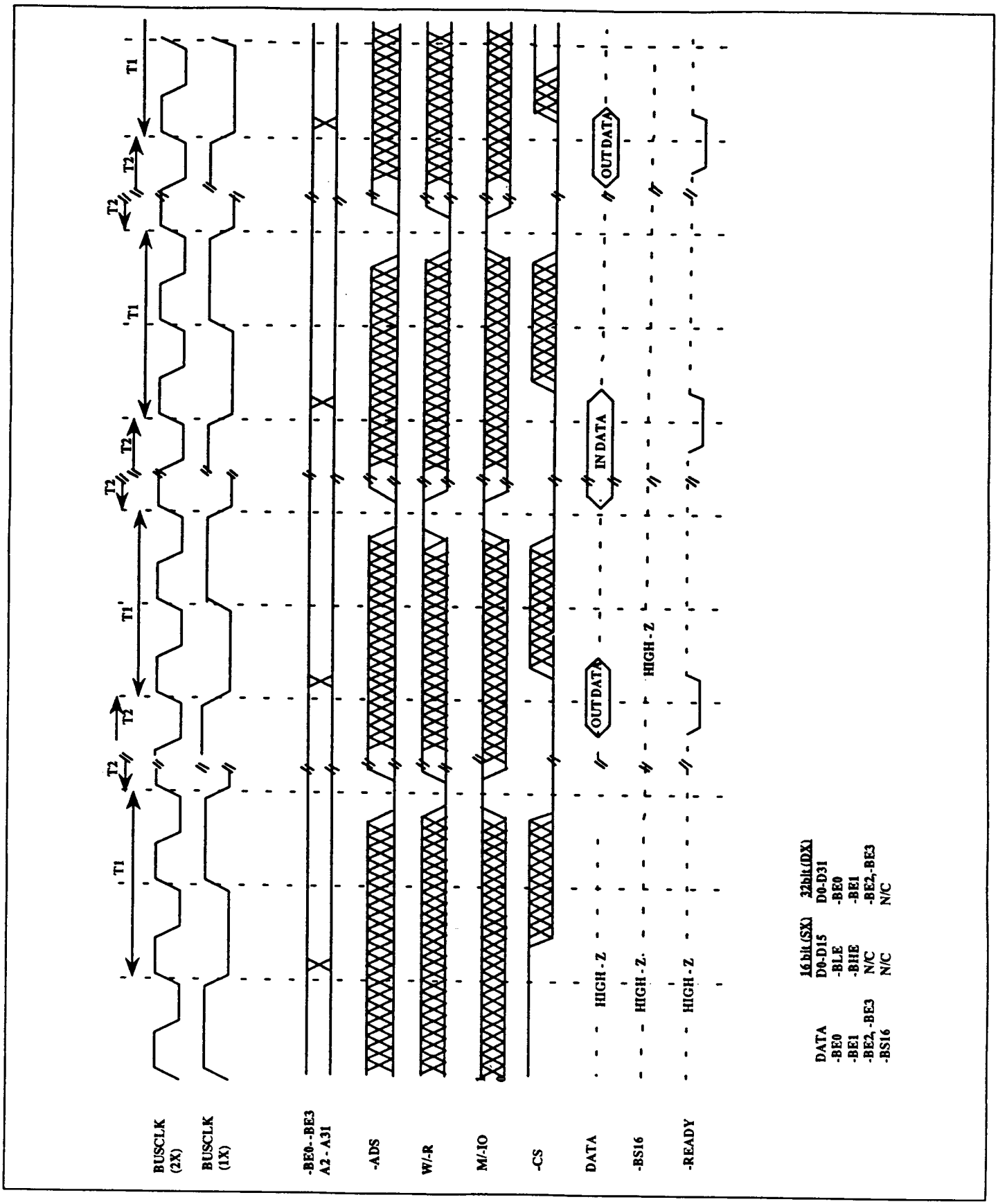


Figure 7-7. **Local Bus Slave I/O Read/Write Functional Timing**

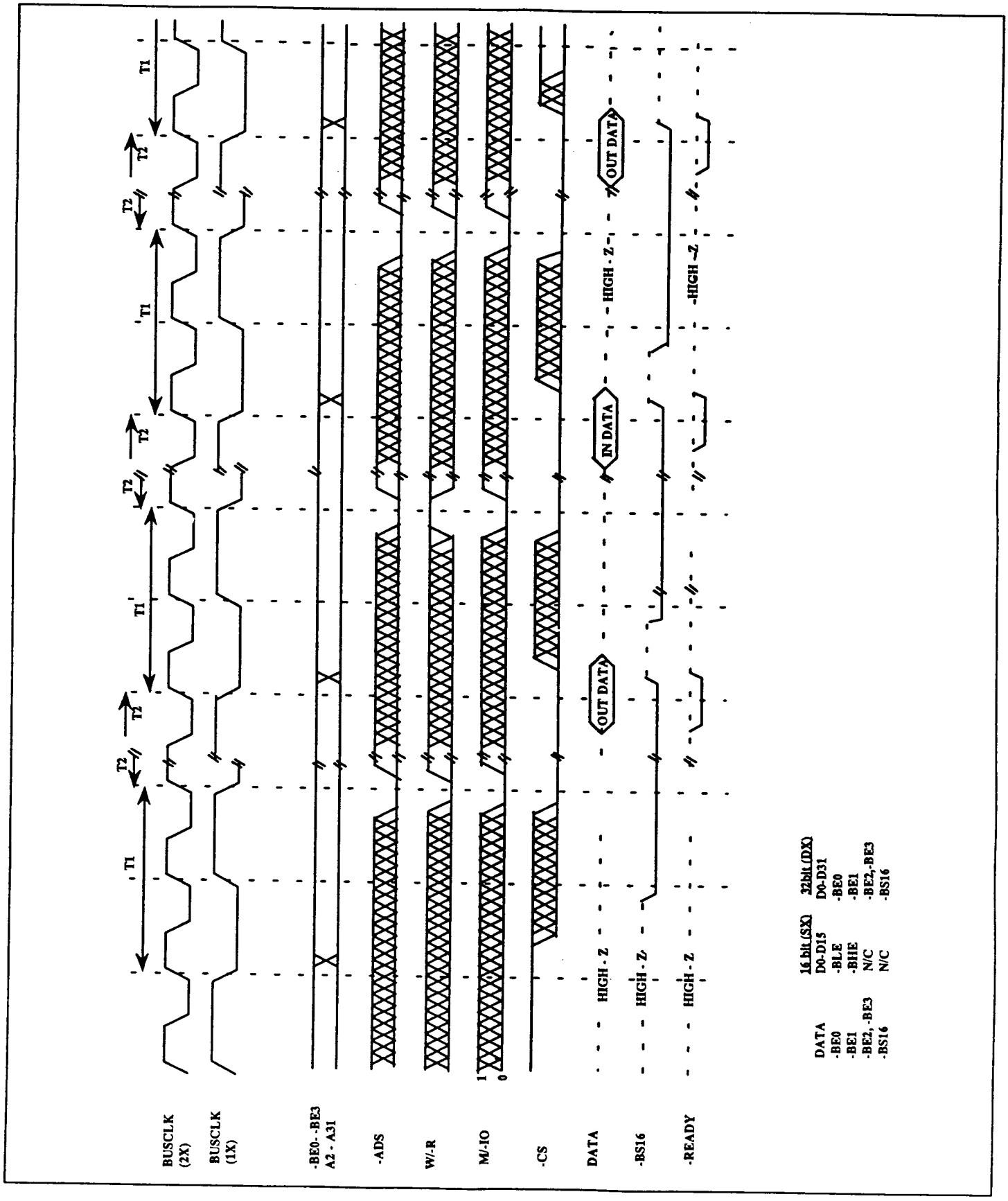
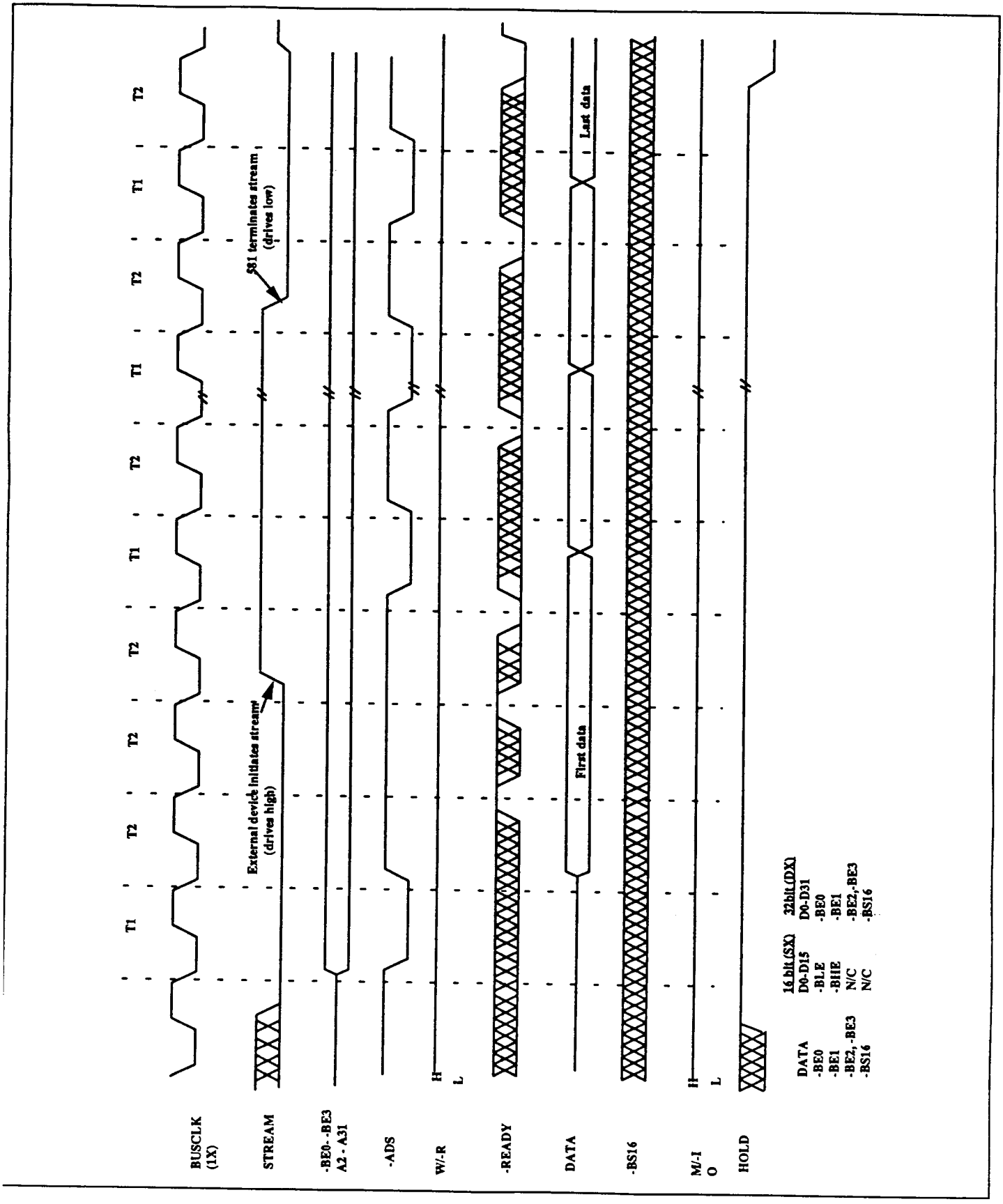


Figure 7-8. **Local Bus Master STREAM Write Functional Timing**



AT/ISA Bus Interface

Figure 7-9. AT/ISA Bus I/O Slave Access Timing

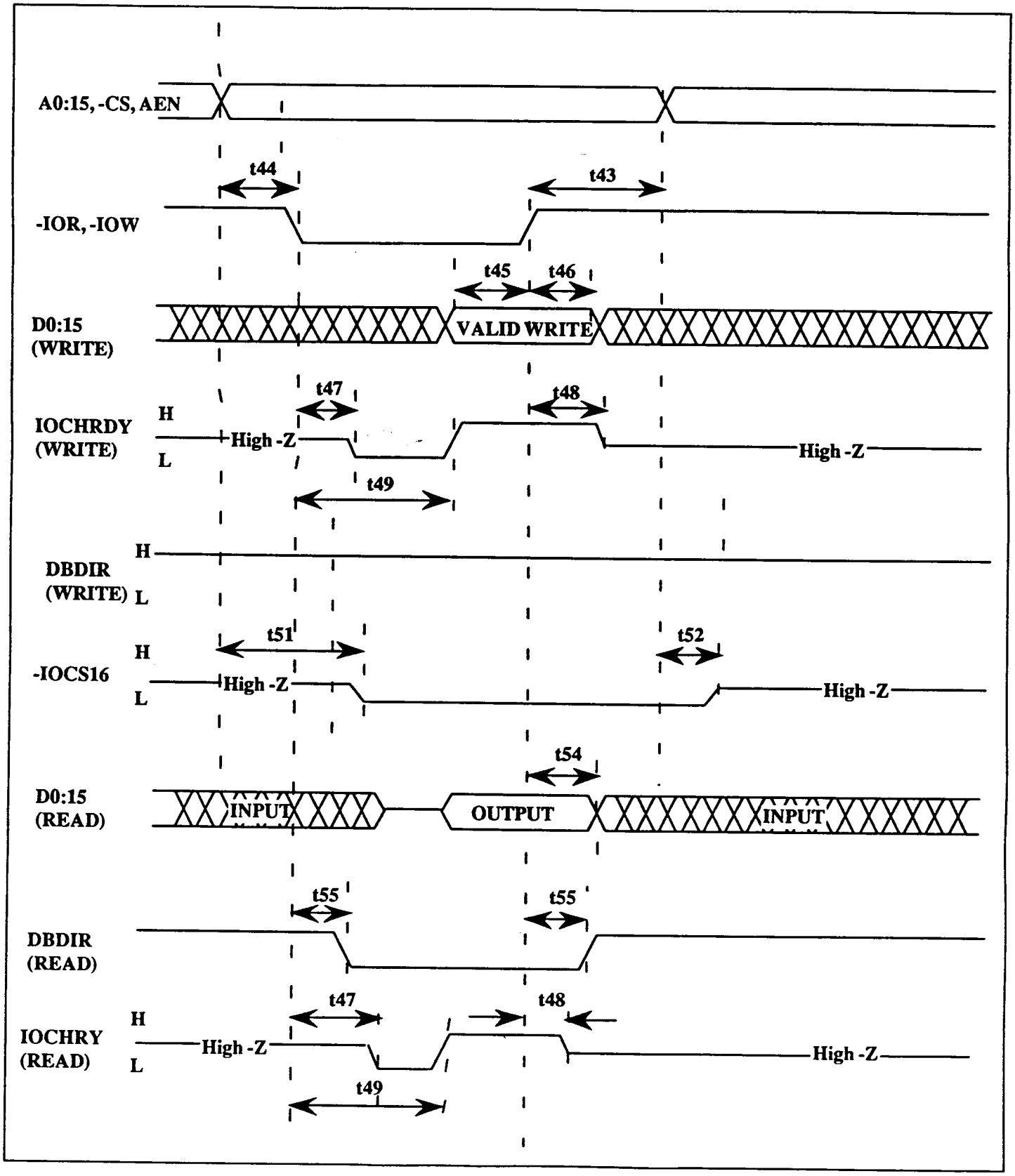


Figure 7-10. **AT/ISA Bus 16-Bit Memory Slave Access Timing**

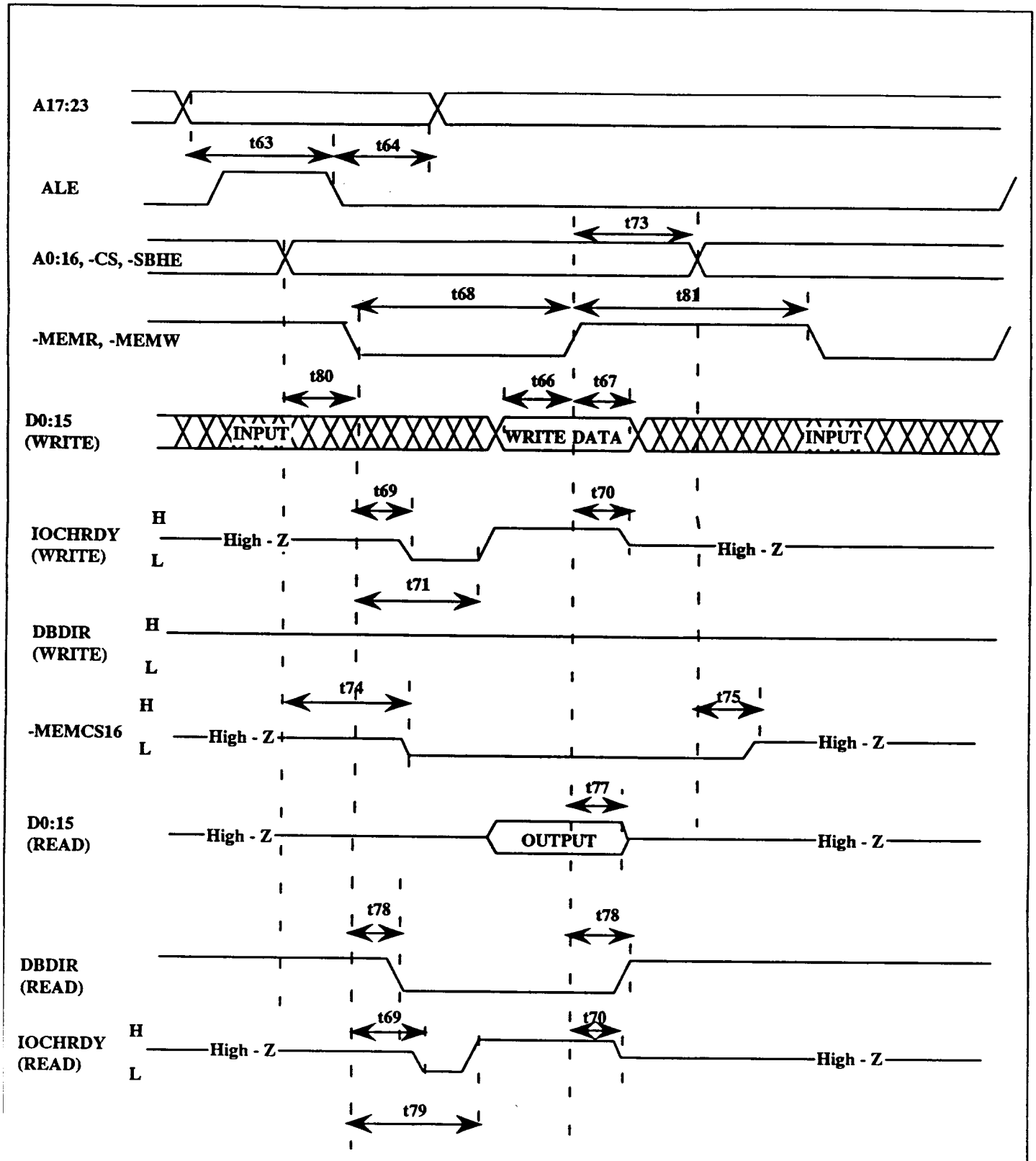


Figure 7-11. **AT/ISA Bus Master Read/Write Timing**

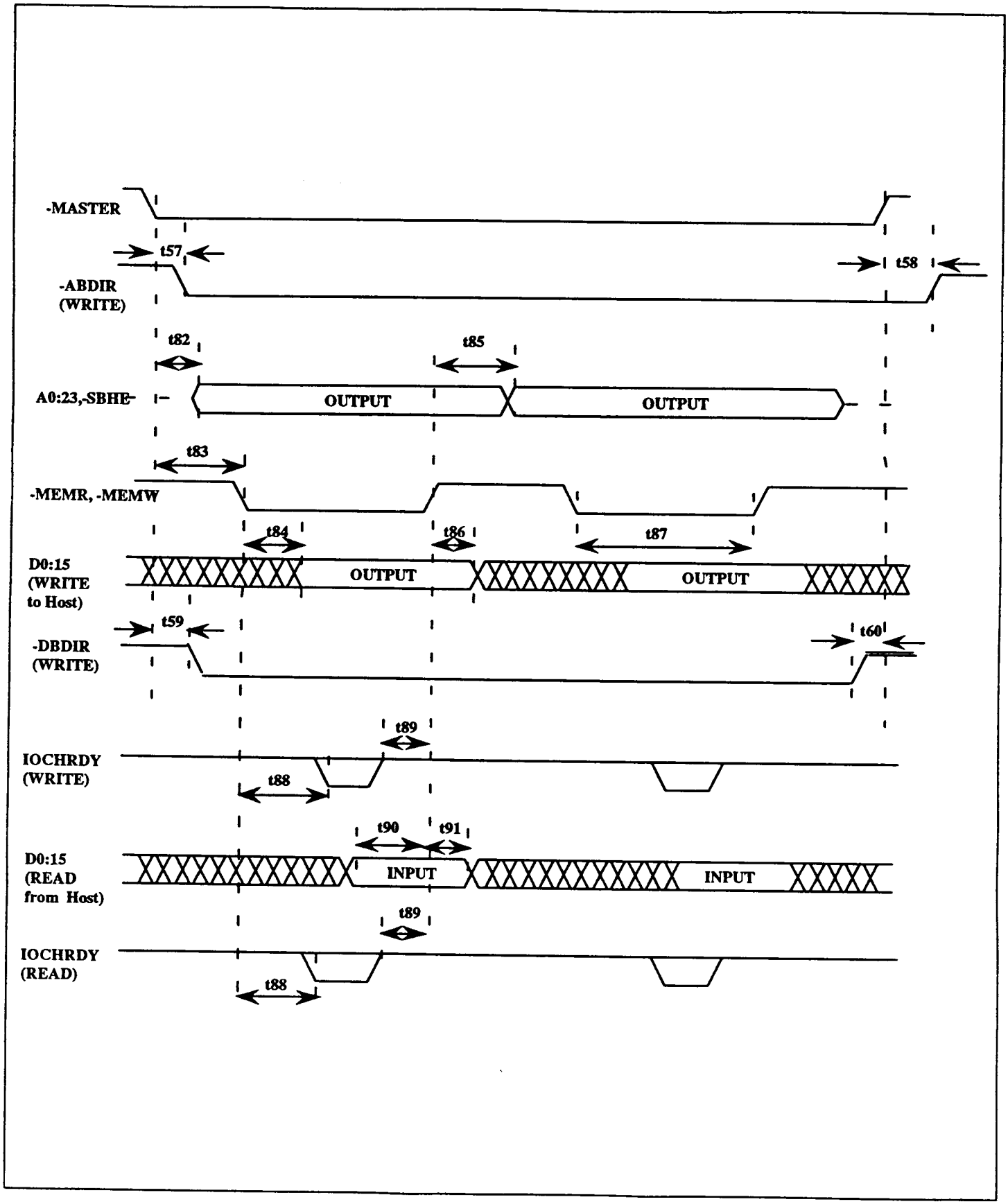


Table 7-5. **AT/ISA Bus Timing Table**

Symbol	Parameter	Min	Typ.	Max	Figure	Notes
t43	A0:15, -CS, AEN, hold from -IOR, -IOW falling edge	11			7-9	
t44	A0:15 , -CS, AEN setup to -IOR, -IOW falling edge	28			7-9	
t45	D0:15 setup to -IOW rising edge	50			7-9	
t46	D0:15 hold to -IOW rising edge	25			7-9	
t47	-IOW and IOR falling edge to IOCHRDY low delay			50	7-9	
t48	-IOW and IOR rising edge delay to IOCHRDY open collector			0	7-9	
t49	IOCHRDY delay			200	7-9	
t51	A0:15 to -IOCS16 driving low delay			50	7-9	
t52	A0:15 to -IOCS16 going high Z delay			30	7-9	
t54	D0:15 hold time from -IOR rising edge	0		30	7-9	
t55	-IOR edge to DBDIR edge delay			25	7-9	
t63	A17:23 setup to ALE falling edge	70			7-10	
t64	A17:23 hold time after ALE falling edge	15			7-10	
t66	D0:15 setup to -MEMW rising edge	50			7-10	
t67	D0:15 hold time to -MEMW rising edge	25			7-10	
t68	-MEMW or -MEMR pulse width	200			7-10	
t69	-MEMW or -MEMR falling edge to IOCHRDY low delay			50	7-10	
t70	-MEMW rising edge to IOCHRDY open collector delay			0	7-10	
t71	IOCHRDY delay	180		600	7-10	
t73	-MEMR or -MEMWR rising edge to -CS rising edge or A0:16 change	11			7-10	
t74	Address change to -MEMCS16 low delay			20	7-10	
t75	Address change to -MEMCS16 open collector			20	7-10	
t77	-MEMR rising edge to D0:15 high Z			30	7-10	
t78	-MEMR edge to DBDIR edge			20	7-10	
t79	IOCHRDY delay	180		600	7-10	
t80	A0:16, -CS, -SBHE setup to -MEMR, -MEMW	28			7-10	
t81	Command recovery time	90			7-10	

Table 7-6. **AT/ISA Bus Master Timing**

Symbol	Parameter	Min	Typ.	Max	Figure	Notes
t57	-MASTER active to -ABDIR falling edge			160	7-11	
t58	-ABDIR rising edge to -MASTER inactive			45	7-11	
t59	-MASTER active to -DBDIR falling edge			320	7-11	
t60	-DBDIR rising edge to -MASTER inactive			150	7-11	
t82	-MASTER falling edge to A0:23 valid			360	7-11	
t83	A0:23 change to falling edge -MEMR, -MEMW			95	7-11	
t84	-MEMW falling edge to D0:15 output. Write to host			0	7-11	
t85	-MEMW and -MEMR rising edge to A0:23 change	40			7-11	
t86	D0:15 hold time from -MEMW rising edge	15			7-11	
t87	-MEMR, -MEMW active to -MEMR, -MEMW inactive	110			7-11	
t88	-MEMR or -MEMW active setup from IOCHRDY inactive			30	7-11	
t89	-MEMR or -MEMW active hold from IOCHRDY active			175	7-11	
t90	D0:15 setup to -MEMR rising edge	50			7-11	
t91	D0:15 hold to -MEMR rising edge	0			7-11	

CP (V30H) Interface

Figure 7-12. CP (V30H) Interface Timing

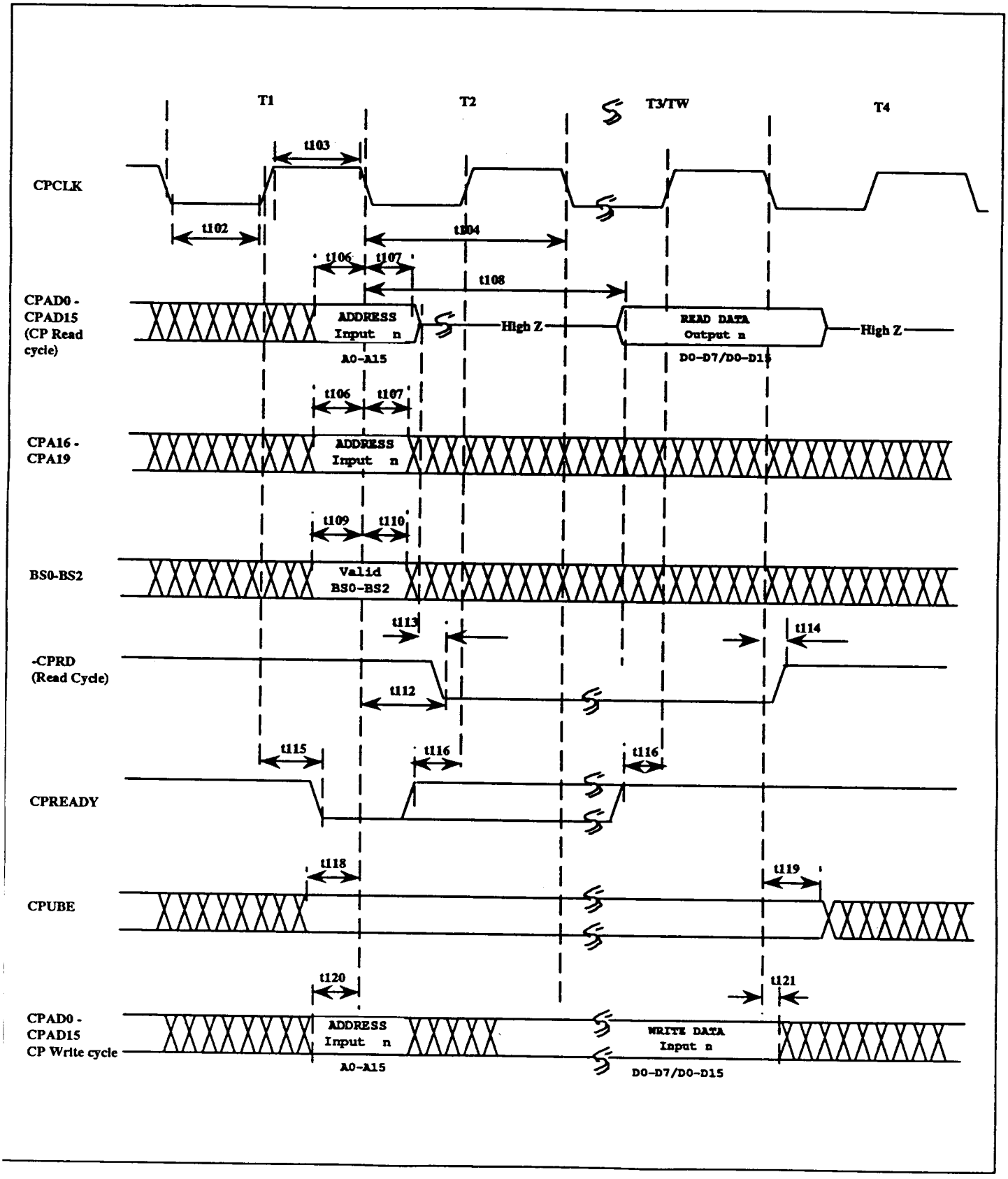


Figure 7-13. **CP (V30H) Interface Interrupt Acknowledge Cycle Timing**

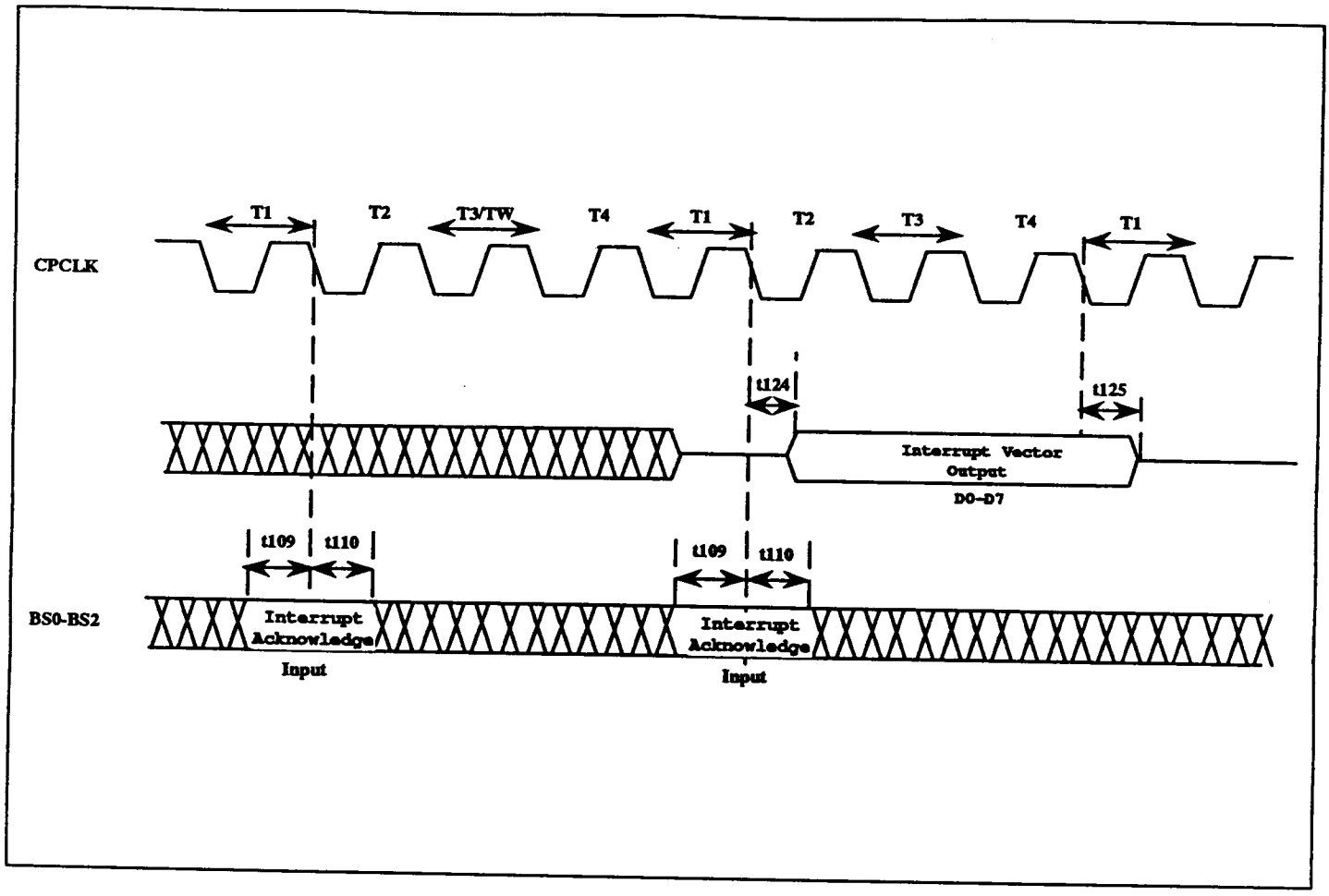


Table 7-7. **CP (V30H) Interface Timing Table**

Symbol	Parameter	Min	Typ.	Max	Figure	Notes
t100	CPCLK falling edge			3		
t101	CPCLK rising edge			3		
t102	CPCLK low time	25			7-12	
t103	CPCLK high time	25			7-12	
t104	CPCLK period	62.5			7-12	
t106	CPAD0:15, CPA16:19 setup time to falling edge of CPCLK at the end of T1 cycle	20			7-12	
t107	CPAD0:15, CPA16:19 hold time to falling edge CPCLK at the end of T1 cycle	5			7-12	
t108	CPAD0:15 data valid to end of T1 read cycle			2 x CPCLK -20	7-12	
t109	BS0:BS2 setup time to end of T1 cycle	20			7-12, 7-13	
t110	BS0:BS2 hold time from end of T1 cycle	5			7-12, 7-13	
t112	-CPRD active delay from end of T1 read cycle	0			7-12	
t113	-CPRD active delay from CPAD0:CPAD15 high- Z (Read cycle)	0			7-12	
t114	-CPRD inactive delay from end of T3 cycle CPCLK falling edge	0		30	7-12	
t115	CPREADY low delay from CPCLK rising edge during T1 cycle			20	7-12	
t116	CPREADY setup time to CPCLK rising edge during T2 or T3 cycle	20			7-12	
t118	CPUBE setup time to CPCLK falling edge at the end of T1 cycle	20			7-12	
t119	CPUBE hold time to CPCLK falling edge at the end of T3 cycle	0			7-12	
t120	CPAD0:15 setup time to falling edge of CPCLK at the end of T2 cycle	20			7-12	
t121	CPAD0:15 hold time to falling edge of CPCLK at the end of T3 cycle	0		30	7-12	
t124	Interrupt vector valid from T1	20			7-13	
t125	Interrupt vector hold from T1	0		5	7-13	

Private Memory Interface

Figure 7-14. SRAM Memory Timing

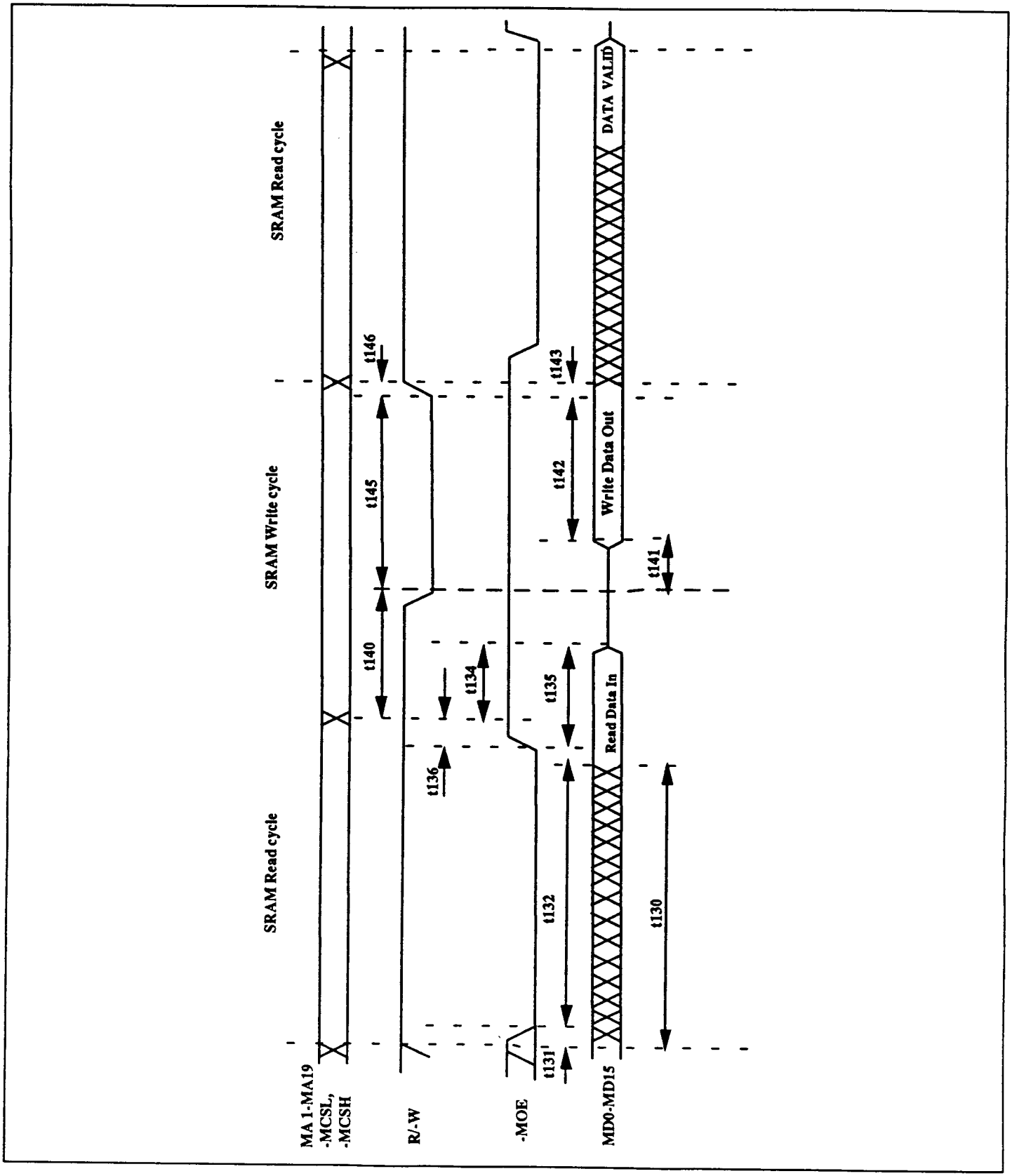


Figure 7-15. **EPROM/IO Timing**

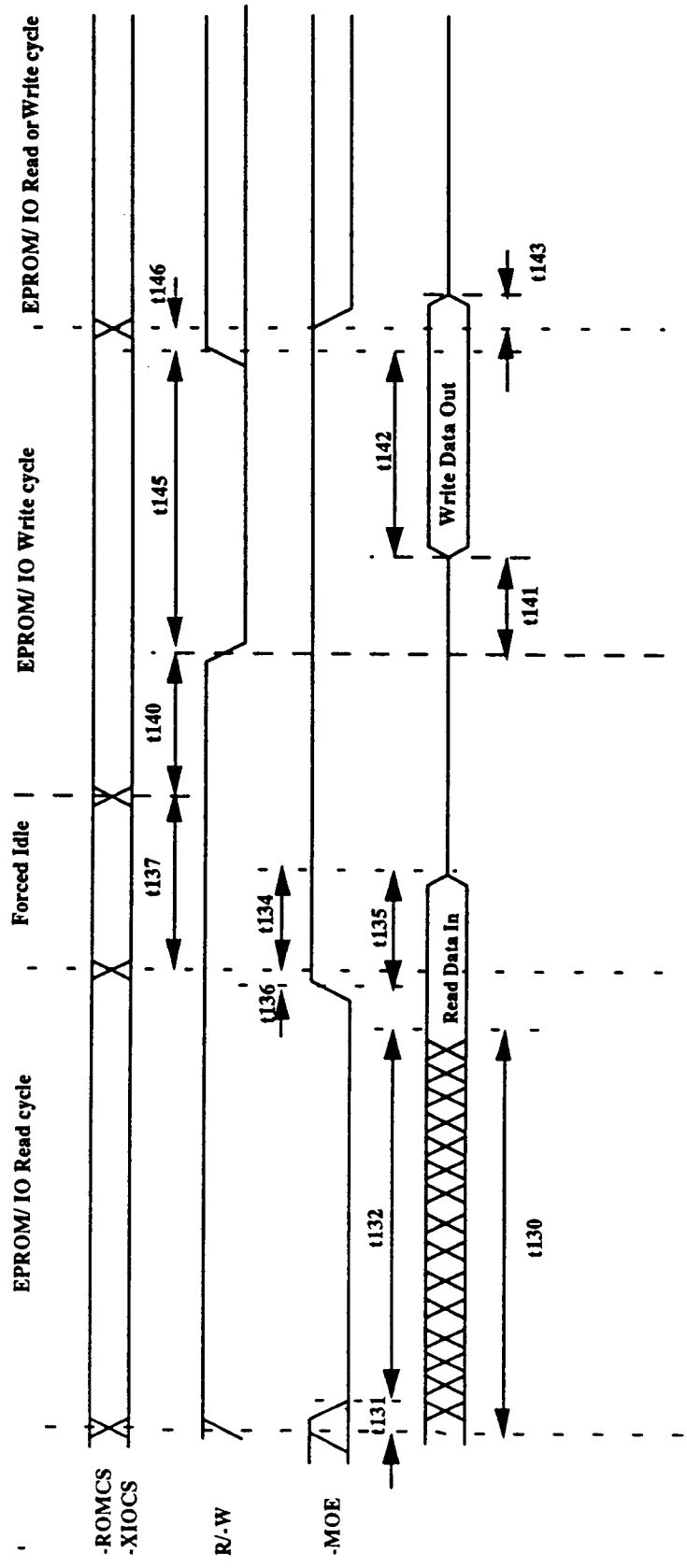


Table 7-8. **Private Memory Timing Table**

		Fast RAM Mode		Slow RAM Mode		EPROM/IO		
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Figure
t130	Address and chip select access time		30		90		200	7-14, 7-15
t131	Address and chip select active to output enable	0	10	0	10	0	10	7-14, 7-15
t132	Output enable access time		20		60		100	7-14, 7-15
t134	Chip disable to high Z output delay		15		40		60	7-14, 7-15
t135	Output disable to high Z output delay		15		40		60	7-14, 7-15
t136	Output disable to address and chip select inactive	0		0		0		7-14
t137	Forced idle time						60	7-15
t140	Address setup time	0		10		10		7-14, 7-15
t141	Write active to write data valid delay	20		50		110		7-14, 7-15
t142	Data setup time	15		40		100		7-14, 7-15
t143	Data hold time	5		10		10		7-14, 7-15
t145	Write pulse width	30		90		210		7-14, 7-15
t146	Write inactive to address and chip select inactive	6		6		6		7-14, 7-15

Ethernet Front End Interface

Figure 7-16. **Ethernet Front End Timing**

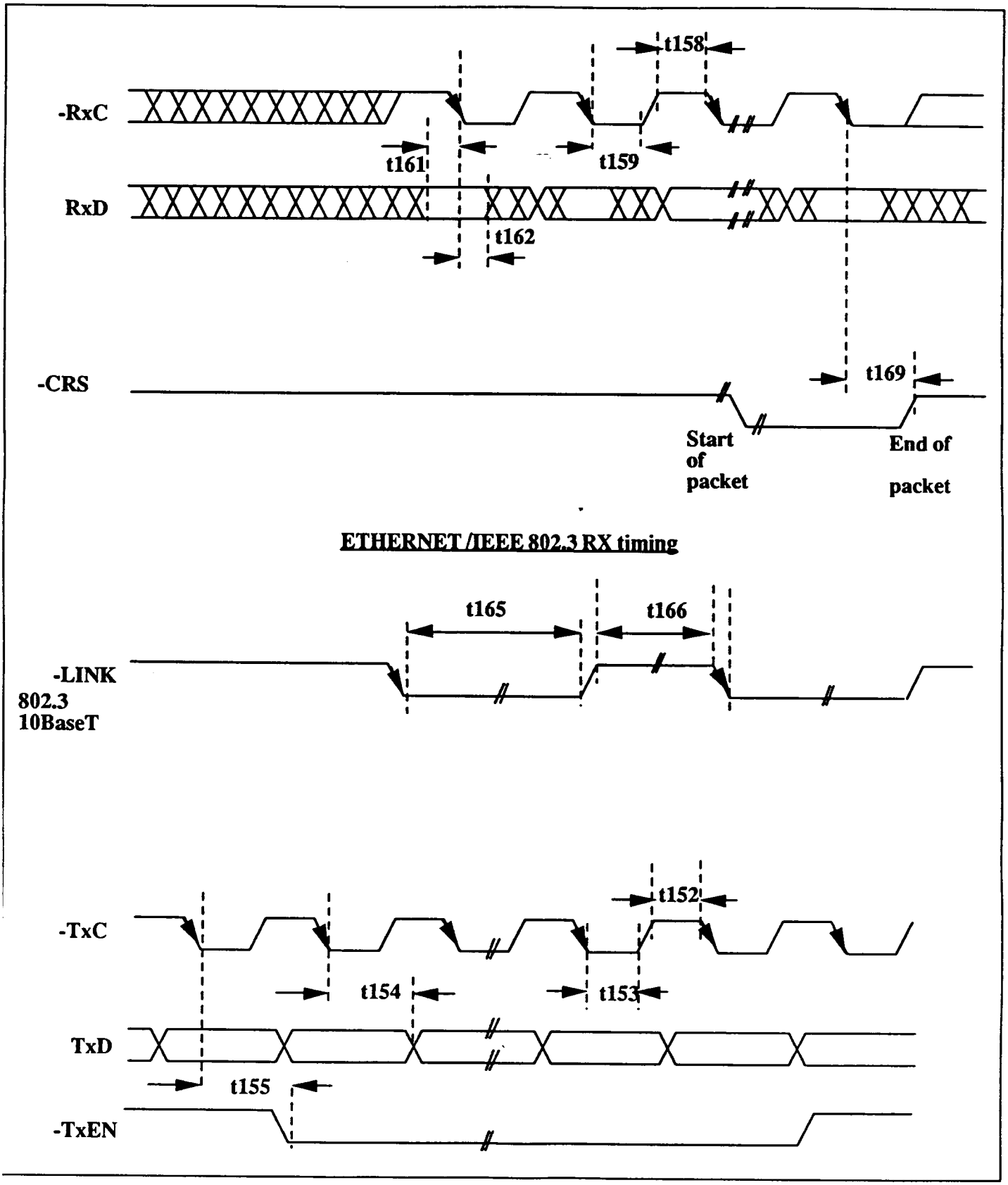
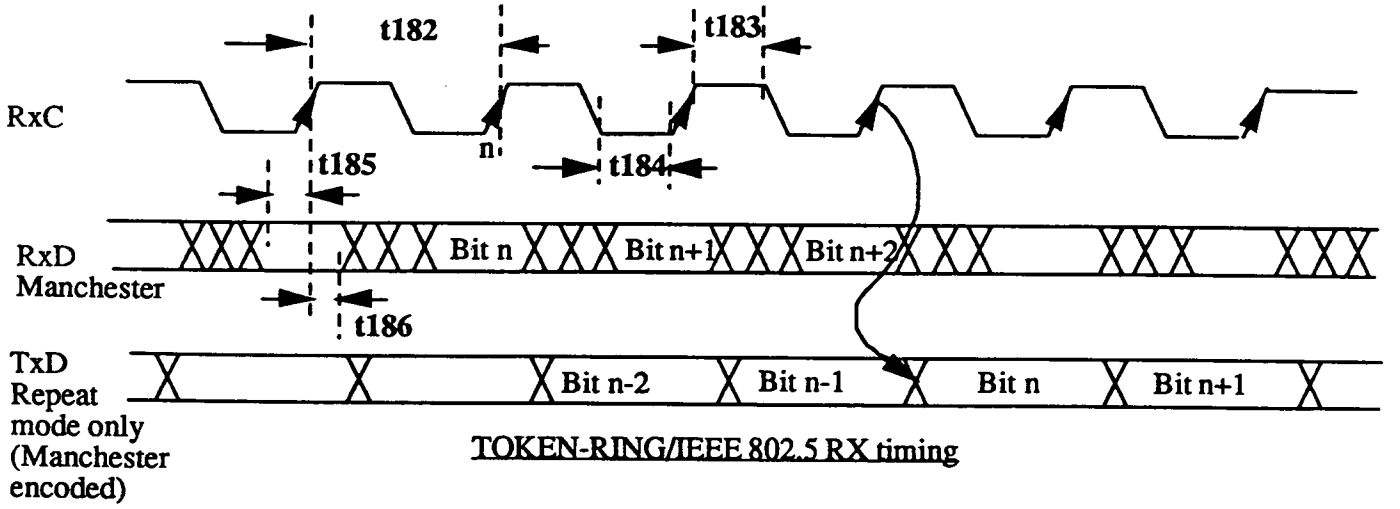


Table 7-9. **Ethernet Front End Timing Table**

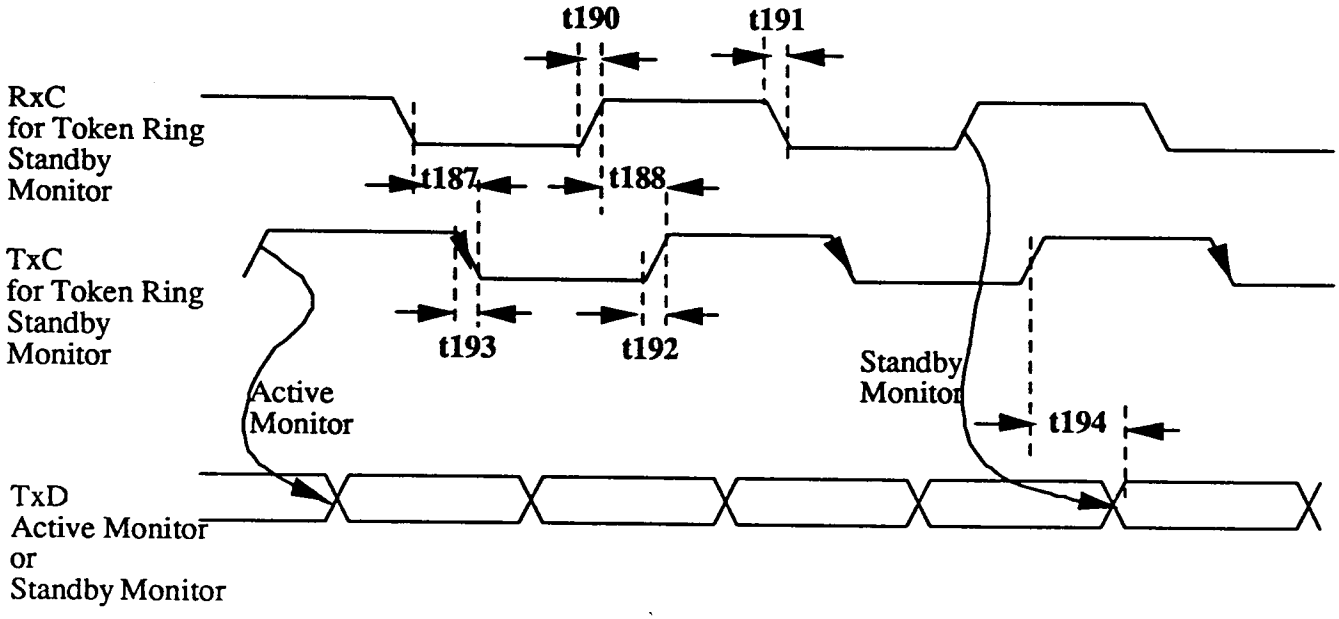
Symbol	Parameter	Min	Typ.	Max	Figure	Notes
t150	-TXC rise time			5		
t151	-TXC fall time			5		
t152	-TXC high time at 10 MBPS Ethernet	35			7-16	
t153	-TXC Low time at 10 MBPS Ethernet	35			7-16	
t154	-TXC falling edge to TXD change			25	7-16	
t155	-TXC falling edge to -TXEN change			30	7-16	
t156	-RXC rise time			5		
t157	-RXC fall time			5		
t158	-RXC high time at 10 MBPS Ethernet	35			7-16	
t159	-RXC low time at 10 MBPS Ethernet	35			7-16	
t161	RXD setup	10			7-16	
t162	RXD hold	10			7-16	
t163	-COL low time	200				
t164	-COL high time	200				
t165	-LINK low time	200			7-16	
t166	-LINK high time	200			7-16	
t167	NOLRN high time	800				
t168	-MATCH/-FLUSH low time	100				
t169	-CRS inactive from -RXC	24			7-16	

Token-Ring Interface

Figure 7-17. **Token-Ring Interface Timing**



TOKEN-RING/IEEE 802.5 RX timing

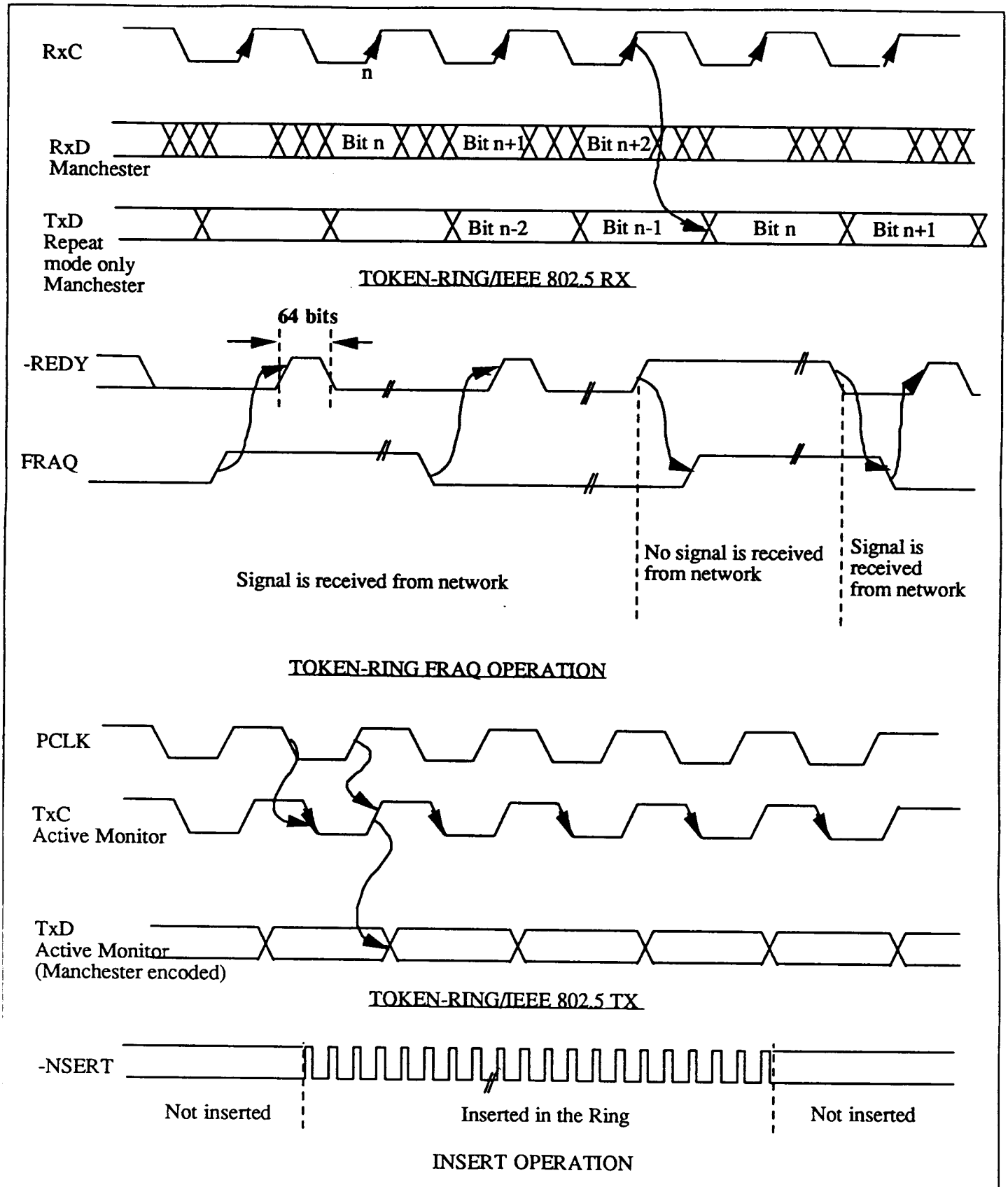


TOKEN-RING/IEEE 802.5 TX timing

Table 7-10. **Token Ring Front End Timing Table**

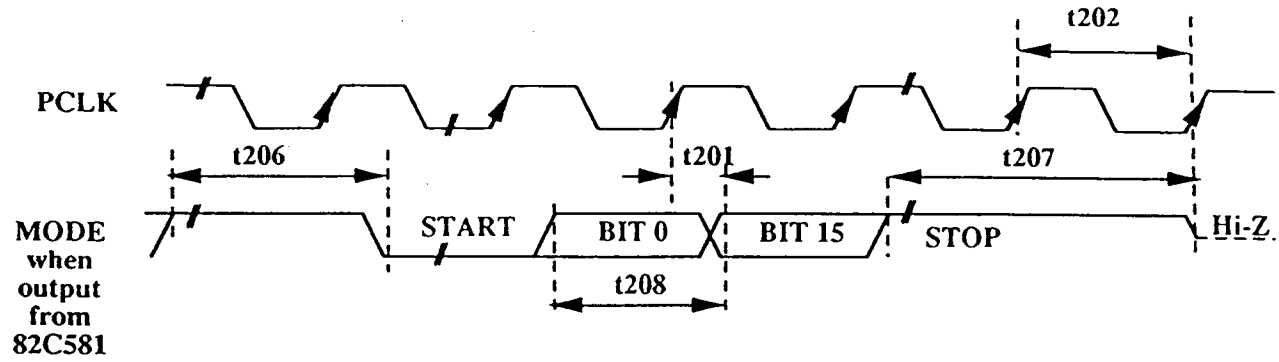
Symbol	Parameter	Min	Typ.	Max	Figure	Notes
t180	PCLK rise time			3	7-17	
t181	PCLK fall time			3		
t182	-RXC period	28			7-17	
t183	-RXC high time	10			7-17	
t184	-RXC low time	10			7-17	
t185	RXD setup time to rising edge RXC	6			7-17	
t186	RXD hold time to rising edge RXC	6			7-17	
t187	-RXC falling edge to TXC falling edge NON active monitor			25	7-17	
t188	-RXC rising edge to TXC rising edge NON active monitor			25	7-17	
t190	-RXC rise time			3	7-17	
t191	-RXC fall time			3	7-17	
t192	TXC rise time			3	7-17	
t193	TXC fall time			3	7-17	
t194	TXC rising edge to TXD change	0		8	7-17	
t197	-WFLT low time	1RXC				
t198	NOLRN high time	16 RXC		?		
t199	-MATCH/-FLUSH low time	4 RXC				

Figure 7-18. **Token-Ring Functional Timing**

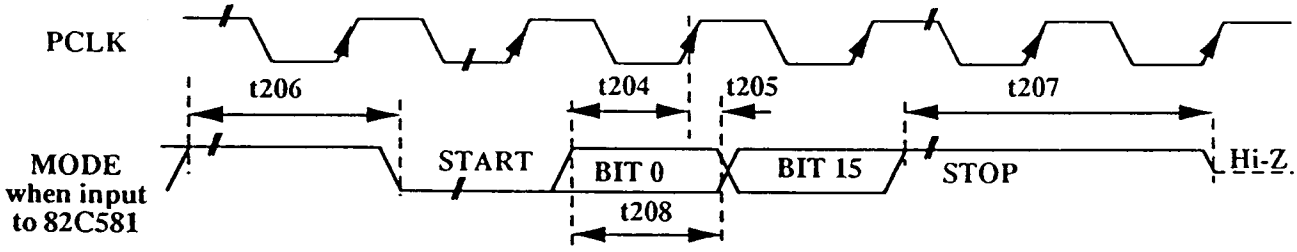


Miscellaneous Interfaces

Figure 7-19. **Miscellaneous Interfaces Timing**



Serial Port
Transmit
Timing



Serial Port
Receive
Timing

Table 7-11. **Miscellaneous Interfaces Timing Table**

Symbol	Parameter	Min	Typ.	Max	Figure	Notes
t201	PCLK rising edge to MODE output change			15	7-19	
t202	PCLK rising edge to MODE float			15	7-19	
t204	MODE setup time	10			7-19	
t205	MODE hold time	10			7-19	
t206	MODE active to START bit	4 PCLKs			7-19	
t207	STOP bit to MODE inactive	4 PCLKs			7-19	
t208	MODE bit length	4 PCLKs			7-19	
t210	32MCLK clock high time	12				
t211	32MCLK clock low time	14				
t212	RESET high time	50 x 62.5				
t213	RESET glitch filter			62.5		
t214	PMAEN, BIMOD0, BIMOD1, BIMOD2, IOID0, IOID1, MID0, MID1, SLOWRAM, BCLKDIV, CPHOLD, PSPD, PTYPE setup time to RESET falling edge	25				Timing for sampling during power up. These pins have a different functionalily after power up.
t215	PMAEN, BIMOD0, BIMOD1, BIMOD2, IOID0, IOID1, MID0, MID1, SLOWRAM, BCLKDIV, CPHOLD, PSPD, PTYPE hold time from RESET falling edge	10				Timing for sampling during power up. These pins have different functionality after power up.