Product Brief

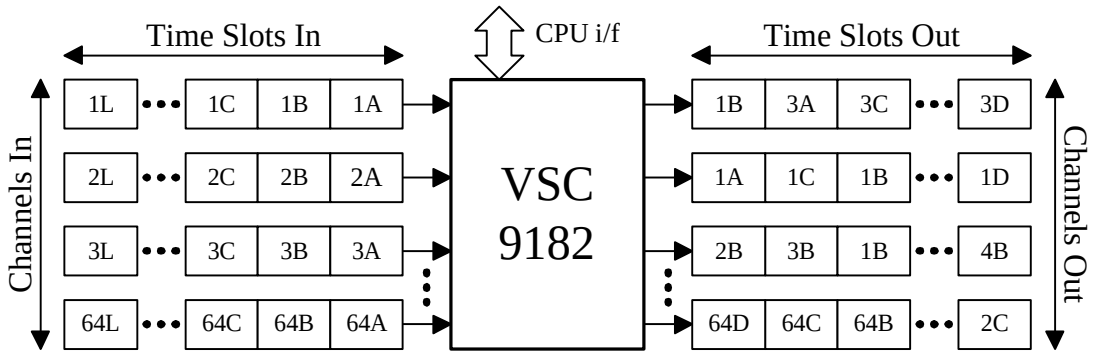
VSC9182 - Timberline

TimeStream Product Family
64x64 STS-12/STM-4 TSI Switch Fabric

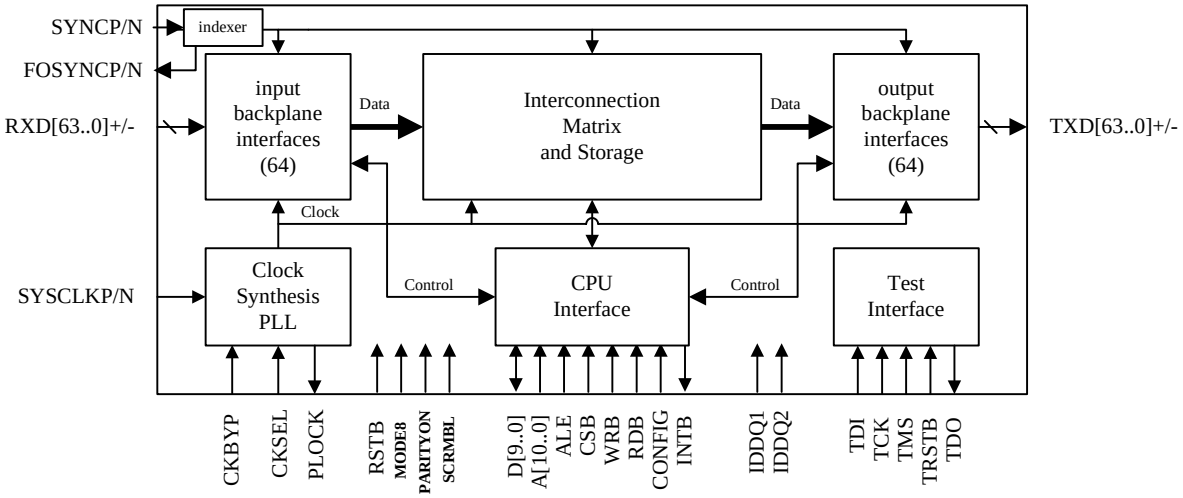
Features

- 64x64 STS-12/STM-4 TSI switch with non-blocking 768x768 STS-1 switch matrix
- Supports both multicast and broadcast
- Serial LVDS 622 Mb/s high-speed interface with PECL/CML compatibility and retiming
- 50MHz 11-bit microprocessor interface
- IEEE P1149.1 test access port
- Compatible with VSC9184 ADM & Pointer Processor and VSC9180 Hitless Backplane Tranceiver
- Integrated clock synthesis with a choice of two reference frequencies
- LOS Detection, input parity checking & output parity insertion; scrambling & descrambling
- Hitless reconfiguration of TSI mapping
- Single +3.3V Power Supply
- Compliant with SONET and SDH requirements as stated in ANSI T1.105, Bellcore GR-253-CORE and ITU-T G.707 documents
- Thermally Enhanced 37.5mm 480 BGA Package

Functional Diagram



VSC9182 Block Diagram



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Functional Overview

The VSC9182 is a 64x64 STS-12/STM-4 Time Slot Interchange Switch IC for Cross Connection and Ring Protection Switching of STS(n) tributaries. All STS-12/STM-4 inputs and outputs are differential serial signals running at 622.08 Mb/s for efficiency in switch card and system backplane design. Together with the STS-48/STM-16 Pointer Processor & Frame Aligner IC (VSC9184), a complete 16x16 STS-48/STM-16 TSI-switch can be built.

Interconnection Matrix

- Time & Space Switches any STS-(n) [n= 1, 3c, 12c] signal of an incoming STS-12 into any byte position of any STS-12 output
- Single Stage non-blocking structure of the switch allows for Multicast and Full Broadcast
- Hitless Switching: programming is queued and takes effect after user intervention during the next frame boundary
- Provides a capability to read out the switch configuration (address map)

Input Backplane Interface

- Serial 622.08 Mb/s Differential LVDS STS-12/STM-4 inputs
- Receives 64 serial 622.08 Mb/s STS-12/STM-4 Line channels (these 64 input signals are presumed frequency synchronous and frame aligned to within +/- 3 time slots of the system SYNC input)
- Provides on-chip data recovery de-skewing functionality to bit-align, byte-align and frame-align all incoming STS-12s (within the above tolerance) to the local clock
- Flags out-of-frame (OOF), loss-of-signal (LOS) and parity errors
- Checks byte-interleaved parity of incoming data vs. B1 byte of following frame
- Inserts unequipped or AIS when channel is in OOF, LOS or unprovisioned state and inhibits alarms
- Optionally de-scrambles SONET-scrambled incoming data

Output Backplane Interface

- Serial 622.08 Mb/s Differential LVDS STS-12/STM-4 outputs
- Optionally inserts byte-interleaved parity into B1 byte of following frame
- Optionally SONET scrambles outgoing data

CPU Interface

- Generic microprocessor (CPU) interface used for device configuration and status checking
- 10-bit data bus and 11-bit address bus
- Interrupt output pin to signal status changes of internal alarms

Test Interface

- IEEE P1149.1 test access port controls external boundary scan

Clock Synthesis PLL

- Monolithic PLL clock multiplier with 8x and 32x multiplication ratios available

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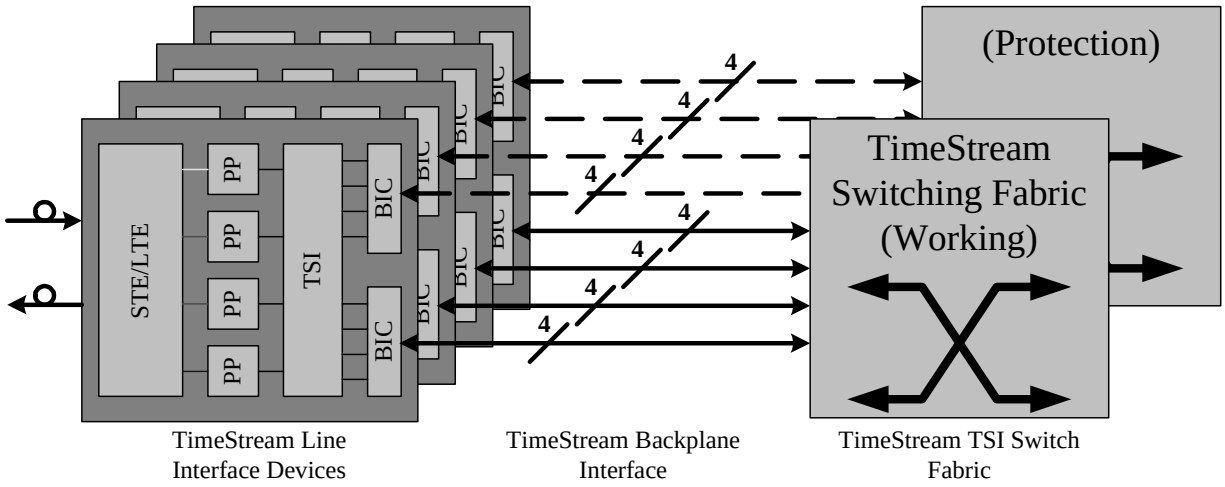
System Applications



The VSC9182 TSI Switch Fabric can be used to construct fabrics of various sizes and line interface speeds when used in conjunction with VSC9184 Line Interface devices. Four VSC9182 devices can be used in parallel to provide a 3072 x 3072 STS-1 switch with 16 STS-192/STM-64 ports, 64 STS-48/STM-16 ports or any combination of STS-3/STM-1 through STS-192/STM-64 tributaries by using the appropriate line interface devices. Larger three-layer VSC9182 Clos architectures are possible for larger fabric requirements.

VSC9184 - 2.5G Line Interface Device

- Pointer processes single STS-48/STM-16, quad STS-12/STM-4 or quad STS-3/STM-1 signals containing any valid combination of TDM and concatenated traffic.
- Section and Line termination and path monitoring of tributaries
- Working and Protection (4 x 622Mb/s) backplane interface with 48x96 and 96x48 TSI.

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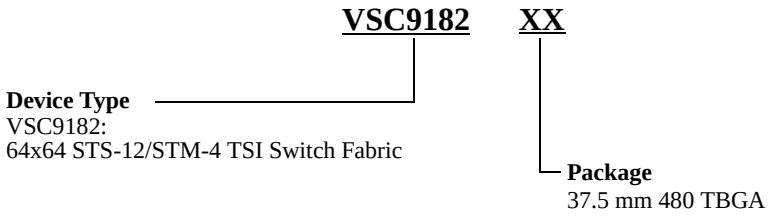
Ordering Information

The order number for this product is formed by a combination of the device number, and package type.



Notice

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Warning

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