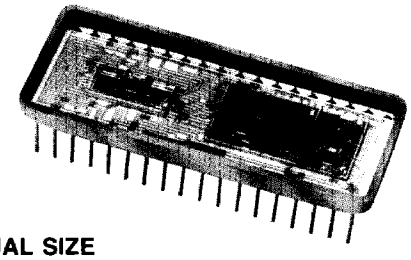
NATEL

HDSR2056 996211

Digital-to-Synchro/Resolver Converter Microprocessor Compatible 16-bit Hybrid

Features

- **Single 36-pin hybrid DDIP package**
- **1 arc-minute accuracy**
- **0.03% radius accuracy**
- **Microprocessor compatible** (8 and 16-bit)
- **Double buffered inputs**
- **Pin-programmable synchro or resolver output**
- **Pin-programmable reference input** (for 1.3, 26 and 115 V-rms)
- **Resistor-programmable** (for non-standard reference)
- **Requires only ± 15-V power supplies**
- **TTL and CMOS compatible**
- **Hi rel MIL-STD-883B processing**
- **Priced at $395/USA single unit price** (HDSR2056-14S)



ACTUAL SIZE

Applications

Polar to rectangular coordinate conversion
Missile and fire control systems
Flight instrumentation
Simulation systems
Digital phase shifting
Rotating PPI sweep
Radar and navigational systems
Axis rotation

Description

The 2056 is a versatile 4-quadrant multiplying digital-to-sin/cos converter. By external pin programming the converter can also provide the angular information in synchro format. Offering both 8- and 16-bit microprocessor compatibility, the HDSR2056 is a second generation, lower cost version of the Natel Model 2006.

Angular accuracy of 1 arc-minute and radius accuracy of 0.03% make HDSR2056 an ideal choice for applications requiring small size and true sine and cosine outputs. Certain closed-loop systems, resolver computing chains, coordinate transformation and PPI (sweep) displays are examples of such applications.

Packaged in a standard 36-pin DDIP, the converter does not require a +5-V logic supply. The digital inputs are TTL and 5-V CMOS compatible, Internally derived logic thresholds are 0.8 V-dc for a logic "low" and 2.4 V-dc for a logic "high."

All data bits (B1 through B16) are actively pulled down to ground. If the converter requires less than 16-bit resolution, the unused data bit pins may be left unconnected. Control Signals LBE, HBE and LDC are actively pulled-up to logic "high." When not required by your application, these pins may also be left open.

Although designed to interface with most microprocessors, the HDSR2056 may be used in conventional applications without any external components or additional connections.

Model HDSR2056 converters are available with angular accuracies of 1, 2 and 4 arc-minutes. These accuracies are guaranteed over the specified operating temperature range. The exceptionally high accuracy of these converters is achieved by a unique design approach that uses buffer amplifier circuits to eliminate the effects of analog switch resistance instead of requiring special compensation circuits.

Matched thin-film resistors are used to scale the reference input at well as the synchro and resolver outputs to assure excellent performance over the entire operating temperature range. All gain resistors are actively laser trimmed to achieve precise performance.

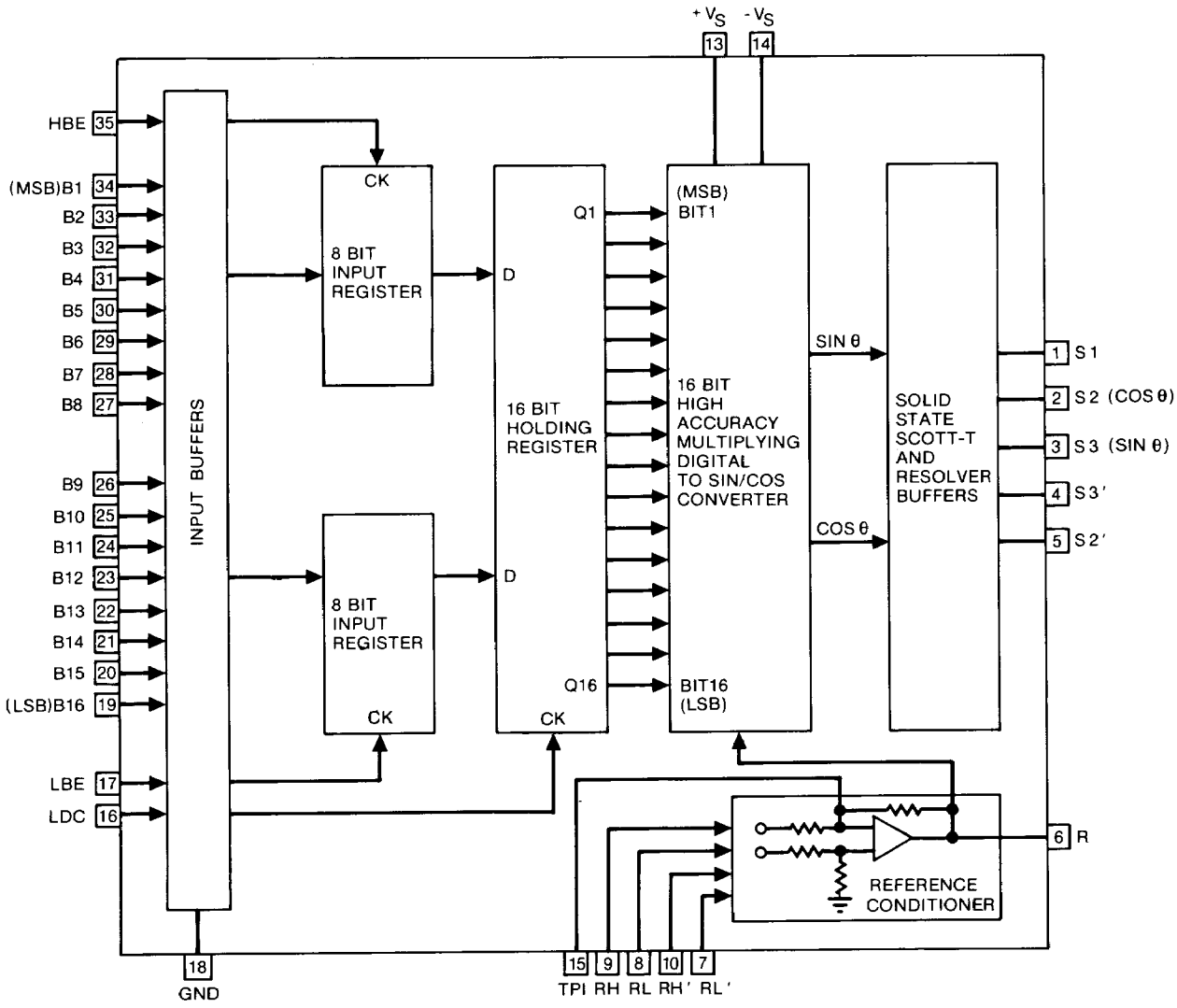


FIGURE 1 2056 Block Diagram

Operation of the Model 2056 is illustrated in the functional diagram of Figure 1. The reference voltage is applied to a differential amplifier to obtain a low level buffered reference. In addition, the reference conditioner allows the user to program for different reference voltages by appropriate pin connections (see Reference Level Adjustment).

The digital word representing the input angle is applied to input buffers. Two input registers accept 16-bits from the microprocessor. In conjunction with an 8-bit data bus, each input register can be independently enabled to accept the 16-bit word in two 8-bit bytes. When interfacing with a 16-bit bus, both input registers are enabled simultaneously to accept a 16-bit parallel input word. The 16-bit data word is then parallel-loaded into a holding register and processed through a Multiplying Digital-to-Sin/Cos converter.

The multiplying digital-to-sin/cos converter is made up of two function generators (sin θ and cos θ) and a quadrant select network. The digital input code is natural binary angle. The two most significant bits (Bit 1 = 180°, Bit 2 = 90°) determine the quadrant information. Bits 3 through 16, containing angular information together with buffered reference voltage, are applied to the two function generators. The operation of the function generators is very similar to a 4-quadrant multiplying DAC. Like a conventional DAC, the 2056 uses resistive ladder networks and solid state switching to control the attenuation of the reference voltage. The ladder networks, however, are designed to attenuate the input reference proportional to the sine and cosine of the digital input angle. A unique approach is used in the design of ladder networks to obtain high accuracy in the sine and cosine generation so that they can be used as independently accurate functions. The outputs of the function generators are then applied to a quadrant select network to obtain true sin θ and cos θ outputs. The outputs of the quadrant select circuit are then applied to a scott-tee and resolver buffer circuit. The output conditioning circuit is configured to allow pin-programming for either synchro or resolver output.

Specifications

PARAMETER	VALUE	REMARKS
Digital Angular Resolution	16 bits (0.33 arc-minutes)	MSB = 180° LSB = 0.0055°
Accuracy	±4 arc-minutes (option S) ±2 arc-minutes (option H) ±1 arc-minute (option V)	Accuracy applies over operating temp. range
Scale Factor Variation (Transformation Ratio Error)	±0.03% maximum	Simultaneous amplitude variation in all outputs as a function of digital angle.
Reference Input		Differential solid state input
Internal Resistors	Pin-programmable for 1.3, 26 and 115 V-rms (±10%)	
External Resistors	Programmable for voltages 1.3 to 115 V-rms by adding two external resistors	See Reference Level Adjustment
Frequency Range	dc to 1000 Hz (option 4) dc to 5 kHz (option 5)	
Input Impedance RH - RL	Differential 200 kΩ±0.25% Single Ended 100 kΩ±0.25%	
RH' - RL'	Differential 10 kΩ±0.25% Single Ended 5 kΩ±0.25%	
Common Mode Voltage Range 26 V-rms (RH-RL) 115 V-rms (RH-RL) 1.3 V-rms (RH'-RL') **Common Mode Rejection Ratio**	 ±80 V peak ±200 V peak ±4 V peak 50dB minimum	 RH', RL' unterminated RH', RL' connected to GND RH, RL Unterminated
Analog Outputs		Output voltage varies directly in proportion to reference voltage
Synchro Format	11.8 V-rms line-to-line ±0.2%	S1, S2, S3 outputs
Resolver Format	6.81 V-rms ±0.2%	Sin, Cos output
"R" Output	2.27 V-rms Nominal	
Output current	2 mA-rms	Short circuit proof
Output impedance	< 1 ohm	Operational amplifier output
Zero offset (dc)	±10 mV typical, ±25 mV maximum	
Offset drift	25 μV/°C	
Output Settling time	20 μsec maximum to accuracy of the converter	For any analog or digital step change
Digital Inputs **Logic Voltage Levels**		CMOS transient protected
Logic "0" Logic "1"	−0.3 V-dc to 0.8 V-dc +2.4 V-dc to +5.5 V-dc	Does not need external logic voltage 0.1 TTL load
Input Currents		
Data Bits (B1-B16)	15 μA typical, "active" pull down to Ground (GND)	For less than 16-bits input, unused pins can be left unconnected
HBE, LBE, LDC	−15 μA typical, "active" pull up to internal logic supply	When not used, pins can be left unconnected
Register Controls		
HBE	Logic "1" Logic "0"	8 MSBs enter high byte input register High byte register remains unaffected
LBE	Logic "1" Logic "0"	8 LSBs enter low byte input register Low byte register remains unaffected
LDC	Logic "1" Logic "0"	Data from input registers transferred to holding register Data in holding register remains unaffected
Pulse Width	600 nsec minimum	For guaranteed data transfer
Data Set-up time	200 nsec minimum	Before data transfer
Data Hold time	200 nsec minimum	Before input data changes
Power Supplies		
Supply voltages (±VS) Supply Currents Supply Rejection	±15 V-dc ± 10% ±25 mA maximum 80 dB typical	Without output clipping
Physical Characteristics		
Type	36 PIN Double DIP	
Size	0.78 x 1.9 x 0.21 inch (20 x 48 x 5.3 mm)	3 standoffs are added to the package to insulate it from printed circuit board traces. (Standoffs included in 0.21-inch height dimension)
Weight	0.6 oz (17 g) max	

Pin Designations

B1 - B16	Parallel Data Input Bits B1 is MSB = 180 degrees B16 is LSB = 0.0055 degree
HBE	High Byte Enable - Data inputs B1 through B8 enter the input buffer register when HBE is set to a Logic "High." When HBE is set to Logic "Low" the input register is in the hold mode and is not affected by digital activity at the input data bits B1-B8 pins.
LBE	Low Byte Enable - Data inputs B9 through B16 enter the input buffer register when LBE is set to Logic "High." When LBE is set to Logic 'Low" the input register is in the hold mode and is not affected by digital activity at the input data bits B9-B16 pins.
LDC	Load Converter - When LDC is set to a Logic "High," the converter will transfer the contents of the input buffer registers to the 16-bit holding register. When LDC is set to Logic "Low," the converter is in the hold mode and is not affected by digital activity in the input registers.
Note:	For continuous updating HBE, LBE and LDC may be left open. Internal active pull-up will force these functions to a Logic "High."
TP1	Test Point - Leave this pin open (no external power should be applied to this pin)
$+V_S$, $-V_S$	Supply Voltages - Typically ±15 V-dc
GND	Power Supply Ground Digital Ground Analog Signal Ground
RH, RL, RH', RL'	Reference Voltage Input - Pin programmable for 1.3, 26 and 115 V-rms inputs (See text for connections)

S1	1	36	N.C.
(COS) S2	2	35	HBE
(SIN) S3	3	34	B1
S3'	4	33	B2
S2'	5	32	B3
R	6	31	B4
RL'	7	30	B5
RL	8	29	B6
RH	9	28	B7
RH'	10	27	B8
N.C.	11	26	B9
N.C.	12	25	B10
$+V_S$	13	24	B11
$-V_S$	14	23	B12
TPI	15	22	B13
LDC	16	21	B14
LBE	17	20	B15
GND	18	19	B16

FIGURE 2 HDSR2056 Pin Assignments

R	Buffered Reference Voltage - Nominal output 2.27 V-rms for standard input reference voltages
S1, S2, S3, S2' S3'	Output Analog Signal- Pin programmable for Synchro or Resolver output (See text for connections)

Absolute Maximum Ratings

Reference Input ..... Twice specified Voltage
Power Supply Voltages ($\pm V_S$) ..... ±18 V-dc
Digital Inputs ..... −0.3 V-dc to +6.5 V-dc
Storage Temperature ..... −65°C to +135°C

Although Digital inputs are CMOS protected, storage in conductive foam is recommended.

When installing on or removing the converter from printed circuit boards or sockets, it is recommended that the power supply be turned off. Decoupling capacitors are recommended on the $+V_S$ and $-V_S$ supplies. A 1μF tantalum capacitor in parallel with 0.01μF ceramic capacitor should be mounted as close to the supply pins as possible.

Caution: Reversal of $+V_S$ and $-V_S$ power supply connections will result in permanent damage to the converter.

Reference Level Adjustment

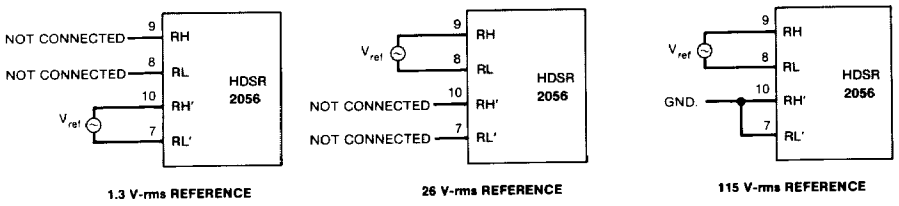
Operation of the HDSR2056 is very similar to that of a multiplying digital-to-analog converter. The sine and cosine outputs are directly proportional to and have the same waveform as the reference voltage. Any distortion or harmonics present at the reference will appear at the output lines.

Internal resistors permit pin programming for three standard reference voltages with the normal analog output (6.81 V-rms for Resolvers and 11.8 V-rms for Synchros). The connections for the three reference voltages — 1.3 V-rms, 26 V-rms and 115 V-rms — are shown in figure 3. Proportionally higher or lower voltages will be obtained for analog outputs when higher or lower reference voltages are used.

To obtain nominal analog output with non-standard reference voltages, two external resistors are required. The input resistance for RH and RL is 100 kΩ. RH' and RL' are each 5 kΩ. The circuit configuration for reference voltages other than nominal is shown in figure 4.

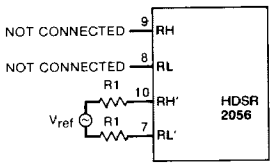
For high reference voltages (26 to 115 V-rms), the resistor values for R1 might become too large to be practical. In those situations the external resistor should be connected as shown in figure 5.

For reference voltages greater than 115 V-rms the external resistors should be connected as shown in figure 6.



1.3 V-rms REFERENCE — 26 V-rms REFERENCE — 115 V-rms REFERENCE

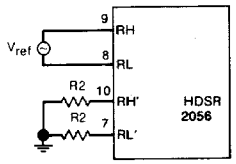
FIGURE 3



$$R1 = \frac{5}{1.3}(V_{ref} - 1.3)\ \text{K Ohms}$$

V_{ref} (V-rms)	2	3	5	7	10	13	16	20	25
R1 (K Ohms)	2.69	6.54	14.23	21.92	33.46	45.00	56.54	71.92	91.15

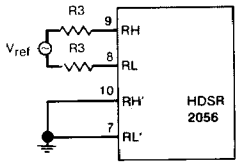
FIGURE 4 V_{ref} = 1.3 V-rms to 26 V-rms



$$R2 = \left(\frac{97.54}{V_{ref} - 26} - 1.096\right)\ \text{K Ohms}$$

V_{ref} (V-rms)	30	40	50	60	70	80	90	100	110
R2 (K Ohms)	23.28	5.87	2.97	1.77	1.12	0.710	0.428	0.222	0.065

FIGURE 5 V_{ref} = 26 V-rms to 115 V-rms



$$R3 = (0.8558\ V_{ref} - 98.417)\ \text{K Ohms}$$

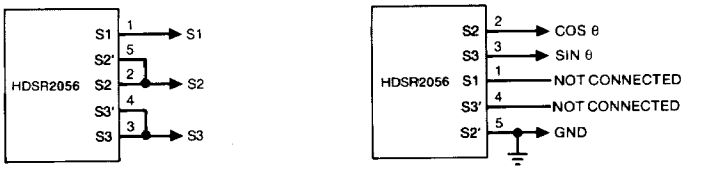
V_{ref} (V-rms)	120	130	140	150	160	170	180	190	200
R3 (K Ohms)	4.28	12.84	21.40	29.95	38.51	47.07	55.63	64.19	72.74

FIGURE 6 V_{ref} Greater than 115 V-rms

Synchro/Resolver Connections — Output Phasing and Gain

The connections for synchro and resolver outputs are shown in figure 7. For standard reference voltages, the gain of the converter is factory adjusted to provide voltages of 6.81 V-rms for maximum sine and cosine outputs in the resolver configuration and 11.8 V-rms in the synchro configuration. The gain accuracy using internal resistors is ±0.2%. Applications requiring exact gain can be accommodated by using external resistors (see Reference Adjustment). Contact factory for gain accuracies of better than ±0.2%, if it is not practical to use external resistors.

With ±15-V supply voltages, clipping of the output waveform will occur if the reference amplitude exceeds the specified value by more than 10%.



$E_{S3-S1} = K_1 V_{ref} (1 + n) \sin\theta$

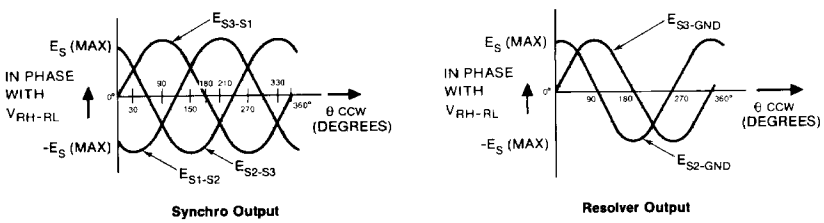
$E_{S2-S3} = K_1 V_{ref} (1 + n) \sin(\theta + 120°)$

$E_{S1-S2} = K_1 V_{ref} (1 + n) \sin(\theta + 240°)$

$E_{S3-GND} = K_2 V_{ref} (1 + n) \sin\theta$

$E_{S2-GND} = K_2 V_{ref} (1 + n) \cos\theta$

K is the gain of the converter and n is the scale factor variation as a function of digital angle. (±0.03%)



Synchro Output — Resolver Output

FIGURE 7 Synchro/Resolver Outputs

Digital Interface

The double buffered input registers of the HDSR2056 offer the user an easily implemented interface with 8- or 16-bit microprocessor data buses. For applications not involving a microprocessor, independently controlled 8-bit latching registers give the user the flexibility of designing his own interface system. Provision has also been made for asynchronous data inputs through the use of the LDC control function. Asynchronous data inputs up to 16 bits can be accommodated.

Continuous Operation

Asynchronous converter operation, without timing controls, is shown in figure 8. Inputs LBE, HBE and,t LDC have internal pull-up circuitry, permitting these pins to be left open. The parallel information at the data inputs B1-B16 is continuously converted to synchro or resolver format information at the analog outputs. For applications requiring less than 16-bit resolution, unused pins can be left open. Internal pull-down circuitry applies a logic "0" to unconnected data inputs B1-B16.

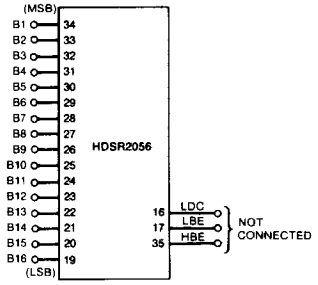


FIGURE 8 Digital Connection for Continuous Operation

Two-Byte Loading

The circuit configuration for two-byte loading of angular data from a data bus is shown in figure 9. As shown in figure 10 timing diagram, the 8 LSBs (B9-B16) are transferred to the low-byte input register when LBE is a logic "1". LBE can be "High" when data bits are changing, but must remain "High" for a minimum of 800 nsec after the data is stable. Data should be held for 200 nsec (data hold time) after LBE goes "Low." Bits B1-B8 are transferred to the high-byte input register when HBE is a logic "1." The timing requirements are the same as those for LBE. Data are transferred from the two input registers to the holding register when LDC (load converter) is at logic "1." If LDC is at logic "0," the contents of the holding register are latched and remain at their previous values unaffected by changes at the data inputs or input registers.

Note that LBE, HBE and LDC are level-actuated functions.

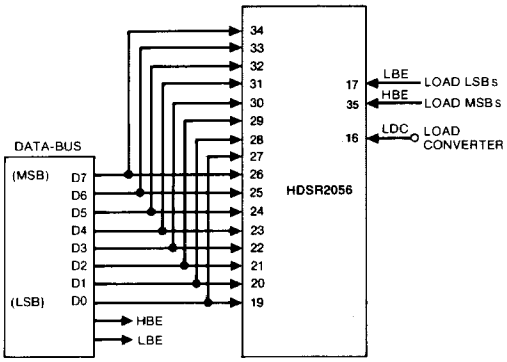


FIGURE 9 Digital Connections for Two-Byte Loading

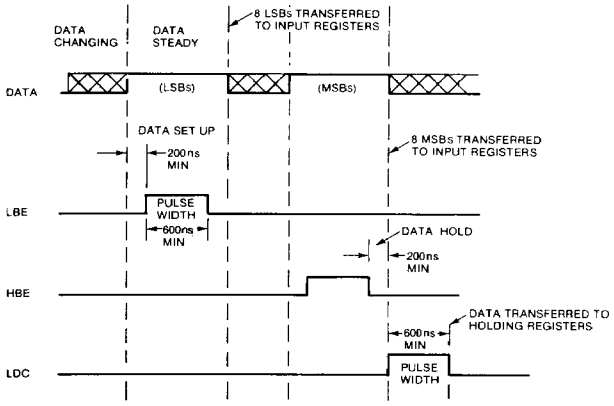


FIGURE 10 Two-Byte Loading

Single Byte Loading

Single 16-bit byte loading is illustrated in figure 11. As shown in the timing diagram (figure 12), 200 nsec after the data is stable, the input angular information is transferred to the holding register when LDC is at a logic "1." LDC is a level-actuated function and must remain high for the times specified in the timing diagram.

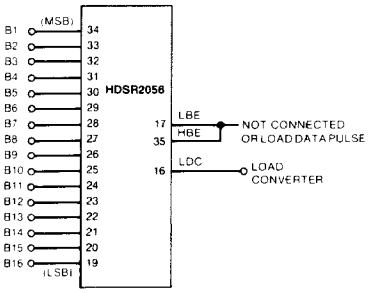


FIGURE 11 Digital Connections for One Byte (16 bits) Loading

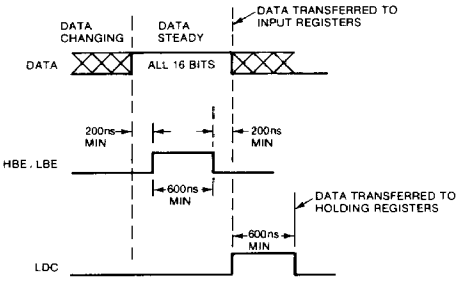


FIGURE 12 Single-Byte Loading

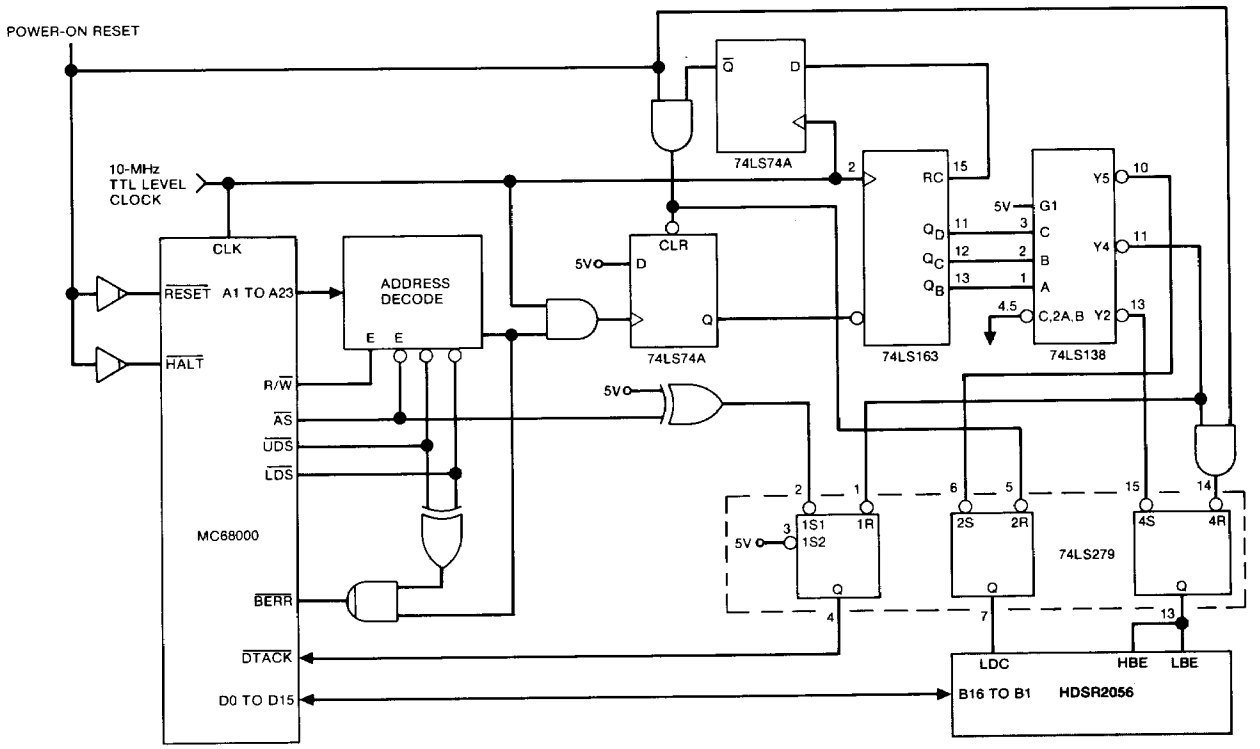


FIGURE 13 Interfacing Digital-To-Synchro/Resolver Converter With 16-Bit Microprocessor.

The interface between a digital-to resolver converter and an 8-bit microprocessor is described in the Natel data sheet for HDSC2016. Figure 13 shows the interface for a digital-to-synchro/resolver converter with a 16-bit microprocessor. Interface timing is shown in figure 14. To simplify the interface, a counter driven controller sequences the converter's control lines. Whenever the microprocessor performs a 16-bit word write, the 74LS163 counter is enabled. Outputs of the counter drive a 74LS138, which generates the strobes to sequence HBE/LBE, $\overline{\text{DTACK}}$ and LDC. If the microprocessor attempts to do a byte write (only one data strobe active), then a bus error ($\overline{\text{BERR}}$) is generated. $\overline{\text{BERR}}$ terminates the bus cycle and automatically generates an exception call to the operating system. To move a 16-bit word from a memory location or microprocessor register, the instruction MOVE, W EA, HDSR2056 could be used.

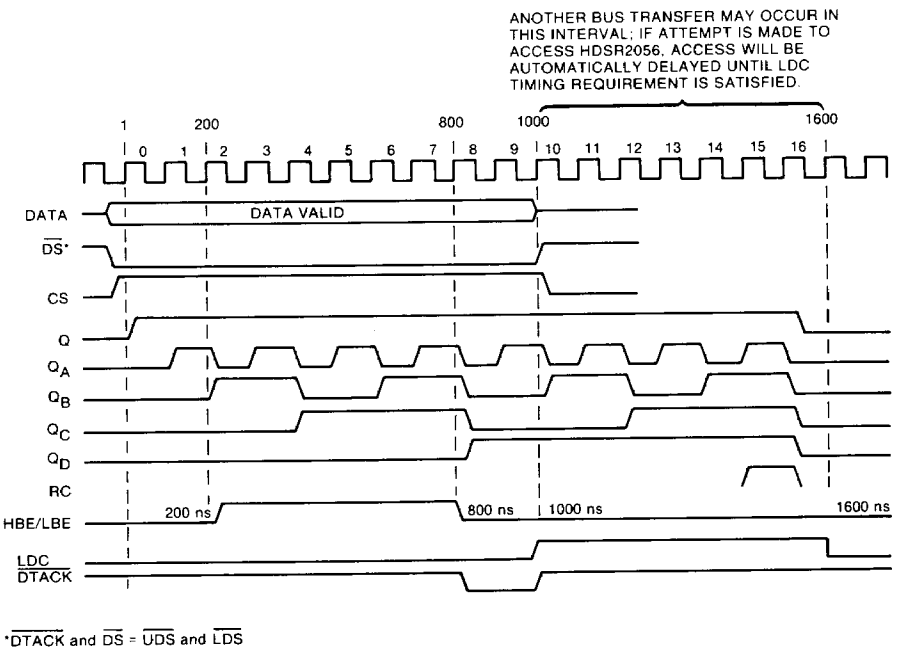
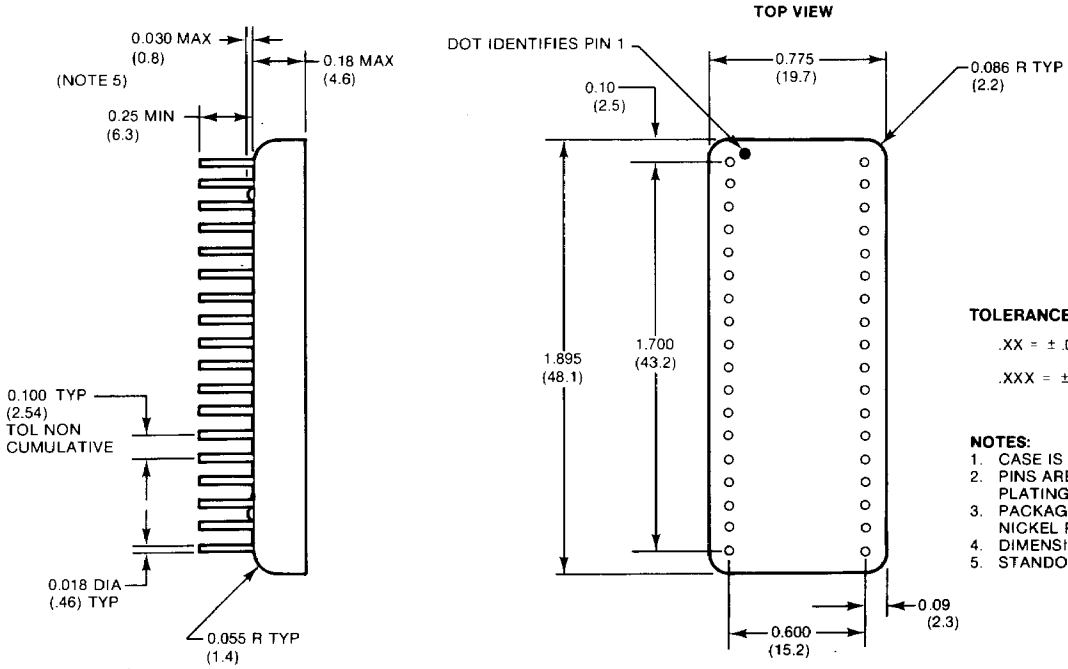


FIGURE 14 16-Bit Microprocessor Interface Timing



TOLERANCES:

.XX = ± .01 (±.25)

.XXX = ± .005 (±.13)

NOTES:
1. CASE IS ELECTRICALLY FLOATING
2. PINS ARE KOVAR WITH GOLD PLATING: (50μINCH MIN).
3. PACKAGE IS KOVAR WITH ELECTROLESS NICKEL PLATING.
4. DIMENSIONS SHOWN IN INCHES AND (MM).
5. STANDOFFS (3) CERAMIC OR GLASS

MECHANICAL OUTLINE (36 PIN DOUBLE DIP)

Ordering Information

HDSR2056 — T F A

Temperature Range

1 = 0°C to+70°C
2 = −25°C to+85°C
3 = −55°C to+125°C

Accuracy

S = ±4 arc-minutes
H = ±2 arc-minutes
V = ±1 arc-minute

Frequency Range

4 = dc to 1000 Hz
5 = dc to 5 kHz

As a standard practice, all converters are built in accordance with the requirements of MIL-STD-883B, including 168 hours of active burn-in.

Other products available from NATEL

- Hybrid (36-pin DDIP size) Synchro (Resolver)-to-Digital converters with 10- to 16-bit resolutions (1000 series)
- Second generation Four Quadrant Multiplying Sin/Cos DAC (HDSC2026)
- Low cost Digital to Sin/Cos converter in a ceramic package (HDSC2306)
- 2-channel Digital-to-Sin/Cos converter in a single 36-pin hybrid (HDSC2036)
- 2VA output, Digital to Resolver Converter in a 32-pin package (HDR2116)
- Resolver Control Differential Transmitter in a single 36-pin package (HCDX3106)
- 22-bit Binary-to-BCD and BCD-to-Binary converters (SBD227 and SDB724)

A wide range of applications assistance is available from Natel. Application Notes can be requested when available . . . and Natel's applications engineers are at your disposal for specific problems.

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