Preliminary

Am7985A

FDDI ENDEC Data Separator (EDS)

Advanced Micro Devices

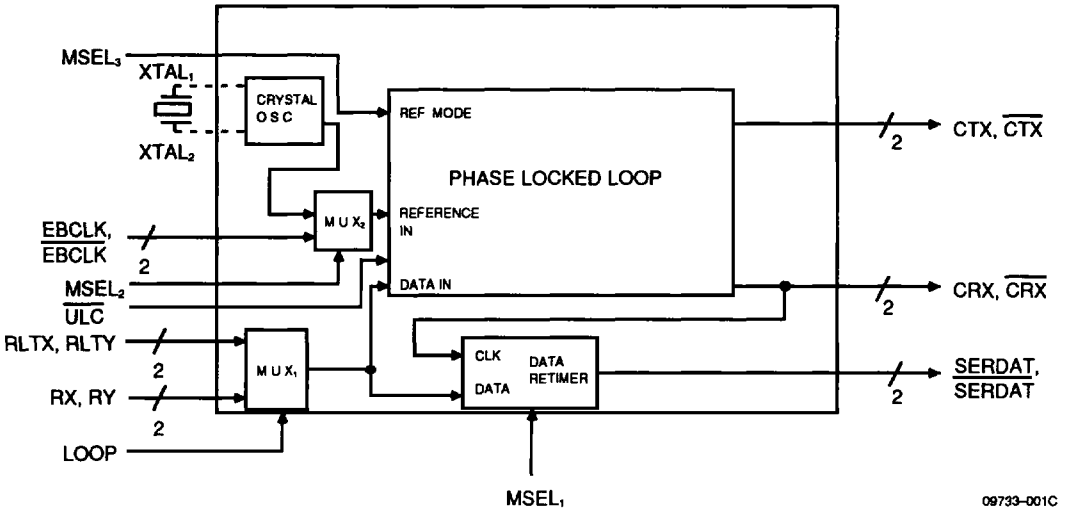
DISTINCTIVE CHARACTERISTICS

- 100 Mbps, 125 MBaud serial input
- Clock recovery
- Meets ANSI X3T9.5 Jitter Requirements
- Selectable loopback modes
- Single +5-V supply

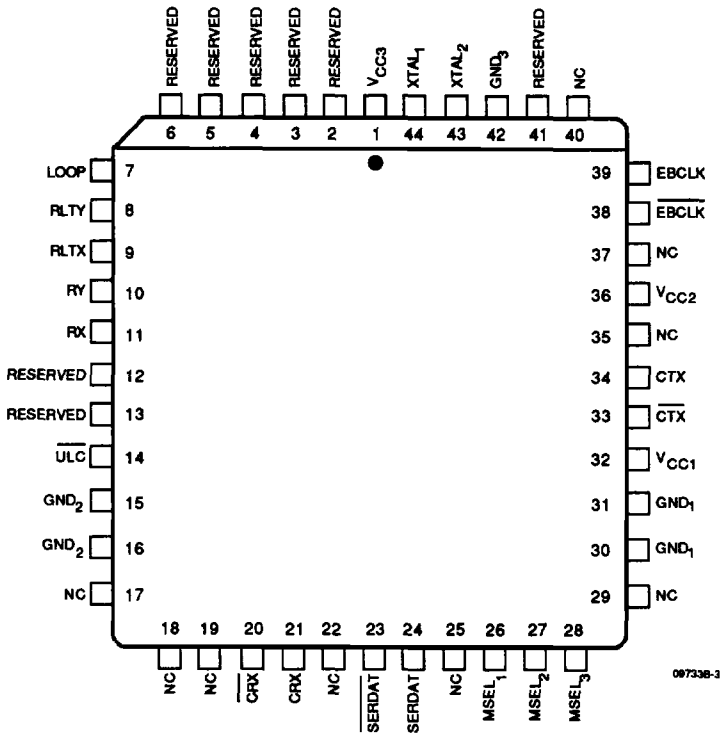
GENERAL DESCRIPTION

The Am7985A ENDEC Data Separator (EDS) recovers clock and data from an FDDI bit stream. Running from a single +5-V supply, this device needs only a clock source (generally provided by an Am7984A ENDEC) to fulfill its role in the AMD SUPERNET chip set.

BLOCK DIAGRAM

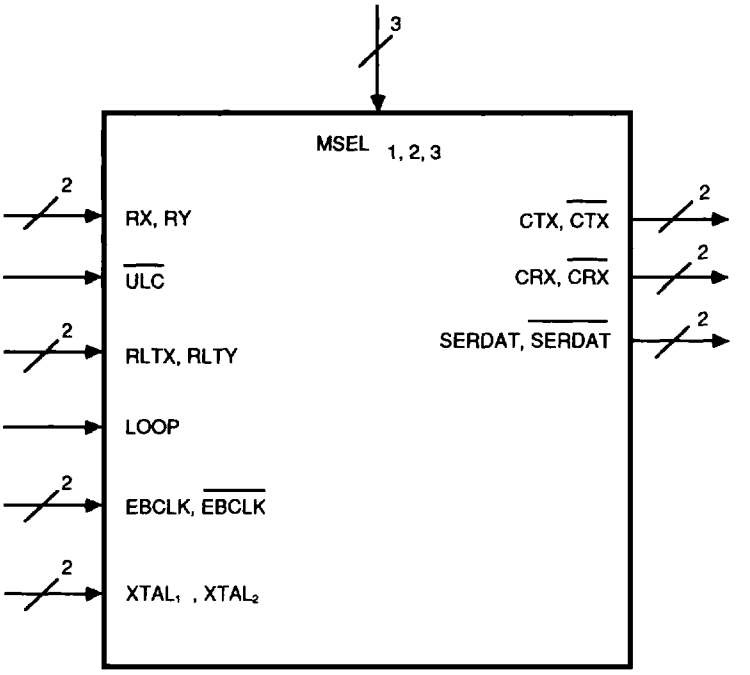


CONNECTION DIAGRAM
PL044 (Top View)



09733-002C

LOGIC SYMBOL



V_{CC} = Power (3)
GND = Ground (3)

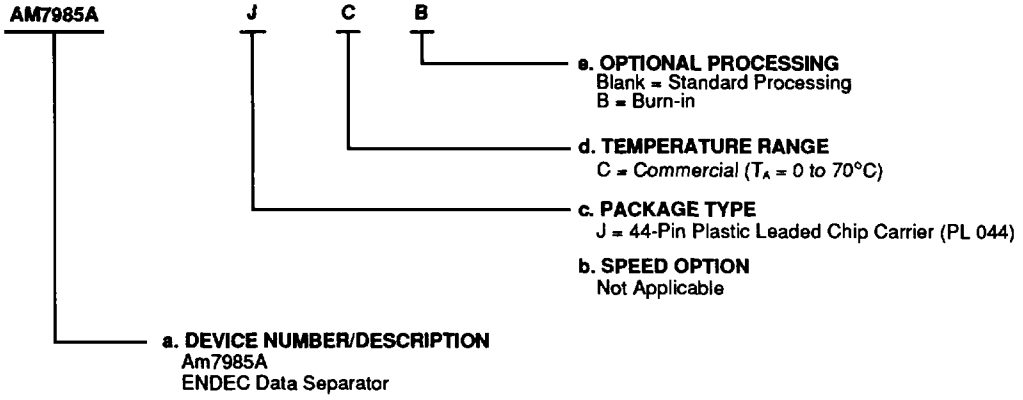
09733-003C

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM7985A	JC, JCB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.