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SSI 33P3733/34
8-26.5 Mbit/s Read Channel

Preliminary Data

December 1993

DESCRIPTION

The SSI 33P3733/34 device is a high performance BiCMOS single chip read channel IC that contains all the functions needed to implement a complete zoned recording read channel for magneto-optical (MO) drive systems. Functional blocks include the pulse detector, programmable filter, time base generator, and data synchronizer. MO data rates from 8 to 26.5 Mbit/s for (1,7) code, 6 to 20 Mbit/s for (2,7) code can be programmed using an internal DAC whose reference current is set by a single external resistor.

Programmable functions of the SSI 33P3733/34 device are controlled through a bi-directional serial port and banks of internal registers. This allows zoned recording applications to be supported without changing external component values from zone to zone.

The SSI 33P3733/34 utilizes an advanced BiCMOS process technology along with advanced circuit design techniques which result in a high performance device with low power consumption.

FEATURES

- **Programmable MO data rate of 8 to 26.5 Mbit/s for (1,7) code, 6 to 20 Mbit/s for (2,7) code, internal DAC controlled**
- **Complete zoned recording application support**
- **Low-power operation (375 mW typical @ 5V)**
- **Bi-directional serial port for register access**
- **Register programmable power management (Sleep mode <5 mW)**
- **Power supply range (4.5 to 5.5 volts)**
- **Small footprint 64-lead TQFP package**

PULSE DETECTOR

- **Fast Attack/Decay modes for rapid AGC recovery**
- **Dual rate charge pump for fast transient recovery**
- **Low Drift AGC hold circuitry**
- **Temperature compensated, exponential control AGC**
- **Wide bandwidth, high precision full-wave rectifier**
- **Programmable LEVEL pin time constant with separate MO data and emboss registers**
- **Separate Read and emboss AGC levels (4-bit DAC)**
- **Dual mode pulse qualification circuitry (user selectable)**
- **Internal fast decay timing**
- **External $\overline{\text{LOW\_Z}}$ control pin**
- **0.5 ns max. pulse pairing with sine wave input**

PROGRAMMABLE FILTER

- **Programmable cutoff frequency of 4 to 12 MHz**
- **Programmable boost/equalization of 0 to 13 dB**
- **Matched normal and differentiated outputs**
- **± 10 to 15% *fc* accuracy**
- **± 2% maximum group delay variation**
- **Less than 1.5% total harmonic distortion**
- **Low-Z input switch controlled by $\overline{\text{LOW\_Z}}$ pin**
- **No external filter components required**

TIME BASE GENERATOR

- **Better than 1% frequency resolution**
- **Up to 75 MHz frequency output**
- **Independent divide-by M and N registers**
- **VCO center frequency matched to data synchronizer VCO**
- **VCO (FOUT) output available in both Read and Write mode**

DATA SEPARATOR

- **Fast acquisition phase lock loop with zero phase restart technique**
- **Fully integrated data separator**
  - **No external delay lines, active devices, or active PLL components required**
- **Programmable decode window symmetry control via serial port**
  - **Window shift control ± 30% (4-bit)**
  - **Includes delayed read MO data and VCO clock monitor points**
- **Programmable write precompensation (3-bit) (33P3734)**

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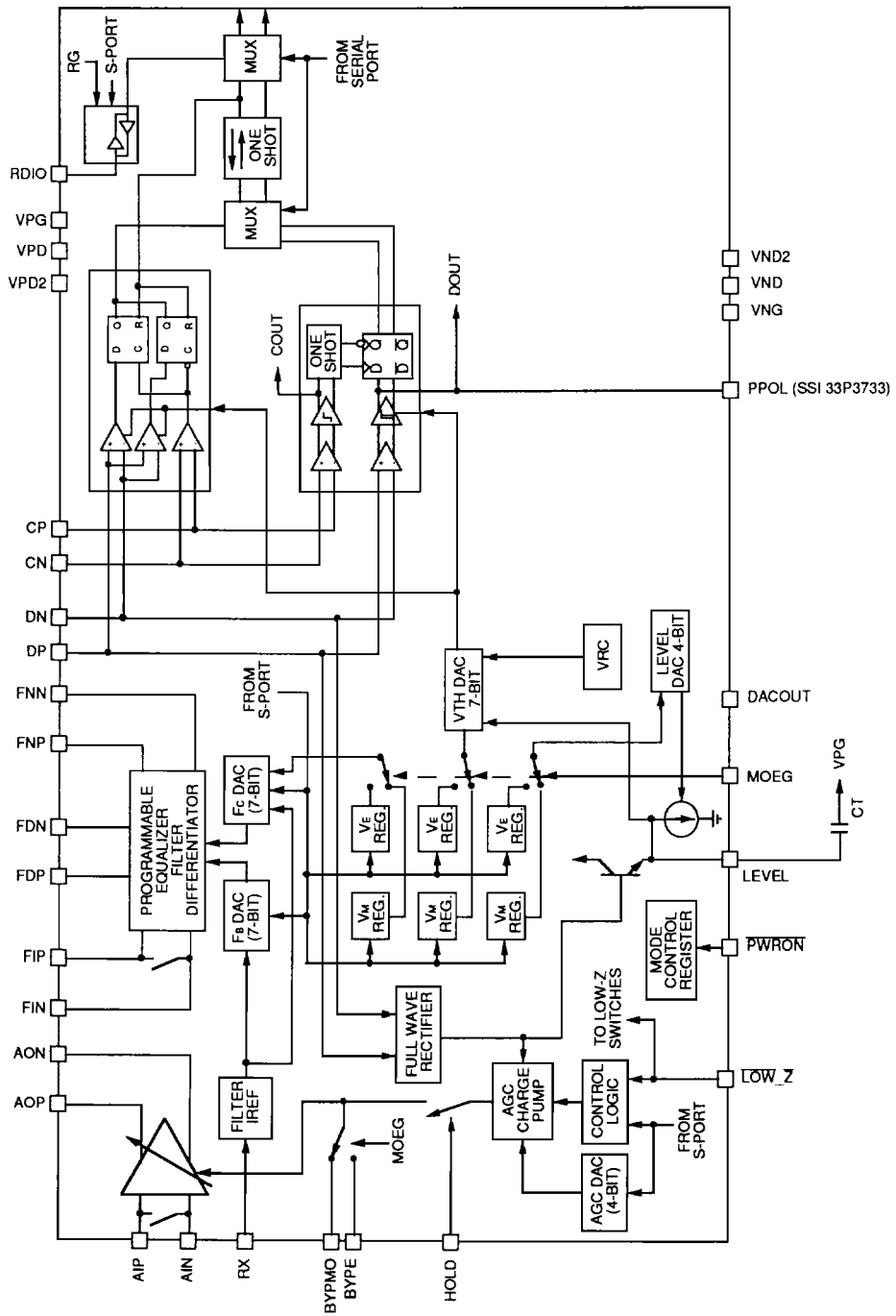

FIGURE 1A: Block Diagram, Front End

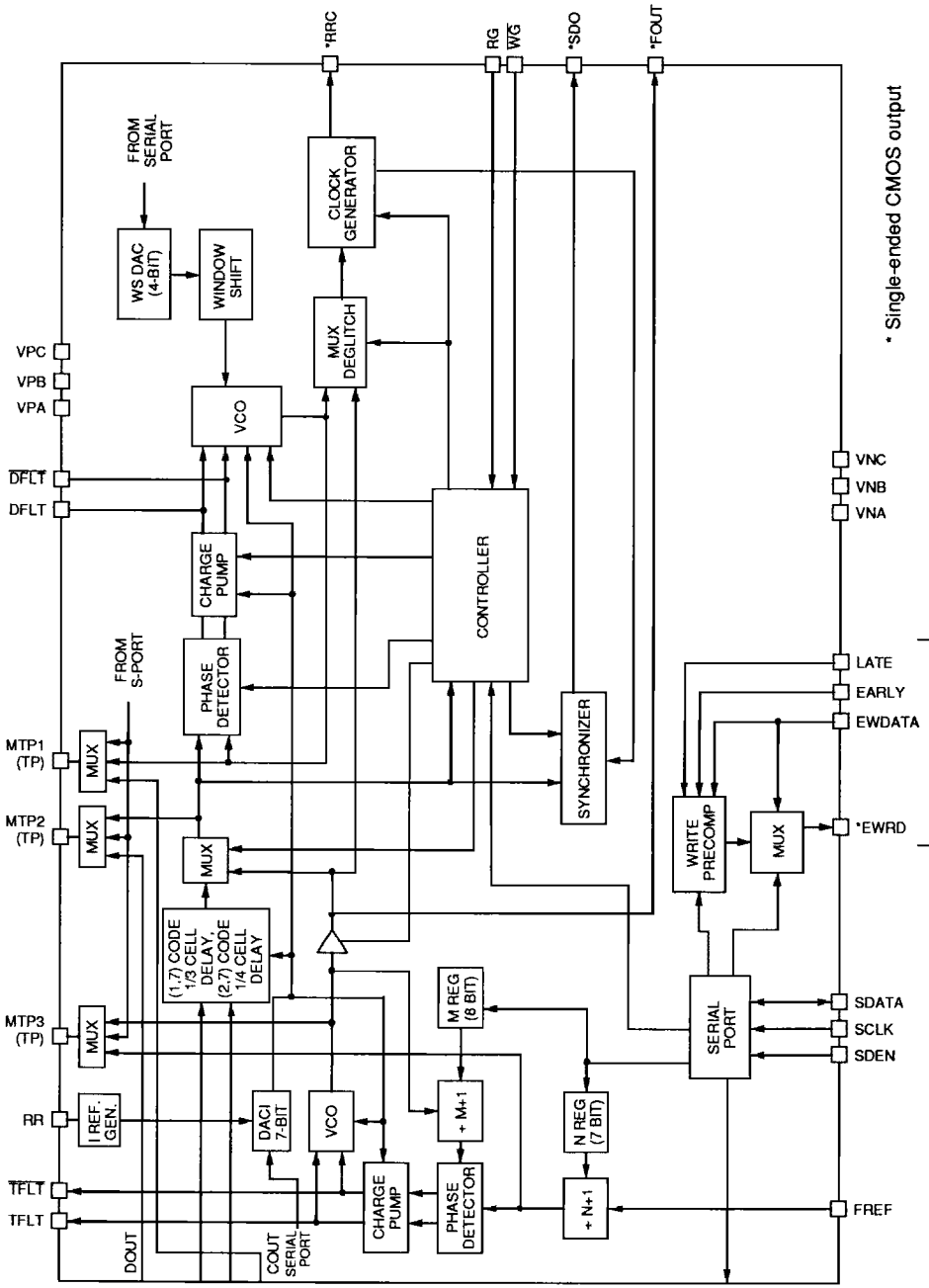

FIGURE 1B: Block Diagram, Back End

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FUNCTIONAL DESCRIPTION

The SSI 33P3733/34 implements a high performance complete read channel, including pulse detector, programmable active filter, time base generator, and data synchronizer, at MO data rates up to 26.5 Mbit/s for (1,7) code, 20 Mbit/s for (2,7) code. A circuit block diagram is shown in Figure 1.

PULSE DETECTOR CIRCUIT DESCRIPTION

The pulse detector, in conjunction with the programmable filter, provides all the MO data processing functions necessary for detection and qualification of encoded read signals. The signal processing circuits include a wide bandwidth variable gain amplifier, a precision wide bandwidth fullwave rectifier, and a dual rate charge pump. The entire signal path is fully-differential to minimize external noise pick up.

AGC CIRCUIT

The gain of the AGC amplifier is controlled by the voltage (V_{BYPx}) stored on the BYPx hold capacitor (C_{BYPx}). A dual rate charge pump drives C_{BYPx} with currents that depend on the instantaneous differential voltage at the DP/DN pins. Attack currents lower V_{BYPx} which reduces the amplifier gain, while decay currents increase V_{BYPx} which increases the amplifier gain. When the signal at DP/DN is greater than 100% of the programmed AGC level, the nominal attack current of 0.18 mA is used to reduce the amplifier gain. If the signal is greater than 125% of the programmed AGC level, a fast attack current of eight (8) times nominal is used to reduce the gain. This dual rate approach allows AGC gain to be quickly decreased when it is too high/low yet minimizes distortion when the proper AGC level has been acquired.

A constant decay current of 4 µA acts to increases the amplifier gain when the signal at DP/DN is less than the programmed AGC level. The large ratio (0.18 mA:4 µA) of the nominal attack and nominal decay currents enable the AGC loop to respond to the peak amplitudes of the incoming read signal rather than the average value. A Fast Decay Current mode is provided to allow the AGC gain to be rapidly increased, if required. In Fast Decay mode, the decay current is increased by a factor of 21.

In Read mode and Write mode, the reference voltage for the AGC charge pump is a nominal 1.0V. When MOEG is high, the reference voltage for the AGC charge pump is set by a 4-bit DAC (DACA) controlled by the serial port. The DAC output voltage is offset so that "1111" results in a 0.75V output, and "0000" results in a 1.00V output:

$$V_{AGC} = 1.00 - (DACA \times 0.01667)\ Vpp$$

where DACA is the decimal value of the DACA register

When the chip is in Power Down mode, the AGC dual rate charge pump is disabled.

Upon power up, the Low-Z/fast decay sequence should be executed to rapidly recover from any transients or drift which may have occurred on the BYPx hold capacitors.

BYPMO AND BYPE CONTROL VOLTAGE

The BYPMO capacitor voltage will be held constant (subject to leakage currents) during Sleep mode, Emboss mode (MOEG = high), Write mode, or when the HOLD signal is high. Upon the transition of $\overline{PWRON}$ from high to low, there is a 1 µs delay inserted before the AGC charge pump is allowed to drive the BYPMO capacitor. When MOEG is high, the charge pump drives the BYPE capacitor. When MOEG is low, the BYPE capacitor voltage will be held constant (subject to leakage currents).

AGC MODE CONTROL

When write gate ($\overline{WG}$) is driven low, the dual rate charge pump is disabled causing the AGC amplifier gain to be held constant. When the WG pin transitions from low to high, the LOW_Z mode can be entered using the $\overline{LOW\_Z}$ control pin. When this pin is brought low, the input impedance at both the AGC amplifier and the programmable filter are reduced to allow for quick recovery of the AC coupling capacitors. When the $\overline{LOW\_Z}$ pin goes high, the Fast Decay mode is triggered allowing rapid acquisition of the proper AGC level. The duration of the Fast Decay mode is internally set at a nominal 1 µs. Fast Decay mode is also triggered by a transition of the MO/emboss gate (MOEG) pin in either direction. When the pulse detector is powered-down, V_{BYPx} will be held constant subject to leakage currents only.

External control for enabling the dual rate charge pump is also provided. Driving the HOLD pin high forces the dual rate charge pump output current to zero. In this mode, V_{BYPx} will be held constant subject to leakage currents only.

RDIO OUTPUT PIN

A CMOS compatible, 10 ns wide (min), Raw Data Output (RDIO) signal is provided. This pin will be held low when either RG is high or WG is low to reduce noise and accompanying jitter during Read or Write modes. Its rising edge indicates the presence of a valid MO data pulse.

QUALIFIER SELECTION

The 33P3733/34 provides both hysteresis and dual comparator pulse qualification circuits that may be independently selected for Read mode and Embossed mode operation. For Read mode operation the pulse qualifier method is selected by setting the MSB in the MO data threshold control register (MODTCR). The lower 7 bits of the MODTCR also set the hysteresis level of the comparators for Read mode. For Emboss mode operation the pulse qualifier method is selected by setting the MSB in the emboss threshold control register (ETCR). The lower 7 bits of the ETCR set the hysteresis level of the comparators for Emboss mode.

DUAL COMPARATOR QUALIFICATION

When in Dual Comparator mode, independent positive and negative threshold qualification comparators are used to suppress the error propagation of a positive and negative threshold hysteresis comparator. However a slight amount of hysteresis is included to increase the comparator output time when a signal that just exceeds the threshold level is detected. This eases the timing with respect to the zero crossing clock comparator. A differential comparator with programmable hysteresis threshold allows differential signal qualification for noise rejection. The floating hysteresis threshold, VTH, is driven by a multiplying DAC which is driven by LEVEL and referenced to VRC. Hysteresis thresholds from 10 to 80% may be set with a resolution of 1%. The internal current sink LEVEL DAC (DACL) and external capacitor CT set the hysteresis threshold time constant. DACL is switched between two 4-bit registers by MO/emboss gate (MOEG) to determine the sink current magnitude in MO Data mode and Emboss mode. In MO Data mode, the four LSBs of the Hysteresis Decay Register (HDR) determine the value of the pull-down current. In Emboss mode the four MSBs are selected. The LSB value of DACL is 3.125 μA, and DACL is offset by 1 LSB such that "0000" corresponds to 3.125 μA, and "1111" results in 50 μA. A qualified signal zero crossing at the CP-CN inputs triggers the output one shot. Dual comparator timing is shown in Figure 2A.

HYSTERESIS COMPARATOR QUALIFICATION

When the Hysteresis Qualification mode is selected, the same threshold qualification comparators and clock comparators are used to implement a polarity checking rule. In this mode, a positive peak that clears the established threshold level will set the hysteresis comparator and trigger the bidirectional one-shot that creates the read MO data pulses. In order to get another pulse clocked out, a peak of the opposite polarity must clear the negative threshold level to reset the hysteresis comparator and trigger the bidirectional one-shot. Hysteresis comparator timing is shown in Figure 2B.

PROGRAMMABLE FILTER CIRCUIT DESCRIPTION

The SSI 33P3733/34 programmable filter consists of an electronically controlled low-pass filter with a separate differentiated low-pass output. A seven-pole, low-pass filter is provided along with a single-pole, single-zero differentiator. Both outputs have matched delays. The delay matching is unaffected by any amount of programmed equalization or bandwidth. Programmable bandwidth and boost/equalization is provided by internal 7-bit control DACs. The programmable characteristics are automatically switched during Emboss mode to improve signal to noise ratio. Differentiation pulse slimming equalization is accomplished by a two-pole, low-pass with a two-pole, high-pass feed forward section to provide complimentary real axis zeros. A variable attenuator is used to program the zero locations.

The filter implements a 0.05 degree equiripple linear phase response. The normalized transfer functions (i.e., $Wc = 2\pi fc = 1$) are:

$$Vnorm/Vi = [(-Ks2 + 17.98016)/D(s)] \times A_N$$

and

$$Vdiff/Vi = (Vnorm/Vi) \times (s/0.86133) \times A_D$$

where D (s)=

$$(S^2 + 1.68495s + 1.31703)(S^2 + 1.54203s + 2.95139)(S^2 + 1.14558s + 5.37034)(s + 0.86133),$$

A_N and A_D are adjusted for a gain of 2 at $fs = (2/3)fc$.

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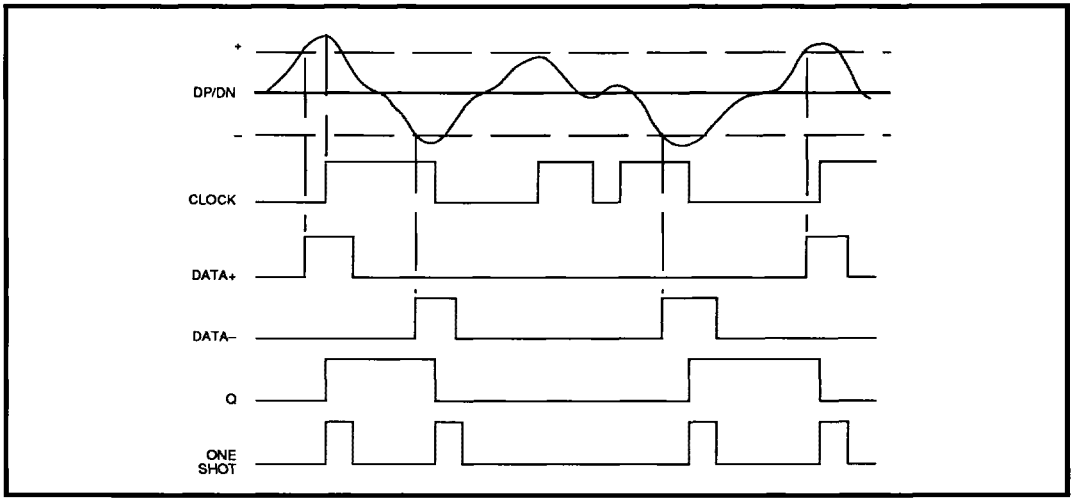

FIGURE 2A: Dual Comparator Timing Diagram

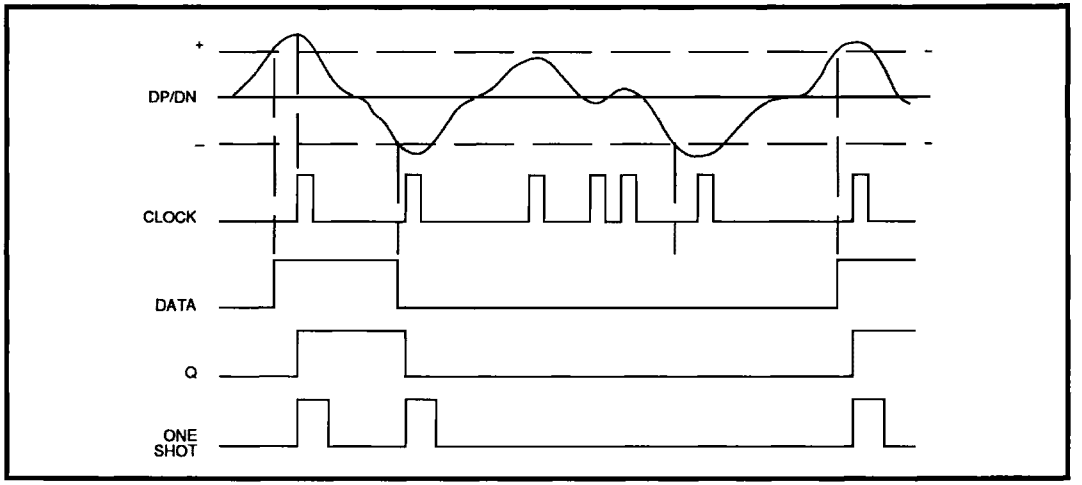

FIGURE 2B: Hysteresis Comparator Timing Diagram

FUNCTIONAL DESCRIPTION (continued)

FILTER OPERATION

AC coupled differential signals from the AGC are applied to the FIP/FIN inputs of the filter. To improve settling time of the coupling capacitors, the FIP/FIN inputs are placed into a Low-Z state when the $\overline{LOW\_Z}$ pin is brought low. The programmable bandwidth and boost/equalization features are controlled by internal DACs and the registers programmed through the serial port. The current reference for both DACs is set using a single 12.1 kΩ external resistor connected from pin RX to ground. The voltage at pin RX is proportional to absolute temperature (PTAT), hence the current for the DACs is a PTAT reference current.

BANDWIDTH CONTROL

The programmable bandwidth is set by the filter cutoff DAC. This DAC has two separate 7-bit registers that can program the DAC value as follows:

fc = 0.09449 x DACF (MHz)
where DACF = MODMCR or EMCR value

In the MO Data mode, the MO Data Mode Cutoff Register (MODMCR) is used to determine the filter's 3 dB cutoff frequency. In the Emboss mode, the Emboss Mode Cutoff Register (EMCR) is used. Switching of the registers is controlled by the MO/emboss gate (MOEG) pin. The filter cutoff set by the internal DAC is the unboosted 3 dB frequency. When boost/equalization is added, the actual 3 dB point will move out. Table 1 provides information on boost verses 3 dB frequency.

TABLE 1: 3 dB cutoff frequency versus boost magnitude

BOOST (dB)	fc (3 dB)	BOOST (dB)	fc (3 dB)
0	1.00	7	2.42
1	1.21	8	2.51
2	1.50	9	2.59
3	1.80	10	2.66
4	2.04	11	2.73
5	2.20	12	2.80
6	2.32	13	2.86

BOOST/EQUALIZATION CONTROL

The programmable equalization is also controlled by an internal DAC. The 7-bit Filter Boost Control Register (FBCR) determines the amount of equalization that will be added to the 3 dB cutoff frequency, as follows:

Boost = 20 log [(0.0273 x FBCR) + 1] (dB)

For example, with the DAC set for maximum output (FBCR = 7 fH or 127) there will be 13 dB of boost added at the 3 dB frequency. This will result in +10 dB of signal boost above the 0 dB baseline. When MOEG is active the boost can be disabled by setting bit 7 in Control A register (CAR). When bit 7 is "0" and MOEG is active the boost will automatically be set to 0 dB. If bit 7 is "1" the boost will remain at its programmed value regardless of the state of MOEG.

TIME BASE GENERATOR CIRCUIT DESCRIPTION

The time base generator, which is a PLL based circuit, provides a programmable frequency reference for constant density recording applications. The frequency can be programmed with an accuracy better than 1%. An external passive loop filter is required to control the PLL locking characteristics. The filter is fully-differential and balanced in order to suppress common mode noise generated, for example, from the data synchronizer's PLL.

In Read, Write and Idle modes, the time base generator is programmed to provide a stable reference frequency for the data synchronizer. In Read mode the internal reference clock is disabled after the data synchronizer has achieved lock and switched over to read MO data as the source for the RRC. This minimizes jitter in the data synchronizer PLL. The reference frequency is programmed using the M and N registers of the time base generator via the serial port, and is related to the external reference clock input, FREF, as follows:

Reference Frequency = ((M+1)/(N+1))FREF

TIME BASE GENERATOR CIRCUIT DESCRIPTION (continued)

The VCO center frequency and the phase detector gain of the time base generator are controlled by an internal DAC addressed through the MO data recovery control register (MODRCR). This DAC also sets the 1/3 cell delay for (1,7) code or 1/4 cell delay for (2,7) code, VCO center frequency, and phase detector gain for the data synchronizer circuitry. When changing frequencies, the M and N registers must be loaded first, followed by the MODRCR register. A frequency change is initiated only when the MODRCR register has been changed.

$$Fvco = [12.5/(RR + 0.4)] \times [(0.622 \times IDAC) + 4.27] \text{ MHz};$$
for $Fvco < 24$ MHz

$$Fvco = [12.5/(RR + 0.4)] \times [(0.7 \times IDAC) + 1.4] \text{ MHz}$$

where IDAC is the value in the MODRCR and RR is the value (kΩ) of the external RR resistor.

DATA SYNCHRONIZER CIRCUIT DESCRIPTION

In the Read mode, the data synchronizer performs sync field search and data synchronization. In the Write mode, the circuit provides write precompensation. Data rate is established by the time base generator and the internal reference DACI controlled by the MODRCR. The DAC generates a reference current which sets the VCO center frequency, the phase detector gain, and the 1/3 or 1/4 cell delay.

PHASE LOCKED LOOP

The circuit employs a dual mode phase detector; harmonic in the Read mode and non-harmonic in the Write and Idle modes. In the Read mode the harmonic phase detector updates the PLL with each occurrence of a $\overline{DRD}$ pulse. In the Write and Idle modes the non-harmonic phase detector is continuously enabled, thus maintaining both phase and frequency lock onto the reference frequency of the internal time base generator. By acquiring both phase and frequency lock to the input reference frequency and utilizing a zero phase restart technique, the VCO transient is minimized and false lock to DLYD DATA is eliminated. The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error.

The data synchronizer also requires an external passive loop filter to control its PLL locking characteristics. The filter is again fully-differential and balanced in order to suppress common mode noise which may be generated from the time base generator's PLL.

MODE CONTROL

The read gate (RG) and write gate (WG) inputs control the Device Operating mode. RG is an asynchronous input and may be initiated or terminated at any position on the disk. WG is also an asynchronous input, but should not be terminated prior to the last output write MO data pulse.

READ MODE

The data synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the decode window. Read gate (RG) initiates the PLL locking sequence and selects the PLL reference input; a high level (Read mode) selects the internal RD input and a low level selects the reference clock. In the Read mode the falling edge of $\overline{DRD}$ enables the phase detector while the rising edge is phase compared to the rising edge of the VCO reference (VCOR). $\overline{DRD}$ is a 1/3 (for (1,7) code or 1/4 for (2,7) code) cell wide (TVCO) pulse whose leading edge is defined by the falling edge of RD. A decode window is developed from the VCOR clock.

PREAMBLE SEARCH

When RG is asserted, an internal counter is triggered to count positive transitions of the incoming read MO data, RD. Once the counter reaches a count of 3, the internal read gate is enabled. This switches the phase detector reference from the internal time base to the delayed read data ($\overline{DRD}$) signal. At the same time an internal zero phase restart signal restarts the VCO in phase with the $\overline{DRD}$. This prepares the VCO to be synchronized to MO data when the bit sync circuitry is enabled after VCO lock is established.

VCO LOCK AND BIT SYNC ENABLE

One of two VCO locking modes will be entered depending on the state of the gain shift (GS) bit, or bit 1, in the Control B register. If GS = "1", the phase detector will enter a gain shift mode of operation. The phase detector starts out in a high gain mode of operation to support fast phase acquisition. After an internal counter counts the first 11 transitions of the internal $\overline{DRD}$ signal, the gain is reduced by a factor of 3. This reduces the bandwidth and dampening factor of the loop by $\sqrt{3}$ which provides improved jitter performance in the MO data follow mode. The counter continues to count the next 5 $\overline{DRD}$ transitions (a total of 19 pulses from assertion of RG) and then asserts an internal VCO lock signal.

When the VCO lock signal is asserted, the internal RRC source is also switched from the time base generator to the VCO clock signal that is phase locked to $\overline{DRD}$. During the internal RRC switching period the external RRC signal may be held for a maximum of 2 VCO clock periods, however no short duration glitches will occur.

When the GS bit is set to "0" the phase detector gain shift function is disabled. The VCO lock sequence is identical to that of the gain shift mode explained above, except that no gain shift is made after the first 11 transitions.

WINDOW SHIFT

Shifting the phase of the VCO clock effectively shifts the relative position of the $\overline{DRD}$ pulse within the decode window. Decode window control is provided via the WS control bits of the Window Shift Control Register (WSCR). Further description of the WSCR is provided in the window shift control section.

NON-READ MODE

In the Non-Read modes, the PLL is locked to the reference clock. This forces the VCO to run at a frequency which is very close to that required for tracking actual MO data. When the reference input to the PLL is switched, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse. By minimizing the phase alignment error in this manner, the acquisition time is substantially reduced.

WRITE MODE (SSI 33P3734)

Write mode is entered by asserting the write gate ($\overline{WG}$) while the RG is held low. During Write mode the VCO and the RRC are referenced to the internal time base generator signal.

DIRECT WRITE FUNCTION

The SSI 33P3734 includes a Direct Write (DW) function that allows the EWDATA MO data to bypass the write precomp circuitry. When the D3 bit of the WPR is set to zero, the MO data applied to EWDATA will bypass the write precomp and directly control the EWRD output buffer. This allows the user to perform DC erase and media tests.

OPERATING MODES AND CONTROL

The SSI 33P3733/34 has several operating modes that support Read, Write, Emboss, and power management functions. Mode selection is accomplished by controlling the read gate (RG), write gate ($\overline{WG}$), MO/emboss gate (MOEG), and $\overline{PWRON}$ pins. Additional modes are also controlled by programming the Power Down Control Register (PDCR), the Control A register (CAR), and the Control B register (CBR) via the serial port.

EXTERNAL MODE CONTROL

All operating modes of the device are controlled by driving the read gate (RG), write gate ($\overline{WG}$), MO/emboss gate (MOEG), and $\overline{PWRON}$ pins with TTL compatible signals. For normal operation the $\overline{PWRON}$ pin is driven low. During normal operation the SSI 33P3733/34 is controlled by the read gate (RG), write gate ($\overline{WG}$), and MO/emboss gate (MOEG) pins. When RG is high and $\overline{WG}$ is high the device is in Read mode. When $\overline{WG}$ is low and RG is low the device is in Write mode. If the RG is low and $\overline{WG}$ is high the device will be in Idle mode. During the Idle mode, the MOEG pin can be activated to enable the Emboss mode of operation.

FUNCTIONAL DESCRIPTION (continued)

POWER DOWN CONTROL

For power management, the $\overline{\text{PWRON}}$ pin can be used in conjunction with the Power Down Control Register (PDCR) to set the operating mode of the device. The PDCR provides a control bit for each of the functional blocks. When the $\overline{\text{PWRON}}$ pin is brought high ("1") the device is placed into Sleep mode (<5 mW) and all circuits are powered down except the serial port. This allows the user to program the serial port registers while still conserving power. Register information is retained during the Sleep mode so it is not necessary to reprogram the serial port registers after returning to an active mode. When the $\overline{\text{PWRON}}$ pin is driven low ("0"), the contents of the PDCR determine which blocks will be active. Register mapping for the PDCR is shown in Table 3. To improve recovery time from the Sleep mode, the $\overline{\text{LOW\_Z}}$ pin should be asserted following power down to initiate the AGC recovery sequence.

SERIAL INTERFACE OPERATION

The serial interface is a CMOS bi-directional port for reading and writing programming data from/to the internal registers of the SSI 33P3733/34. The serial port data transfer format is shown in Figure 3. For data transfers SDEN is brought high, serial data is presented at the SDATA pin, and a serial clock is applied to the SCLK pin. After the SDEN goes high, the first 16 pulses applied to the SCLK pin will shift the data presented at the SDATA pin into an internal shift register on the rising edge of each clock. An internal counter prevents more than 16 bits from being shifted into the register. The data in the shift register is latched when SDEN goes low. If less than 16 clock pulses are provided before SDEN goes low, the data transfer is aborted.

All transfers are shifted into the serial port LSB first. The first byte of the transfer is address and instruction information. The LSB of this byte is the R/W bit which determines if the transfer is a read (1) or a write (0). The remaining 7-bits determine the internal register to be accessed. Table 3 provides register mapping information. The second byte contains the programming data. In Read mode (R/W=1) the SSI 33P3733/34 will output the register contents of the selected address. In Write mode the device will load the selected register with data presented on the SDATA pin. At initial power-up, the contents of the internal registers will be in an unknown state and must be programmed prior to operation. During power down modes, the serial port remains active and register programming data is retained. Detailed timing information is provided in Figure 4.

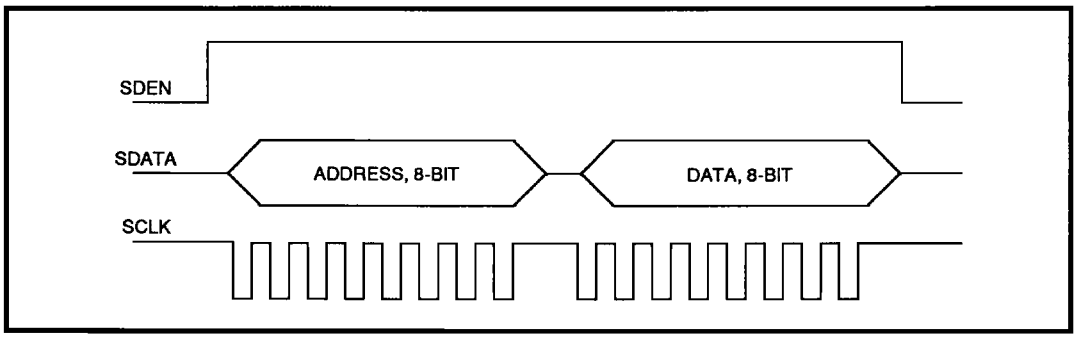

FIGURE 3: Serial Port Data Transfer Format

TABLE 2: MODE CONTROL

CONTROL LINE				DEVICE MODE	DAC CONTROL			
$\overline{PWRON}$	RG	MOEG	$\overline{WG}$		VTH	FC	BOOST	HYSTERESIS
1	X	X	X	**SLEEP MODE:** All functions are powered down. The serial port registers remain active and register programming data is saved.	off	off	off	off
0	0	0	0	**WRITE MODE:** The pulse detector is inactive. The data synchronizer VCO is locked to the internal time base generator. Write precomp circuit is clocked by internal time base. (SSI 33P3734)	MR	MR	MR	MR
0	1	0	1	**READ MODE:** The pulse detector is active. The data synchronizer begins the preamble lock sequence. RDIO is active	MR	MR	MR	MR
0	0	1	1	**EMBOSS MODE:** The pulse detector is active and the emboss control registers are enabled for the Fc DAC and the VTH DAC. The data synchronizer and time base generator can be disabled using the PDCR.	ER	ER	off	ER
0	0	0	1	**IDLE MODE:** The contents of the PDCR determine which blocks are powered-up. In normal operation with all blocks powered-up, the pulse detector is active, the data synchronizer VCO is locked to the time base generator, and the MO data control registers are used for VTH and FC.	MR	MR	MR	MR
-	-	-	-	All other states are illegal. If an illegal state is programmed, the chip function will be in an indeterminable state, but no damage will occur.	MR	MR	MR	MR

DAC CONTROL KEY: MR = MO DATA REGISTER, ER = EMBOSS RIGISTER, OFF = DISABLED

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REGISTER NAME	A6	ADDRESS					A0	R/W	D7	DATA BIT MAP							D0
POWER DOWN CONTROL	0	0	0	0	0	1	0	0	--	--	--	TBG 1=DISABLE 0=ENABLE	DATA SEP 1=DISABLE 0=ENABLE	FILTER 1=DISABLE 0=ENABLE	--	PD 1=DISABLE 0=ENABLE
MO DATA MODE CUTOFF	0	0	0	0	0	1	1	0	--	F_{CM} DAC BIT 6	F_{CM} DAC BIT 5	F_{CM} DAC BIT 4	F_{CM} DAC BIT 3	F_{CM} DAC BIT 2	F_{CM} DAC BIT 1	F_{CM} DAC BIT 0
EMBOSS MODE CUTOFF	0	0	1	0	0	1	1	0	--	F_{CE} DAC BIT 6	F_{CE} DAC BIT 5	F_{CE} DAC BIT 4	F_{CE} DAC BIT 3	F_{CE} DAC BIT 2	F_{CE} DAC BIT 1	F_{CE} DAC BIT 0
FILTER BOOST	0	0	0	1	0	1	1	0	EMBOSS BOOST 1=ENABLE 0=DISABLE	F_BDAC BIT 6	F_B DAC BIT 5	F_B DAC BIT 4	F_B DAC BIT 3	F_B DAC BIT 2	F_B DAC BIT 1	F_B DAC BIT 0
MO DATA THRESHOLD	0	0	0	1	0	1	0	0	1=DUAL 0=HYS	T_MDAC BIT 6	T_M DAC BIT 5	T_M DAC BIT 4	T_M DAC BIT 3	T_M DAC BIT 2	T_M DAC BIT 1	T_M DAC BIT 0
EMBOSS THRESHOLD	0	0	1	0	0	1	0	0	1=DUAL 0=HYS	T_EDAC BIT 6	T_E DAC BIT 5	T_E DAC BIT 4	T_E DAC BIT 3	T_E DAC BIT 2	T_E DAC BIT 1	T_E DAC BIT 0
CONTROL A	0	0	1	1	0	1	0	0	Fast Decay test mode 0=ENABLE	TMS1	TMS0	TBG 1=BYPASS 0=NORMAL	TBG TEST POINT ENABLE	PUMP DWN 1=TP ON 0=TP OFF	PUMP UP 1=TP ON 0=TP OFF	PHASE DET 1=ENABLE 0=DISABLE
CONTROL B	0	0	0	1	1	0	0	0	--	MTPE 1=ENABLE 0=DISABLE	PUMP DWN 1=TP ON 0=TP OFF	PUMP UP 1=TP ON 0=TP OFF	PHASE DET 1=ENABLE 0=DISABLE	RDIO 1 = INPUT 0 = OUTPUT	GAIN SHFT 1 = ON 0 = OFF	--
N COUNTER	0	0	0	0	1	1	0	0	--	N COUNT BIT 6	N COUNT BIT 5	N COUNT BIT 4	N COUNT BIT 3	N COUNT BIT 2	N COUNT BIT 1	N COUNT BIT 0
M COUNTER	0	0	0	1	1	1	0	0	M COUNT BIT 7	M COUNT BIT 6	M COUNT BIT 5	M COUNT BIT 4	M COUNT BIT 3	M COUNT BIT 2	M COUNT BIT 1	M COUNT BIT 0
DATA RECOVERY	0	0	0	0	1	0	0	0	--	DAC I BIT 6	DAC I BIT 5	DAC I BIT 4	DAC I BIT 3	DAC I BIT 2	DAC I BIT 1	DAC I BIT 0
WINDOW SHIFT	0	0	0	0	1	0	1	0	TDAC 1	TDAC 0	WIN SHFT 1=ENABLE 0=DISABLE	WS DIR 1=LATE 0=EARLY	$\overline{WS3}$	$\overline{WS2}$	$\overline{WS1}$	$\overline{WS0}$
WRITE PRECOMP	0	0	0	1	1	0	1	0	--	$\overline{WL2}$	$\overline{WL1}$	$\overline{WL0}$	WR PRCMP 1=ENABLE 0=DISABLE	$\overline{WE2}$	$\overline{WE1}$	$\overline{WE0}$
AGC LEVEL	0	1	0	0	0	1	0	0	--	--	--	--	AGC DAC BIT 3	AGC DAC BIT 2	AGC DAC BIT 1	AGC DAC BIT 0
HYSTERESIS DECAY	0	1	0	1	0	1	0	0	EMBOSS BIT 3	EMBOSS BIT 2	EMBOSS BIT 1	EMBOSS BIT 0	DATA BIT 3	DATA BIT 2	DATA BIT 1	DATA BIT 0

TABLE 3: Serial Port Register Mapping

FUNCTIONAL DESCRIPTION (continued)

CONTROL REGISTERS

Control registers CAR and CBR allow the user to configure the SSI 33P3733/34 test points for evaluation of different internal signals and also control other device functions. CAR controls functions of the pulse detector, filter, and time base generator. CBR controls test points and functions of the data separator. The bits of the CA and CB registers are defined as follows:

CONTROL REGISTER CA

BIT	NAME	FUNCTION
0	EPDT	Enable Phase Detector (Time Base Generator)
1	UT	Pump Up (TFLTR sources current, $\overline{\text{TFLTR}}$ sinks Current)
2	DT	Pump Down (TFLTR sinks current, $\overline{\text{TFLTR}}$ sources Current)
3	ET	Enable Time Base Generator Test Point Output
4	BYPT	Bypass Time Base Generator Circuit Function
5	TMS0	Control bit for selecting test point source (see Table 4)
6	TMS1	Control bit for selecting test point source (see Table 4)
7	FDTM	Constant fast decay current test mode

CONTROL REGISTER CB

0	-	Not Used
1	GS	Enable Phase Detector Gain Switching
2	RDI	RDIO Pin Input Control
3	EPDD	Enable Phase Detector (Data Separator)
4	UD	Pump Up (DFLTR sources current, $\overline{\text{DFLTR}}$ sinks current)
5	DD	Pump Down (DFLTR sinks current, $\overline{\text{DFLTR}}$ sources current)
6	MTPE	Enable Test Points MTP1, 2, 3 (see Table 4)
7	-	Not used

PIN DESCRIPTION

POWER SUPPLY PINS

NAME	TYPE	DESCRIPTION
VPA	-	Data separator PLL analog power supply pin
VPB	-	Time base generator PLL analog power supply pin
VPC	-	Internal ECL, CMOS logic power supply pin
VPD, VPD2	-	CMOS buffer I/O digital power supply pin
VPG	-	Pulse detector, filter, analog power supply pin
VNA	-	Data separator PLL analog ground pin
VNB	-	Time base generator PLL analog ground pin
VNC	-	Internal ECL, CMOS logic ground pin
VND, VND2	-	CMOS buffer I/O digital ground pin
VNG	-	Pulse detector, filter, analog ground pin

INPUT PINS

AIP, AIN	I	AGC AMPLIFIER INPUTS: Differential AGC amplifier input pins.
DP, DN	I	ANALOG INPUTS FOR MO DATA PATH: Differential analog inputs to MO data comparators, full-wave rectifier.
CP, CN	I	ANALOG INPUTS FOR CLOCK PATH: Differential analog inputs to the clock comparator.
$\overline{\text{LOW\_Z}}$	I	LOW IMPEDANCE ENABLE: TTL compatible input pin that activates the Low-Z switches. A low level activates the switches and the falling edge of the internal LOW_Z triggers the fast decay circuit.
$\overline{\text{PWRON}}$	I	POWER ENABLE: TTL compatible power control input. A low level input enables power to circuitry according to the contents of the PDCR. A high level input shuts down all circuitry.
HOLD	I	HOLD CONTROL: TTL compatible control pin which, when pulled high, disables the AGC charge pump and holds the AGC amplifier gain at its present value.
FIP, FIN	I	FILTER SIGNAL INPUTS: The AGC output signals must be AC coupled into these pins.
FREF	I	REFERENCE FREQUENCY INPUT: Frequency reference input for the time base generator. FREF may be driven either by a direct coupled TTL signal or by an AC coupled ECL signal. Pin FREF has an internal pull down resistor.
EWDATA	I	WRITE INPUT: TTL compatible write MO data input. (SSI 33P3734)
EARLY, LATE	I	WRITE PRECOMPENSATION CONTROL: TTL compatible inputs. The EARLY and LATE signals control on-the-fly precompensation of the EWDATA. (SSI 33P3734)

INPUT PINS (continued)

NAME	TYPE	DESCRIPTION
RG	I	READ GATE: TTL compatible read gate input. A high level TTL input selects the RD input and enables the Read mode/address detect sequences. A low level selects the FREF input.
MOEG	I	MO/emboss GATE: TTL compatible MO/emboss gate input. A high level TTL input activates the Emboss mode by selecting the emboss control registers, the RTS resistor, and the BYPE capacitor.
$\overline{WG}$	I	WRITE GATE: TTL compatible write gate input. A low level TTL input enables the Write mode.

OUTPUT PINS

MTP1-3	O	MULTIPLEXED TEST POINTS: Open emitter ECL output test points. Internal test signals are routed to these test points as determined by the CAR and CBR. External resistors are required to use these pins. They should be removed during normal operation to reduce power dissipation.
SDO	O	SYNCHRONIZED READ DATA: CMOS output pin. Read MO data output when RG is high.
FDP, FDN	O	DIFFERENTIAL DIFFERENTIATED OUTPUTS: Filter differentiated outputs. These outputs are AC coupled into the CP/CN inputs.
FNP, FNN	O	DIFFERENTIAL NORMAL OUTPUTS: Filter normal low pass output signals. These outputs are AC coupled into the DP/DN inputs.
RDIO	I/O	READ MO DATA I/O: Bi-directional CMOS output / TTL compatible input pin. RDIO is an output when RG is low and the RDIO bit is low in the CBR. RDIO is an input when the RDIO bit is high in the CBR. The minimum RDIO input pulse width is TBD ns. The RG and pulse detector functions override the bit in the CBR. When RDIO is used as an input pin, 1/3 or 1/4 cell delay in the data synchronizer is made from the rising edge.
RRC	O	READ REFERENCE CLOCK: Read clock CMOS output. During a mode change, no glitches are generated and no more than one lost clock pulse will occur. When RG goes high, RRC initially remains synchronized to the reference clock. When the Sync Bits are detected, RRC is synchronized to the Read MO Data. When RG goes low, RRC is synchronized back to the reference clock.
AOP, AON	O	AGC AMPLIFIER OUTPUT: Differential AGC amplifier output pins. These outputs are AC coupled into the filter inputs (FIP/FIN).
EWRD	O	WRITE MO DATA: Encoded write MO data CMOS output. When direct write is active EWRD is directly driven by EWDATA.
FOUT	O	TIME BASE GENERATOR VCO OUTPUT: CMOS output pin. This clock signal is the data separator PLL reference. This output is independent of the RG/WG pin.
PPOL	O	PULSE POLARITY: Pulse polarity CMOS output pin. The output is high when the pulse being qualified is positive and it is low when the pulse being qualified is negative. (SSI 33P3733)

PIN DESCRIPTION (continued)

ANALOG PINS

NAME	TYPE	DESCRIPTION
BYPMO	-	The AGC Read mode integration capacitor CBYPMO, is connected between BYPMO and VPG.
BYPE	-	The AGC Emboss mode integration capacitor CBYPE, is connected between BYPE and VPG.
DACOUT	-	DAC VOLTAGE TEST POINT: This test point monitors the outputs of the internal DACs. The source DAC is selected by programming the two MSBs of the WSCR register (see Table 5).
TFLT, $\overline{\text{TFLT}}$	-	PLL LOOP FILTER: These pins are the connection points for the time base generator loop filter.
DFLT, $\overline{\text{DFLT}}$	-	PLL LOOP FILTER: These pins are the connection points for the data separator loop filter.
LEVEL	-	An NPN emitter output that provides a full-wave rectified signal from the DP, DN inputs. An external capacitor should be connected from LEVEL to VPG to set the hysteresis threshold time constant in conjunction with the internal current DAC, (DACA).
RR	-	REFERENCE RESISTOR INPUT: An external 12.1 kΩ, 1% resistor is connected from this pin to VNA to establish a precise internal reference current for the data separator and time base generator.
RX	-	REFERENCE RESISTOR INPUT: An external 12.1 kΩ, 1% resistor is connected from this pin to ground to establish a precise PTAT (proportional to absolute temperature) reference current for the filter.

SERIAL PORT PINS

SDEN	-	SERIAL DATA ENABLE: Serial enable CMOS input. A high level TTL input enables the serial port.
SDATA	-	SERIAL DATA: Serial data CMOS input. NRZ programming data for the internal registers is applied to this input.
SCLK	-	SERIAL CLOCK: Serial clock CMOS input. The clock applied to this pin is synchronized with the data applied to SDATA.

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, the recommended operating conditions are as follows: 4.5V < POSITIVE SUPPLY VOLTAGE < 5.5V, 0°C < T (ambient) < 70°C, and 25°C < T(junction) < 135°C. Currents flowing into the chip are positive. Current maximum are currents with the highest absolute value.

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATING
Storage Temperature	-65 to 150°C
Junction Operating Temperature	+135°C
Positive Supply Voltage (Vp)	-0.5 to 7V
Voltage Applied to Logic Inputs	-0.5V to Vp + 0.5V
All other Pins	-0.5V to Vp + 0.5V

POWER SUPPLY CURRENT AND POWER DISSIPATION

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
ICC (VPA,B,C,D,G)	Outputs and test point pins open, Ta = 27°C, VPn = 5V, 24 Mbit/s		75		mA
PWR Power Dissipation	Outputs and test point pins open, Ta = 27°C, VP = 5V, 24 Mbit/s		375		mW
Sleep mode Power	$\overline{\text{PWRON}}$ = 1			5	mW
Emboss mode Power	$\overline{\text{PWRON}}$ = 0 TBG Disabled Data Sep. Disabled		200		mW

DIGITAL INPUTS AND OUTPUTS

TTL COMPATIBLE INPUTS

Input low voltage	VIL		-0.3		0.8	V
Input high voltage	VIH		2		VPD + 0.3	V
Input low current	IIL	VIL = 0.4V			-100	µA
Input high current	IIH	VIH = 2.4V			50	µA

CMOS COMPATIBLE INPUTS - Schmitt trigger type (not to be left open.) Nominal 1.0V hysteresis around VPD/2.

Input low voltage		-0.3		1.5	V
Input high voltage		3.5		VPD + 0.3	V

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DIGITAL INPUTS AND OUTPUTS (continued)

CMOS COMPATIBLE OUTPUTS

Output low voltage	5V, 25°C IOL = 4.07 mA			0.5	V
Output high voltage	5V, 25°C IOH = -4.83 mA	4.5			V
Rise time	4.5V, 70°C, C = 15 pF			8	ns
Fall time	4.5V, 70°C, C = 15 pF			8	ns

PSEUDO ECL OUTPUT LEVELS (MTP1, MTP2, MTP3)
For all tests, 261Ω to VPA and 402Ω to VNA with VPA = 5.0V

Output high level		VPA -1.02			V
Output low level				VPA -1.62	V

SERIAL PORT

SCLK period	T_{CLK}		100			ns
SCLK low time	T_{CKL}		40			ns
SCLK high time	T_{CKH}		40			ns
Enable to SCLK	T_{SENS}		35			ns
SCLK to disable	T_{SENH}		35			ns
Data set-up time	T_{DS}		15			ns
Data hold time	T_{DH}		15			ns
SDATA tri-state delay	T_{SENDL}				50	ns
SDATA turnaround time	T_{TRN}		70			ns
SDEN low time	T_{SL}		200			ns

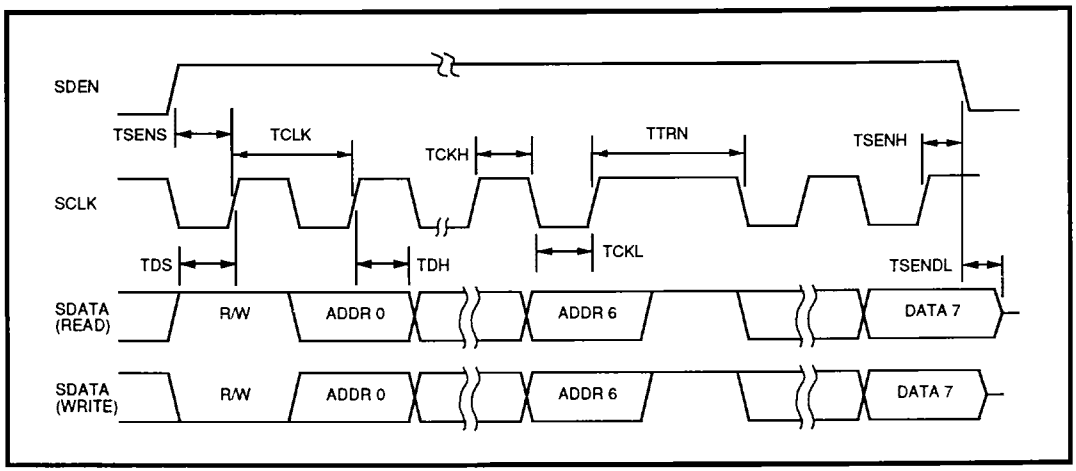

FIGURE 4: Serial Port Timing Information

ELECTRICAL SPECIFICATIONS (continued)

PULSE DETECTOR CHARACTERISTICS

AGC AMPLIFIER

Input signals are AC coupled to AIP/AIN, AOP/AON outputs are AC coupled to FIP/FIN, and FNP/FNN are AC coupled to DP/DN. 1000 pF capacitors are connected from BYPMO to VPG (C_{BYPMO}) and from BYPE to VPG (C_{BYPE}). Unless otherwise specified, outputs are measured differentially at AOP/AON, FIN = 8 MHz, and filter boost = 0 dB.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input range	Filter boost 0 to 13 dB	20		190	mVpp
DP-DN voltage	AIP - AIN = 0.1 Vpp	0.9	1	1.1	Vpp
	MOEG = high, AGC DAC = 0	0.9	1	1.1	Vpp
	MOEG = high, AGC DAC = 15	0.68	0.76	0.84	Vpp
DP-DN voltage variation	20 mV < AIP - AIN < 190 mV			8	%
Gain range		0.45		18	V/V
Gain sensitivity	BYPx voltage change		28		dB/V
AOP-AON dynamic range	THD = 1%	0.6			Vpp
Differential input impedance	$\overline{LOW\_Z}$ = high	4.7	6	8.4	kΩ
	$\overline{LOW\_Z}$ = low		350		Ω
Single-ended input impedance	$\overline{LOW\_Z}$ = high		3.3		kΩ
	$\overline{LOW\_Z}$ = low		250		Ω
Single-ended output impedance	AOP/AON to ground			120	Ω
Output offset voltage variation	Gain = 0.45 to 18			200	mV
Input noise voltage	Gain = 18, AOP - AON = 0V			20	nV/√Hz
Bandwidth	Gain = 18, CL ≤ 15 pF	35			MHz
CMRR Gain = 18, fc = 5 MHz		40			dB
PSRR Gain = 18, fc = 5 MHz		45			dB
Gain decay time	AIP - AIN = 250 to 125 mV, AOP - AON > 0.9 Final Value		36		µs
Gain attack time	AIP - AIN = 125 to 250 mV, AOP - AON < 1.1 Final Value		0.65		µs

AGC CONTROL

The input signals are AC coupled into DN/DP, C_{BYPX} = 1000 pF to VPG, MOEG = low.

DP-DN input range	For test only			1	1.5	Vpp
Decay current	Normal decay	I_D		4		µA
	Fast Decay mode	I_{DF}		21 x I_D		µA
Attack current	Normal attack	I_{CH}		0.18		mA
	Fast Attack mode	I_{CHF}		8 x I_{CH}		mA

AGC CONTROL (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
BYPMO leakage current	$\overline{WG}$ = high	-10		10	nA
Fast decay duration			1		µs
LEVEL output gain	|DP-DN| = 0.5 to 1.5V	0.60	0.65	0.70	V/Vpp
LEVEL output bandwidth	-1 dB	10			MHz
LEVEL pin pull-down current	DACL = 0000	1.56	3.125	4.69	µA
	DACL = 1111 where I_{LEVEL} = 3.125 x (1 + DACL) µA	47	50	53	µA

DATA COMPARATOR
The input signals are AC coupled into DP/DN.

DP-DN input range			1	1.5	Vpp
Differential input resistance	$\overline{LOW\_Z}$ = Off	8.0		14	kΩ
	$\overline{LOW\_Z}$ = On	0.4		1.2	kΩ
Differential input capacitance				5	pF
Threshold voltage hysteresis			10		%T
Threshold voltage gain (K_{TH}) tolerance	0.47 < |DP - DN| < 1.19 T = V_{THDAC} x 0.93/127 38 < V_{THDAC} < 127	T - 10		T + 10	%
Minimum threshold voltage	|DP - DN| < 0.16 V_{THMIN} = V_{THDAC} • 97.6%/127		V_{THMIN}		V
PPOL rise time (SSI 33P3733)	10% to 90% points, CL ≤ 15 pF			8	ns
PPOL fall time (SSI 33P3733)	90% to 10% points, CL ≤ 15 pF			8	ns

CLOCK SECTION
The input signals are AC coupled into CP/CN.

CP-CN input range				1.5	Vpp
Comparator offset voltage		-4		4	mV
Differential input resistance		8		14	kΩ
Differential input capacitance				5	pF
Pulse pairing	DP/DN = 1 Vpp sine, CP/CN = 1 Vpp - 90°sine Fsine = 8 MHz			0.5	ns
RDIO pulse width	CL ≤ 15 pF	6		15	ns
RDIO input pulse width		10			ns
RDIO rise time	10% to 90% points, CL ≤ 15 pF			8	ns
RDIO fall time	90% to 10% points, CL ≤ 15 pF			8	ns

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PULSE DETECTOR CHARACTERISTICS (continued)

PROGRAMMABLE FILTER CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Filter cutoff range	*fc* @ -3 dB point *fc* = (0.09449 MHz) x DACF, Boost = 0 dB 42 ≤ DACF ≤ 127 DACF = MODMCR	4		12	MHz
Filter cutoff accuracy	DACF = 127	-10		10	%
	DACF = 42 to DACF < 127	-15		15	%
FNP, FNN differential gain (A_N)	F = 0.67 x *fc*, boost = 0 dB	1.6	2	2.4	V/V
FDP, FDN differential gain (A_D)	F = 0.67 x *fc*, boost = 0 dB	0.8 A_N		1.2 A_N	V/V
Frequency boost @ *fc* = 12 MHz	DACS = 127		13		dB
Boost accuracy	@ 6 dB, DACS = 37	-1		+1	dB
	@ 9 dB, DACS = 67	-1.25		+1.25	dB
	@ 13 db, DACS = 127	-1.5		+1.5	dB
MO/Emboss mode group delay variation	*fc* = 4 to 12 MHz F = 0.2 *fc* to *fc*, boost = 0 and 3 dB	-2		+2	%
FNP, FNN; FDP, FDN	*fc* = 4 to 12 MHz F = *fc* to 1.75 *fc*, boost = 3 dB	-3		+3	%
Filter Output THD @ 1 Vpp	F = 0.67 *fc* *fc* = 4 to 12 MHz			1.5	%
Filter differential input resistance	Normal	3			kΩ
	Low-Z		140		Ω
Filter differential input capacitance				7	pF
Output noise voltage	BW = 100 MHz, Rs = 50Ω				
differentiated output	*fc* = 12 MHz, boost = 0 dB		2.6		mV Rms
differentiated output	*fc* = 12 MHz, boost = 13 dB		5.6		mV Rms
normal output	*fc* = 12 MHz, boost = 0 dB		2		mV Rms
normal output	*fc* = 12 MHz, boost = 13 dB		3.6		mV Rms
Filter output sink current			0.5		mA
Filter output offset voltage				200	mV
Filter output source current		2			mA
Filter output resistance	Single ended			200	Ω
Rx pin voltage	Ta = 27°C		600		mV
	Tj = 127°C		800		mV
Rx resistance 1% fixed value			12.1		kΩ

TIME BASE GENERATOR CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
FREF input range		8		20	MHz
FOUT frequency range				75	MHz
FOUT jitter	T_{OUT} = 1/FOUT Loop acquisition time = 30 µs	-TBD goal = 200		+TBD goal = 200	ps (rms)
M counter range		2		255	
N counter range		2		127	
VCO center frequency TVCO period	Fvco = [12.5/(RR + 0.4)] x [(0.622 x IDAC)+ 4.27] MHz TFLT - $\overline{TFLT}$ = TBD Fvco < 24 MHz Fvco = [12.5/(RR + 0.4)] x [(0.7 x IDAC) + 1.4] MHz	0.85 T0		1.15 T0	ns
VCO dynamic range	-2V ≤ TFLT - $\overline{TFLT}$ ≤ +2V FOUT = 36 MHz RR = 12.1 kΩ	±25		±45	%
VCO control gain KVCO	ωi = 2π/TVCO -2V ≤ TFLT - $\overline{TFLT}$ ≤ +2V	0.12 ωi		0.24 ωi	rad/(V-S)
Phase detector gain KD	KD = [12.5/(RR+0.4)] x (0.656 x IDAC + 3.38) x 10^{-6}	0.83 KD		1.17 KD	A/rad
KVCO x KD product accuracy		-28		+28	%
RR resistor range			12.1		kΩ
FREF input low time		20			ns
FREF input high time		20			ns
FOUT rise time	10% to 90% points, CL ≤ 20 pF			8	ns
FOUT fall time	90% to 10% points, CL ≤ 20 pF			8	ns

DATA SYNCHRONIZER CHARACTERISTICS

READ MODE

Read clock rise time	TRRC	10% to 90% points CL ≤ 15 pF			8	ns
Read clock fall time	TFRC	90% to 10% points CL ≤ 15 pF			8	ns
RRC duty cycle	TRD	Except during re-sync	40		60	%
		During re-sync	40			%
SD0 out set-up and hold time	TSDS, TSDH		10			ns
1/3 or 1/4 cell delay		TD = TVCO/2	0.8 TD		1.2 TD	ns

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DATA SYNCHRONIZER CHARACTERISTICS (continued)

WRITE MODE (SSI 33P3734)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Write MO data pulse width TWD	1.5V, CL ≤ 15 pF	TVCO -0.5		TVCO +0.5	ns
Write MO data rise time TRWD	10% to 90% points, CL ≤ 15 pF			8	ns
Write MO data fall time TFWD	90% to 10% points, CL ≤ 15 pF			8	ns
EARLY, LATE set-up time TSEL		5			ns
EARLY, LATE hold time THEL		5			ns
Write MO data input rise time TRWC	0.8 to 2V CL ≤ 15 pF			10	ns
Write MO data input fall time TFWC	2 to 0.8V, CL ≤15 pF			8	ns
Write MO data jitter	24 Mbit/s, 3T	-1		1	ns

DATA SYNCHRONIZATION

VCO center frequency period TVCO	FVCO = [12.5/(RR + 0.4)] x [(0.622 x IDAC) + 4.27] MHz TVCO = 1/FVCO, DFLT - $\overline{DFLT}$ = TBD RR = 12.1 kΩ FVCO < 24 MHz FVCO = [12.5/(RR + 0.4)] x [(0.7 x IDAC) + 1.4] MHz	0.85 T0		1.15 T0	ns
VCO dynamic range	-2V ≤ DFLT - $\overline{DFLT}$ ≤ +2V	±25		±45	%
VCO control gain KVCO	ωi = 2π/TVCO -2V ≤ DFLT- $\overline{DFLT}$ +2V	0.12 ωi		0.24 ωi	rad/(V-S)
Phase detector gain KD	Idle mode = 1 x KD Read mode = 3 x KD Read mode after gain shift = 1 x KD KD = [12.5/(RR + 0.4)] x (0.656 x IDAC + 3.38) x 10^{-6}	0.83 KD		1.17 KD	A/rad
VCO phase restart error	FVCO = 72 MHz	-2		+2	ns
Decode window center accuracy		-0.75		+0.75	ns
Decode window width		TVCO - 0.75			ns

WINDOW SHIFT CONTROL

Window shift magnitude is set by the value in the Window Shift (WS) register. The WS register bits are as follows:

BIT	NAME	FUNCTION
0	$\overline{WS0}$	
1	$\overline{WS1}$	
2	$\overline{WS2}$	
3	$\overline{WS3}$	
4	WSD	Window shift direction. 0=early, 1=late
5	WSE	Window shift enable
6	TDAC0	Used to route signals to DAC test point
7	TDAC1	Used to route signals to DAC test point

The window shift magnitude is set as a percentage of the full decode window, in 2% steps. This results in a window shift capability of ± 30% of the full decode window. The tolerance of the window shift magnitude is ± 30%. Window shift should be set during Idle mode or Write mode.

$\overline{WS3}$	$\overline{WS2}$	$\overline{WS1}$	$\overline{WS0}$	Shift Magnitude
1	1	1	1	No shift
1	1	1	0	2% (minimum shift)
1	1	0	1	4%
1	1	0	0	6%
1	0	1	1	8%
1	0	1	0	10%
1	0	0	1	12%
1	0	0	0	14%
0	1	1	1	16%
0	1	1	0	18%
0	1	0	1	20%
0	1	0	0	22%
0	0	1	1	24%
0	0	1	0	26%
0	0	0	1	28%
0	0	0	0	30% (maximum shift)

DATA SYNCHRONIZER CHARACTERISTICS (continued)

WRITE PRECOMP CONTROL (SSI 33P3734)

Write precomp magnitude is set by the value in the Write Precomp (WP) register. The WP register bits are as follows:

BIT	NAME	FUNCTION
0	$\overline{WE0}$	
1	$\overline{WE1}$	
2	$\overline{WE2}$	
3	WPE	Write precomp enable
4	$\overline{WL0}$	
5	$\overline{WL1}$	
6	$\overline{WL2}$	
7	-	Not used

The write precomp magnitude is calculated as:

$$TPE = n \times 0.04 \times TREF$$

where n = precomp magnitude scaling factor as shown below. The magnitude of early precomp is set by the $\overline{WEx}$ bits. The magnitude of late precomp is set by the $\overline{WLx}$ bits. TREF is the period of the reference frequency provided by the internal time base generator.

$\overline{WE2}$	$\overline{WE1}$	$\overline{WE0}$	Precomp Magnitude Scaling Factor	$\overline{WL2}$	$\overline{WL1}$	$\overline{WL0}$
1	1	1	No precomp	1	1	1
1	1	0	1X	1	1	0
1	0	1	2X	1	0	1
1	0	0	3X	1	0	0
0	1	1	4X	0	1	1
0	1	0	5X	0	1	0
0	0	1	6X	0	0	1
0	0	0	7X (maximum)	0	0	0

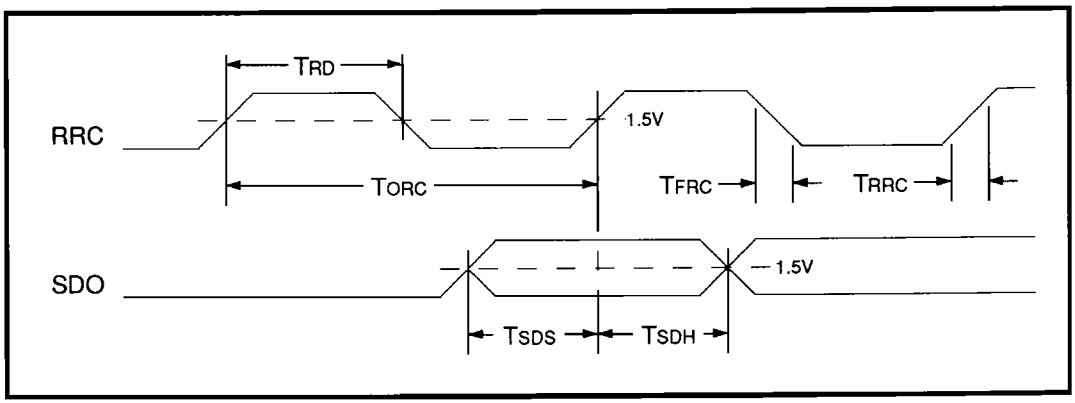


FIGURE 5: SDO Read Timing

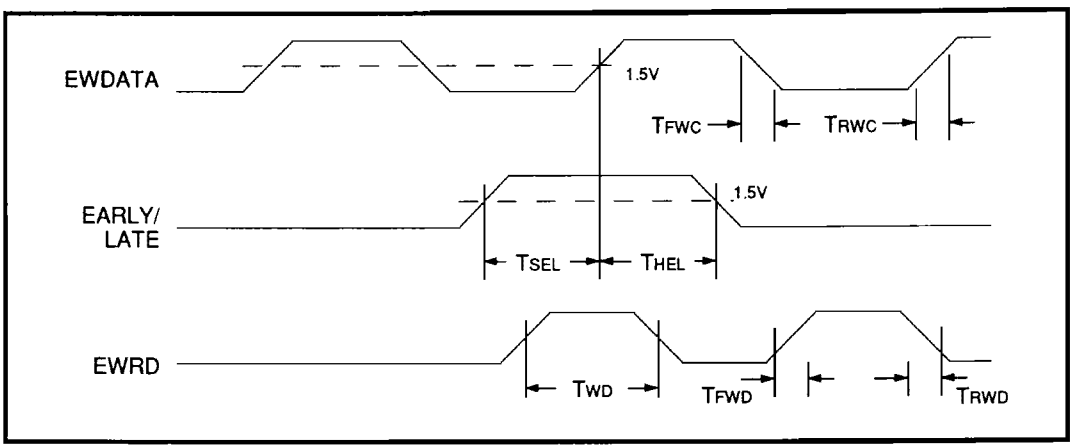


FIGURE 6: EWRD and EWDATA Write Timing

DATA SYNCHRONIZER CHARACTERISTICS (continued)

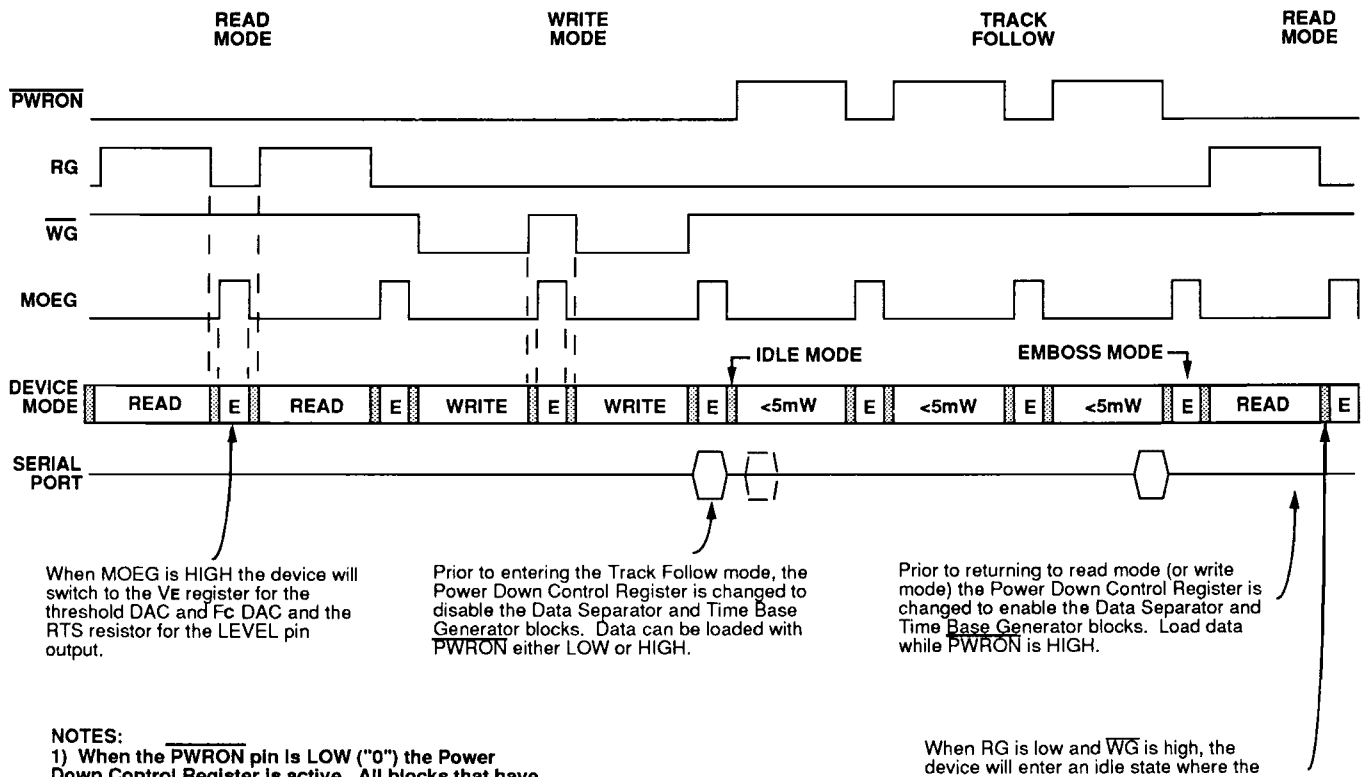
TABLE 4: Multiplexed Test Point Signal Selection

MTPE	TMS1	TMS0	MTP1	MTP2	MTP3
0	X	X	OFF	OFF	OFF
1	0	0	VCOREF	$\overline{DRD}$	DSREF
1	0	1	RD	DOUT	COUT
1	1	0	—	—	NCTR
1	1	1	SET	RESET	COUT

COUT Output of the pulse qualifier clock circuit
DOUT Output of the pulse qualifier data comparators
DSREF Output of the time base generator
NCTR Ncounter output of the time base generator
RD Read MO data output from the pulse qualifier
RESET Output of the negative threshold comparator
SET Output of the positive threshold comparator

TABLE 5: DACOUT Test Point Signal Selection

TDAC1	TDAC0	DAC MONITORED
0	0	Filter *fc* DAC
0	1	Qualifier threshold DAC (VTH)
1	0	Window shift DAC
1	1	Write precomp DAC



NOTES:

1) When the PWRON pin is LOW ("0") the Power Down Control Register is active. All blocks that have their control bit set to "1" will be powered down. When the PWRON pin is HIGH ("1") the device goes into a sleep mode with all blocks powered down except the serial port.

2) When the threshold DAC reference is switched, there is a maximum settling time of 1.5μsec for the DAC.

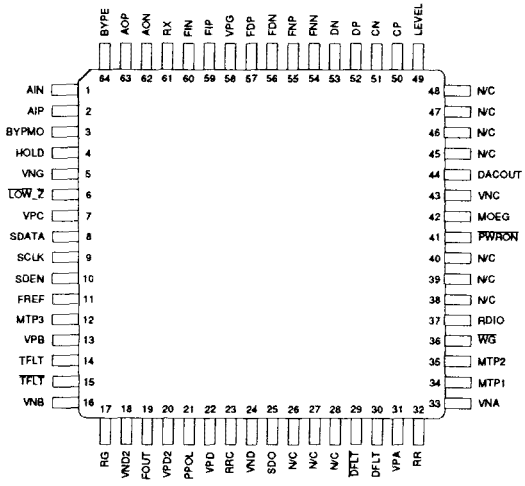
FIGURE 7: Power Control Timing

SSI 33P3733/34
8-26.5 Mbit/s Read Channel

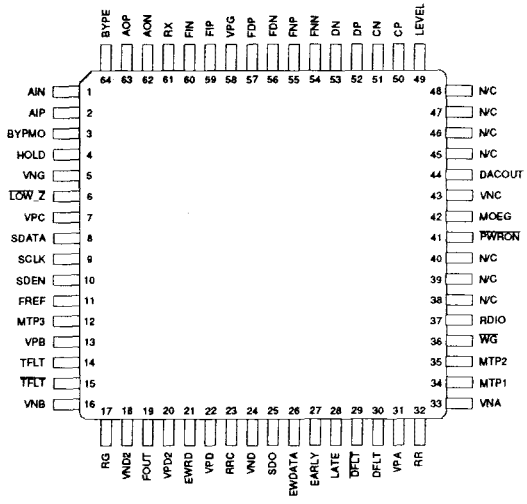
PACKAGE PIN DESIGNATIONS
(Top View)

Thermal Characteristics: θjA

64-lead TQFP	75° C/W



64-Lead TQFP
SSI 33P3733



64-Lead TQFP
SSI 33P3734

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION		ORDER NUMBER	PACKAGE MARK
SSI 33P3733	64-Lead TQFP	33P3733-CGT	33P3733-CGT
SSI 33P3734	64-Lead TQFP	33P3734-CGT	33P3734-CGT

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

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