

# 16-BIT LOW COST, LOW POWER $\Sigma - \Delta$ A/D CONVERTER

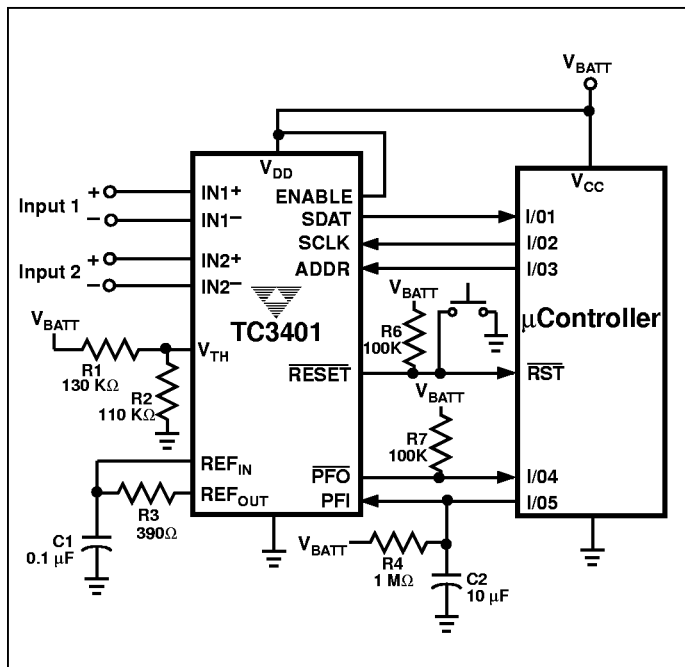
## FEATURES

- 16-Bit Resolution at Eight Conversions Per Second, Adjustable Down to 10-Bit Resolution at 512 Conversions Per Second
- 1.8V – 5.5V Operation, Low Power Operating .... 300 $\mu$ A  
..... Sleep: 50 $\mu$ A
- True Differential Inputs with Built-In Multiplexer Provide Ratiometric Conversions
- MicroPort™ Serial Bus Requires Only Two Interface Lines
- Uses Internal or External Reference
- V<sub>DD</sub> Monitor and Reset Generator Operational in Shutdown Mode
- Early Warning Power Fail Detector, Also Suitable as Wake-Up Timer Operational in Shutdown Mode
- Automatically Enters Sleep Mode When Not In Use
- 16-Pin QSOP and PDIP Packages

## TYPICAL APPLICATIONS

- Consumer Electronics, Thermostats, CO Monitors, Humidity Meters, Security Sensors
- Embedded Systems, Data Loggers, Portable Equipment
- Medical Instruments

## TYPICAL APPLICATION



## GENERAL DESCRIPTION

The TC3401 is a low cost, low power analog-to-digital converter based on TelCom's Sigma-Delta technology. It will perform 16-bit conversions (15-bit plus sign) at up to eight per second. The TC3401 is optimized for use as a microcontroller peripheral in low cost, battery operated systems. A voltage reference is included, or an external reference can be used. A V<sub>DD</sub> monitor with reset generator provides Power-On Reset and Brown-out protection while an extra threshold detector is suitable for use as an early warning power fail detector, or as a wake-up timer.

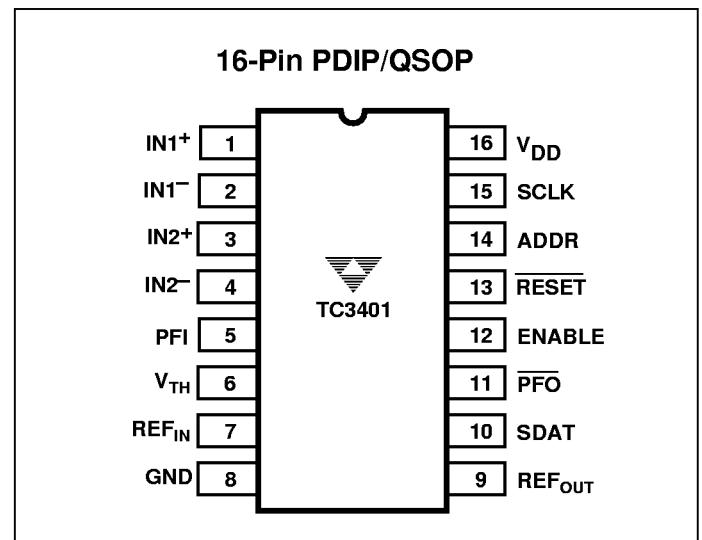
The TC3401's 2-wire MicroPort™ digital interface is used for starting conversions and for reading out the data. Driving the SCLK line low starts a conversion. After the conversion starts, each additional falling edge (up to six) detected on SCLK for t<sub>4</sub> seconds reduces the A/D resolution by one bit and cuts conversion time in half. After a conversion is completed, clocking the SCLK line puts the MSB through LSB of the resulting data word onto the SDAT line, much like a shift register. The part automatically sleeps when not performing a data conversion.

The TC3401 is available in a 16-Pin PDIP and a 16-Pin QSOP package.

## ORDERING INFORMATION

Part No.	Package	Temp. Range
TC3401EPE	16-Pin PDIP(Narrow)	0°C to +85°C
TC3401EQR	16-Pin QSOP(Narrow)	0°C to +85°C

## PIN CONFIGURATIONS



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## TC3401

### ABSOLUTE MAXIMUM RATINGS\*

Supply Voltage .....	6.0V
Voltage on Pins:	
PFO, RESET, .....	(GND – 0.3V) to 5.5V
Input Voltage (All Other Pins) .....	
.....	(GND – 0.3V) to (V <sub>DD</sub> + 0.3V)
Operating Temperature .....	0°C to 85°C
Maximum Chip Temperature .....	+150°C
Storage Temperature Range .....	– 65°C to +150°C
Lead Temperature (Soldering, 10 sec) .....	+300°C

\*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

**DC ELECTRICAL CHARACTERISTICS:** T<sub>A</sub> = 25°C and V<sub>DD</sub> = 2.7V, unless otherwise specified. Specifications in Bold type apply over a temperature range of 0°C to 85°C. V<sub>REF</sub> = .25V, Internal Clock Freq = 520kHz

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
<b>POWER SUPPLY</b>						
V <sub>DD</sub>	Supply Voltage		1.8	—	5.5	V
I <sub>DD</sub>	Supply Current, During Data Conversion		—	300	—	μA
I <sub>DD(SLEEP)</sub>	Supply Current, Sleep Mode	T <sub>A</sub> = +25°C	—	50	80	μA
I <sub>DD(SLEEP)</sub>			—	<b>50</b>	<b>130</b>	μA
<b>ACCURACY (Differential Inputs)</b>						
RES	Resolution		—	16	—	Bits
INL	Integral Non-Linearity	V <sub>DD</sub> = 2.7V	—	.0038	—	%FSR
V <sub>OS</sub>	Offset Error	<b>IN<sup>+</sup> = IN<sup>-</sup> = 0V</b>	—	—	<b>±0.9</b>	%FSR
V <sub>NOISE</sub>	Referred to input		—	60	—	μVrms
CMR	Common Mode Rejection	at DC	—	75	—	dB
FSE	Full Scale Error		—	0.4%	—	%FS
PSRR	Power Supply Rejection Ratio	V <sub>DD</sub> = 2.5V to 3.5V	—	75	—	dB
<b>IN<sup>+</sup>, IN<sup>-</sup></b>						
V <sub>IN±</sub>	Differential Input Voltage	(Note 1)	—	—	V <sub>DD</sub>	V
	Absolute Voltage Range on <b>IN<sup>+</sup>, IN<sup>-</sup></b>		GND	—	V <sub>DD</sub>	V
	Input Bias Current		—	1	100	nA
C <sub>IN</sub>	Input Sampling Capacitance		—	2	—	pF
R <sub>IN</sub>	Differential Input Resistance	(Note 2)	—	2.0	—	MΩ
<b>REF<sub>IN</sub>, REF<sub>OUT</sub>, ENABLE</b>						
V <sub>REF</sub>	<b>REF<sub>IN</sub></b> Voltage Range		0	—	1.25	V
I <sub>REF</sub>	<b>REF<sub>IN</sub></b> Input Current		—	1	—	μA
V <sub>REFOUT</sub>	<b>REF<sub>OUT</sub></b> Voltage		—	1.193	—	V
REF <sub>SINK</sub>	<b>REF<sub>OUT</sub></b> Current Sink Capability		—	10	—	μA
REF <sub>SRC</sub>	<b>REF<sub>OUT</sub></b> Current Source Capability		300	—	—	μA
<b>SCLK, ADDR</b>						
V <sub>IL</sub>	Input Low Voltage		—	—	<b>0.3 x V<sub>DD</sub></b>	V
V <sub>IH</sub>	Input High Voltage		<b>0.7 x V<sub>DD</sub></b>	—	—	V
I <sub>LEAK</sub>	Leakage Current		—	1	—	μA

Notes: 1. Differential input voltage defined as (V<sub>IN+</sub> – V<sub>IN-</sub>)  
2. Resistance from IN<sub>n+</sub> to IN<sub>n-</sub> or IN<sub>n</sub> to GND.

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**DC ELECTRICAL CHARACTERISTICS (CONT.):**  $T_A = 25^\circ\text{C}$  and  $V_{DD} = 2.7\text{V}$ , unless otherwise specified. Specifications in Bold type apply over a temperature range of  $0^\circ\text{C}$  to  $85^\circ\text{C}$ .

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
<b>SDAT, <math>\overline{\text{RESET}}</math></b>						
$V_{OL}$	Output Low Voltage	$I_{OL} = 2\text{ mA}$	—	—	0.4	V
$V_{OH}$	Output High Voltage (SDAT)	$I_{SOURCE} = 400\mu\text{a}$ (Note 2)	$0.9 \times V_{DD}$	—	—	V
$V_{DD(MIN)}$	Minimum $V_{DD}$ for $\overline{\text{PFO}}$ , $\overline{\text{RESET}}$ Valid		—	1.1	1.3	V
<b><math>V_{TH}</math></b>						
$V_{CCPFI}$	PFI Input Voltage Range		0	—	$V_{DD}$	V
	$V_{TH}$ , PFI Input Current		-0.1	.01	0.1	$\mu\text{a}$
$V_{THR}$	Threshold		—	1.23	—	V
	Threshold Hysteresis		—	30	—	mV

**AC ELECTRICAL CHARACTERISTICS:** Typical values are measured at  $T_A = 25^\circ\text{C}$  and  $V_{DD} = 2.7\text{V}$ . Minimums and maximums are guaranteed in the range  $T_A = \text{min to max}$ ,  $V_{DD} = 2.7\text{V}$  unless otherwise specified. (See Figures 2 and 5.)

Symbol	Parameter	Description	Min	Typ	Max	Unit
$t_1$		Width of SCLK (Negative)	1	—	—	$\mu\text{sec}$
$t_2$	Resolution Reduction Clock Width	Width of SCLK (Positive)	1	—	—	$\mu\text{sec}$
$t_3$	Conversion Time (15-Bit Plus Sign)	16-bit conversion, $T_A = 25^\circ$ (Note 1)	—	125	—	msec
	Conversion Time (14-Bit Plus Sign)	15-bit conversion	—	t3/2.0	—	msec
	Conversion Time (13-Bit Plus Sign)	14-bit conversion	—	t3/4.0	—	msec
	Conversion Time (12-Bit Plus Sign)	13-bit conversion	—	t3/7.8	—	msec
	Conversion Time (11-Bit Plus Sign)	12-bit conversion	—	t3/15.1	—	msec
	Conversion Time (10-Bit Plus Sign)	11-bit conversion	—	t3/28.6	—	msec
	Conversion Time (9-Bit Plus Sign)	10-bit conversion	—	t3/51.4	—	msec
$t_4$	Resolution Reduction Window	Width of SCLK	—	t3/85.7	—	msec
$t_5$	SCLK to Data Valid	SCLK falling edge to SDAT valid	1000	—	—	nsec
$t_6$	Address Setup	Address valid to SCLK	0	—	—	nsec
$t_7$	Address Hold	SCLK to address valid hold	1000	—	—	nsec
$t_8$	Acknowledge Delay	SCLK to SDAT delay	—	—	1000	nsec
$t_9$	$\overline{\text{RESET}}$ Active Timeout Period	Delay from POR or brown-out recovery to $\overline{\text{RESET}} = V_{OH}$	—	t3*2	—	msec
$t_{10}$	$\overline{\text{PFO}}$ Delay	PFI to $\overline{\text{PFO}}$ delay	—	25	—	$\mu\text{sec}$
$t_{11}$	$\overline{\text{RESET}}$ Delay	Delay for $V_{TH}$ falling at 10 V/msec to $\overline{\text{RESET}}$ low	5	—	64	$\mu\text{sec}$

- Notes: 1. Nominal temperature drift is -2830 ppm/ $^\circ\text{C}$  for temperature less than  $25^\circ\text{C}$  and -1340 ppm/ $^\circ\text{C}$  for temperatures greater than  $25^\circ\text{C}$ .  
2. @ $V_{DD} = 1.8\text{V}$ ,  $I_{SOURCE} \leq 200\mu\text{a}$

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## TC3401

### PIN DESCRIPTION

TC3401 Pin No.	Symbol	Description
1, 3	INn <sup>+</sup>	Analog Input. This is the positive terminal of a true differential input consisting of INn <sup>+</sup> and INn <sup>-</sup> . $V_{IN(n)} = (INn^+ - INn^-)$ .
2, 4	INn <sup>-</sup>	Analog Input. This is the negative terminal of a true differential input consisting of INn <sup>+</sup> and INn <sup>-</sup> . $V_{IN(n)} = (INn^+ - INn^-)$ INn <sup>-</sup> can swing to, but not below, ground.
5	PFI	Analog Input. This is the positive input to an internal comparator used as a threshold detector. The negative input is tied to an internal reference.
6	V <sub>TH</sub>	Analog Input. This is the positive input to the internal comparator used to monitor the voltage supply. The negative input is tied to an internal reference. When V <sub>TH</sub> falls below the internal reference, the reset generator drives $\overline{\text{RESET}}$ low as specified in the <i>Electrical Characteristics</i> section.
7	REF <sub>IN</sub>	Analog Input. The converter's reference voltage is the differential between this pin and ground times two. It may be tied directly to REF <sub>OUT</sub> or scaled using a resistor divider. Any user supplied reference voltage or the power supply rail may be used in place of REF <sub>OUT</sub> .
8	GND	Ground Terminal.
9	REF <sub>OUT</sub>	Analog Output. The internal reference connects to this pin. It may be scaled externally, if desired, and tied to the REF <sub>IN</sub> input to provide the converter's reference voltage. Care must be taken in connecting external circuitry to this pin. This pin is in a high impedance state during sleep mode.
10	SDAT	Digital Output (push-pull). This is the MicroPort™ serial data output. SDAT is driven low while the TC3401 is converting data, effectively providing a "busy" signal. After the conversion is complete, every high-to-low transition on the SCLK pin puts a bit from the resulting data word on the SDAT pin (fromMSB to LSB).
11	$\overline{\text{PFO}}$	Digital Output (open drain). This is the output of the internal threshold detector. When PFI is less than the internal reference, $\overline{\text{PFO}}$ is driven low.
12	ENABLE	Digital Input. When this input control is pulled low, the part is internally restarted. That is, any data conversion or data read sequence is cleared and the part goes into sleep mode. When ENABLE returns high, the part resumes normal operation.
13	RESET	Digital Output (open drain). This is the output of the V <sub>DD</sub> monitor reset generator. $\overline{\text{RESET}}$ is driven low when a power-on reset or brown-out condition is detected. (See <i>AC Electrical Characteristics</i> .)
14	ADDR	Digital Input. This input controls the analog input multiplexer to select one of two input channels. This address is latched at the falling edge of the SCLK, which starts an A/D conversion. 0 = Input 1, 1 = Input 2.
15	SCLK	Digital Input. This is the MicroPort™ serial clock input. The TC3401 comes out of sleep mode and a conversion cycle begins when this pin is driven low. After the conversion starts, each additional falling edge (up to six) detected on SCLK for t <sub>4</sub> seconds reduces the A/D resolution by one bit. When the conversion is complete, the data word can be shifted out on the SDAT pin by clocking the SCLK pin.
16	V <sub>DD</sub>	Power Supply Input.

### GENERAL THEORY OF OPERATION

The TC3401 has a 16-bit sigma-delta A/D converter. It has two differential inputs, an analog multiplexer, a  $V_{DD}$  monitor with reset generator, and an early warning power fail detector. The detailed description of the key components of the TC3401 is outlined below. (Also refer to the *A/D Operational Flowchart* on page 10 and the Timing Diagrams in Figures 2 through 5).

#### A/D Converter Operation

When the TC3401 is not converting, it is in sleep mode with both the SCLK and SDAT lines high. An A/D conversion is initiated by a high to low transition on the SCLK line at which time the internal clock of the TC3401 is started and the address value (ADDR) is internally latched. The address value steers the analog multiplexer to select the input channel to be converted. Each additional high to low transition of SCLK (following the initial SCLK falling edge) and during the time interval  $t_4$  will decrement the conversion accuracy by one bit and reduce the conversion time by one half. The time interval  $t_4$  is referred to as the resolution reduction window. The minimum conversion resolution is 10 bits so any more than 6 SCLK transitions during  $t_4$  will be ignored.

After each high to low transition of SCLK, in the  $t_4$  interval, the SDAT output is driven high by the TC3401 to acknowledge that the conversion has been decremented. When the SCLK returns high or the  $t_4$  interval ends, the SDAT line returns low (see Figure 2). When the conversion is complete SDAT is driven high. The 3401 now enters sleep mode and the conversion value can be read as a serial data word on the SDAT line.

#### Reading the Data Word

After the conversion is complete and SDAT goes high, the conversion value can be clocked serially onto the SDAT line by high to low transitions of the SCLK. The data word is in two's complement format with the sign bit clocked onto the SDAT line first followed by the MSB and ending in the LSB. For a 16 bit conversion the data word would consist of a sign bit followed by 15 magnitude bits, Table 1 shows the data word versus input voltage for a 16 bit conversion. Note that the full scale input voltage range is  $\pm(2 \text{ REF}_{IN} - 1 \text{ LSB})$ . When  $\text{REF}_{OUT}$  of the TC3401 is fed back directly to the  $\text{REF}_{IN}$  pin then  $\text{REF}_{IN}$  is typically 1.193V and an LSB is 73 $\mu$ V for a 16 bit conversion.

Figure 4 shows typical SCLK and SDAT waveforms for 16, 12 and 10 bit conversions. Note that any complete convert and read cycle requires 17 netgative edge clock pulses. The first is the convert command. Then, up to six of these can occur in the resolution reduction window,  $t_4$ , to

decrement accuracy. The remaining pulses clock out the conversion data word.

**Table 1. Data Conversion Word vs. Voltage Input ( $\text{REF}_{IN} = 1.193\text{V}$ )**

Data Word	$\text{INn}^+ - \text{INn}^-$ (Volts)
0111 1111 1111 1111	2.38596 (Positive Full Scale)
0000 0000 0000 0001	72.8 E – 6
0000 0000 0000 0000	0
1111 1111 1111 1111	-72.8 E – 6
1000 0000 0000 0001	-2.38596 (Negative Full Scale)
1000 0000 0000 0000	Reserved Code

The SCLK input has a filter which rejects any positive or negative pulse of width less than 50nsec to reduce noise. The rejection width of this pulse can vary between 50nsec and 750nsec depending on processing parameters and supply voltage.

Figure 3 shows a truth table for determining the mode of operation for the TC3401 part by recording the value of SDAT for SCLK in a high, then low, then high state. For example, if SCLK goes through a 1-0-1 transition and the corresponding values of SDAT are 1-1-0, then the SCLK falling edge started a new data conversion. A 0-1-0 for SDAT would have indicated a resolution reduction had occurred. This is useful if the microcontroller has a watchdog reset or otherwise loses track of where the TC3401 part is in the conversion and data readout sequence. The microcontroller can simply transition SCLK until it "finds" a Start Conversion condition.

#### $V_{DD}$ Monitor

The TC3401  $\overline{\text{RESET}}$  output is high provided the voltage at  $V_{TH}$  is greater than the internal voltage reference. This reference is approximately the same value as the voltage appearing at  $\text{REF}_{OUT}$ . When  $V_{TH}$  is less than the internal reference,  $\overline{\text{RESET}}$  is pulled low. When  $V_{TH}$  rises above the internal reference voltage again  $\overline{\text{RESET}}$  is held low for the reset active timeout period,  $t_9$ , before being released high. The  $\overline{\text{RESET}}$  output is guaranteed to be valid for  $V_{DD} = 1.3\text{V}$  to 5.5V.

When used to generate a power-on or brown-out reset an external resistor network is required to divide the appropriate  $V_{DD}$  threshold down to 1.23V at the  $V_{TH}$  input (see Figure 1). For example, to generate a POR for a  $V_{DD}$  at 3V-10%, then the values of R1 and R2 should be 137k $\Omega$  and 115k $\Omega$  respectively.

Since  $\overline{\text{RESET}}$  is an open drain it can be wired-OR'ed with another open drain or external switch if desired.

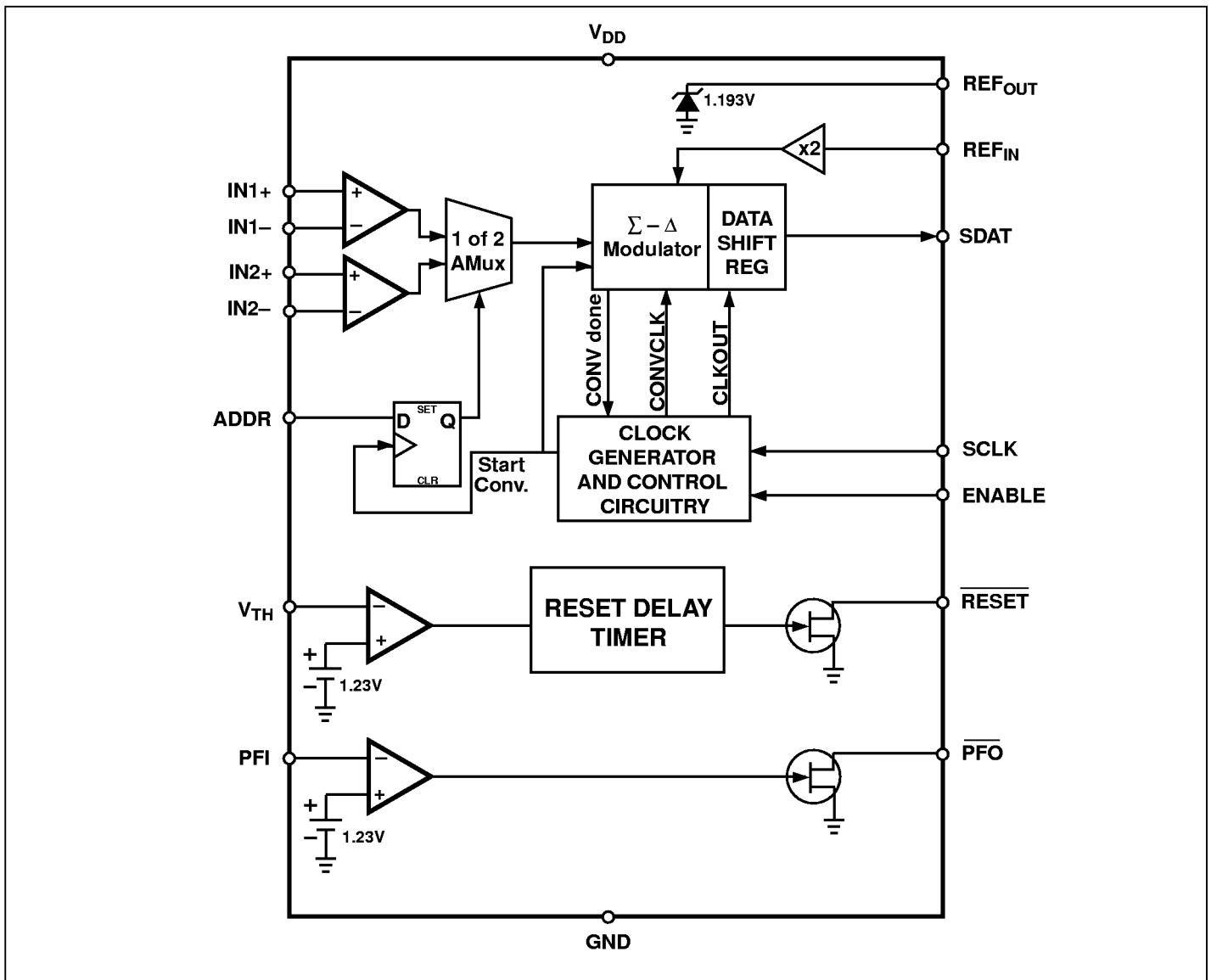
## TC3401

### Power Fail Detector

The power fail detector is a comparator in which the inverting input is connected to the internal voltage reference, the non-inverting input is the PFI pin of the TC3401 and the PFO pin is the active low, open collector output. This comparator is suitable as an early warning fail or low battery indicator. In a typical application, where a voltage regulator is being used to supply power to a system, the power fail comparator would monitor the input voltage to the regulator while the  $V_{DD}$  monitor would measure the output voltage of the regulator. Both PFO and RESET would drive interrupt pins of a microcontroller.

The Power Fail detector, may be used as a Wake-up or Watch-dog Timer. The *Typical Application Circuit* on Page 1 shows an RC network on PFI with the capacitor tied to a tri-stated  $\mu\text{C}$  I/O pin. If  $R_4$  is 1 M $\Omega$  and  $C_2$  is 10 $\mu\text{F}$ , the time constant is roughly ten seconds. The  $\mu\text{C}$  resets the RC network by driving the I/O tied to PFI low and then tri-stating it. The RC network will ramp to 1.23V in roughly 9 seconds, assuming a  $V_{BATT}$  of 3.0V. With  $\overline{\text{PFO}}$  tied to a  $\mu\text{C}$  input or interrupt, the  $\mu\text{C}$  will see a low-to-high transition on  $\overline{\text{PFO}}$  when voltage on PFI exceeds 1.23V. The  $\overline{\text{PFO}}$  output is guaranteed to be valid for  $V_{DD} = 1.3$  to 5.5V.

### FUNCTIONAL BLOCK DIAGRAM



TIMING DIAGRAMS

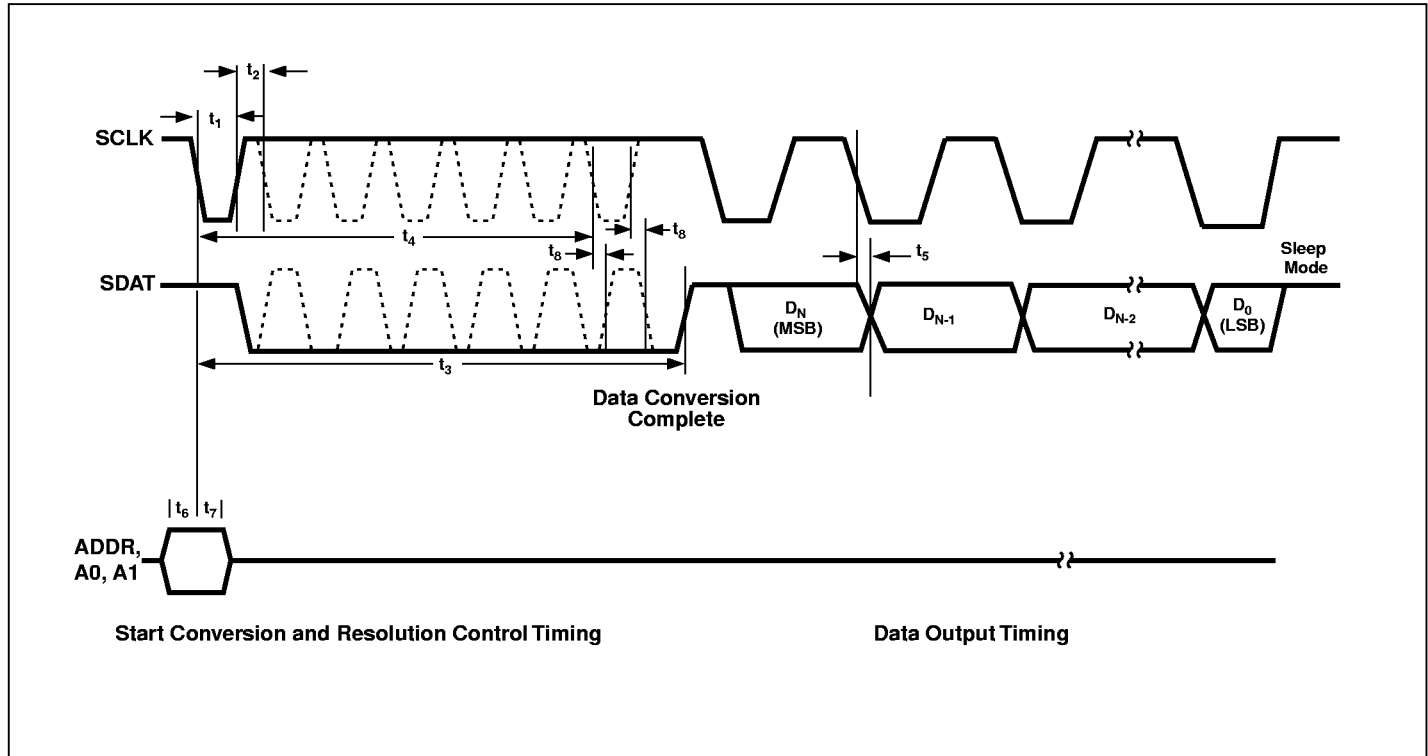


Figure 2. Conversion and Data Output Timing

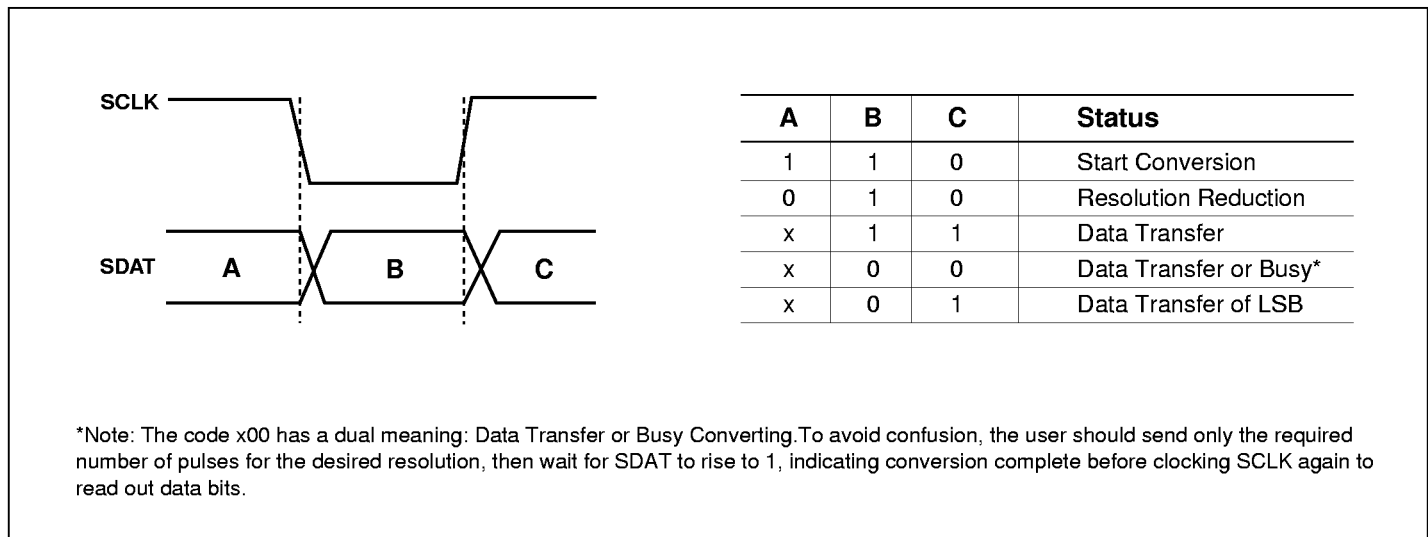


Figure 3. SCLK, SDAT Logic State Table

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TIMING DIAGRAMS (CONT.)

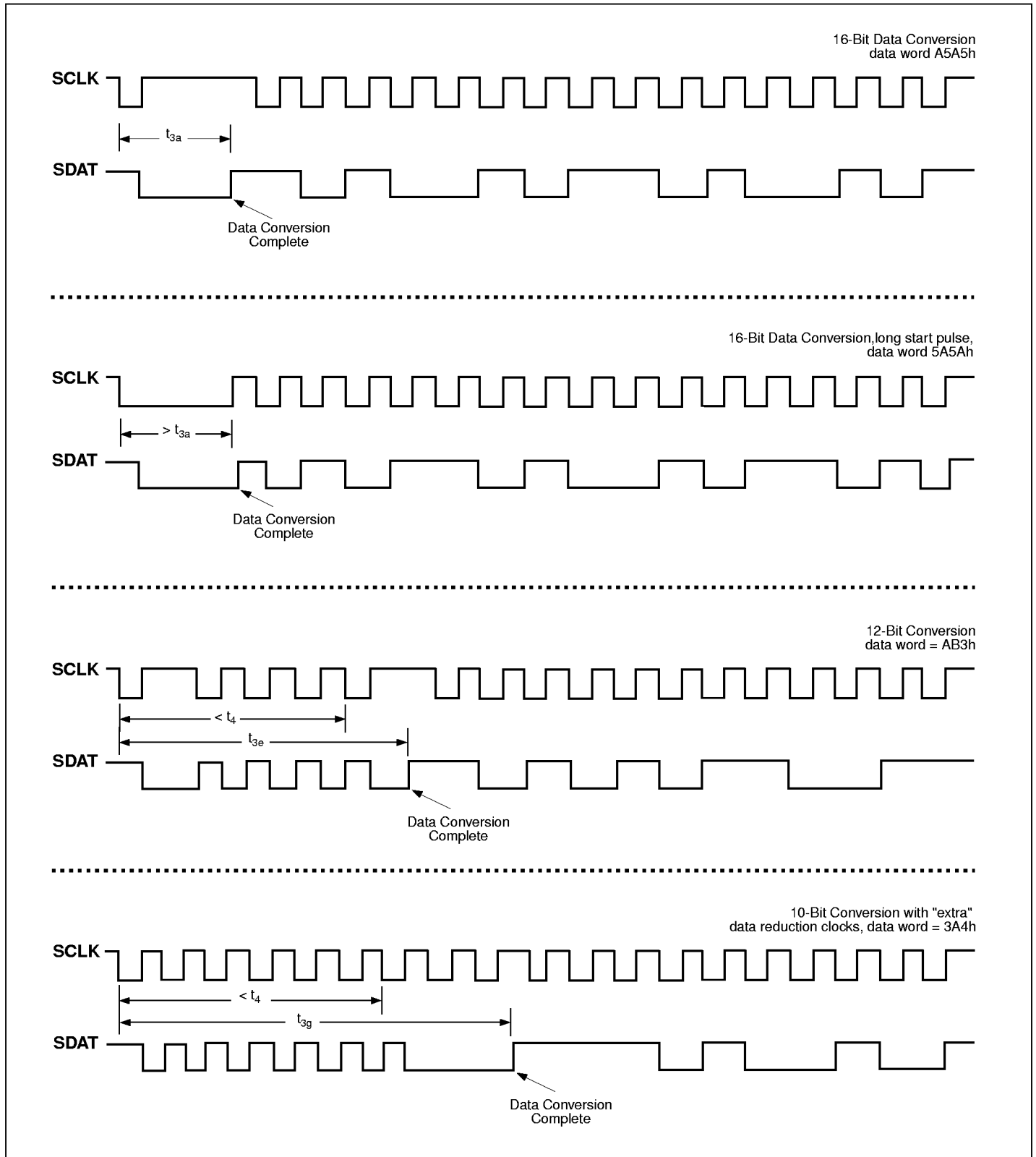


Figure 4. Example Timing Diagrams

TIMING DIAGRAMS (CONT.)

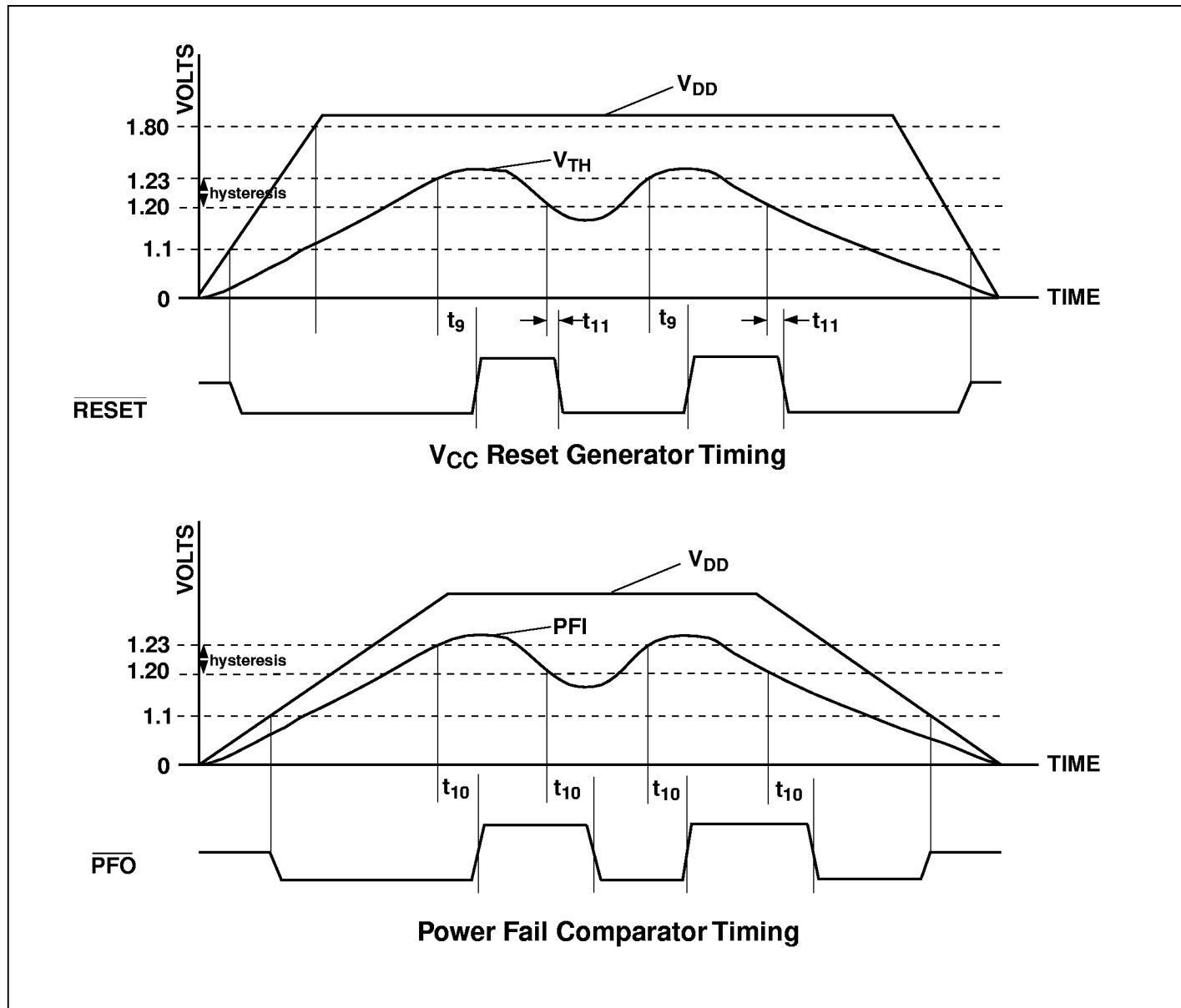
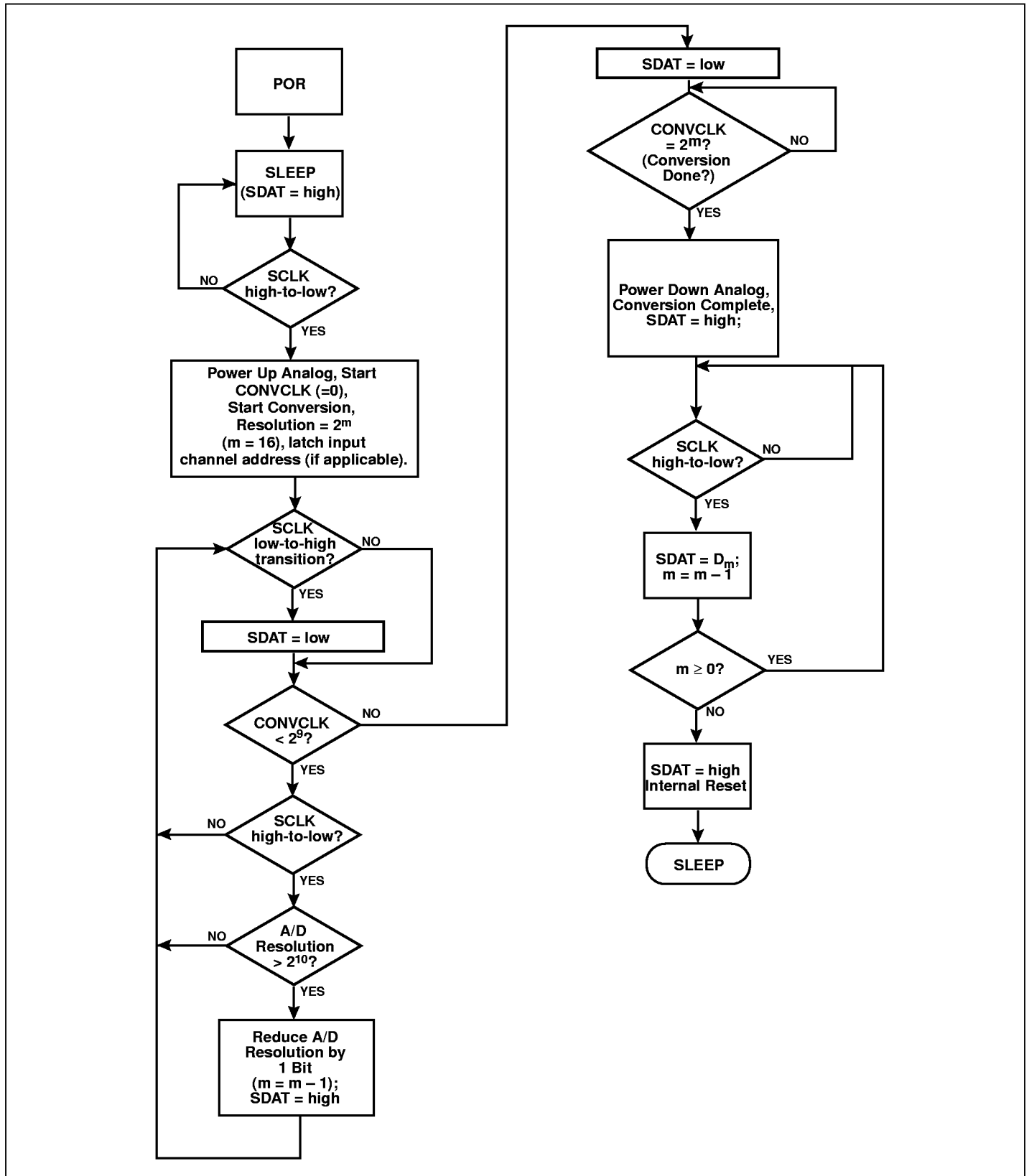


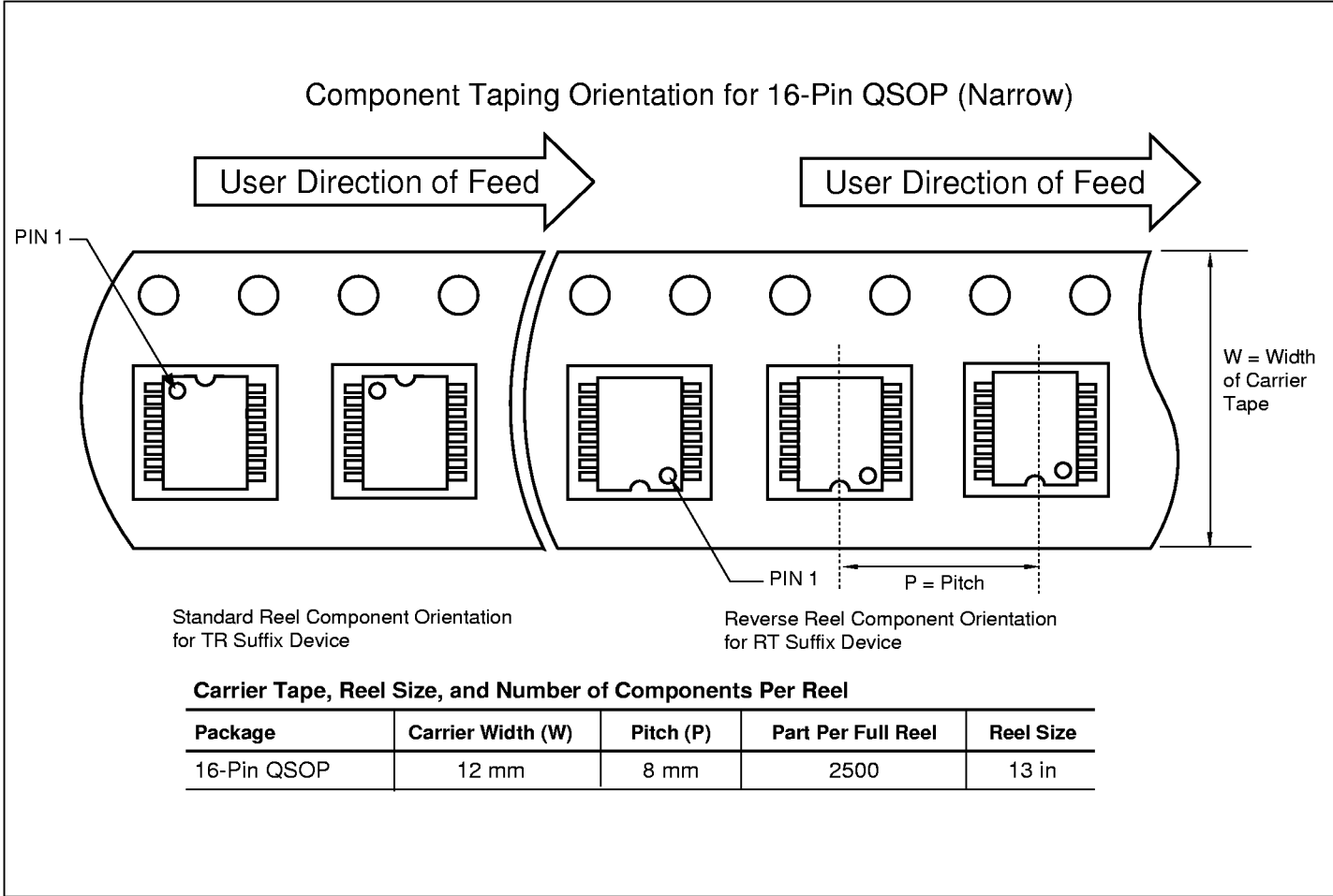
Figure 5. Reset and Power Fail Timing

TC3401

A/D OPERATIONAL FLOWCHART



**TAPING FORM**

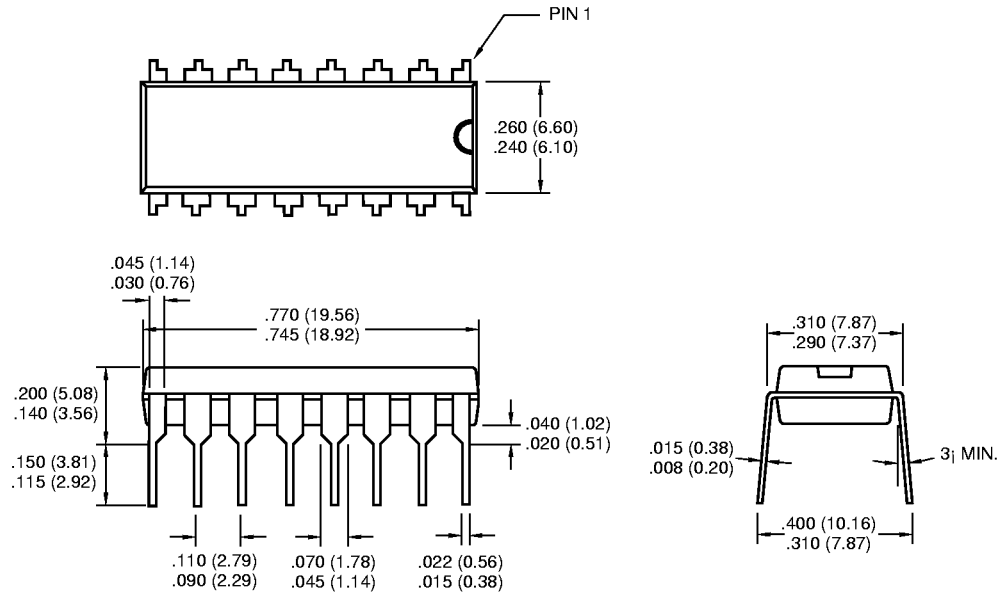


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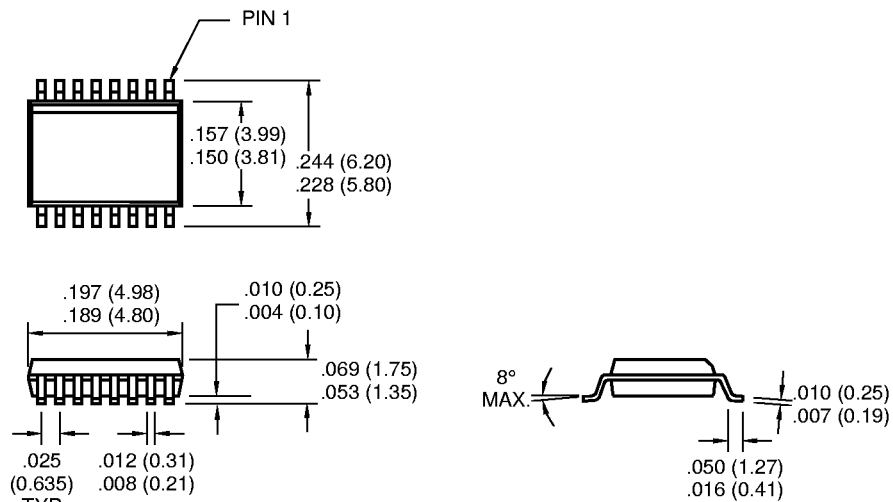
## TC3401

### PACKAGE DIMENSIONS

#### 16-Pin PDIP (Narrow)



#### 16-Pin QSOP (Narrow)



Dimensions: inches(mm)

### Sales Offices

**TelCom Semiconductor, Inc.**  
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