M5M417405DJ,TP -5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE) MODE 16777216-BIT (4194304-WORD BY 4-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 4194304-word by 4-bit dynamic RAMs with EDO (Extended Data Out : Hyper Page) mode function, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of double-layer metal process combined with twin-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities. Self refresh current is low enough for battery back-up application.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M417405DXX-5,5S	50	13	25	13	90	655
M5M417405DXX-6,6S	60	15	30	15	110	540
M5M417405DXX-7,7S	70	20	35	20	130	475

XX=J,TP

- Standard 26 pin SOJ,26 pin TSOP
- Single 5V±10% supply
- Low stand-by power dissipation
  - 2.75mW (Max) ----------CMOS Input level
  - 1.10mW (Max)* ---------- CMOS Input level
- Low operating power dissipation
  - M5M417405Dxx- 5,5S ---------- 800mW (Max)
  - M5M417405Dxx- 6,6S ---------- 660mW (Max)
  - M5M417405Dxx- 7,7S ---------- 580mW (Max)
- Self refresh capability*
  - Self refresh current ---------- 200µA(Max)
- EDO mode (2048-column random access), Read-modify- write, RAS-only refresh, CAS before RAS refresh, Hidden refresh capabilities.
- Early-write mode, $\overline{OE}$ and $\overline{W}$ to control output buffer impedance
- All inputs, outputs TTL compatible and low capacitance
- 2048 refresh cycles every 32ms (A0 ~ A10)

*:Applicable to self refresh version(M5M417405DJ, TP -5S, -6S,-7S :option) only

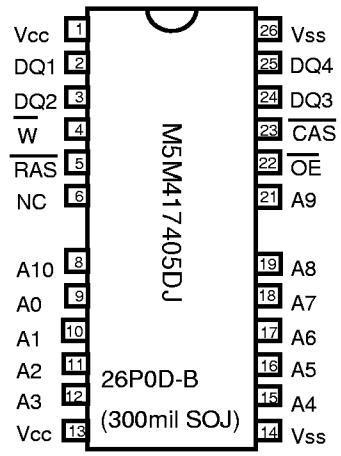
APPLICATION

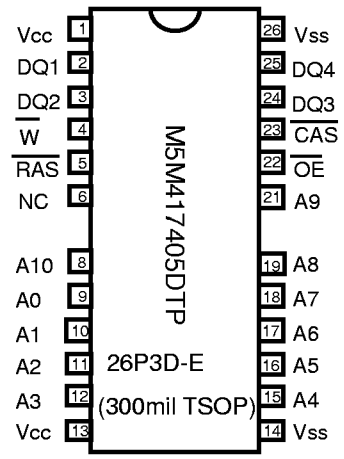
Main memory unit for computers, Microcomputer memory, Refresh memory for CRT,

PIN DESCRIPTION

Pin Name	Function
A0-A10	Address Inputs
DQ1-DQ4	Data Inputs / Outputs
$\overline{RAS}$	Row Address Strobe Input
$\overline{CAS}$	Column Address Strobe Input
$\overline{W}$	Write Control Input
$\overline{OE}$	Output Enable Input
Vcc	Power Supply (+5V)
Vss	Ground (0V)

PIN CONFIGURATION (TOP VIEW)





NC: NO CONNECTION

M5M417405DJ,TP -5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE) MODE 16777216-BIT (4194304-WORD BY 4-BIT) DYNAMIC RAM

FUNCTION

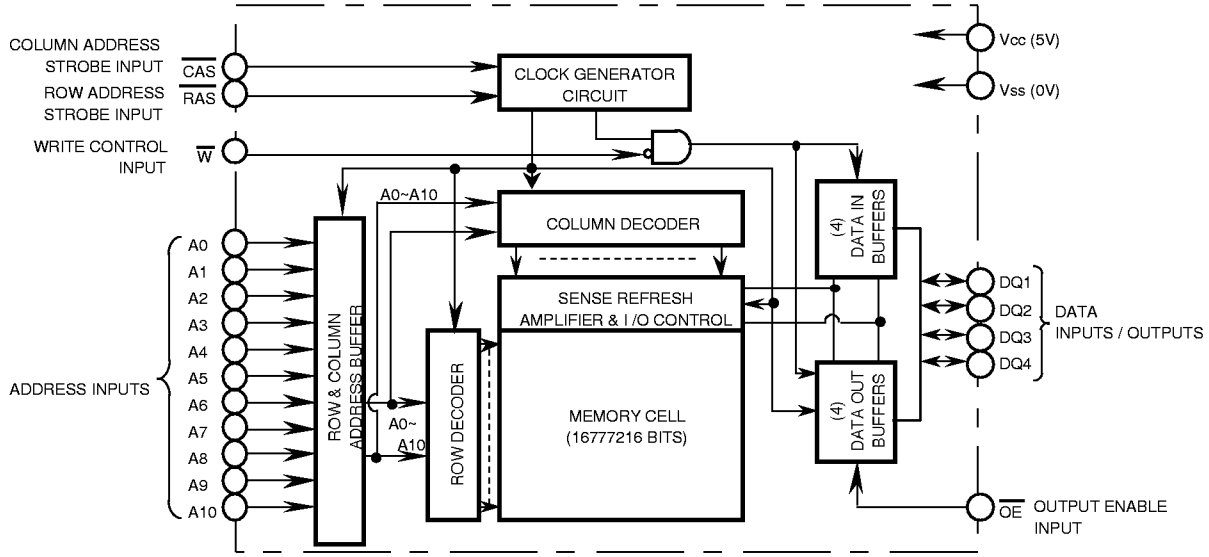
In addition to normal read, write and read-modify-write operations , the M5M417405DJ, TP provides a number of other functions,e.g.,, EDO Mode, RAS-only refresh,and delayed-write. The input condition and output state for each are shown in Table 1.

Table 1 Input condition and output state for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	EDO mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Write (Delayed write)	ACT	ACT	ACT	DNC	APD	APD	VLD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	NAC	ACT	APD	DNC	OPN	VLD	YES	
Self refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : Invalid,APD : applied, OPN : open

BLOCK DIAGRAM



M5M417405DJ,TP -5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE) MODE 16777216-BIT (4194304-WORD BY 4-BIT) DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	With respect to Vss	-1~7	V
VI	Input voltage		-1~7	V
V0	Output voltage		-1~7	V
I0	Output current		50	mA
Pd	Power dissipation	Ta=25°C	1000	mW
Topr	Operating temperature		0 ~70	°C
Tstg	Storage temperature		-65 ~150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
Vcc	Supply voltage	4.5	5.0	5.5	V
Vss	Supply voltage	0	0	0	V
VIH	High-level input voltage, all inputs	2.4		5.5	V
VIL	Low-level input voltage, all inputs	-1.0**		0.8	V

Note 1 : All voltage values are with respect to Vss

** : VIL(Min) is -2.0V when undershoot width is less than 25ns.(The width is defined as the period when the voltage level is below Vss.)

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, Vcc= 5V±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
VOH	High-level output voltage		IOH = -5.0mA	2.4		Vcc	V
VOL	Low-level output voltage		IOL = 4.2mA	0		0.4	V
IOZ	Off-state output current		Q floating, 0V≤VOUT≤5.5V	-10		10	µA
II	Input current		0V≤VIN≤+5.5V, Other inputs pins=0V	-10		10	µA
ICC1 (AV)	Average supply current from Vcc operating (Note 3,4,5)	M5M417405D-5,5S	RAS, CAS cycling tRC=tWC=min. output open			145	mA
		M5M417405D-6,6S				120	
		M5M417405D-7,7S				105	
ICC2	Supply current from Vcc , stand-by (Note 6)		RAS= CAS =VIH, output open			2	mA
			RAS= CAS≥Vcc -0.2V, output open			0.5	
ICC3 (AV)	Average supply current from Vcc,RAS only refresh mode (Note 3,5)	M5M417405D-5,5S	RAS cycling, CAS= VIH tRC=min. output open			145	mA
		M5M417405D-6,6S				120	
		M5M417405D-7,7S				105	
ICC4(AV)	Average supply current from Vcc EDO Mode (Note 3,4,5)	M5M417405D-5,5S	RAS=VIL, CAS cycling tHPC=min. output open			140	mA
		M5M417405D-6,6S				115	
		M5M417405D-7,7S				90	
ICC6(AV)	Average supply current from Vcc CAS before RAS refresh mode (Note 3,5)	M5M417405D-5,5S	CAS before RAS refresh cycling tRC=min. output open			145	mA
		M5M417405D-6,6S				120	
		M5M417405D-7,7S				105	

Note 2: Current flowing into an IC is positive, out is negative.

3: Icc1 (AV), Icc3(AV),Icc4(AV), and Icc6(AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

4: Icc1 (AV) and Icc4 (AV) are dependent on output loading. Specified values are obtained with the output open.

5: Under condition of column address is changed not more than once while RAS=VIL and CAS=VIH.

CAPACITANCE (Ta=0~ 70°C, Vcc = 5V±10%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
CI (A)	Input capacitance, address inputs	VI=Vss f=1MHz VI=25mVrms			5	pF
CI (CLK)	Input capacitance, clock inputs				7	pF
CI / O	Input/Output capacitance, data ports				7	pF

SWITCHING CHARACTERISTICS (Ta=0~70℃, Vcc = 5V±10%, Vss=0V, unless otherwise noted , see notes 6,14,15)

Symbol	Parameter		Limits						Unit
			M5M417405D-5,-5S		M5M417405D-6,-6S		M5M417405D-7,-7S		
			Min	Max	Min	Max	Min	Max	
tCAC	Access time from $\overline{CAS}$	(Note 7,8)		13		15		20	ns
tRAC	Access time from $\overline{RAS}$	(Note 7,9)		50		60		70	ns
tAA	Column address access time	(Note 7,10)		25		30		35	ns
tCPA	Access time from $\overline{CAS}$ precharge	(Note 7,11)		30		35		40	ns
tOEA	Access time from $\overline{OE}$	(Note 7)		13		15		20	ns
tOHC	Output hold time from $\overline{CAS}$ high	(Note 13)	5		5		5		ns
tOHR	Output hold time from $\overline{RAS}$ high	(Note 13)	5		5		5		ns
tCLZ	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		5		ns
tOEZ	Output disable time after $\overline{OE}$ high	(Note 12)		13		15		20	ns
tWEZ	Output disable time after $\overline{WE}$ low	(Note 12)		13		15		20	ns
tOFF	Output disable time after $\overline{CAS}$ high	(Note 12,13)		13		15		20	ns
tREZ	Output disable time after $\overline{RAS}$ high	(Note 12,13)		13		15		20	ns
tDOH	Output hold time from $\overline{CAS}$ low		5		5		5		ns

Note 6: An initial pause of 500μs is required after power-up followed by a minimum of eight initialization $\overline{RAS}$ cycles. The initialization cycles should be done either by $\overline{RAS}$-Only refresh cycles or by $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles only.
Note the $\overline{RAS}$ may be cycled during the initial pause . And any 8 $\overline{RAS}$ or $\overline{RAS}$/$\overline{CAS}$ cycles are required after prolonged periods (greater than 32 ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.
After the initialization cycles, $\overline{RAS}$ should be kept either higher than VIHmin or lower than VILmax except $\overline{RAS}$ transition time.

7: Measured with a load circuit equivalent to 100pF.
The reference levels for measuring of output signals are 2.0V(VOH) and 0.8V(VOL).

8: Assumes that $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$ and $t_{CP} \geq t_{CP(max)}$.

9: Assumes that $t_{RCD} \leq t_{RCD(max)}$ and $t_{RAD} \leq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RAD} exceeds the value shown.

10: Assumes that $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$.

11: Assumes that $t_{CP} \leq t_{CP(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.

12: $t_{OEZ\,(max)}$,$t_{WEZ(max)}$,$t_{OFF(max)}$ and $t_{REZ(max)}$defines the time at which the output achieves the high impedance state ($I_{OUT} \leq$ I ±10μA I) with no reference to $V_{OH(min)}$ or $V_{OL(max)}$.

13: Output is disabled after both RAS and $\overline{CAS}$ go to high.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write ,Refresh, and EDO Mode Cycles)

(Ta=0~70℃, Vcc = 5V±10%, Vss=0V, unless otherwise noted See notes 14,15)

Symbol	Parameter	Limits						Unit
		M5M417405D-5,-5S		M5M417405D-6,-6S		M5M417405D-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{REF}	Refresh cycle time		32		32		32	ms
t_{REF}*	Refresh cycle time		128		128		128	ms
t_{RP}	$\overline{RAS}$ high pulse width	30		40		50		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (Note16)	18	37	20	45	20	50	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		5		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		ns
t_{CPN}	$\overline{CAS}$ high pulse width	8		10		13		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low (Note17)	13	25	15	30	15	35	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low	0		0		0		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low (Note18)	0	10	0	13	0	13	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low	8		10		10		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low	8		10		10		ns
t_{DZC}	Delay time, data to $\overline{CAS}$ low (Note19)	0		0		0		ns
t_{DZO}	Delay time, data to $\overline{OE}$ low (Note19)	0		0		0		ns
t_{RDD}	Delay time, $\overline{RAS}$ high to data	13		15		20		ns
t_{CDD}	Delay time, $\overline{CAS}$ high to data	13		15		20		ns
t_{ODD}	Delay time, $\overline{OE}$ high to data	13		15		20		ns
t_{WED}	Delay time, $\overline{W}$ low to data	13		15		20		ns
t_T	Transition time (Note20)	1	50	1	50	1	50	ns

Note 14: The timing requirements are assumed t_T =2ns.

15: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.

16: $t_{RCD(max)}$ is specified as a reference value only to guarantee the valid operation. If t_{RCD} is less than $t_{RCD(max)}$,,access time is controled by t_{RAC}. If t_{RCD} is greater than $t_{RCD(max)}$, access time is controlled by t_{CAC} or t_{AA}.

17: $t_{RAD(max)}$ is specified as a reference value only to guarantee the valid operation. If $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$, access time is controlled by tAA.

18: $t_{ASC(max)}$ is specified as a reference value only to guarantee the valid operation. If $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$, access time is controlled exclusively by t_{CAC}.

19: Either t_{DZC} or t_{DZO} must be satisfied.

20: t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

Read and Refresh Cycles

Symbol	Parameter	Limits						Unit
		M5M417405D-5,-5S		M5M417405D-6,-6S		M5M417405D-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read cycle time	90		110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width	50	10000	60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	8	10000	10	10000	13	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	40		48		55		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	13		15		20		ns
t_{RCS}	Read Setup time before $\overline{CAS}$ low	0		0		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (Note 21)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (Note 21)	0		0		0		ns
t_{RAL}	Column address to $\overline{RAS}$ hold time	25		30		35		ns
t_{CAL}	Column address to $\overline{CAS}$ hold time	15		18		20		ns
t_{ORH}	$\overline{RAS}$ hold time after $\overline{OE}$ low	13		15		20		ns
t_{OCH}	$\overline{CAS}$ hold time after $\overline{OE}$ low	13		15		20		ns

Note 21: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits						Unit
		M5M417405D-5,-5S		M5M417405D-6,-6S		M5M417405D-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write cycle time	90		110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width	50	10000	60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	8	10000	10	10000	13	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	40		48		55		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	13		15		20		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low (Note 23)	0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	8		10		13		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low	8		10		13		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low	8		10		13		ns
t_{WP}	Write pulse width	8		10		13		ns
t_{DS}	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low	0		0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low	8		10		13		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits						Unit
		M5M417405D-5,-5S		M5M417405D-6,-6S		M5M417405D-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{RWC}	Read write/read modify write cycle time (Note22)	109		133		161		ns
t_{RAS}	$\overline{RAS}$ low pulse width	75	10000	89	10000	107	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	38	10000	44	10000	57	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	70		82		99		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	38		44		57		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Note23)	28		32		42		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Note23)	65		77		92		ns
t_{AWD}	Delay time, address to $\overline{W}$ low (Note23)	40		47		57		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low	13		15		20		ns

Note 22: t_{RWC} is defined as $t_{RWC(min)}=t_{RAC(max)}+t_{ODD(min)}+t_{RWL(min)}+t_{RP(min)}+4t_T$.

23: t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and, t_{CPWD} are specified as reference values only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD(min)}$, $t_{RWD} \geq t_{RWD(min)}$, $t_{AWD} \geq t_{AWD(min)}$ and $t_{CPWD} \geq t_{CPWD(min)}$ (for EDO mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. Under conditions other than those specified above (for delayed write) of the DQ output (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is invalid.

EDO Mode Cycle (Read, Early Write, Read-Write, Read-Modify-Write Cycle, , Read Write Mix Cycle, Hi-Z control by $\overline{OE}$ or $\overline{W}$) (Note 24)

Symbol	Parameter	Limits						Unit
		M5M417405D-5,-5S		M5M417405D-6,-6S		M5M417405D-7,-7S		
		Min	Max	Min	Max	Min	Max	
tHPC	EDO mode read/write cycle time (Note25)	20		25		30		ns
tHPRWC	EDO Mode read write / read modify write cycle time	57		66		79		ns
tRAS	$\overline{RAS}$ low pulse width for read or write cycle (Note26)	65	100000	77	100000	92	100000	ns
tCP	$\overline{CAS}$ high pulse width (Note27)	8	13	10	16	13	16	ns
tCPRH	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	28		33		38		ns
tCPWD	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note23)	43		50		60		ns
tCHOL	Hold time to maintain the data Hi-Z until CAS access	7		7		7		ns
tOEPE	$\overline{OE}$ Pulse Width (Hi-Z control)	7		7		7		ns
tWPE	$\overline{W}$ Pulse Width (Hi-Z control)	7		7		7		ns
tHCWD	Delay time, $\overline{CAS}$ low to $\overline{W}$ low after read	28		32		42		ns
tHAWD	Delay time, Address to $\overline{W}$ low after read	40		47		57		ns
tHPWD	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low after read	43		50		60		ns
tHCOD	Delay time, $\overline{CAS}$ low to $\overline{OE}$ high after read	13		15		20		ns
tHAOD	Delay time, Address to $\overline{OE}$ high after read	25		30		35		ns
tHPOD	Delay time, $\overline{CAS}$ precharge to $\overline{OE}$ high after read	28		33		38		ns

Note 24: For those timing requirements which are not listed above parameters of regular cycles are applicable.
25: tHPC(min) is specified in the case of read-only and early write-only in EDO Mode.
26: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed. It is defined as tRAS(min)=tCS(min)+tPC(min)
27: $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 28)

Symbol	Parameter	Limits						Unit
		M5M417405D-5,-5S		M5M417405D-6,-6S		M5M417405D-7,-7S		
		Min	Max	Min	Max	Min	Max	
tCSR	$\overline{CAS}$ setup time before $\overline{RAS}$ low	5		5		5		ns
tCHR	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		10		15		ns
tCAS	$\overline{CAS}$ low pulse width	17		17		22		ns
tRSR	Read setup time before $\overline{RAS}$ low	5		5		5		ns
tRHR	Read hold time after $\overline{RAS}$ low	10		10		15		ns

Note 28 : Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Hidden Refresh Cycle (Note 30)

Symbol	Parameter	Limits						Unit
		M5M417405D-5,-5S		M5M417405D-6,-6S		M5M417405D-7,-7S		
		Min	Max	Min	Max	Min	Max	
tRSR	Read setup time before $\overline{RAS}$ low	5		5		5		ns
tRHR	Read hold time after $\overline{RAS}$ low	10		10		15		ns

Note 30: Read early write, delayed write, read write or read-modify-write cycle is applicable to hidden refresh cycle. In all cases tRSR and tRHR should be satisfied.

SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -5S / -6S / -7S. The other characteristics and requirements than the below are same as normal devices.

ELECTRICAL CHARACTERISTICS (Ta=0 ~70 °C, Vcc=5V±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
$I_{CC8\ (AV)}$	Average supply current from Vcc Slow - Refresh cycle (note 6)	M5M417405D (S)	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling ,or, $\overline{RAS}$ cycling & $\overline{CAS} \le 0.2V$ $\overline{OE}$&$\overline{W} \le 0.2V$,or, $\overline{OE}$&$\overline{W} \ge Vcc-0.2V$ A0~A10 ≥ 0.2V ,or, A0 ~ A10 ≥ Vcc-0.2V tREF=128mS (2048cycles) output = OPEN tRAS=tRASmin. ~1µS			500	µA
$I_{CC9\ (AV)}$*	Average supply current from Vcc Self - Refresh cycle (note 6)	M5M417405D (S)	$\overline{RAS}$ = $\overline{CAS} \le 0.2V$ output = OPEN			200	µA

TIMING REQUIREMENTS (Ta=0 ~ 70℃ , Vcc=5V±10%, Vss=0V, unless otherwise noted) (Notes 14,15)

Symbol	Parameter	Limits						Unit
		M5M417405D-5S		M5M417405D-6S		M5M417405D-7S		
		Min	Max	Min	Max	Min	Max	
t_{RASS}	Self Refresh $\overline{RAS}$ low pulse width	100		100		100		µs
t_{RPS}	Self Refresh $\overline{RAS}$ high precharge time	90		110		130		ns
t_{CHS}	Self Refresh $\overline{RAS}$ hold time	- 50		- 50		- 50		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		10		15		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

(1) In the case of distributed refresh

The last / first full refresh cycles (2K) must be made within tNS / tSN before / after self refresh , on the condition that tNS ≤ 32 ms and tSN ≤ 32 ms.

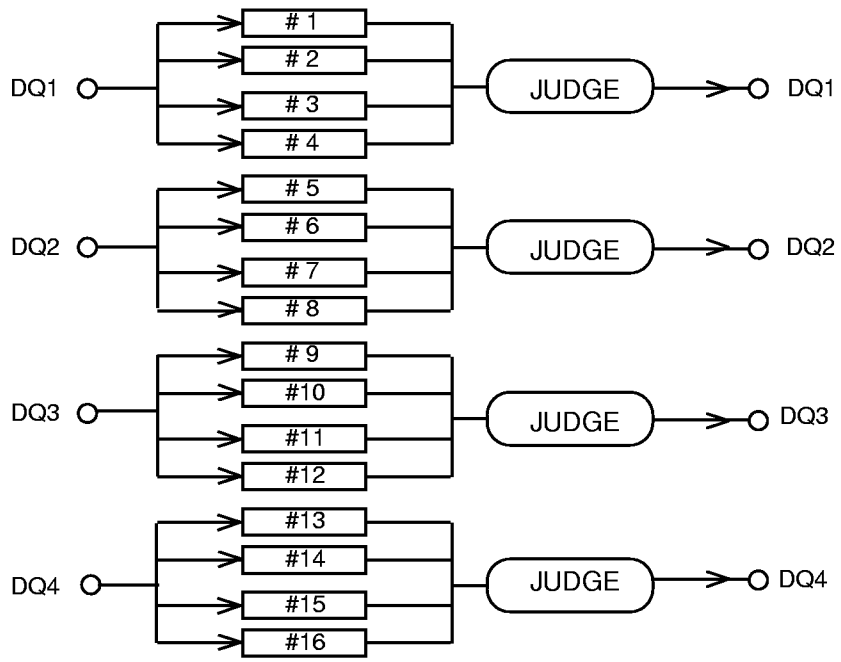
(2) In the case of burst refresh

The last / first full refresh cycles (2K) must be made within tNS / tSN before / after self refresh , on the condition that tNS + tSN ≤ 32 ms.

TEST Mode SET Cycle (Note 31)

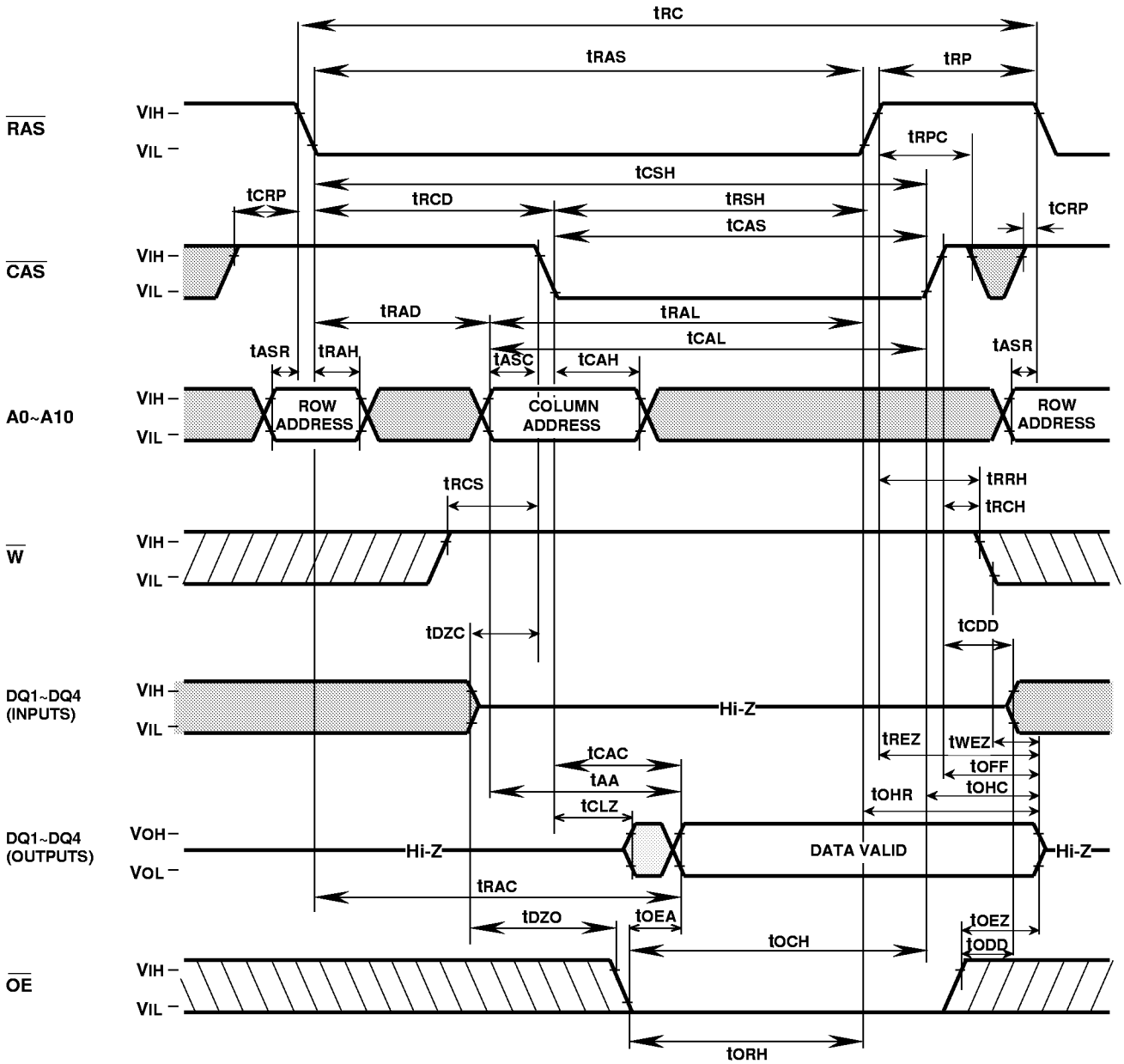
Symbol	Parameter	Limits						Unit
		M5M417405D-5,-5S		M5M417405D-6,-6S		M5M417405D-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{WSR}	$\overline{W}$ setup time before $\overline{RAS}$ low	10		10		10		ns
t_{WHR}	$\overline{W}$ hold time after $\overline{RAS}$ low	10		10		15		ns

Note 31 : The test mode function is initiated by a $\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ cycle (WCBR cycle) as specified in timing diagram.
The test mode function is terminated by either a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (CBR refresh cycle) or a $\overline{RAS}$ only refresh cycle.
During the test mode, the device is internally organized as 16 bits wide (1M bytes depth) . Addresses of CA0 ,CA1 is not required.
During a write cycle, data must be applied to all DQ (input) pins. The data can be different between DQ pins. The data on each DQ pin is written into 4 bits memory cells, respectively. During a read cycle, each DQ (output) pin shows the test result of the 4 bits, respectively. High state indicates that they are same. These high and low outputs are used to determine Pass and Fail respectively.
During the test mode operation, only WCBR cycle can be used to perform refresh.



Timing Diagrams (Note 29)

Read Cycle

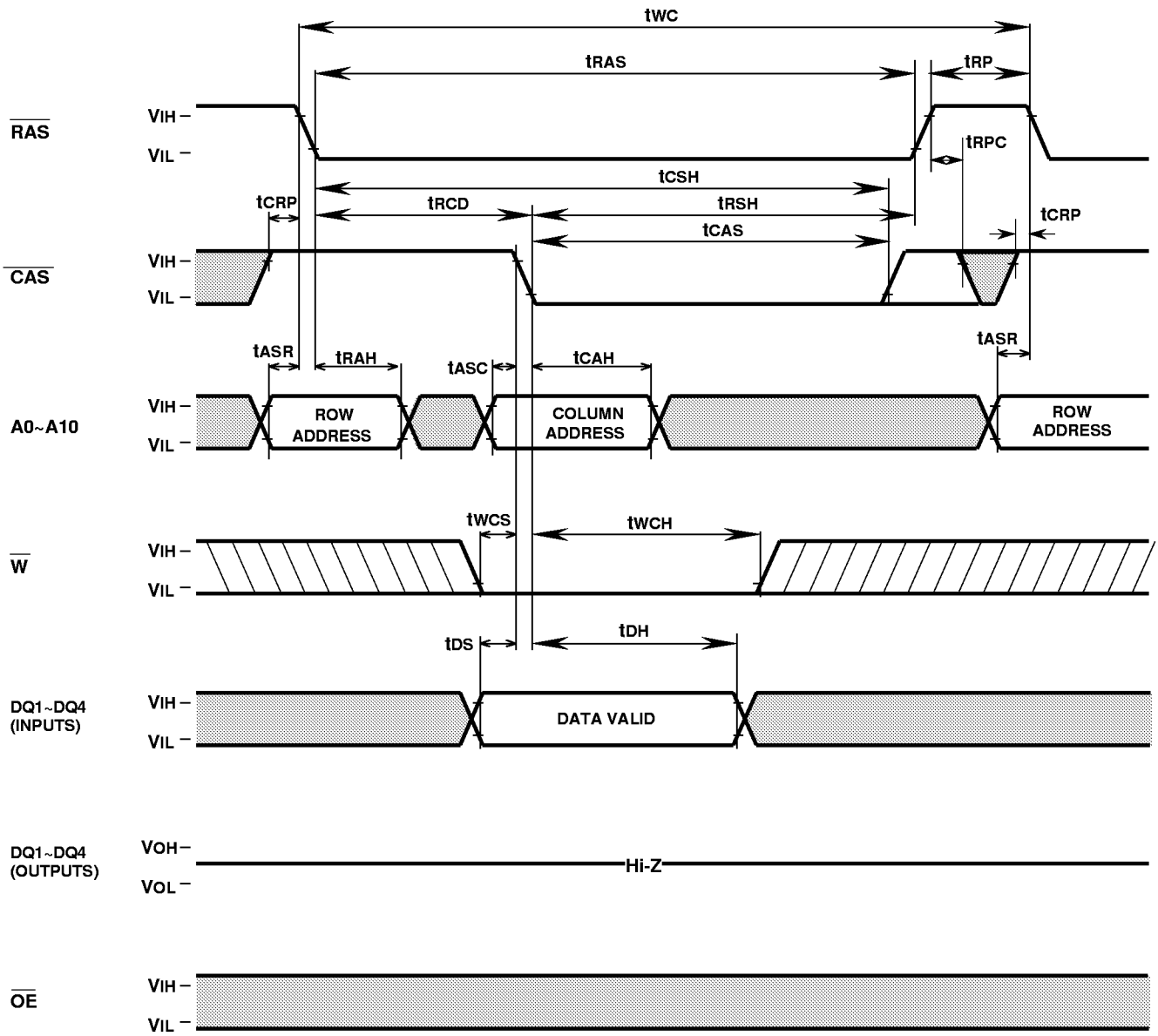


Note 29

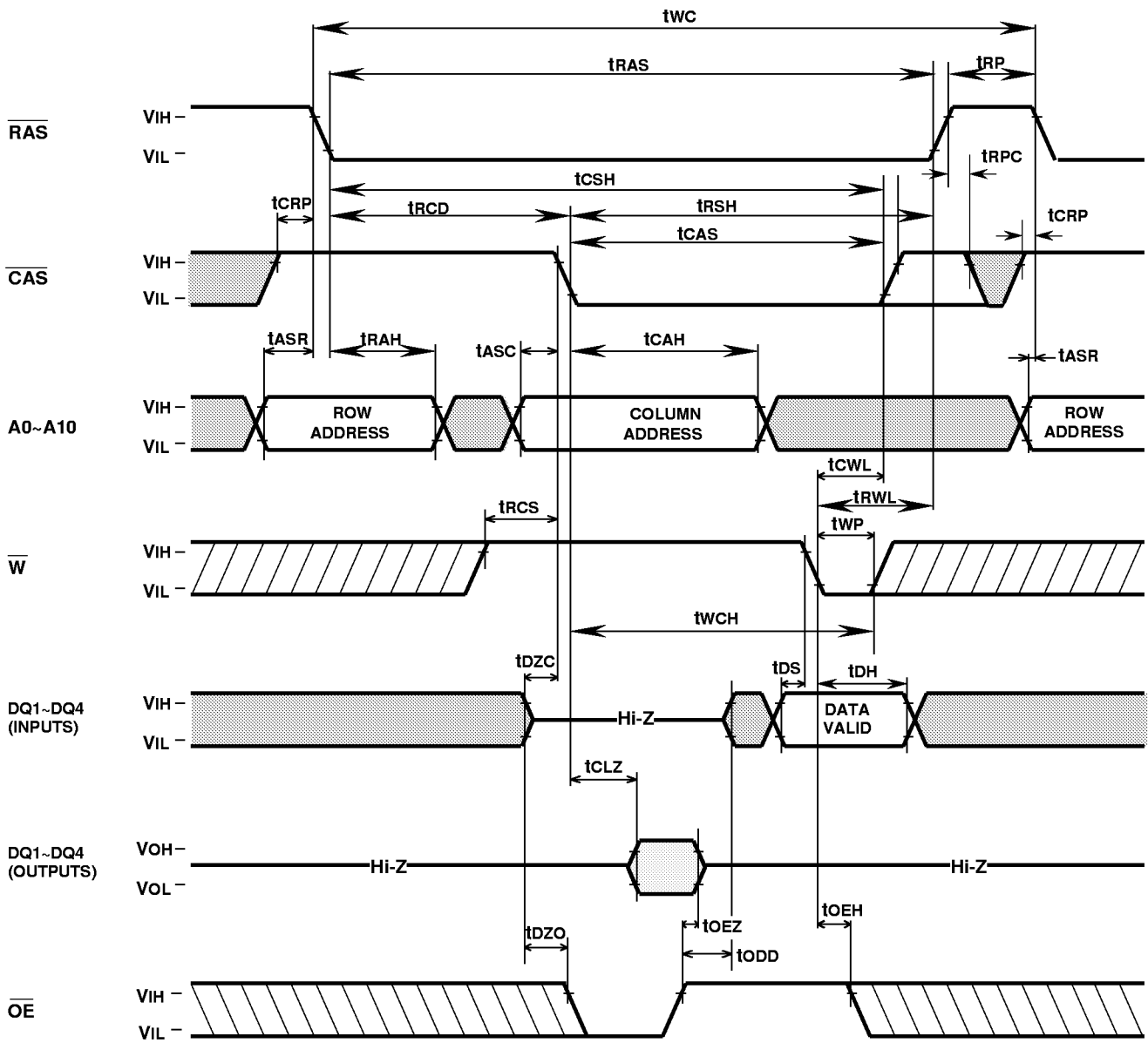
Indicates the don't care input.
VIH(min)≤VIN≤VIH(max) or VIL(min)≤VIN≤VIL(max)

Indicates the invalid output.

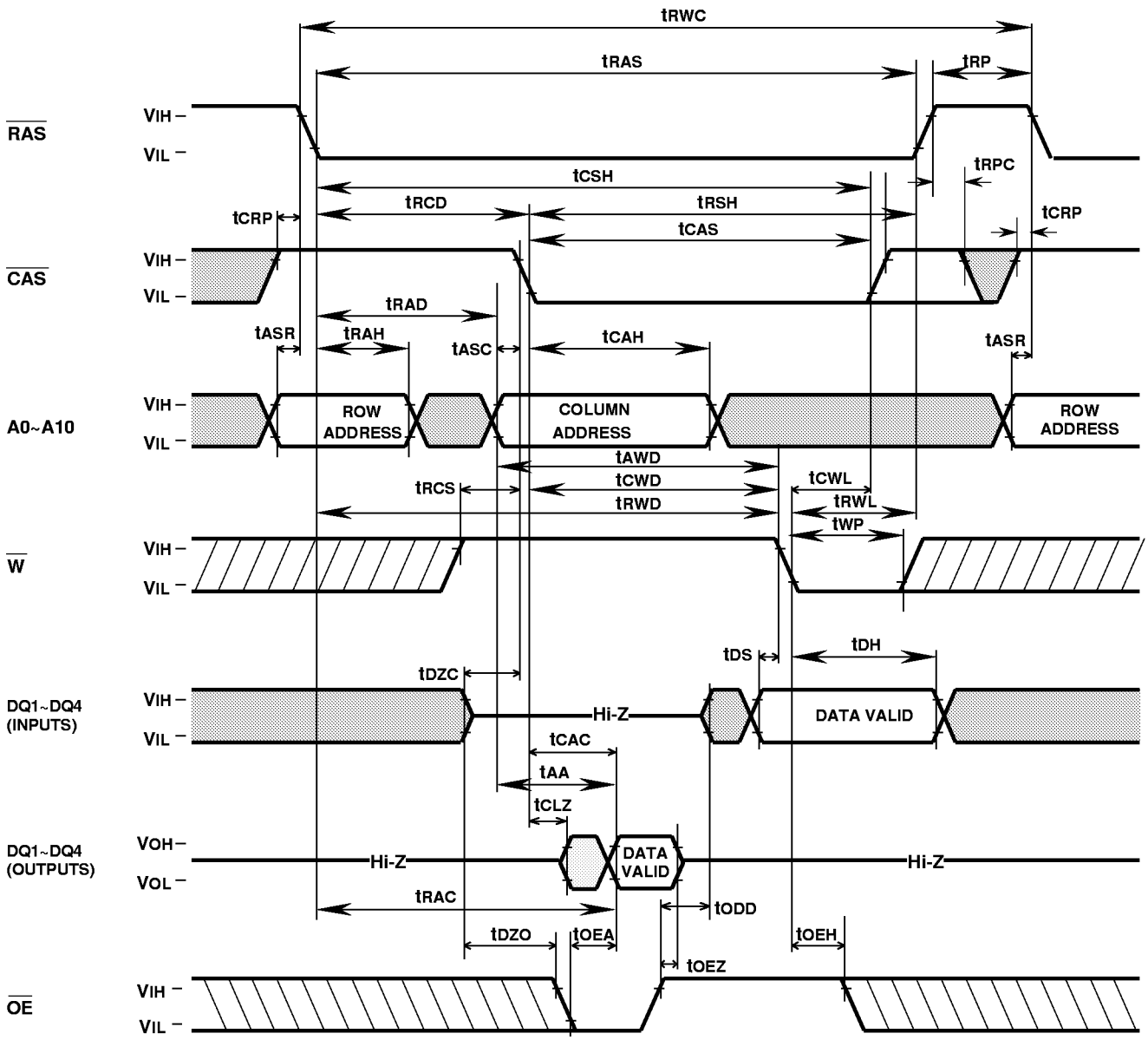
Early Write Cycle



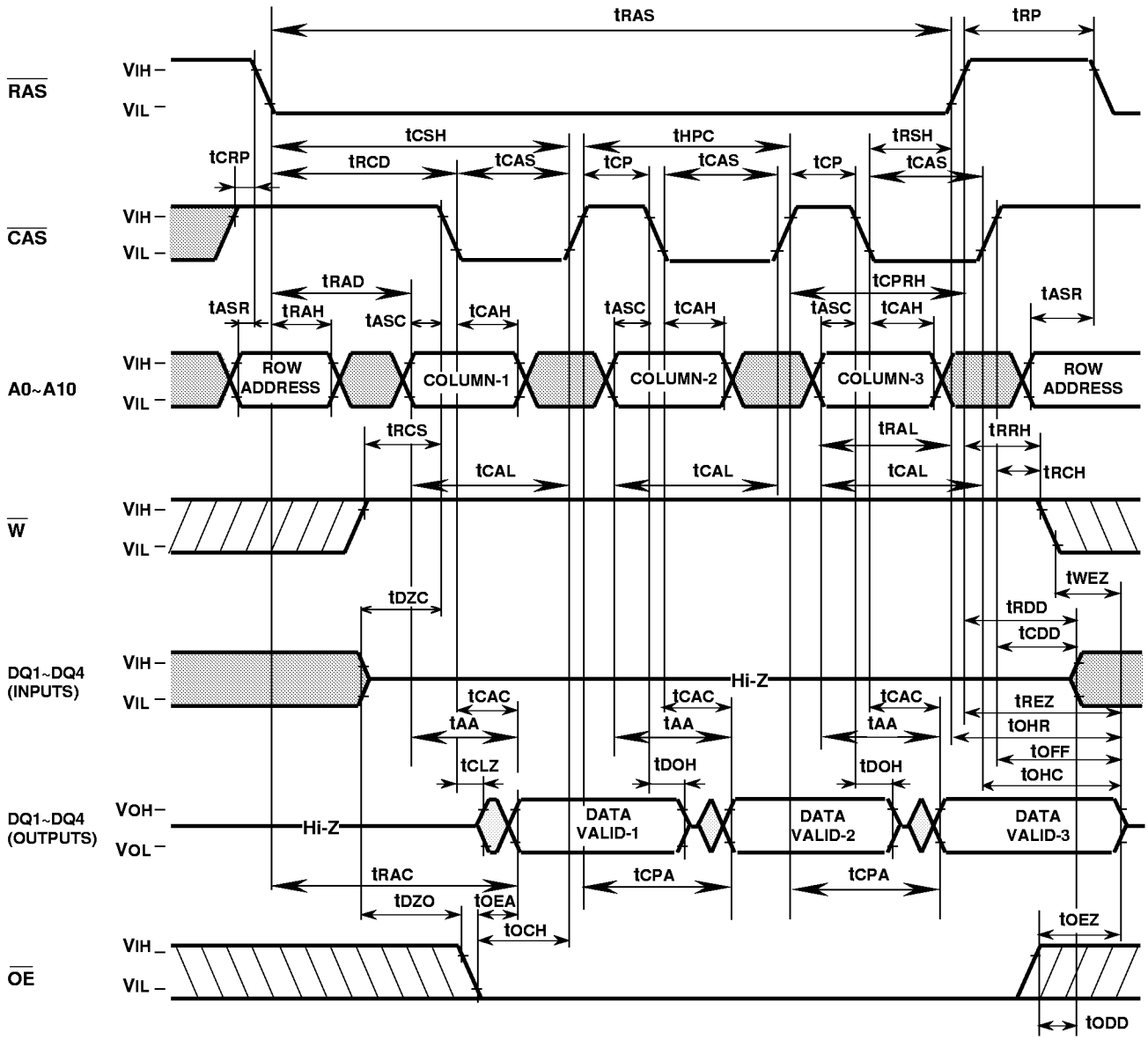
Delayed Write Cycle



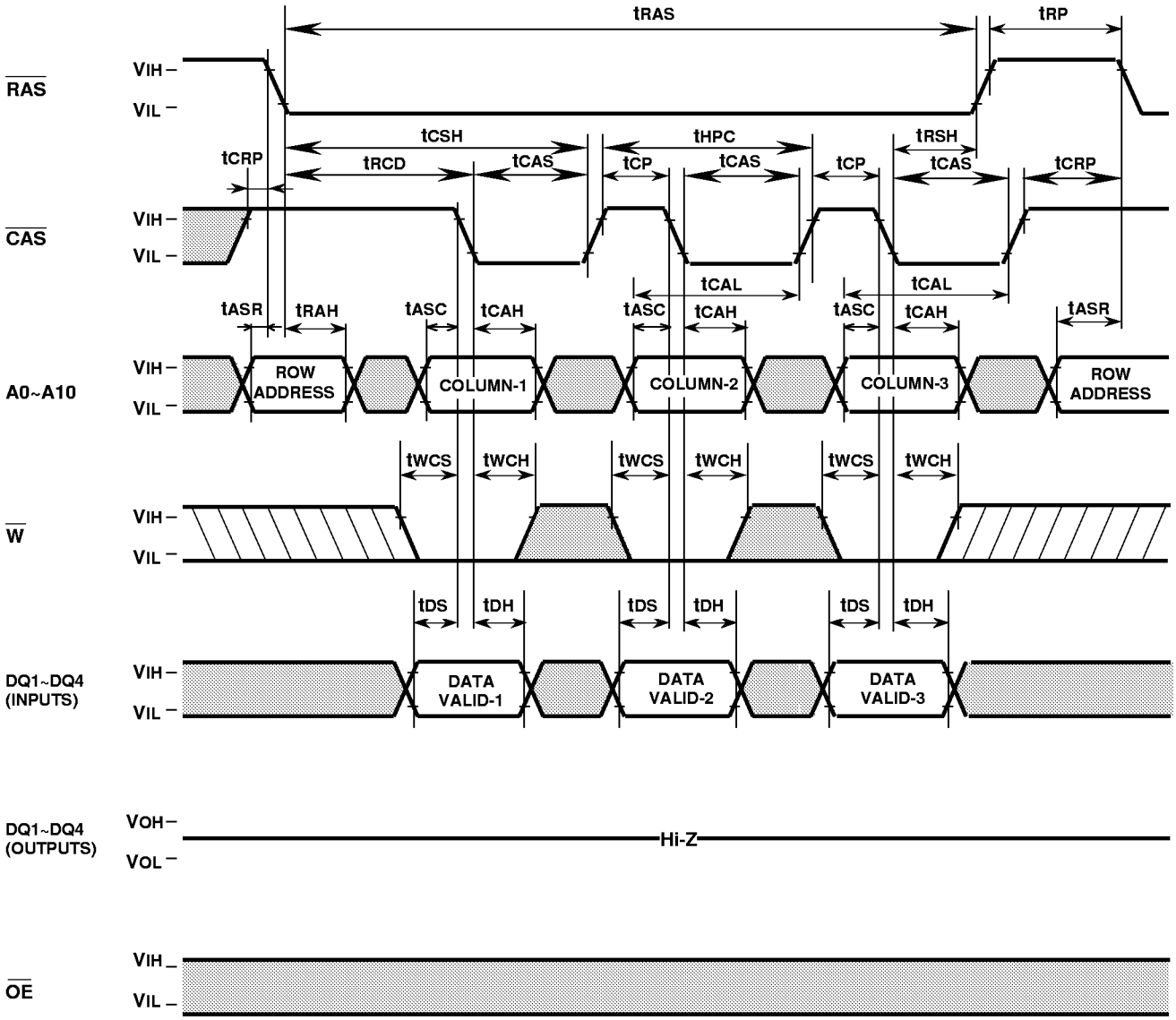
Read-Write, Read-Modify-Write Cycle



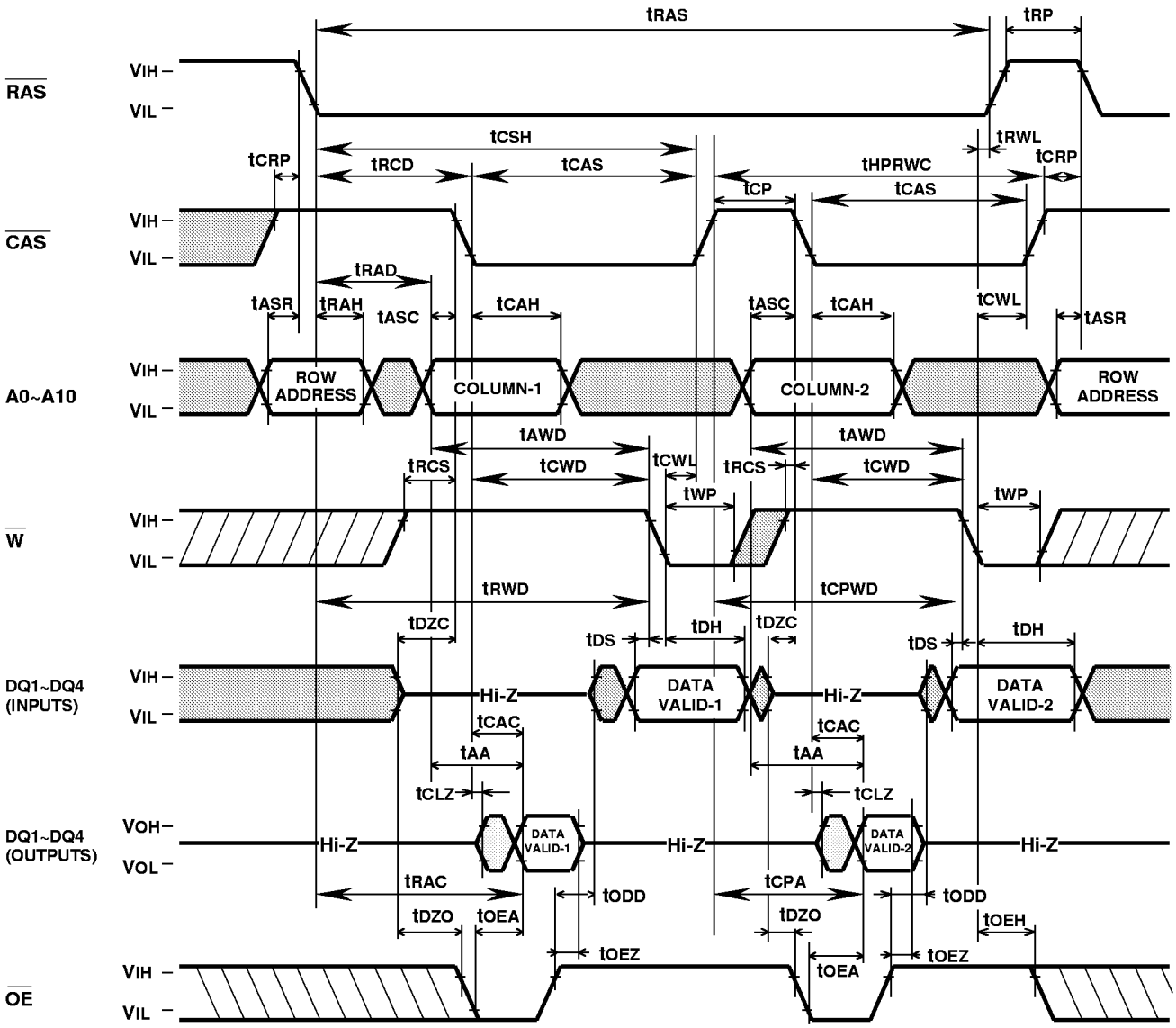
EDO Mode Read Cycle



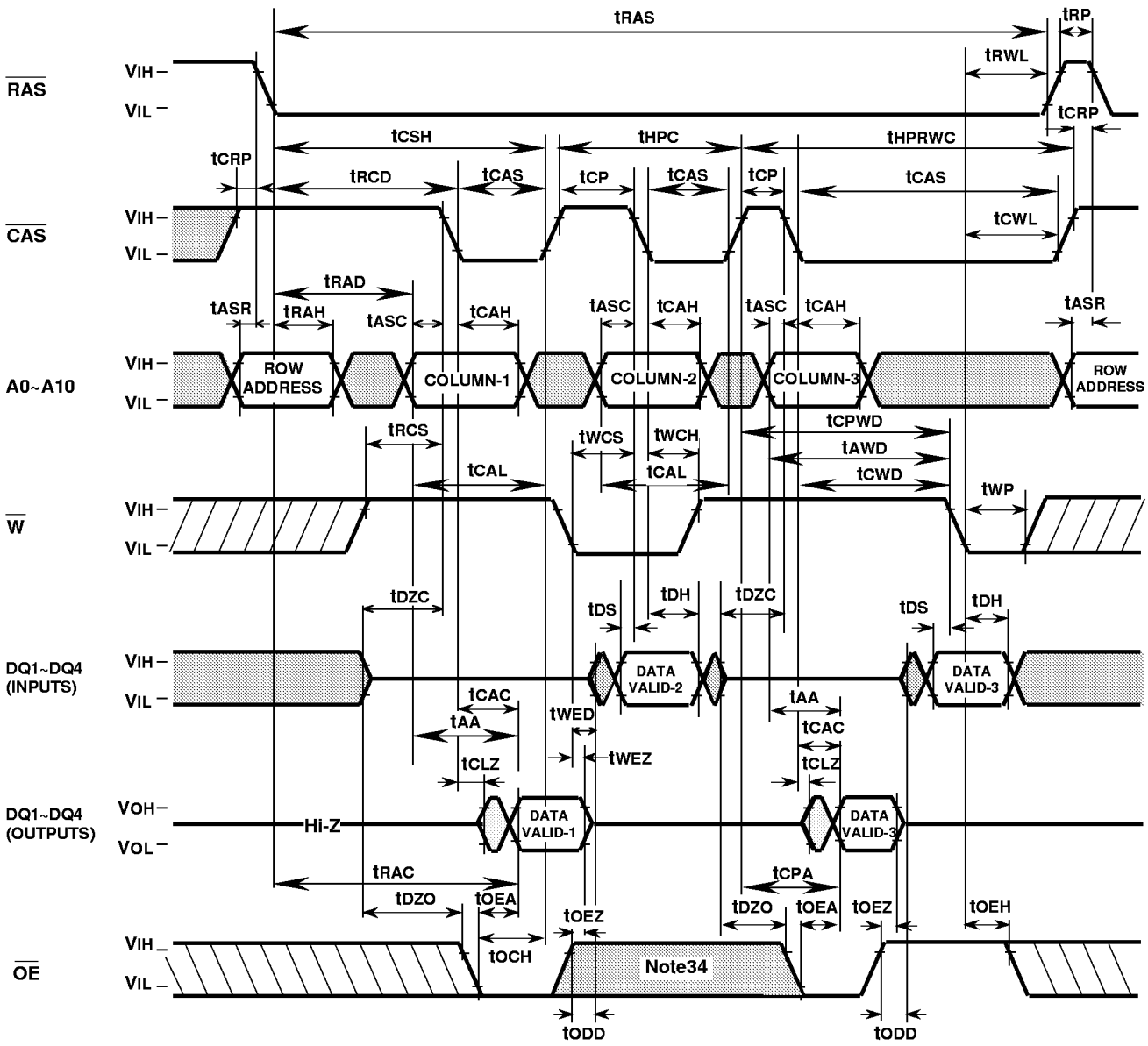
EDO Mode Early Write Cycle



EDO Mode Read-Write,Read-Modify-Write Cycle



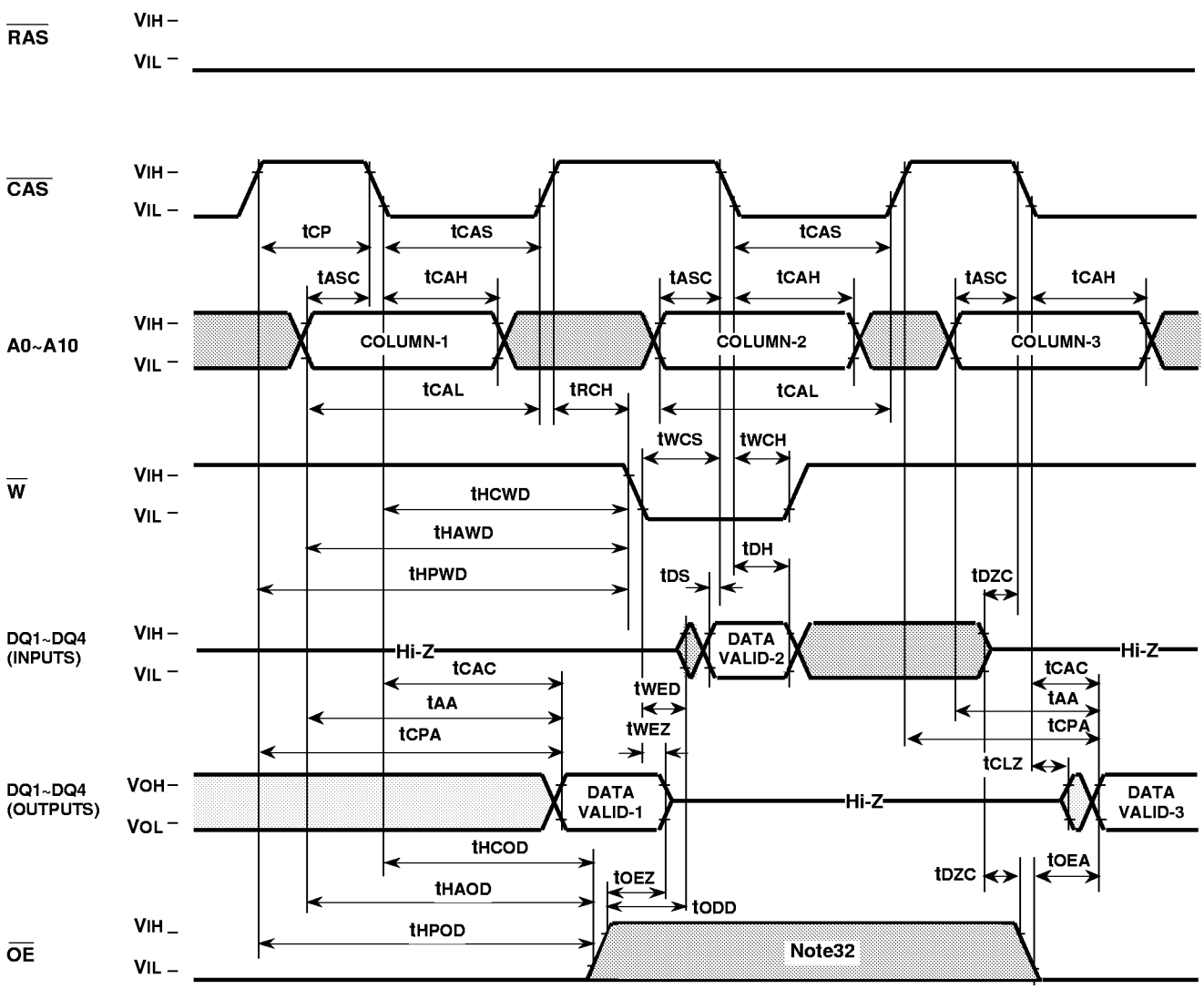
EDO Mode Mix Cycle (1) (Note32)



Note 32 : $\overline{OE}$ low ; Hi-Z control by $\overline{W}$

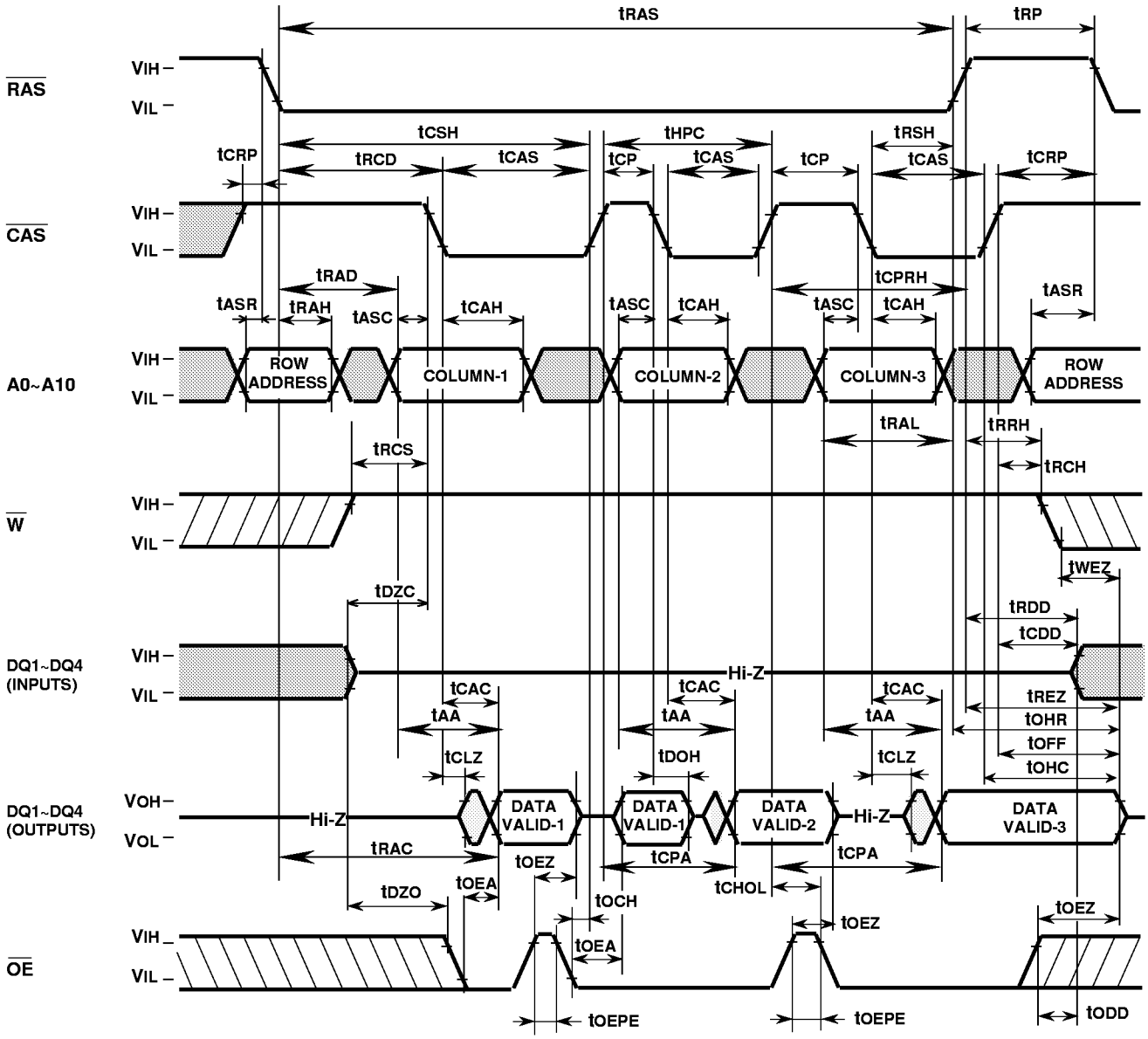
$\overline{OE}$ high ; Hi-Z control by $\overline{OE}$

EDO Mode Mix Cycle (2) (Note32)

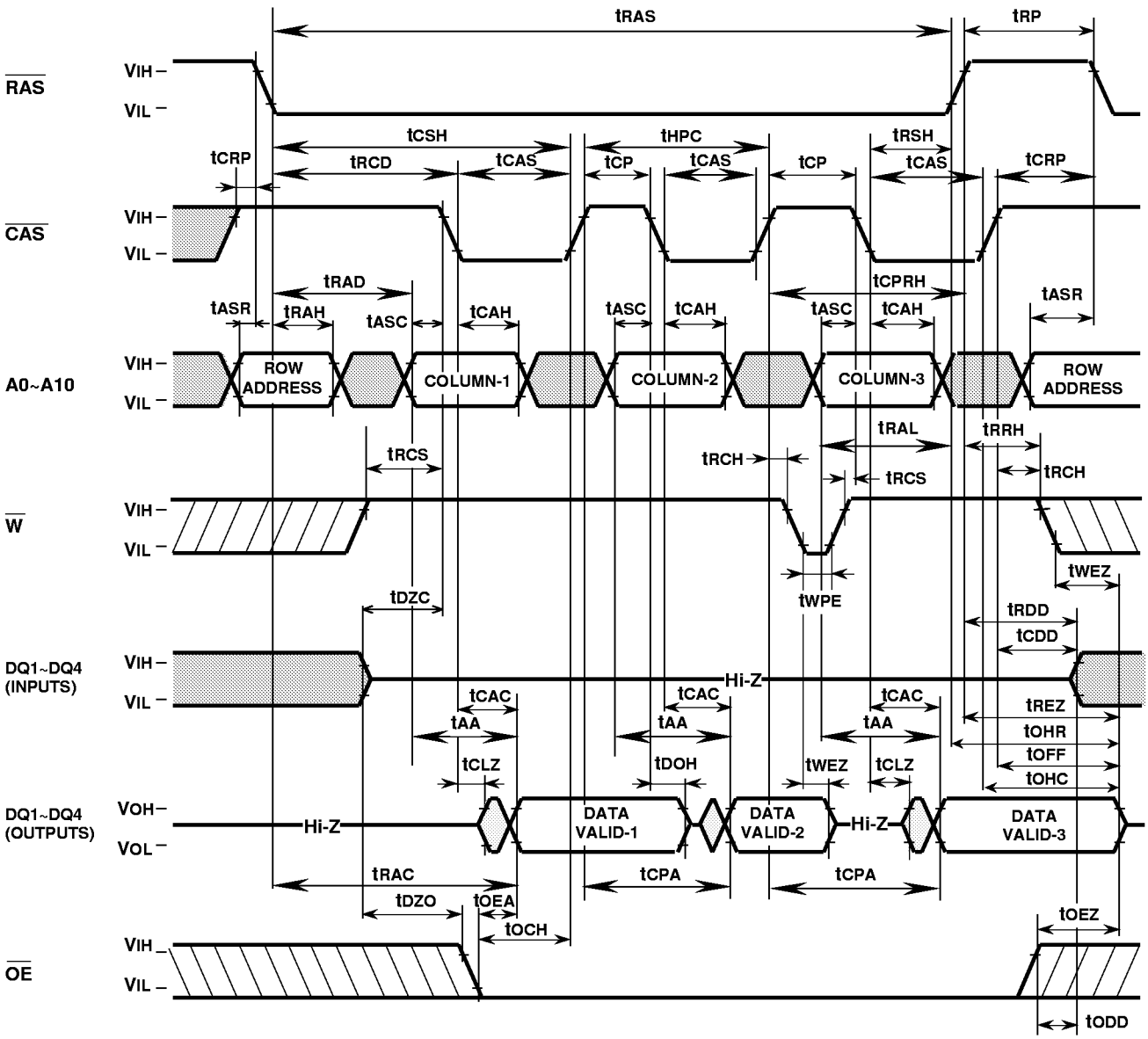


Note 32 : $\overline{OE}$ low ; Hi-Z control by $\overline{W}$
$\overline{OE}$ high ; Hi-Z control by $\overline{OE}$

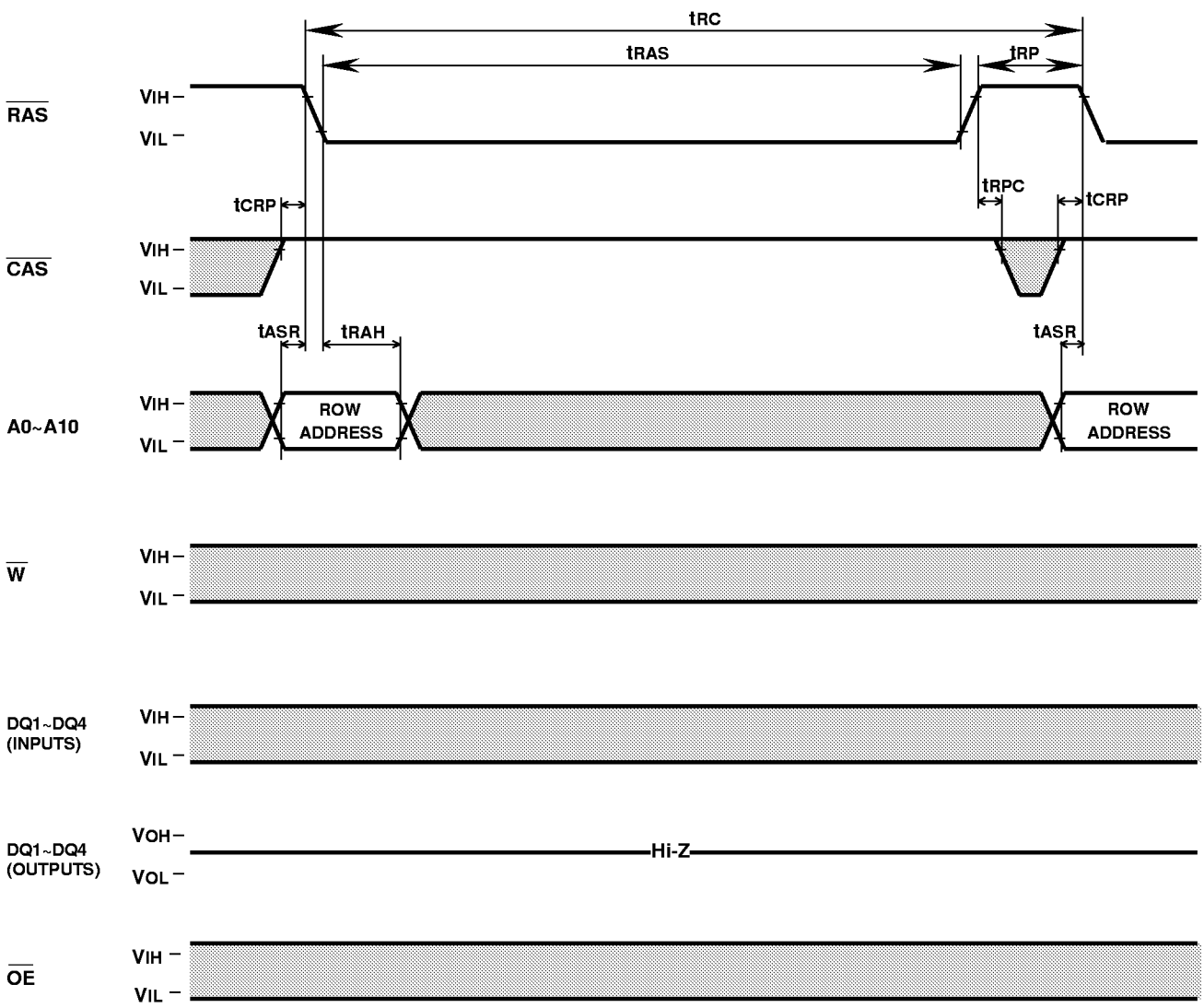
EDO Mode Read Cycle (Hi-Z control by $\overline{OE}$)



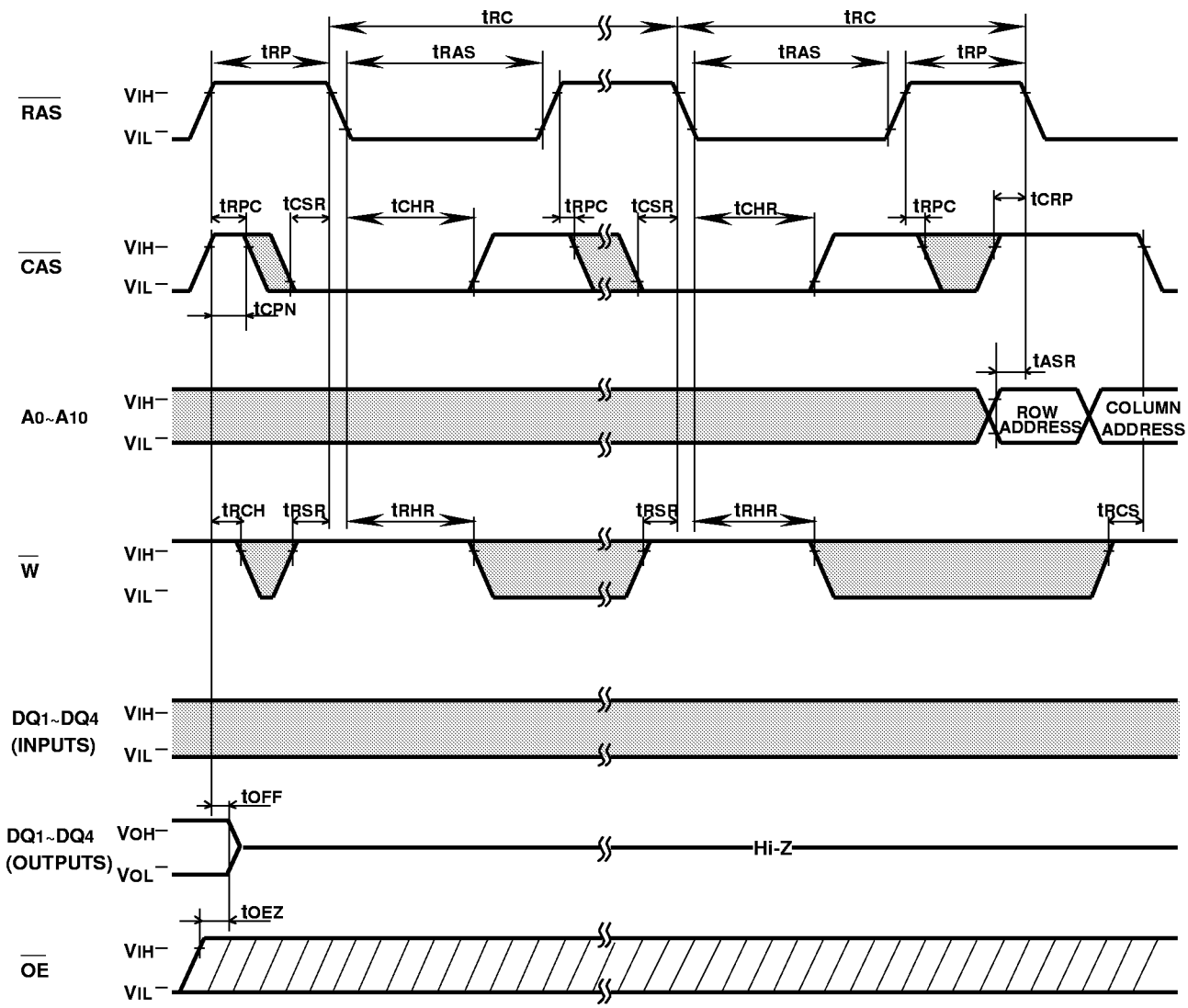
EDO Mode Read Cycle (Hi-Z control by $\overline{W}$)



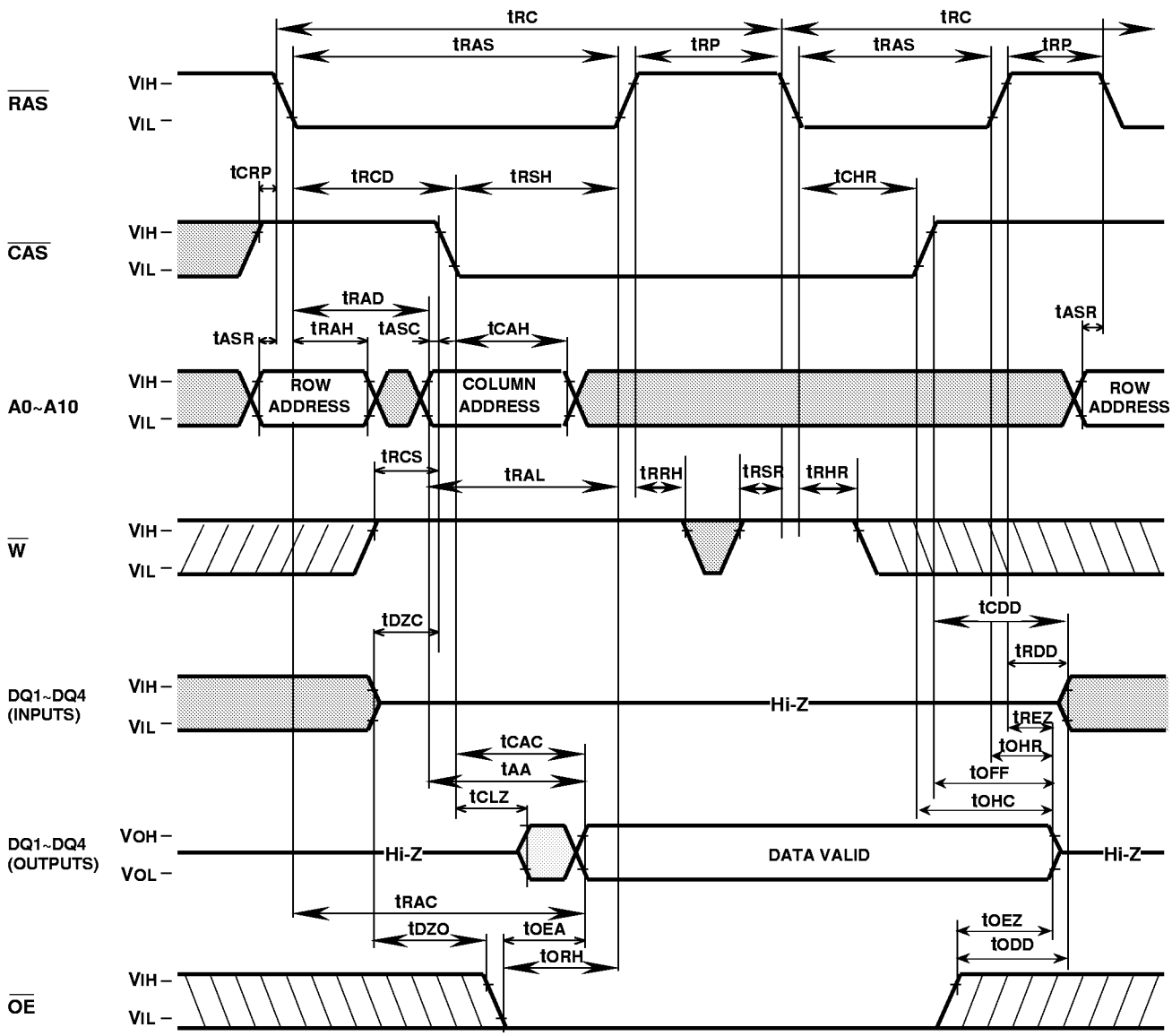
$\overline{RAS}$-only Refresh Cycle



$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle

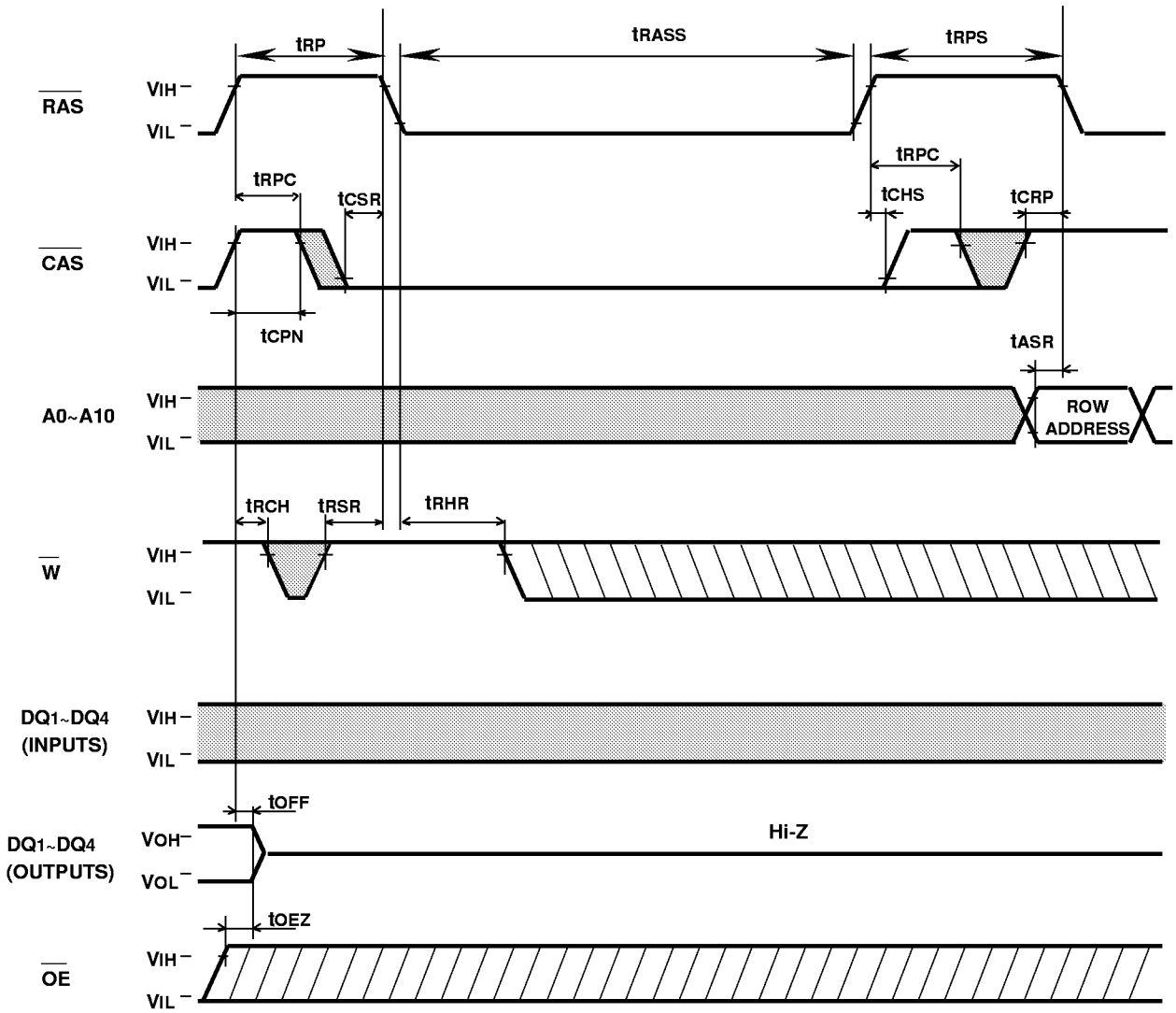


Hidden Refresh Cycle (Read) (Note 30)

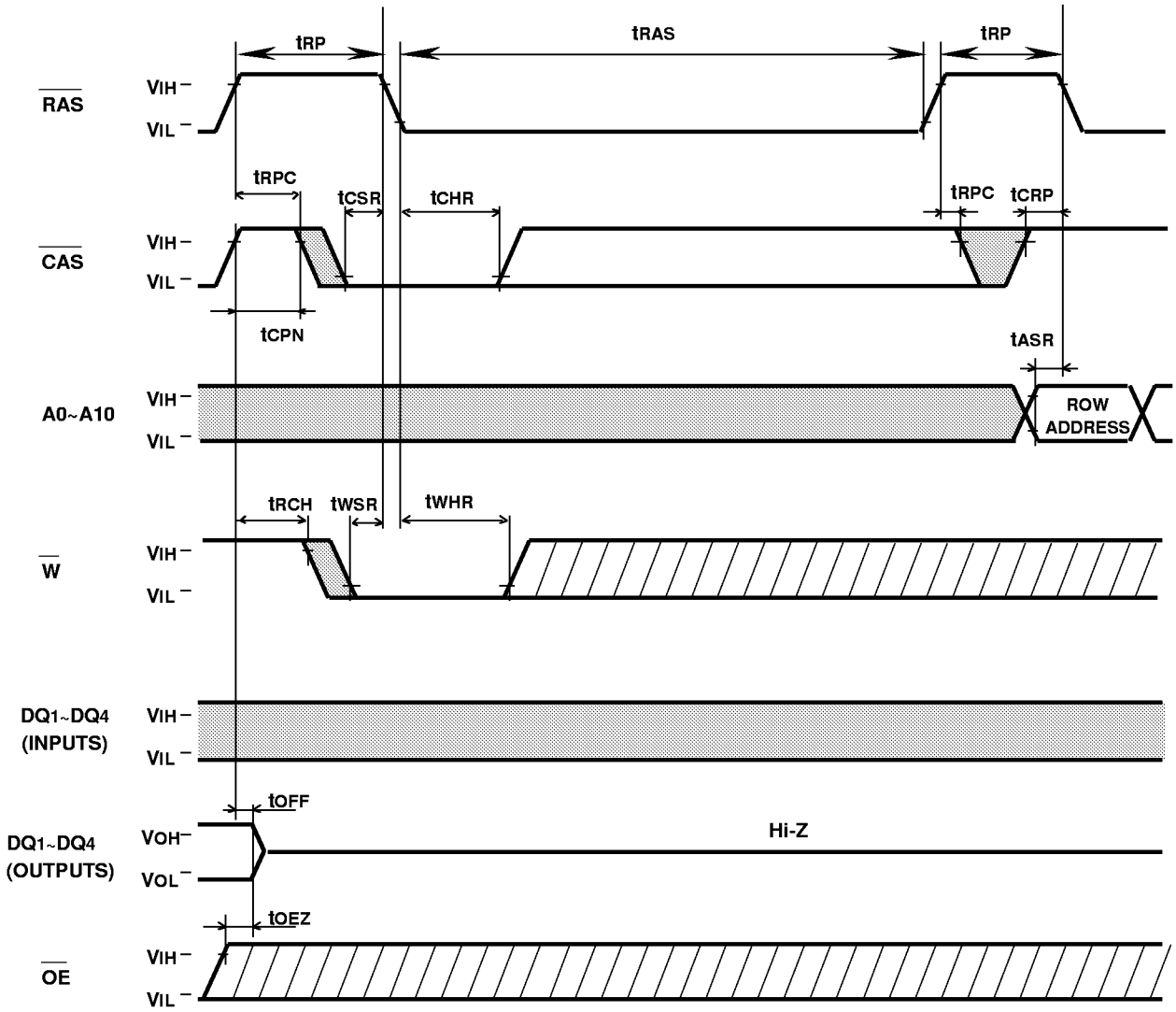


Note 30: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.
In all cases t_{RSR} and t_{RHR} should be satisfied.

Self Refresh Cycle, Slow Refresh Cycle



TEST Mode SET Cycle (Note31)



Note 31 : This cycle can be used for initialized cycle after power-up , however entried into Test Mode.