STEL-1179

Data Sheet

STEL-1179

24-Bit Resolution CMOS Numerically Controlled Oscillator

intel

FEATURES

- **HIGH FREQUENCY RESOLUTION**
  - **24-BITS, 1.5 Hz @ 25 MHz**
- **WIDE OUTPUT BANDWIDTH**
  - **0 TO 10 MHz @ 25 MHz CLOCK**
- **SINE SIGNAL GENERATION**
  - **12-BIT OUTPUTS**
- **HIGH SPECTRAL PURITY**
  - **ALL SPURS < –75dBc (AT DIGITAL OUTPUTS)**
- **25 MHz MAXIMUM CLOCK FREQUENCY OVER FULL INDUSTRIALIAL TEMPERATURE RANGE**
- **3-BIT PARALLEL PHASE MODULATION**
- **SERIAL FREQUENCY CONTROL INPUT**
- **LOW POWER DISSIPATION**
- **FAST FREQUENCY UPDATE RATE**
- **5 CLOCK CYCLE LATENCY**
- **28-PIN PLCC PACKAGE**

TYPICAL APPLICATIONS

- **FREQUENCY SYNTHESIZERS**
- **PSK MODULATORS**
- **DIGITAL SIGNAL PROCESSORS**
- **FAST HOPPED FREQUENCY SOURCES**

FUNCTIONAL DESCRIPTION

The STEL-1179 Modulated Numerically Controlled Oscillator (MNCO) uses digital techniques to provide a compact, cost-effective solution for low noise signal sources. The NCO features 24-bit frequency resolution with frequency update rates up to 50% of the clock frequency and high spectral purity of outputs up to 10 MHz. The STEL-1179 also features 3-bit phase modulation at rates up to 100% of the clock frequency. The device combines low power 1.5µ CMOS technology with a unique architectural design resulting in a power efficient, high-speed sinusoidal waveform generator able to achieve fine tuning resolution and high spectral purity at clock frequencies up to 25 MHz. The NCO is designed to provide a simple serial interface, with the data written with a separate asynchronous clock. The pipeline delay associated with the NCO is only 5 clock cycles.

The NCO maintains a record of phase which is accurate to 24 bits. At each clock cycle, the number stored in the 24-bit Δ-Phase register is added to the previous value of the phase accumulator. The number in the phase accumulator represents the current phase of the synthesized sine function. The number in the Δ-Phase register represents the phase change for each cycle of the clock. This number is directly related to the output frequency by the following:

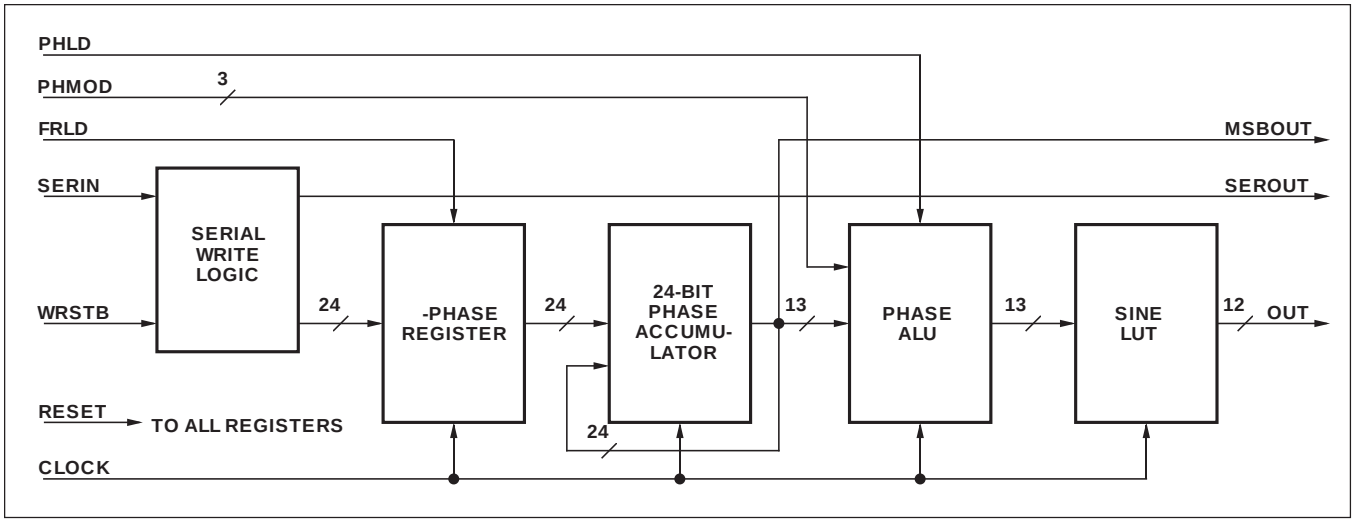
$$f_o = \frac{f_c \times \Delta\text{-Phase}}{2^{24}}$$

where: f_o is the frequency of the output signal

and: f_c is the clock frequency.

The sine function is generated from the 13 most

BLOCK DIAGRAM



significant bits of the phase accumulator. The frequency of the NCO is determined by the number stored in the Δ-Phase Register, which is programmed via the serial interface.

The NCO generates a sampled sine wave where the sampling function is the clock. The practical upper limit of the NCO output frequency is about 40% of the clock frequency due to spurious components that are created by sampling. Those components are at frequencies greater than half the clock frequency, and can be removed by means of a low-pass filter.

The phase noise of the NCO output signal may be determined from the phase noise of the clock signal input and the ratio of the output frequency to the clock frequency. This ratio squared times the phase noise power of the clock specified in a given bandwidth is the phase noise power that may be expected in that same bandwidth relative to the output frequency.

FUNCTION BLOCK DESCRIPTION

SERIAL WRITE LOGIC BLOCK

This block controls the writing of data into the device via the **SERIN** input. One bit of data is written at each cycle of the **WRSTB** input, as shown in the timing diagram. The data is written into a serial-in parallel-out buffer. As new data is written into this register the previous contents appear at the **SEROUT** output pin.

Δ-PHASE REGISTER BLOCK

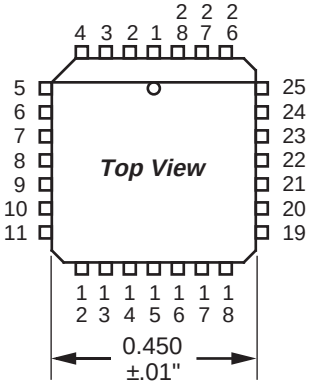
This block controls the updating of the Δ-Phase word used in the Phase Accumulator. The frequency data stored in the Serial Write Logic Block is loaded into this block on the rising edge of **CLOCK** following a falling edge on the **FRLD** input.

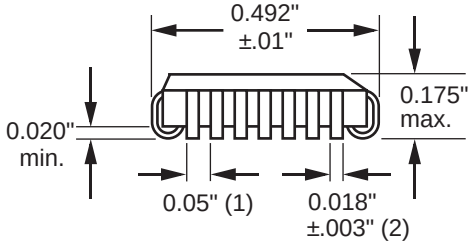
PHASE ACCUMULATOR BLOCK

This block forms the core of the NCO function. It is a high-speed 24-bit parallel accumulator, generating a new sum in every clock cycle. The MSB of the accumulator is brought out as the **MSBOUT** signal.

PIN CONFIGURATION

Package: 28 pin PLCC
Thermal coefficient, θ_{ja} = 45° / W





PIN CONNECTIONS

1	V_{SS}	8	$PHMOD_0$	15	OUT_{11}	22	OUT_5
2	CLOCK	9	$PHMOD_1$	16	OUT_{10}	23	OUT_4
3	WRSTB	10	$PHMOD_2$	17	OUT_9	24	OUT_3
4	RESET	11	V_{DD}	18	V_{SS}	25	V_{DD}
5	SERIN	12	I.C.	19	OUT_8	26	OUT_2
6	FRLD	13	SEROUT	20	OUT_7	27	OUT_1
7	PHLD	14	MSBOUT	21	OUT_6	28	$OUT_{0(LSB)}$

Notes: 1. I.C. denotes Internal Connection. ThIs pin must be left unconnected. Do not use for a via.
2. Connect all unused inputs to V_{SS}, leave unused outputs unconnected.

PHASE ALU BLOCK
The Phase ALU performs the addition of the Phase Modulation data to the Phase Accumulator output. The 3-bit PM data word is added to the 13 most significant bits from the Phase Accumulator to form the modulated phase used to address the look-up table.

SINE LOOK-UP TABLE BLOCK
This block is the sine memory. The 13 bits from the Phase ALU are used to address this memory to generate the 12-bit $\mathbf{OUT_{11-0}}$ outputs.

INPUT SIGNALS

RESET
The **RESET** input is asynchronous and active low, and clears all the registers in the device. When **RESET** goes low, all registers are cleared within 20 nsecs, and normal operation will resume after this signal returns high. The data on the $\mathbf{OUT_{11-0}}$ bus will then be invalid for 1 clock cycle, and thereafter will remain at the value corresponding to zero phase (801_H) until new frequency or phase modulation data is loaded with the **FRLD** or **PHLD** inputs after the **RESET** returns high.

CLOCK
All synchronous functions performed within the NCO are referenced to the rising edge of the **CLOCK** input. The **CLOCK** signal should be nominally a square wave at a maximum frequency of 25 MHz. A non-repetitive **CLOCK** waveform is permissible as long as the minimum duration positive or negative pulse on the waveform is always greater than 10 nanoseconds.

SERIN
The **Ser**ial **In**put pin is used to load the 24-bit frequency data word into the NCO. The format of the data is LSB first and one bit is written on each rising edge of the **WRSTB** input.

WRSTB
The **Wr**ite **St**ro**b**e input is used to latch the data on the **SERIN** input into the device. One bit is written on each rising edge of the **WRSTB** input. This signal can be completely asynchronous with respect to **CLOCK**.

FRLD
The **Fr**equency **Loa**d input is used to control the transfer of the data from the Serial Buffer Register Block to the Δ-Phase Register Block. The falling edge of **FRLD** can be coincident with the last rising edge of **WRSTB**. One complete cycle of **CLOCK** (starting at the next rising edge) must occur after the falling edge of **FRLD** before the next rising edge of **WRSTB**. The frequency of the NCO output will change 5 clock cycles after the **FRLD** command due to the pipeline delay.

$\mathbf{PHMOD_{2-0}}$
The 3-bit **Ph**ase **Mod**ulation input is used to load the phase modulation data word into the NCO. $\mathbf{PHMOD_2}$ is the MSB and represents a 180° phase change.

PHLD
The **Ph**ase **Loa**d input is used to control the latching of the Phase Modulation data into the Phase ALU. The 3-bit data at the $\mathbf{PHMOD_{2-0}}$ inputs must be valid during the clock cycle following the falling edge of **PHLD**. The data is then transferred during the subsequent cycle. The 3-bit phase data is added to the 3 most significant bits of the accumulator output, so that the MSB of the phase data represents a 180° phase change.The phase of the NCO output will change 3 clock cycles after the **PHLD** command due to the pipeline delay.

OUTPUT SIGNALS

$\mathbf{OUT_{11-0}}$
The signal appearing on the $\mathbf{OUT_{11-0}}$ output bus is derived from the 13 most significant bits of the Phase Accumulator. The 12-bit sine or cosine function is presented in offset binary format. When the phase modulation is zero the value of the output for a given phase value follows the relationship:

$\mathbf{OUT_{11-0}}$=2047 x sin (360 x (phase+0.5)/8192)°+2048

The result is accurate to within 1 LSB. When the phase accumulator is zero, e.g., after a reset, the decimal value of the output is 2049 (801_H). $\mathbf{OUT_{11}}$ is the MSB.

MSBOUT
The **MSBOUT** is the MSB of the Phase Accumulator. This signal will be a square wave at the same frequency as the output signal. However, unless the output frequency is a submultiple of the clock frequency, i.e., $f_{out} = f_{clk}/N$, where N is an integer, there will be jitter on the edges of this signal. The peak-peak value of the jitter will be 1 clock cycle.

SEROUT
The **Ser**ial **Out**put signal is the output of the Serial Buffer Register. It is a replica of the **SERIN** signal delayed by 24 cycles of **WRSTB**.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Warning: Stresses greater than those shown below may cause permanent damage to the device. Exposure of the device to these conditions for extended periods may also affect device reliability. All voltages are referenced to V_{ss}.

Symbol	Parameter	Range	Units
T_{stg}	Storage Temperature	–40 to +125	°C
V_{DDmax}	Supply voltage on V_{DD}	–0.3 to + 7	volts
$V_{I(max)}$	Input voltage	–0.3 to V_{DD} + 0.3	volts
I_i	DC input current	± 10	mA

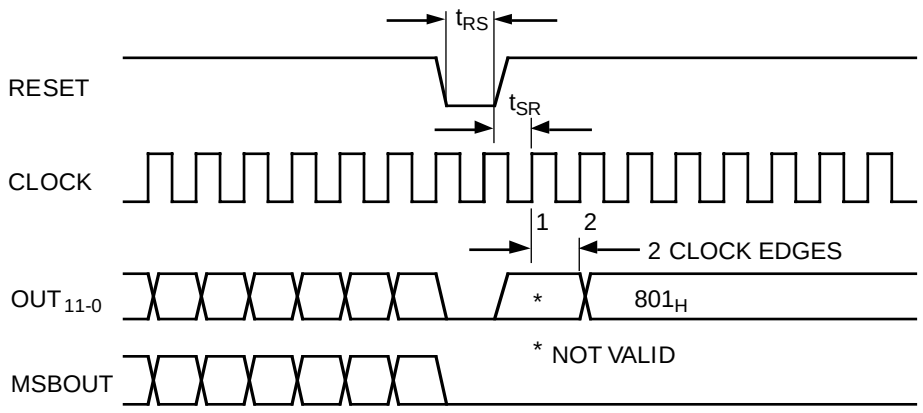
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Range	Units
V_{DD}	Supply Voltage	+5 ± 5%	Volts
T_a	Operating Temperature (Ambient)	–40 to +85	°C

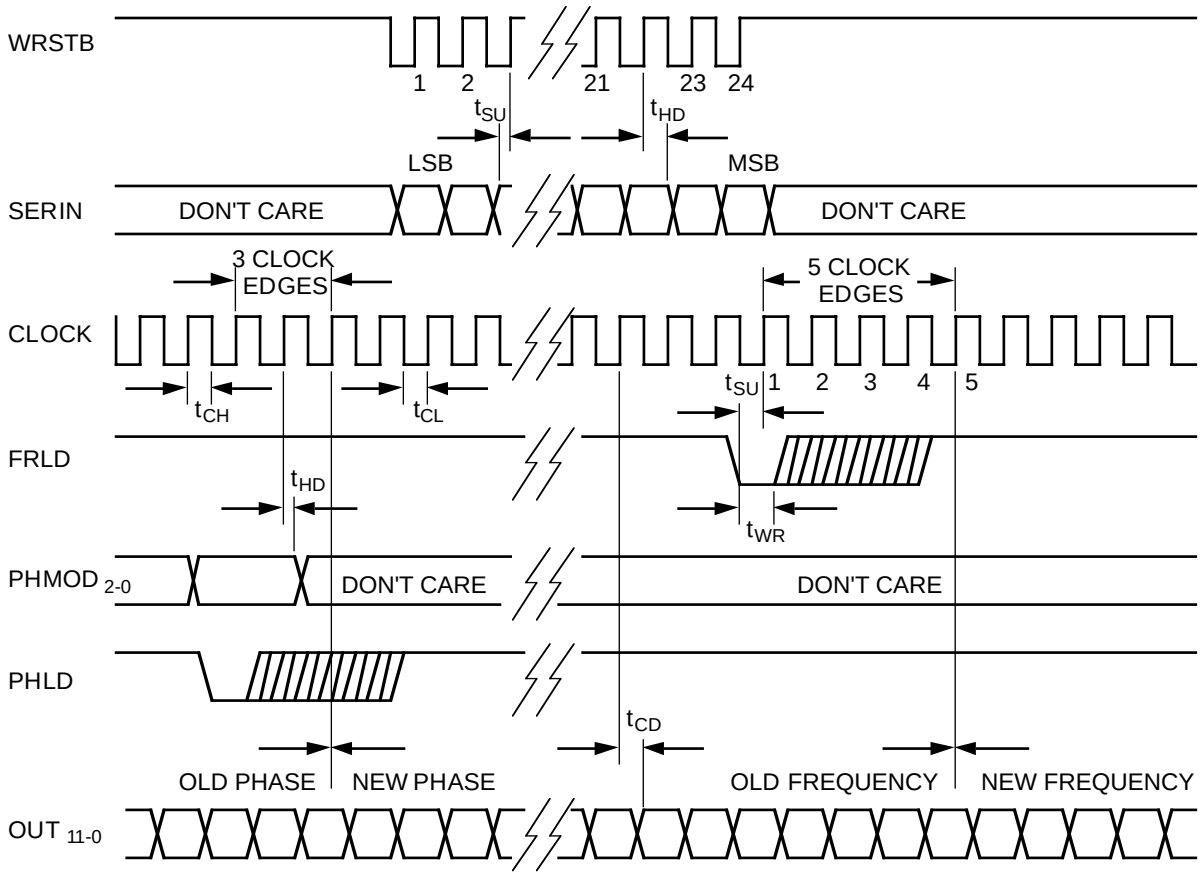
D.C. CHARACTERISTICS (Operating Conditions: V_{DD}= 5.0 V ± 5%, V_{SS}=0 V, T_a= –40° to +85° C

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_{DD(Q)}$	Supply Current, Quiescent			1.0	mA	Static, no clock
I_{DD}	Supply Current, Operational			2.0	mA/MHz	
$V_{IH(min)}$	High Level Input Voltage	2.0			volts	Logic '1'
$V_{IL(max)}$	Low Level Input Voltage			0.8	volts	Logic '0'
$I_{IH(min)}$	High Level Input Current			10	µA	All inputs, $V_{IN} = V_{DD}$
$I_{IL(max)}$	Low Level Input Current	–15	–45	–130	µA	All inputs, $V_{IN} = V_{SS}$
$V_{OH(min)}$	High Level Output Voltage	2.4	4.5		volts	I_O = –6.0 mA
$V_{OL(max)}$	Low Level Output Voltage		0.2	0.4	volts	I_O = +6.0 mA
I_{OS}	Output Short Circuit Current	20	65	130	mA	$V_{OUT} = V_{DD}$, V_{DD} = max
		–10	–45	–130	mA	$V_{OUT} = V_{SS}$, V_{DD} = max
C_{IN}	Input Capacitance		2		pF	All inputs
C_{OUT}	Output Capacitance		4		pF	All outputs

NCO RESET SEQUENCE



NCO FREQUENCY AND PHASE CHANGE SEQUENCES



ELECTRICAL CHARACTERISTICS

A.C. CHARACTERISTICS (Operating Conditions: V_{DD}= 5.0 V ± 5%, V_{SS}=0 V, T_a= –40° to +85° C

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
t_{RS}	**RESET** pulse width	20			nsec.	
t_{SR}	**RESET** to **CLOCK** Setup	10			nsec.	
t_{SU}	**SERIN** to **WRSTB** Setup, and **FRLD** or **PHLD** to **CLOCK** Setup	5			nsec.	
t_{HD}	**SERIN** to **WRSTB** Hold, and **CLOCK** to **FRLD** or **PHMOD** Hold	5			nsec.	
t_{CH}	**WRSTB** or **CLOCK** high	10			nsec.	f_{CLK} = 25 MHz
t_{CL}	**WRSTB** or **CLOCK** low	10			nsec.	f_{CLK} = 25 MHz
t_W	**FRLD** or **PHLD** pulse width	5			nsec.	
t_{CD}	**WRSTB** to **SEROUT** delay	7		12	nsec.	Load = 15 pF
t_{CD}	**CLOCK** to output delay	7		12	nsec.	Load = 15 pF (All other outputs)

SPECTRAL PURITY

In many applications the NCO is used with a digital to analog converter (DAC) to generate an analog waveform which approximates an ideal sinewave. The spectral purity of this synthesized waveform is a function of many variables including the phase and amplitude quantization, the ratio of the clock frequency to output frequency, and the dynamic characteristics of the DAC.

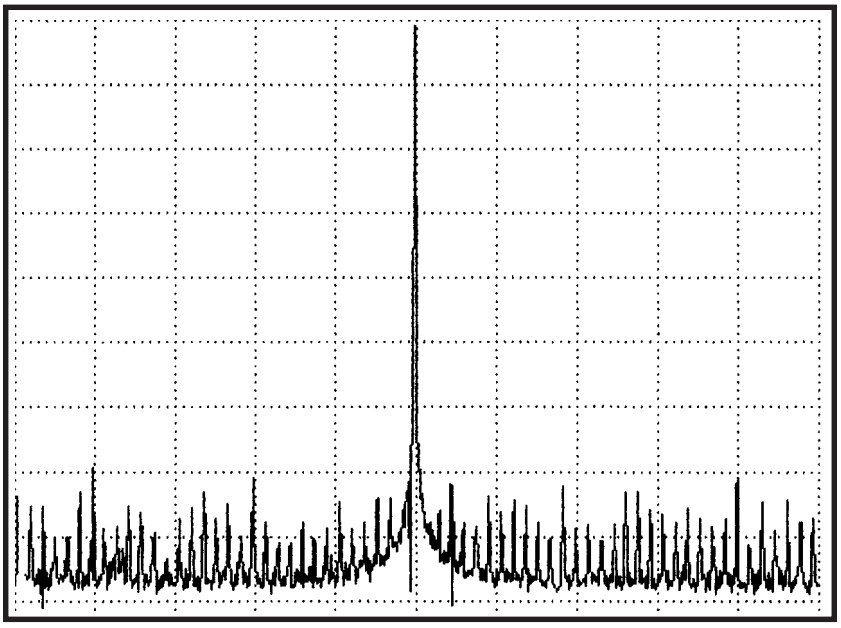
The sine or cosine signals generated by the STEL-1179 have 12 bits of amplitude resolution and 13 bits of phase resolution which results in spurious levels which are theoretically at least 75 dB down. The highest output frequency the NCO can generate is half the clock frequency ($f_c/2$), and the spurious components at frequencies greater than $f_c/2$ can be removed by filtering. As the output frequency f_o of the

NCO approaches $f_c/2$, the "image" spur at $f_c - f_o$ (created by the sampling process) also approaches $f_c/2$ from above. If the programmed output frequency is very close to $f_c/2$ it will be virtually impossible to remove this image spur by filtering. For this reason, the maximum practical output frequency of the NCO should be limited to about 40% of the clock frequency.

A spectral plot of the NCO output after conversion with a low cost 8-bit DAC (HA19510) is shown below. In this case, the clock frequency is 25 MHz and the output frequency is programmed to 4.567890 MHz. The maximum non-harmonic spur level observed over the entire useful output frequency range in this case is –69 dBc. The spur levels are limited by the dynamic linearity of the DAC. It is important to remember that when the output frequency exceeds 25% of the clock frequency, the second harmonic frequency will be higher than the Nyquist frequency, 50% of the clock frequency. When this happens, the image of the harmonic at the frequency $f_c - 2f_o$, which is not harmonically related to the output signal, will become intrusive since its frequency falls as the output frequency rises, eventually crossing the fundamental output when its frequency crosses through $f_c/3$. It would be necessary to select a DAC with better dynamic linearity to improve the harmonic spur levels. (The dynamic linearity of a DAC is a function of both its static linearity and its dynamic characteristics, such as settling time and slew rates.) At higher output frequencies the waveform produced by the DAC will have large output changes from sample to sample. For this reason, the settling time of the DAC should be short in comparison to the clock period. As a general rule, the DAC used should have the lowest possible glitch energy as well as the shortest possible settling time.

TYPICAL SPECTRUM

Center Frequency:	5 MHz
Frequency Span:	10 MHz
Reference Level:	–4 dBm
Resolution Bandwidth:	1 KHz
Video Bandwidth:	3 kHz
Scale:	Log, 10 dB/div
Output frequency:	4.567890 MHz
Clock frequency:	25 MHz



For Further Information Call or Write

INTEL CORPORATION
Cable Network Operation
350 E. Plumeria Drive, San Jose, CA 95134
Customer Service Telephone: (408) 545-9700
Technical Support Telephone: (408) 545-9799
FAX: (408) 545-9888