AmPAL*22V10B

24-Pin IMOX™ Programmable Array Logic (PAL)

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

- B-speed (t_{PD} = 15 ns) performance
- Increased logic power — up to 22 inputs and 10 outputs
- Increased product terms — average 12 per output
- Variable product-term distribution improves ease of use
- Each output user-programmable for registered or combinatorial operation
- Individually user-programmable output polarity
- Extra terms provide logical synchronous-PRESET and asynchronous-RESET capability
- Also comes in A-speed Low-Power (L) and Standard-speed Quarter-Power (Q) versions
- TTL level PRELOAD for improved testability
- 24-pin Slim DIP and 28-pin chip carrier packages
- Platinum silicide fuses ensure high programming yield, fast programming and unsurpassed reliability
- Full AC and DC testing done at the factory utilizing special designed-in test features
- 3000-V Input ESD Protection

GENERAL DESCRIPTION

The AmPAL22V10B is a second-generation Programmable Array Logic (PAL) device. It utilizes the familiar sum-of-products (AND-OR) logic structure, allowing users to program custom logic functions. The AmPAL22V10B is an extension of the PAL concept. First-generation devices were largely limited to TTL replacement applications. The AmPAL22V10B permits the development of custom LSI functions of 500 to 800 equivalent gate complexity.

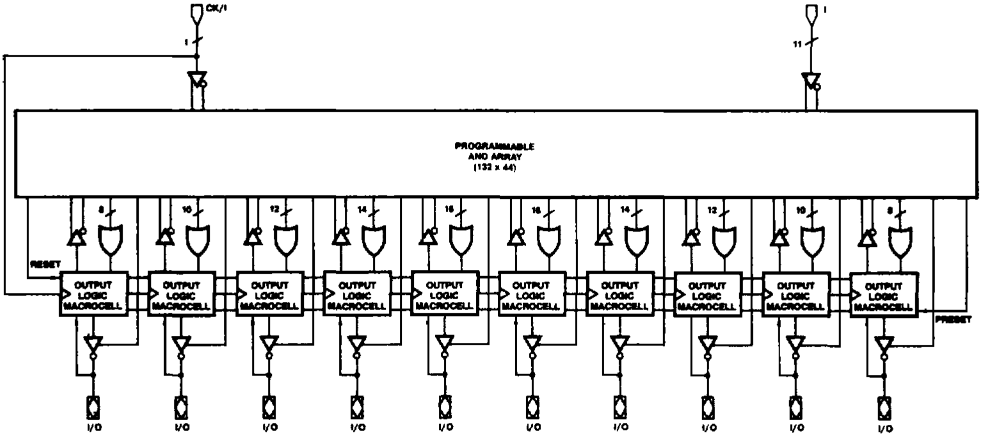
The AmPAL22V10B contains up to 22 inputs and 10 outputs. It incorporates the unique capability of defining and programming the architecture of each output on an individual basis. Each output is user-programmable for either registered or combinatorial operation. This allows the designer to optimize the device design, by having only as many registers as needed. In addition, each output has user-programmable output polarity, further simplifying design and contributing to the precise application requirements.

Increased logic power has been built into the AmPAL22V10B by increasing the number of product terms from 8-per-output to an average of 12-per-output. Further innovation can be seen in the introduction of variable product-term distribution. This technique allocates from 8 to 16 logical product terms to each output (please refer to block diagram for distribution details). This variable allocation of terms allows far more complex functions to be implemented than in previous devices .

System operation has been enhanced by the addition of a synchronous-PRESET and an asynchronous-RESET product term. These terms are common to all output registers.

The AmPAL22V10B also incorporates power-up RESET and the unique capability to PRELOAD the output registers to any desired state during testing. PRELOAD is essential to permit full logical verification during test.

BLOCK DIAGRAM



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08601	A	/0
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OPERATING RANGES

Temperature (T_A) Operating Free Air .....0°C to +75°C
Supply Voltage (V_{CC}) ....+4.75 to +5.25 V

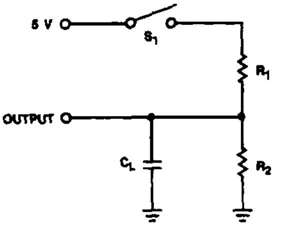
Commercial (C) Devices

SWITCHING CHARACTERISTICS *over operating range unless otherwise specified*

Parameter Symbol	Parameter Description	Test Conditions	Typ. (Note 1)	C Devices				E/M Devices				Units
				[illegible]		TBD		"B"		TBD		
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input or Feedback to Non-Registered Output	C Devices R_1 = [illegible] R_2 = 390			15				20			ns
t_{EA}	Input to Output Enable				15				20			ns
t_{ER}	Input to Output Disable				[illegible]				20			ns
t_{CO}	Clock to Output				10				15			ns
t_S	Input or Feedback Setup Time			1[illegible]				17				ns
t_H	Hold Time			0				0				ns
t_P	Clock Period ($t_S + t_{CO}$)			22				32				ns
t_W	Clock Width			11				16				ns
f_{MAX}	Maximum Frequency				45				31			MHz
t_{AW}	Asynchronous Reset Width	E/M Devices R_1 = 390 R_2 = 750		15				20				ns
t_{AR}	Asynchronous Reset Recovery Time			15				20				ns
t_{AP}	Asynchronous Reset to Registered Output Reset				20				25			ns

Notes: 1. Typical limits are at V_{CC} = 5.0 V and T_A = 25°C.
2. t_{PD} is tested with switch S_1 closed and C_L = 50 pF.
3. For three-state outputs, output enable times are tested with C_L = 50 pF to the 1.5 V level; S_1 is open for high-impedance to HIGH tests and closed for high-impedance to LOW tests. Output disable times are tested with C_L = 5 pF. HIGH to high-impedance tests are made to an output voltage of V_{OH} − 0.5 V with S_1 open; LOW to high-impedance tests are made to the V_{OL} + 0.5 V level with S_1 closed.

SWITCHING TEST CIRCUIT



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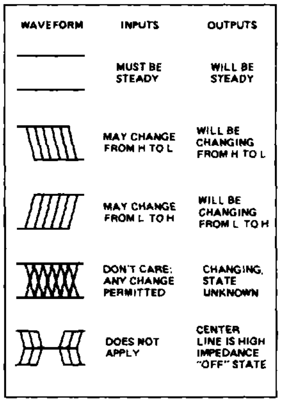
KEY TO SWITCHING WAVEFORMS



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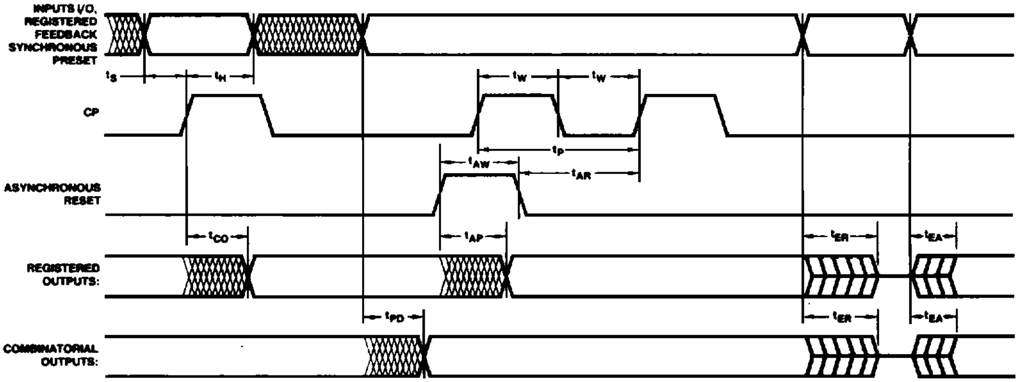
SWITCHING WAVEFORMS



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