Am8177

Video Data Serializer

FINAL

DISTINCTIVE CHARACTERISTICS

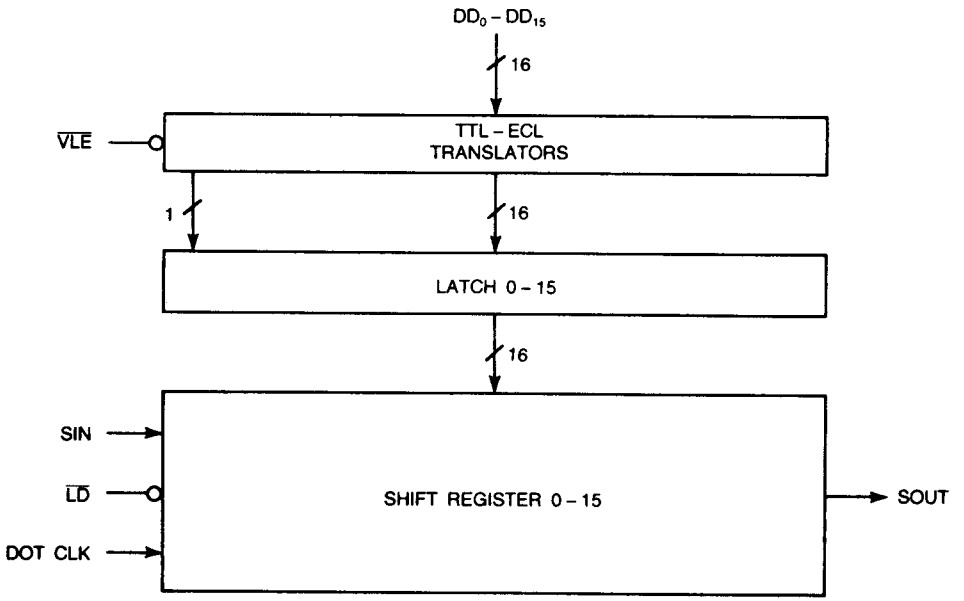
- 200-MHz parallel-to-serial shift register
- Cascadable in increments of 16 bits
- 24-pin slim-line DIP

GENERAL DESCRIPTION

The Am8177 Video Data Serializer (VDS) is a 16-bit parallel-to-serial shift register for use in bit-mapped display applications. The VDS can accommodate video words of up to 16 bits; wider display memories can be handled by cascading VDSs using the Serial In (SIN) line.

The Am8177 VDS is a part of AMD's Display Products Family which also includes the Am8151A Graphics Color Palette, Am8172 Video Data Assembly, FIFO, and the Am95C60 Quad Pixel Dataflow Manager.

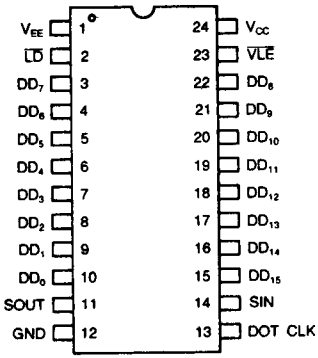
BLOCK DIAGRAM



BD005370

Publication # 07080 Rev. C Amendment /0
Issue Date: August 1989

CONNECTION DIAGRAMS
Top View



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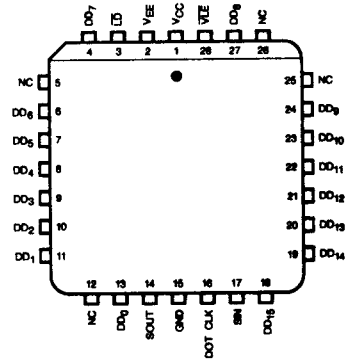

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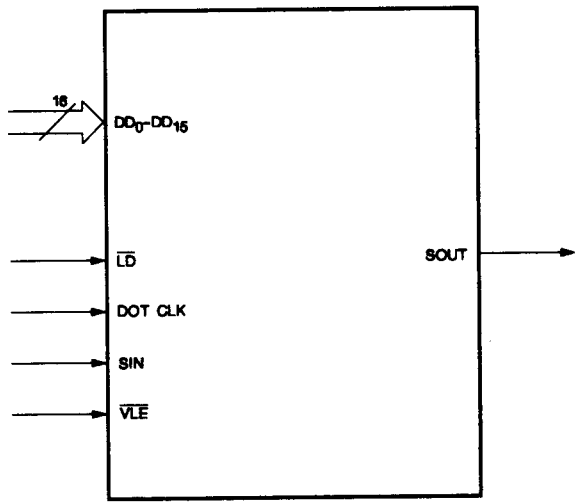
Note: Pin #1 is marked for orientation

LOGIC SYMBOL



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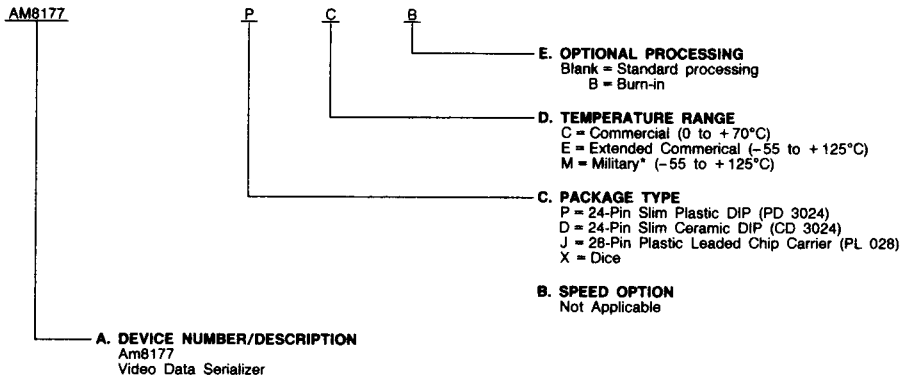
ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM8177	PC, PCB, DC, DCB, DE, DEB, JC, XC

* Military or Limited Military temperature range products are "NPL" (Non-Complaint Products List) or Non-MIL-STD-883C Compliant products only.

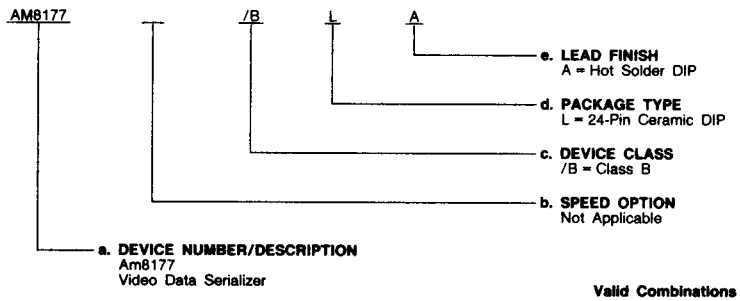
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM8177	/BLA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

PIN DESCRIPTION

DOT CLK Dot Clock (Input, ECL)
Shift Register Clock. All operations in the shift register take place on the rising edge of this clock.

$DD_0 - DD_{15}$ Parallel Data In (Inputs, TTL)
$DD_0 - DD_{15}$ are the parallel data input pins. DD_0 is the first bit to be shifted out; DD_1 is the next.

$\overline{LD}$ Load (Input, ECL)
When $\overline{LD}$ is active (LOW), the shift register is loaded in parallel on the next rising edge of the clock. If $\overline{VLE}$ is HIGH, data is loaded from the latch; if $\overline{VLE}$ is LOW, data is loaded directly from the parallel data input pins.

SIN Serial In (Input, ECL)
SIN is used when cascading VDSs and is connected to SOUT of the higher order VDS.

SOUT Serial Out (Output, ECL)
SOUT is the serialized output of the VDS. It is also used when cascading VDSs and is connected to SIN of the lower order VDS.

$\overline{VLE}$ Video Latch Enable (Input, TTL)
Active LOW enable for the latch. The latch may be used to provide a pipeline between the display RAM and the shift register. The parallel data may be loaded into the latch as soon as it is available at the display RAM outputs and then loaded into the shift register when it is needed. The latch may be kept transparent by keeping $\overline{VLE}$ LOW. When $\overline{VLE}$ goes HIGH, the parallel data is latched into the latch and remains so until $\overline{VLE}$ goes LOW again.

V_{CC} TTL Positive Supply

V_{EE} ECL Negative Supply

GND Ground

FUNCTION TABLE

$\overline{LD}$	$\overline{VLE}$	ACTION
0	0	Load data into shift register from data pins
0	1	Load data into shift register from latch
1	0	Shift
1	1	Shift

$\overline{VLE}$	ACTION
1	Latches data from data pins into latch
0	Latch appears transparent

FUNCTIONAL DESCRIPTION

The Am8177 Video Data Serializer (VDS) is a 16-bit parallel-to-serial shift register intended for use in bit-mapped video applications. The VDS is loaded in parallel with up to 16 bits from a single bit-plane. The bits are then serialized at the DOT CLK rate.

The VDS parallel data inputs are TTL for ease in communicating with the bit map, while the clock and serializer controls are ECL to allow the fast bit rates required for high-density screen formats.

A set of latches are provided between the parallel data input pins and the shift register. This allows the next word of data from the RAMs to be captured without affecting the contents of the shift register. This provides a means of decoupling (to some degree) the video RAM timing and the serializer timing. $\overline{VLE}$ is used to load the latch and then $\overline{LD}$ is used to load the data into the shift register.

The VDS can accommodate video words of up to 16 bits. Wider display memories can be handled by cascading VDSs using the Serial In (SIN) line.

APPLICATIONS

In a typical video system, parallel pixel data is accessed from the bit-map RAMs during the character clock cycle. At the completion of the access, this data can be latched into the Video Data Serializer using $\overline{VLE}$. $\overline{CAS}$, for example, would have the correct timing to drive $\overline{VLE}$, but external logic would be required to discriminate between video cycles and update cycles.

The transfer from the latch to the shift register will normally take place immediately before the next character clock, using the $\overline{LD}$ input.

The $\overline{LD}$ signal occurs every character clock and must be synchronous to DOT CLK. An appropriate signal is provided by the Am8158 Video Timing Controller which receives an asynchronous $\overline{VLE}$ and outputs the required synchronous $\overline{LD}$.

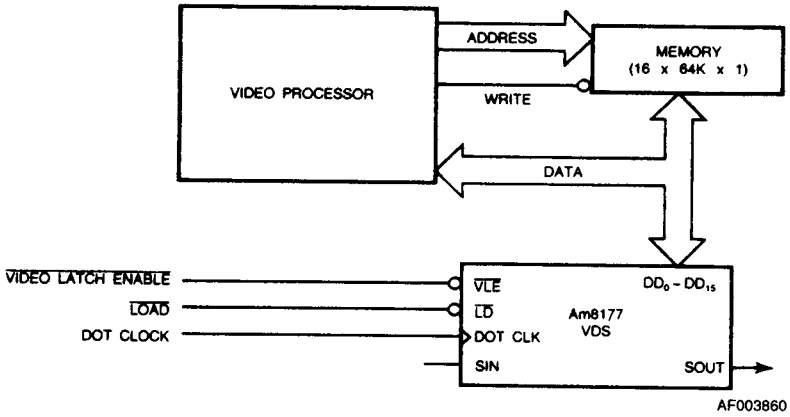


Figure 1. Single Bit-Plane Application

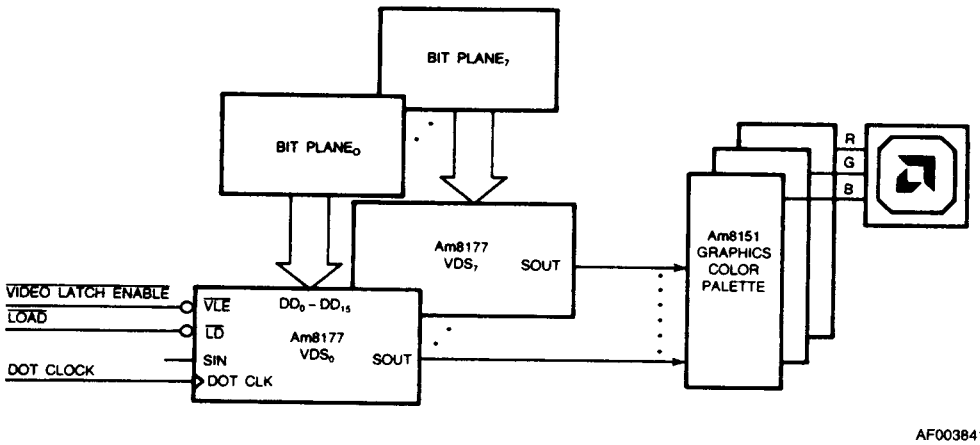


Figure 2. Multiple Bit-Plane Application

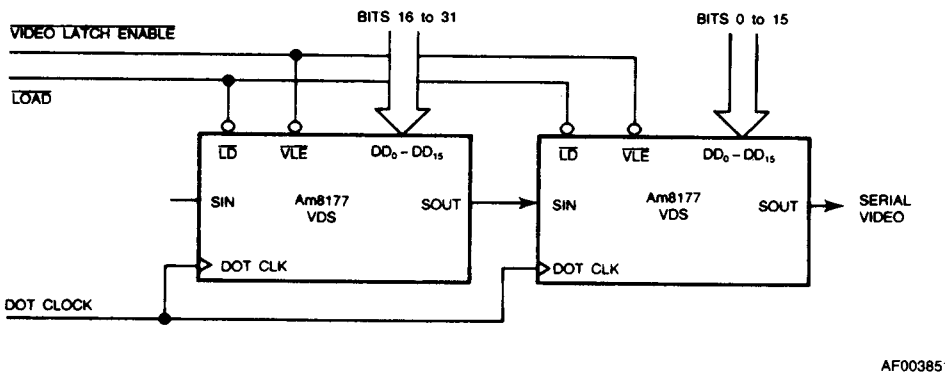


Figure. 3. Typical Cascading Application

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature Under Bias ..... −55 to +125°C
Supply Voltage to Ground Potential
Continuous (TTL) ..... −0.5 to +7.0 V
Supply Voltage to Ground Potential
Continuous (ECL) ..... +0.5 to −7.0 V
DC Input Voltage (TTL) ..... −0.5 to +7.0 V
DC Input Current (TTL) ..... −30 to +5.0 mA
DC Input Voltage (ECL) ..... +0.5 to V_{EE}
DC output Current into Outputs (ECL) ..... −30 to +0.1 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices (Note 2)
Temperature (T_A) ..... 0 to +70°C
TTL Supply Voltage (V_{CC}) ..... +5.0 V ±5%
ECL Negative Supply Voltage (V_{EE}) ..... −5.2 V ±5%

Extended Commercial (E) Devices (Note 6)
Temperature (T_C) ..... −55 to +125°C
TTL Supply Voltage (V_{CC}) ..... +5.0 V ±5%
ECL Supply Voltage (V_{EE}) ..... −5.2 V ±5%

Military* (M) Devices (Note 6)
Temperature (T_C) ..... −55 to +125°C
TTL Supply Voltage (V_{CC}) ..... +5.0 V ±10%
ECL Supply Voltage (V_{EE}) ..... −5.2 V ±10%

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military Product 100% tested at T_C = +25°C, +125°C, and −55°C.

DC CHARACTERISTICS over operating range (TTL) unless otherwise specified (Note 6)

Symbol	Parameter	Test Condition (Note 3)	Min.	Typ. (Note 5)	Max.	Units
V_{IH}	Input HIGH Level	Guaranteed Input HIGH Voltage (Note 4)	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed Input LOW Voltage (Note 4)			0.8	Volts
V_I	Input CLAMP Voltage	V_{CC} = Min., I_{IN} = −18 mA			−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.4 V			−0.4	mA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V			100	μA
I_I	I_{IH} at Max. V_{IN}	V_{CC} = Max., V_{IN} = 5.5 V			1.0	mA
I_{CC}	TTL Supply Current	V_{CC} = Max., V_{EE} = Max.	21	29	43	mA
I_{EE}	ECL Supply Current	V_{EE} = Max., V_{CC} = Max.	98	140	213	mA

Notes:
1. Devices are not subjected to ABSOLUTE MAXIMUM RATINGS in production. Non-production samples have been subjected to ABSOLUTE MAXIMUM RATINGS.
2. OPERATING RANGES are guaranteed for steady state conditions (no air flow). Hot temperature testing is elevated to simulate steady state conditions when using pulse test techniques. Cold testing is at the specified temperatures.
3. For conditions shown as Min. or Max., use the appropriate values specified under recommended operating ranges.
4. V_{IH} threshold is measured at V_{CC} = Max. and V_{EE} = Min. with all other inputs HIGH.
   V_{IL} threshold is measured at V_{CC} = Min. and V_{EE} = Max. with all other inputs LOW.
   This test method is used to guarantee V_{IH} and V_{IL}.
5. All typical values are V_{CC} = 5.0 V, V_{EE} = −5.2 V, T_A = 25°C.
6. Guaranteed with transverse air flow exceeding 500 linear F.P.M. and two minute warm-up period. Typical thermal resistance values of the package are:
   θ_{JA} (Junction-to-Ambient) = °C/Watt (still air)
   θ_{JA} (Junction-to-Ambient) = °C/Watt (at 500 F.P.M. air flow)
   θ_{JC} (Junction-to-Case) = °C/Watt

Plastic	Hermetic DIP
70	55
40	15
40	15

7. f_{CLK}, Setup, Hold Time, and DOT CLK to SOUT limits are guaranteed through characterization and correlation to other tests and not directly measured in production.

DC CHARACTERISTICS over operating range (ECL) unless otherwise specified

	Symbol	Test Conditions	−55°C	0°C	25°C	70°C	125°C	Unit
ECL Output: SOUT	V_{OH} (Max.) V_{OH} (Min.)	50 Ω to −2 V	−860 −1070	840 −1000	−810 −960	730 −910	−650 −860	mV
	V_{OL} (Max.) V_{OL} (Min.)	50 Ω to −2 V	−1690 −1900	−1665 −1870	−1650 −1850	−1630 −1835	−1570 −1800	mV
ECL Inputs: SIN, $\overline{LD}$, DOT CLK	V_{IH} (Max.) V_{IH} (Min.)	(Note 4) (Note 4)	−860 −1215	−840 −1145	−810 −1105	−730 −1055	−650 −1005	mV
	V_{IL} (Max.) V_{IL} (Min.)	(Note 4) (Note 4)	−1515 −1900	−1490 −1870	−1475 −1850	−1455 −1835	−1395 −1800	mV
	I_{IH} I_{IL}	V_{EE} = Max. V_{IN} = V_{IH} (Max.) V_{EE} = Max. V_{IN} = V_{IL} (Min.)	250 200	200 150	200 150	200 150	200 150	μA

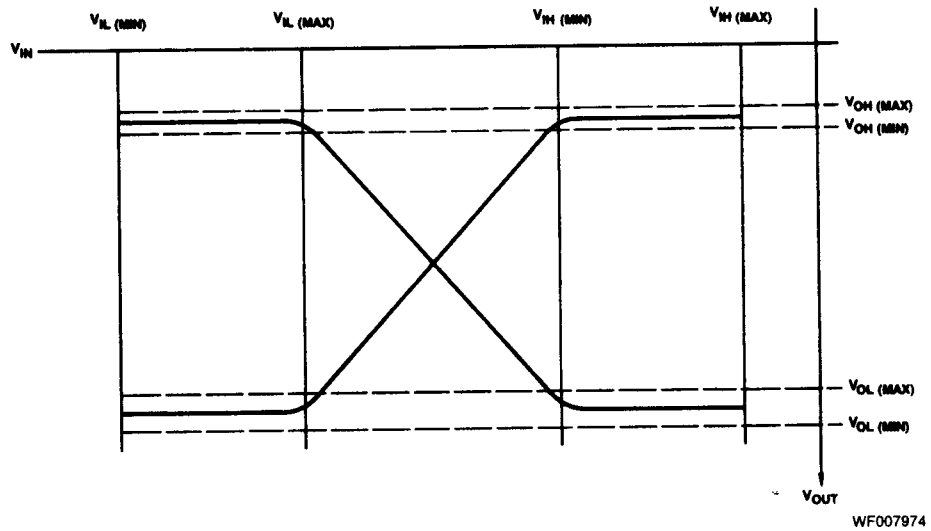


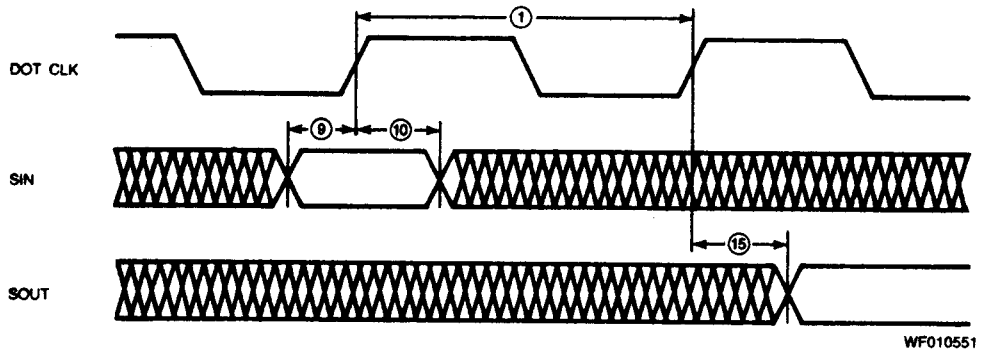
Figure 4. Am8177 ECL Specifications

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Note 7)

No.	Parameter Symbol	Parameter Description		Min.			Max.		Units
1	f_{CLK}	Clock Frequency		0			200		MHz
2	t_S	$\overline{VLE}$ ↓ to DOT CLK ↑ Setup (Transparent)		4					ns
3	t_H	$\overline{VLE}$ ↓ to DOT CLK ↑ Hold (Latch)		0					ns
4	t_W	$\overline{VLE}$ Pulse Width		5					ns
5	t_S	$DD_0 - DD_{15}$ to $\overline{VLE}$ ↑ Setup		2					ns
6	t_H	$DD_0 - DD_{15}$ to $\overline{VLE}$ ↑ Hold		4.5					ns
7	t_S	$DD_0 - DD_{15}$ to DOT CLK ↑ Setup		5					ns
8	t_H	$DD_0 - DD_{15}$ to DOT CLK ↑ HOLD		2					ns
				C Devices (Note 2)			E/M Devices (Note 6)		
No.	Parameter Symbol	Parameter Description		0°C	25°C	70°C	−55°C	125°C	Units
9	t_S	SIN to DOT CLK ↑ Setup	Min.	0.8	0.7	0.6	1.1	0.6	ns
10	t_H	SIN to DOT CLK ↑ Hold	Min.	1.2	1.2	1.4	0.8	1.4	ns
11	t_S	$\overline{LD}$ ↓ to DOT CLK ↑ Setup (Load)	Min.	1.2	1.1	1.0	1.4	0.9	ns
12	t_S	$\overline{LD}$ ↑ to DOT CLK ↑ Setup (No Load)	Min.	0.8	0.8	0.6	1.0	0.6	ns
13	t_H	$\overline{LD}$ ↑ to DOT CLK ↑ HOLD (Load)	Min.	0.6	0.6	0.5	0.8	0.5	ns
14	t_H	$\overline{LD}$ ↓ to DOT CLK ↑ Hold (No Load)	Min.	0.5	0.4	0.3	0.7	0.3	ns
15	t_{PLH}	DOT CLK ↑ to SOUT ↓	Max.	3.3	3.6	4.0	2.8	4.2	ns
	t_{PHL}	DOT CLK ↑ to SOUT ↓	Min.	1.9	2.1	2.5	1.8	2.6	

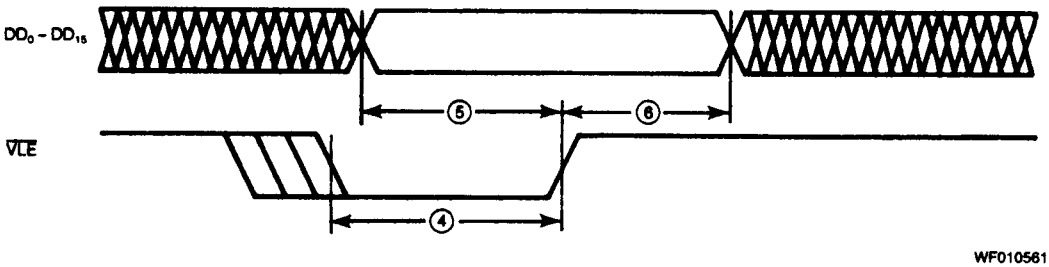
Notes: See notes following the DC Characteristics table.

SWITCHING WAVEFORMS

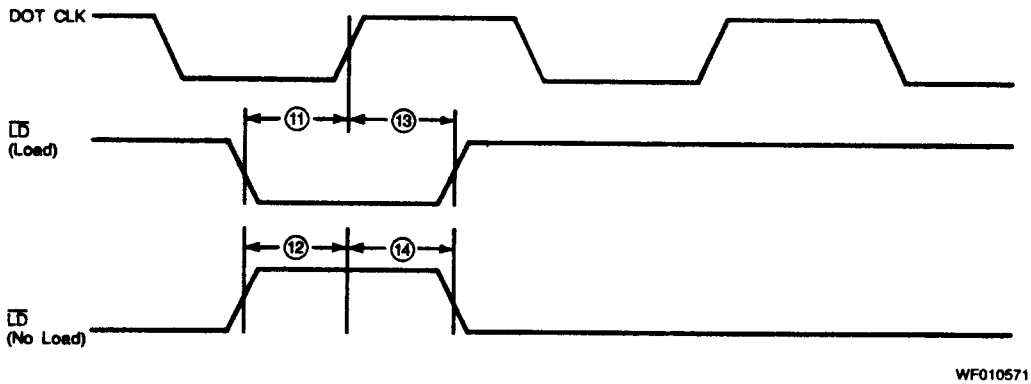


Note: $\overline{LD}$ = HIGH

Shift Timing

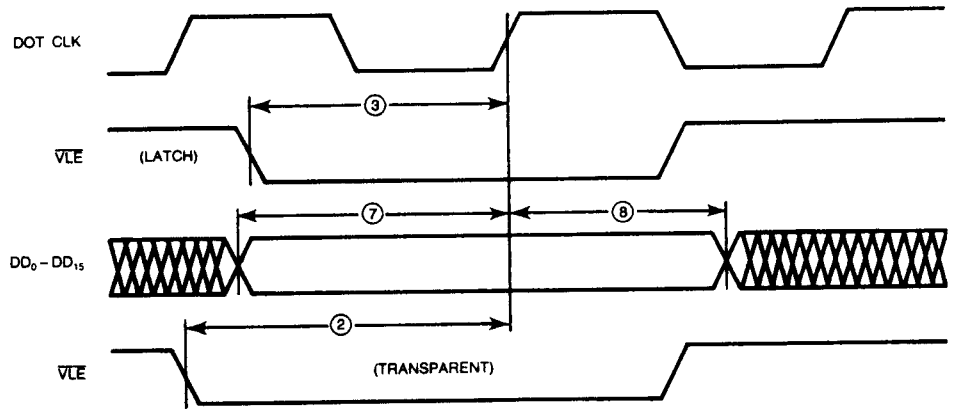


Data Latch Timing



Load and No-Load Timing

SWITCHING WAVEFORMS (Cont'd.)



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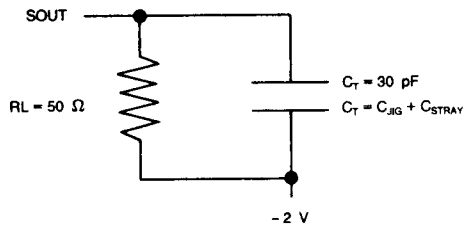
VLE LATCH /TRANSPARENT TIMING

SWITCHING TEST CIRCUIT



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KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
———		
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

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