

# MB81C1001-70/-80/-10/-12

## CMOS 1,048,576 BIT NIBBLE MODE DYNAMIC RAM

### CMOS 1M x 1 Bit Nibble Mode DRAM

The Fujitsu MB81C1001 is a CMOS, fully decoded dynamic RAM organized as 1,048,576 words x 1 bit. The MB81C1001 has been designed for mainframe memories, buffer memories, and peripheral storage applications requiring high speed, low power dissipation, and compact layout.

Fujitsu's advanced three-dimensional stacked capacitor cell technology gives the MB81C1001 high  $\alpha$ -ray soft error immunity. CMOS technology is used in the peripheral circuits to provide low power dissipation and high speed operation.

This specification applies to the BC die revision that was developed to realize faster access time. Faster speed versions (70 and 80 ns) are available on this chip.

### Features

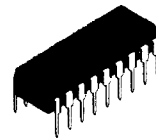
Parameter	MB81C1001 -70	MB81C1001 -80	MB81C1001 -10	MB81C1001 -12
RAS Access Time	70 ns max.	80 ns max.	100 ns max.	120 ns max.
Random Cycle Time	140 ns min.	155 ns min.	180 ns min.	210 ns min.
Address Access Time	43 ns max.	45 ns max.	50 ns max.	60 ns max.
CAS Access Time	25 ns max.	25 ns max.	25 ns max.	35 ns max.
Nibble Mode Cycle Time	50 ns min.	50 ns min.	55 ns min.	60 ns min.
Low Power Dissipation				
• Operating Current	413 mW max.	385 mW max.	330 mW max.	275 mW max.
• Standby Current	11 mW max. (TTL level)/5.5 mW max. (CMOS level)			

- 1,048,576 words x 1 bit organization
- Silicon gate, CMOS, 3D-Stacked Capacitor Cell
- All input and output are TTL compatible
- 512 refresh cycles every 16.4 ms
- Common I/O capability by using early write
- RAS only, CAS-before-RAS, or Hidden Refresh
- Nibble Mode, Read-Modify-Write capability
- On-chip substrate bias generator for high performance

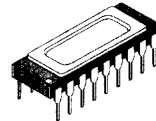
### Absolute Maximum Ratings (See Note)

Parameter	Symbol	Value	Unit	
Voltage at any pin relative to $V_{SS}$	$V_{IN}, V_{OUT}$	-1 to +7	V	
Voltage of $V_{CC}$ supply relative to $V_{SS}$	$V_{CC}$	-1 to +7	V	
Power Dissipation	PD	1.0	W	
Short Circuit Output Current	—	50	mA	
Storage Temperature	Ceramic	$T_{STG}$	-55 to +150	°C
	Plastic		-55 to +125	

**Note:** Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



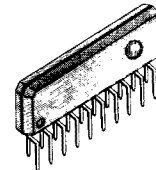
DIP-18P-M04



DIP-18C-A01



LCC-26P-M04

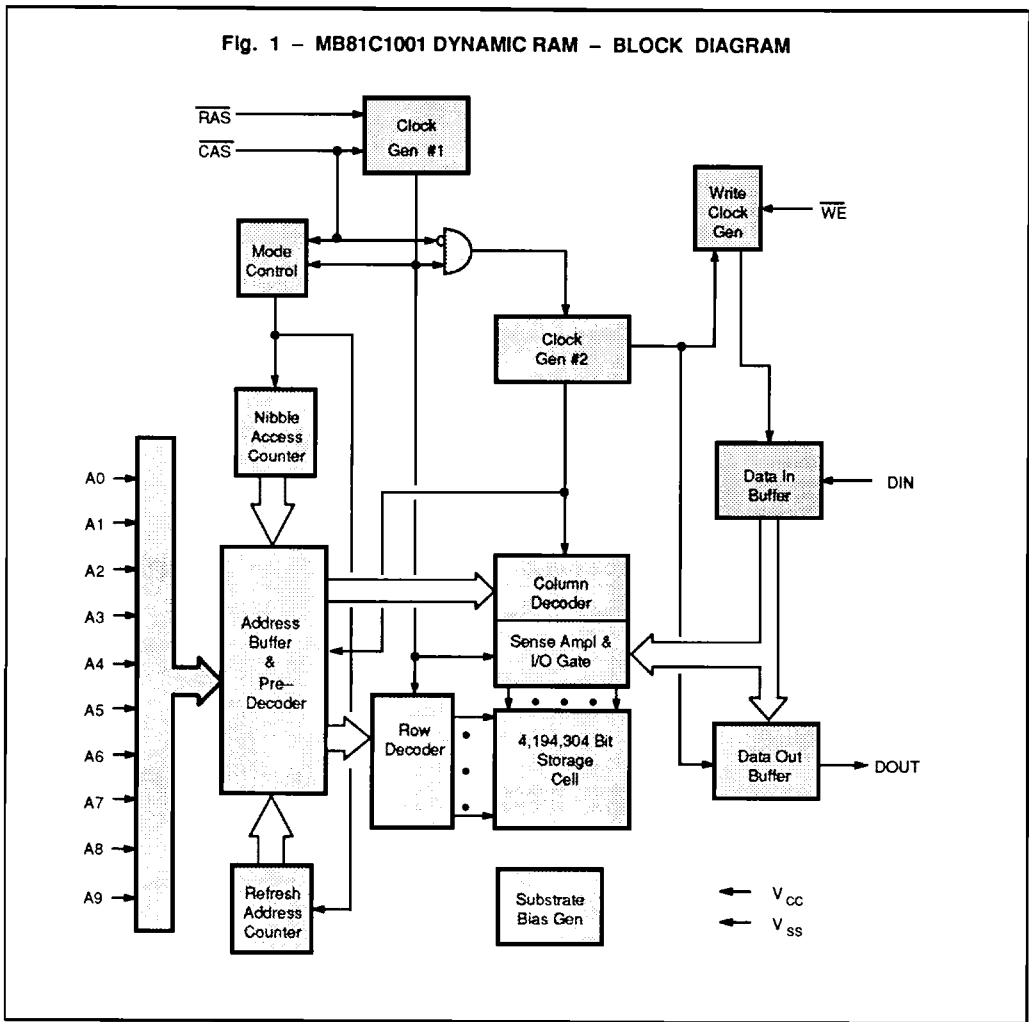


ZIP-20P-M02

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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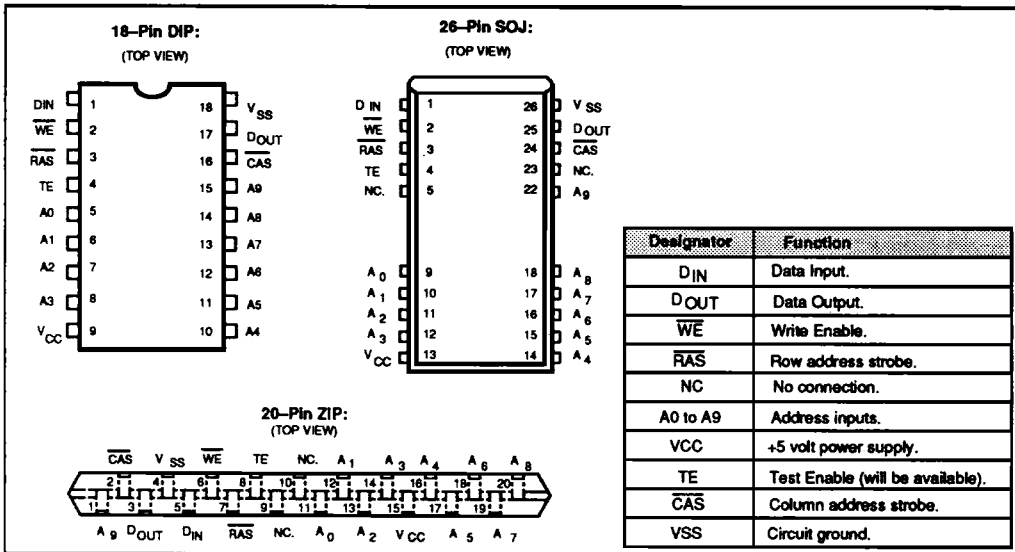
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**CAPACITANCE** ( $T_A = 25^\circ\text{C}$ ,  $f = 1\text{MHz}$ )

Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A9, D <sub>IN</sub>	C <sub>IN1</sub>	—	5	pF
Input Capacitance, $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$	C <sub>IN2</sub>	—	5	pF
Output Capacitance, D <sub>OUT</sub>	C <sub>OUT</sub>	—	5	pF

## PIN ASSIGNMENTS AND DESCRIPTIONS



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## RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min	Typ	Max	Unit	Ambient Operating Temp
Supply Voltage	1	V <sub>CC</sub>	4.5	5.0	5.5	V	0 °C to +70 °C
		V <sub>SS</sub>	0	0	0		
Input High Voltage, all inputs	1	V <sub>IH</sub>	2.4	—	6.5	V	
Input Low Voltage, all inputs	1	V <sub>IL</sub>	-2.0	—	0.8	V	

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## FUNCTIONAL OPERATION

### ADDRESS INPUTS

Twenty input bits are required to decode any one of 1,048,576 cell addresses in the memory matrix. Since only ten address bits are available, the column and row inputs are separately strobed by  $\overline{CAS}$  and  $\overline{RAS}$  as shown in Figure 1. First, nine row address bits are input on pins A0–through–A9 and latched with the row address strobe ( $\overline{RAS}$ ) then, ten column address bits are input and latched with the column address strobe ( $\overline{CAS}$ ). Both row and column addresses must be stable on or before the falling edge of  $\overline{CAS}$  and  $\overline{RAS}$ , respectively. The address latches are of the flow-through type; thus, address information appearing after  $t_{RAH}$  (min) +  $t_r$  is automatically treated as the column address.

### WRITE ENABLE

The read or write mode is determined by the logic state of  $\overline{WE}$ . When  $\overline{WE}$  is active Low, a write cycle is initiated; when  $\overline{WE}$  is High, a read cycle is selected. During the read mode, input data is ignored.

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### DATA INPUT

Data is written into the MB81C1001 during write or read-modify-write cycle. The input data is strobed and latched by the later falling edge of  $\overline{CAS}$  or  $\overline{WE}$ . In an early write cycle, data input is strobed by  $\overline{CAS}$ , and set up and hold times are referenced to  $\overline{CAS}$ . In a delayed write or read-modify-write cycle,  $\overline{WE}$  is set low after  $\overline{CAS}$ . Thus, data input is strobed by  $\overline{WE}$ , and set up and hold times are referenced to  $\overline{WE}$ .

### DATA OUTPUT

The three-state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high-impedance state until the column address strobe goes Low. When a read or read-modify-write cycle is executed, valid outputs are obtained under the following conditions:

- t<sub>TRAC</sub>** : from the falling edge of  $\overline{RAS}$  when  $t_{RCD}$  (max) is satisfied.
- t<sub>TCAC</sub>** : from the falling edge of  $\overline{CAS}$  when  $t_{RCD}$  is greater than  $t_{RCD}$ ,  $t_{RAD}$  (max).
- t<sub>TA</sub>** : from column address input when  $t_{RAD}$  is greater than  $t_{RAD}$  (max).

## DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Notes 3

Parameter	Notes	Symbol	Conditions	Values			Unit
				Min	Typ	Max	
Output high voltage		$V_{OH}$	$I_{OH} = -5 \text{ mA}$	2.4	—	—	V
Output low voltage		$V_{OL}$	$I_{OL} = 4.2 \text{ mA}$	—	—	0.4	
Input leakage current (any input)		$I_{IL}$	$0\text{V} \leq V_{IN} \leq 5.5\text{V};$ $4.5\text{V} \leq V_{CC} \leq 5.5\text{V};$ $V_{SS}=0\text{V};$ All other pins not under test $=0\text{V}$	-10	—	10	$\mu\text{A}$
Output leakage current		$I_{OL}$	$0\text{V} \leq V_{OUT} \leq 5.5\text{V};$ Data out disabled	-10	—	10	
Operating current (Average power supply current) 2	MB81C1001-70	$ICC_1$	$\overline{RAS}$ & $\overline{CAS}$ cycling; $t_{RC} = \text{min}$	—	—	75	mA
	MB81C1001-80					70	
	MB81C1001-10					60	
	MB81C1001-12					50	
Standby current (Power supply current)	TTL level	$ICC_2$	$\overline{RAS}=\overline{CAS}=V_{IH}$	—	—	2.0	mA
	CMOS level		$\overline{RAS}=\overline{CAS} \geq V_{CC}-0.2\text{V}$			1.0	
Refresh current #1 (Average power supply current) 2	MB81C1001-70	$ICC_3$	$\overline{CAS}=V_{IH}, \overline{RAS}$ cycling; $t_{RC} = \text{min}$	—	—	70	mA
	MB81C1001-80					65	
	MB81C1001-10					55	
	MB81C1001-12					45	
Nibble Mode current 2	MB81C1001-70	$ICC_4$	$\overline{RAS} = V_{IL}, \overline{CAS}$ cycling; $t_{RC} = \text{min}$	—	—	45	mA
	MB81C1001-80					45	
	MB81C1001-10					35	
	MB81C1001-12					25	
Refresh current #2 (Average power supply current) 2	MB81C1001-70	$ICC_5$	$\overline{RAS}$ cycling ; $\overline{CAS}$ before $\overline{RAS}$ ; $t_{RC} = \text{min}$	—	—	70	mA
	MB81C1001-80					65	
	MB81C1001-10					55	
	MB81C1001-12					45	

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## AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81C1001-70		MB81C1001-80		MB81C1001-10		MB81C1001-12		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
1	Time Between Refresh		$t_{REF}$	—	8.2	—	8.2	—	8.2	—	8.2	ms
2	Random Read/Write Cycle Time		$t_{RC}$	140	—	155	—	180	—	210	—	ns
3	Read-Modify-Write Cycle Time		$t_{RWC}$	167	—	182	—	210	—	245	—	ns
4	Access Time from $\overline{RAS}$	6.9	$t_{RAC}$	—	70	—	80	—	100	—	120	ns
5	Access Time from $\overline{CAS}$	7.9	$t_{CAC}$	—	25	—	25	—	25	—	35	ns
6	Column Address Access Time	8.9	$t_{AA}$	—	43	—	45	—	50	—	60	ns
7	Output Hold Time		$t_{OH}$	7	—	7	—	7	—	7	—	ns
8	Output Buffer Turn on Delay Time		$t_{ON}$	5	—	5	—	5	—	5	—	ns
9	Output Buffer Turn off Delay Time	10	$t_{OFF}$	—	25	—	25	—	25	—	25	ns
10	Transition Time		$t_T$	3	50	3	50	3	50	3	50	ns
11	$\overline{RAS}$ Precharge Time		$t_{RP}$	60	—	65	—	70	—	80	—	ns
12	$\overline{RAS}$ Pulse Width		$t_{RAS}$	70	100000	80	100000	100	100000	120	100000	ns
13	$\overline{RAS}$ Hold Time		$t_{RSH}$	25	—	25	—	25	—	35	—	ns
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		$t_{CRP}$	0	—	0	—	0	—	0	—	ns
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	11,12	$t_{RCD}$	20	45	22	55	25	75	25	85	ns
16	$\overline{CAS}$ Pulse Width		$t_{CAS}$	25	—	25	—	25	—	35	—	ns
17	$\overline{CAS}$ Hold Time		$t_{CSH}$	70	—	80	—	100	—	120	—	ns
18	$\overline{CAS}$ Precharge Time (C-B-R cycle)	17	$t_{CPN}$	10	—	10	—	10	—	15	—	ns
19	Row Address Set Up Time		$t_{ASR}$	0	—	0	—	0	—	0	—	ns
20	Row Address Hold Time		$t_{RAH}$	10	—	12	—	15	—	15	—	ns
21	Column Address Set Up Time		$t_{ASC}$	0	—	0	—	0	—	0	—	ns
22	Column Address Hold Time		$t_{CAH}$	15	—	15	—	15	—	20	—	ns
23	$\overline{RAS}$ to Column Address Delay Time	13	$t_{RAD}$	15	27	17	35	20	50	20	60	ns
24	Column Address to $\overline{RAS}$ Lead Time		$t_{RAL}$	43	—	45	—	50	—	60	—	ns
25	Read Command Set Up Time		$t_{RCS}$	0	—	0	—	0	—	0	—	ns
26	Read Command Hold Time Referenced to $\overline{RAS}$	14	$t_{RRH}$	0	—	0	—	0	—	0	—	ns
27	Read Command Hold Time Referenced to $\overline{CAS}$	14	$t_{RCH}$	0	—	0	—	0	—	0	—	ns
28	Write Command Set Up Time	15	$t_{WCS}$	0	—	0	—	0	—	0	—	ns
29	Write Command Hold Time		$t_{WCH}$	15	—	15	—	15	—	20	—	ns
30	$\overline{WE}$ Pulse Width		$t_{WP}$	15	—	15	—	15	—	20	—	ns
31	Write Command to $\overline{RAS}$ Lead Time		$t_{RWL}$	22	—	22	—	25	—	30	—	ns
32	Write Command to $\overline{CAS}$ Lead Time		$t_{CWL}$	17	—	17	—	20	—	25	—	ns
33	DIN Set Up Time		$t_{DS}$	0	—	0	—	0	—	0	—	ns
34	DIN Hold Time		$t_{DH}$	15	—	15	—	15	—	20	—	ns

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## AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

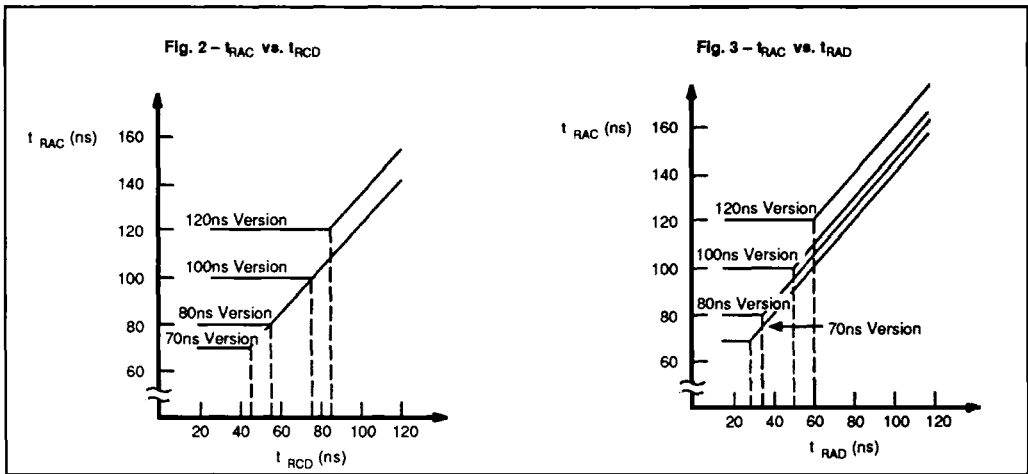
No.	Parameter	Notes	Symbol	MB81C1001-70		MB81C1001-80		MB81C1001-10		MB81C1001-12		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
35	RAS to WE Delay Time	15	$t_{RWD}$	70	—	80	—	100	—	120	—	ns
36	CAS to WE Delay Time	15	$t_{CWD}$	25	—	25	—	25	—	35	—	ns
37	Column Address to WE Delay Time	15	$t_{AWD}$	43	—	45	—	50	—	60	—	ns
38	RAS Precharge Time to CAS Active Time (Refresh Cycles)		$t_{RPC}$	0	—	0	—	0	—	0	—	ns
39	CAS Set Up Time for CAS-before-RAS Refresh		$t_{CSR}$	0	—	0	—	0	—	0	—	ns
40	CAS Hold Time for CAS-before-RAS Refresh		$t_{CHR}$	15	—	15	—	15	—	20	—	ns
41	Access Time from CAS (Counter Test Cycle)		$t_{CAT}$	—	43	—	45	—	50	—	60	ns
50	Nibble Mode Read/Write Cycle Time		$t_{NC}$	45	—	45	—	45	—	60	—	ns
51	Nibble Mode Read-Modify-Write Cycle Time		$t_{NRWC}$	67	—	67	—	70	—	85	—	ns
52	Access Time from CAS Precharge	9,16	$t_{NPA}$	—	40	—	40	—	40	—	55	ns
53	Nibble Mode CAS Precharge Time		$t_{NCP}$	10	—	10	—	10	—	15	—	ns

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### Notes:

- Referenced to VSS
- ICC depends on the output load conditions and cycle rates; The specified values are obtained with the output open.  
 ICC depends on the number of address change as  $\overline{RAS} = V_{IL}$  and  $\overline{CAS} = V_{IH}$ .  
 $ICC_1$ ,  $ICC_3$  and  $ICC_5$  are specified at three time of address change during  $\overline{RAS} = V_{IL}$  and  $\overline{CAS} = V_{IH}$ .  
 $ICC_4$  is specified at one time of address change during  $\overline{RAS} = V_{IL}$  and  $\overline{CAS} = V_{IH}$ .
- An Initial pause ( $\overline{RAS} = \overline{CAS} = V_{IH}$ ) of 200 $\mu$ s is required after power-up followed by any eight  $\overline{RAS}$ -only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight  $\overline{CAS}$ -before- $\overline{RAS}$  initialization cycles instead of 8  $\overline{RAS}$  cycles are required.
- AC characteristics assume  $t_f = 5$ ns.
- $V_{IH}$  (min) and  $V_{IL}$  (max) are reference levels for measuring timing of input signals. Also transition times are measured between  $V_{IH}$  (min) and  $V_{IL}$  (max).
- Assumes that  $t_{RCD} \leq t_{RCD}(\max)$ ,  $t_{RAD} \leq t_{RAD}(\max)$ . If  $t_{RCD}$  is greater than the maximum recommended value shown in this table,  $t_{RAC}$  will be increased by the amount that  $t_{RCD}$  exceeds the value shown. Refer to Fig. 2 and 3.
- If  $t_{RCD} \geq t_{RCD}(\max)$ ,  $t_{RAD} \geq t_{RAD}(\max)$ , and  $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$ , access time is  $t_{CAC}$ .
- If  $t_{RAD} \geq t_{RAD}(\max)$  and  $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$ , access time is  $t_{AA}$ .
- Measured with a load equivalent to two TTL loads and 100 pF.
- $t_{OFF}$  and  $t_{OEZ}$  is specified that output buffer change to high impedance state.
- Operation within the  $t_{RCD}(\max)$  limit ensures that  $t_{RAC}(\max)$  can be met.  $t_{RCD}(\max)$  is specified as a reference point only; if  $t_{RCD}$  is greater than the specified  $t_{RCD}(\max)$  limit, access time is controlled exclusively by  $t_{CAC}$  or  $t_{AA}$ .
- $t_{RCD}(\min) = t_{RAH}(\min) + 2t_T + t_{ASC}(\min)$ .
- Operation within the  $t_{RAD}(\max)$  limit ensures that  $t_{RAC}(\max)$  can be met.  $t_{RAD}(\max)$  is specified as a reference point only; if  $t_{RAD}$  is greater than the specified  $t_{RAD}(\max)$  limit, access time is controlled exclusively by  $t_{CAC}$  or  $t_{AA}$ .
- Either  $t_{RRH}$  or  $t_{RCH}$  must be satisfied for a read cycle.
- $t_{WCS}$ ,  $t_{CWD}$ ,  $t_{RWD}$  and  $t_{AWD}$  are not a restrictive operating parameter. They are included in the data sheet as an electrical characteristic only. If  $t_{WCS} > t_{WCS}(\min)$ , the cycle is an early write cycle and Dout pin will maintain high impedance state throughout the entire cycle. If  $t_{CWD} > t_{CWD}(\min)$ ,  $t_{RWD} > t_{RWD}(\min)$ , and  $t_{AWD} > t_{AWD}(\min)$ , the cycle is a read modify-write cycle and data from the selected cell will appear at the Dout pin. If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear the Dout pin, and write operation can be executed by satisfying  $t_{RWL}$ ,  $t_{CWL}$ , and  $t_{RAL}$  specifications.
- $t_{NPA}$  is access time from the selection of a new column address (that is caused by changing  $\overline{CAS}$  from "L" to "H"). Therefore, if  $t_{NCP}$  is long,  $t_{NPA}$  is longer than  $t_{NPA}(\max)$ .
- Assumes that  $\overline{CAS}$ -before- $\overline{RAS}$  refresh,  $\overline{CAS}$ -before- $\overline{RAS}$  refresh counter test cycle only.

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## FUNCTIONAL TRUTH TABLE

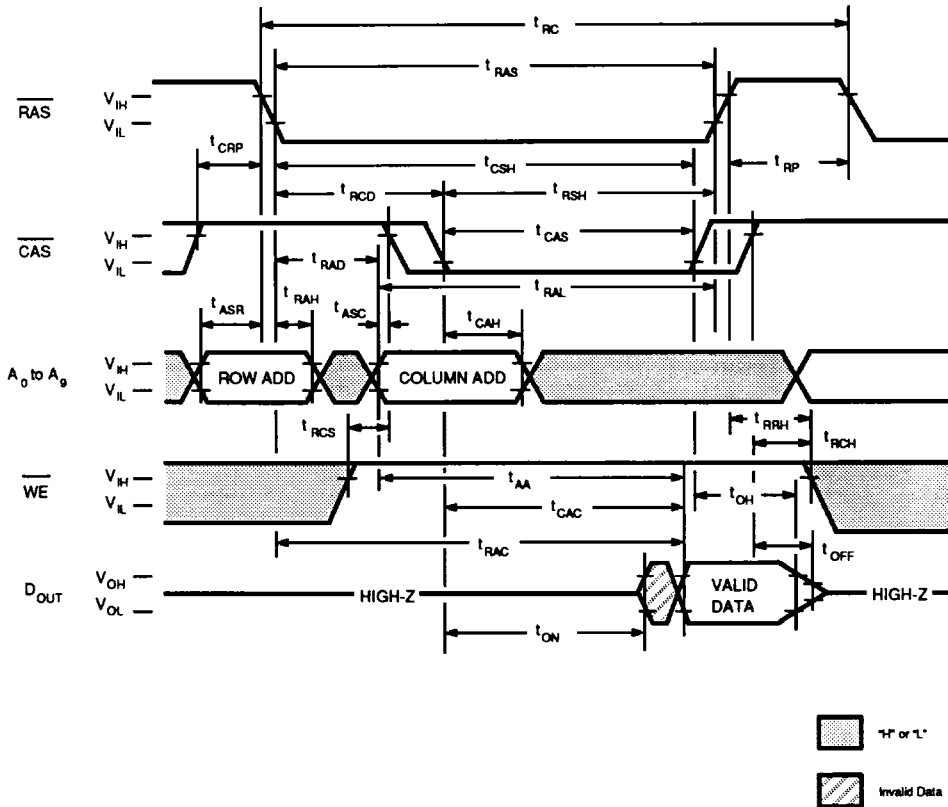
Operation Mode	Clock Input			Address Input		Data		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row	Column	Input	Output		
Standby	H	H	X	—	—	—	High-Z	—	
Read Cycle	L	L	H	Valid	Valid	—	Valid	Yes *1	$t_{RCS} \geq t_{RCS}(\text{min})$
Write Cycle (Early Write)	L	L	L	Valid	Valid	Valid	High-Z	Yes *1	$t_{WCS} \geq t_{WCS}(\text{min})$
Read-Modify-Write Cycle	L	L	H → L	Valid	Valid	X → Valid	Valid	Yes *1	$t_{CWD} \geq t_{CWD}(\text{min})$
RAS-only Refresh Cycle	L	H	X	Valid	—	—	High-Z	Yes	
$\overline{CAS}$ -before- $\overline{RAS}$ Refresh Cycle	L	L	X	—	—	—	High-Z	Yes	$t_{CSR} \geq t_{CSR}(\text{min})$
Hidden Refresh Cycle	H → L	L	X	—	—	—	Valid	Yes	Previous data is kept

**Notes:**

X: "H" or "L"

\*1: It is impossible in Nibble Mode.

Fig. 4 - READ CYCLE

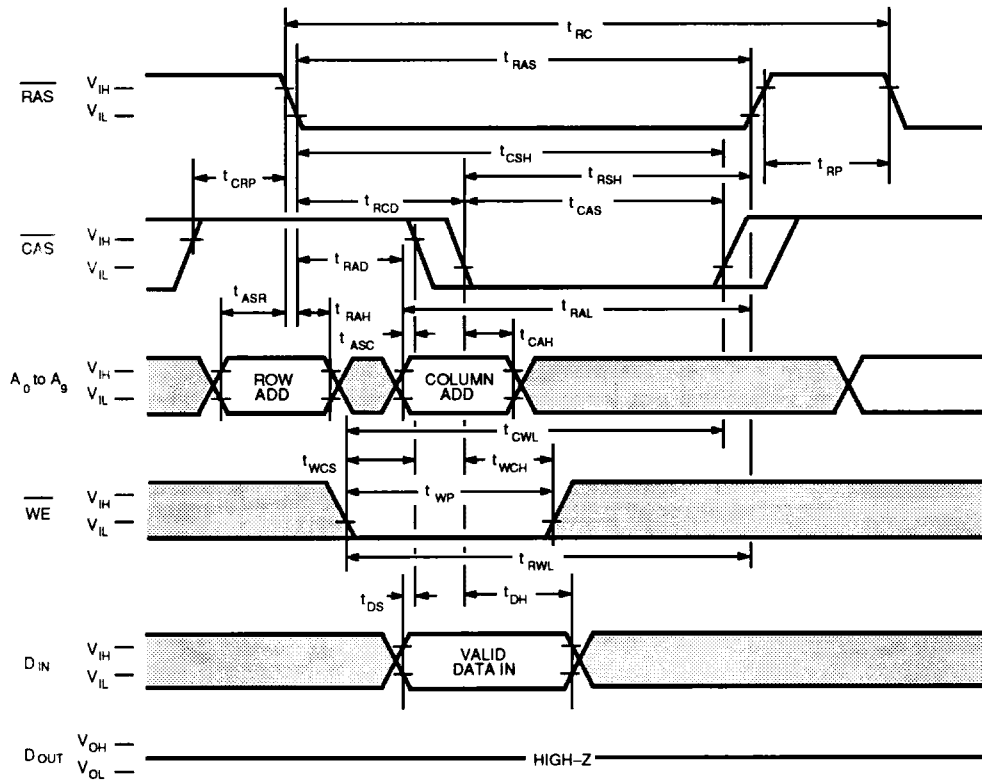


**DESCRIPTION**

The read cycle is executed by keeping both  $\overline{RAS}$  and  $\overline{CAS}$  "L" and keeping  $\overline{WE}$  "H" throughout the cycle. The row and column addresses are latched with  $\overline{RAS}$  and  $\overline{CAS}$ , respectively. The data output remains valid with  $\overline{CAS}$  "L", i.e., if  $\overline{CAS}$  goes "H", the data becomes invalid after  $t_{OH}$  is satisfied. The access time is determined by  $\overline{RAS}$  ( $t_{RAC}$ ),  $\overline{CAS}$  ( $t_{CAC}$ ), or Column address input ( $t_{AA}$ ). If  $t_{RCD}$  ( $\overline{RAS}$  to  $\overline{CAS}$  delay time) is greater than the specification, the access time is  $t_{AA}$ .

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 MB81C1001-12

Fig. 5 - WRITE CYCLE ( Early Write )



DESCRIPTION

The write cycle is executed by the same manner as read cycle except for the state of  $\overline{WE}$  and DIN pins. The data on DIN pin is latched with the later falling edge of CAS or WE and written into memory. In addition, during write cycle,  $t_{RWL}$  and  $t_{RAL}$  must be satisfied with the specifications.





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 MB81C1001-80  
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Fig. 7 - NIBBLE MODE READ CYCLE

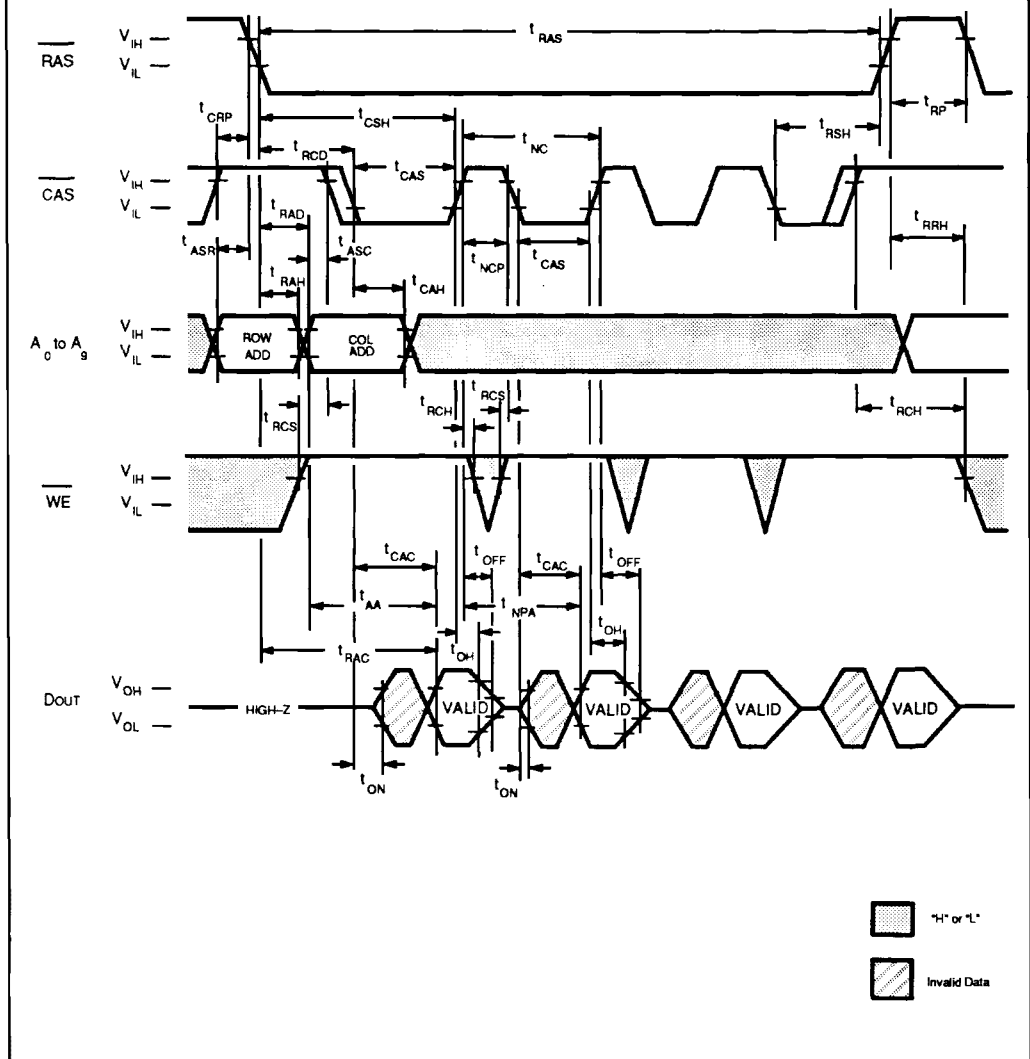
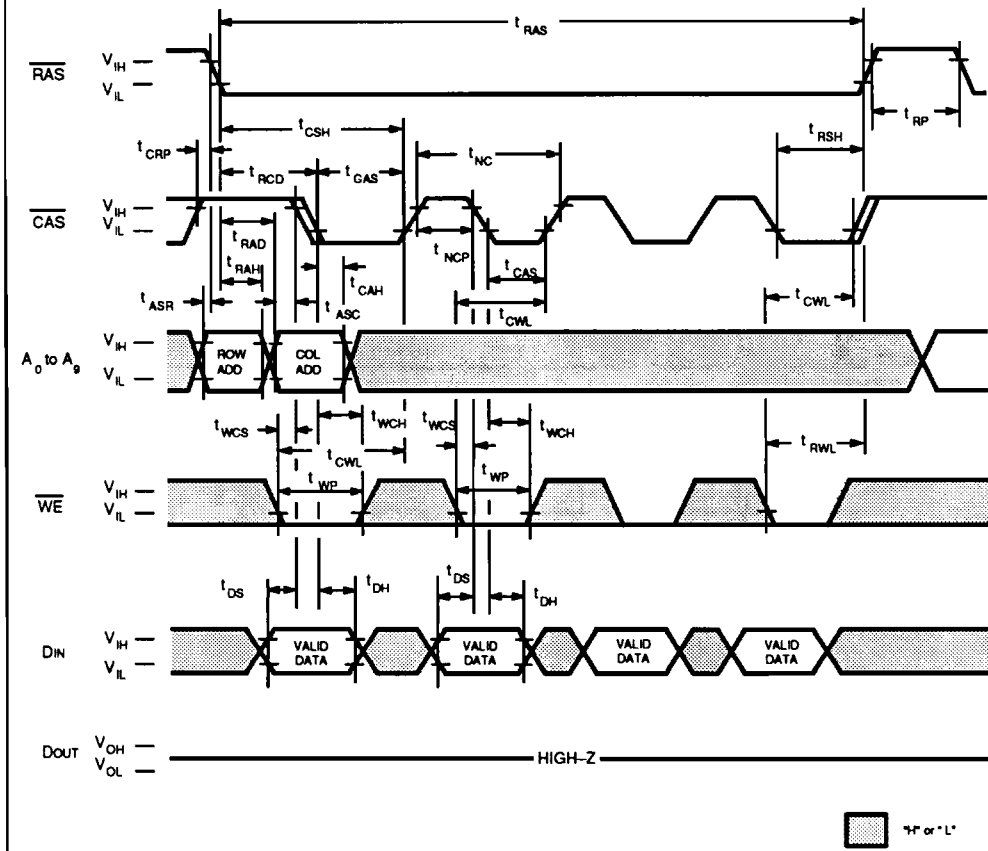


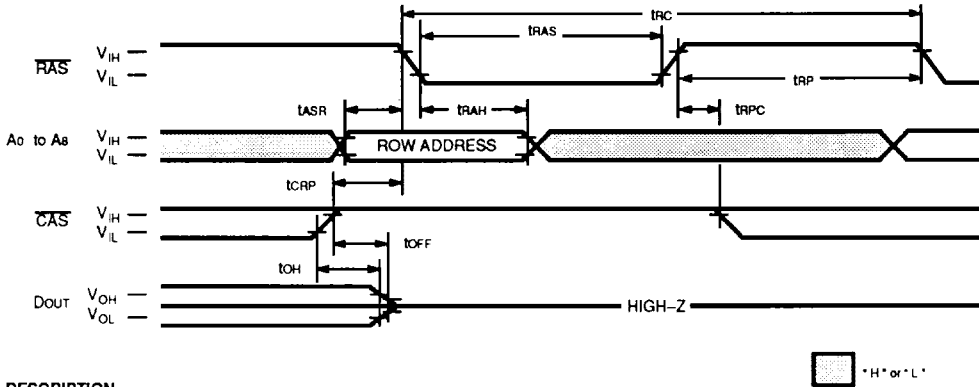
Fig. 8 - NIBBLE MODE WRITE CYCLE (Early Write)

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**Fig. 10 -  $\overline{\text{RAS}}$ -ONLY REFRESH CYCLE**  
 NOTE: A9,  $\overline{\text{WE}}$ , DIN = "H" or "L"



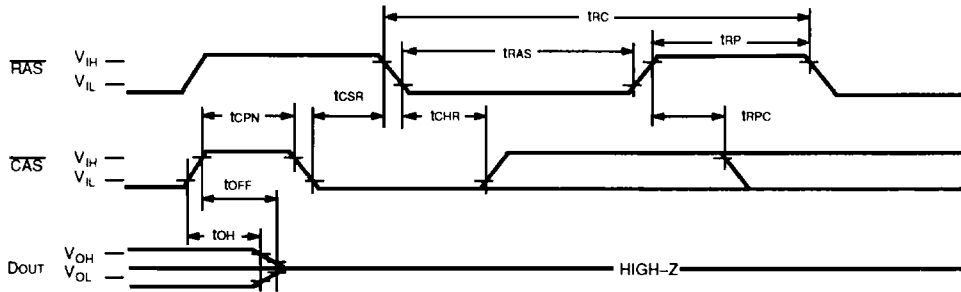
**DESCRIPTION**

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycle at each of 512 row addresses every 8.2-milliseconds. Three refresh modes are available:  $\overline{\text{RAS}}$ -only refresh,  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh, and hidden refresh.

$\overline{\text{RAS}}$ -only refresh is performed by keeping  $\overline{\text{RAS}}$  Low and  $\overline{\text{CAS}}$  High throughout the cycle; the row address to be refreshed is latched on the falling edge of  $\overline{\text{RAS}}$ . During  $\overline{\text{RAS}}$ -only refresh, DOUT pin is kept in a high-impedance state.

□ "H" or "L"

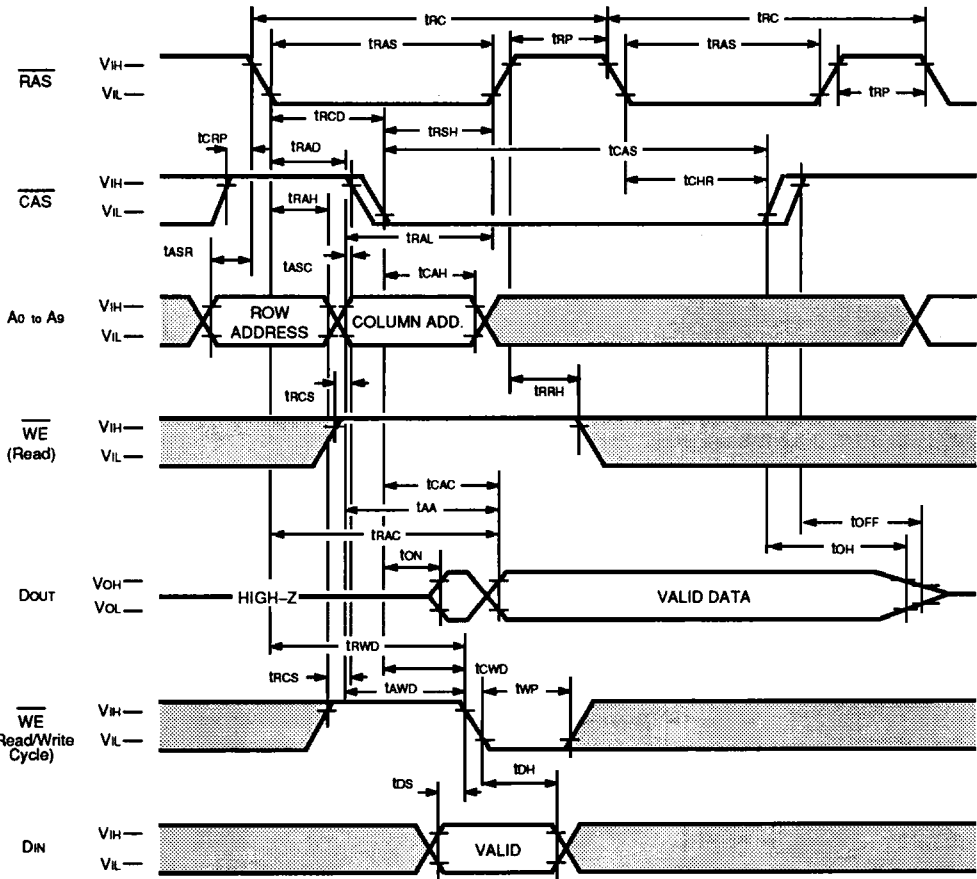
**Fig. 11 -  $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$  REFRESH CYCLE**  
 NOTE: A0 to A9,  $\overline{\text{WE}}$ , DIN = "H" or "L"



**DESCRIPTION**

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If  $\overline{\text{CAS}}$  is held Low for the specified setup time (tCSR) before  $\overline{\text{RAS}}$  goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh operation.

Fig. 12 – HIDDEN REFRESH CYCLE

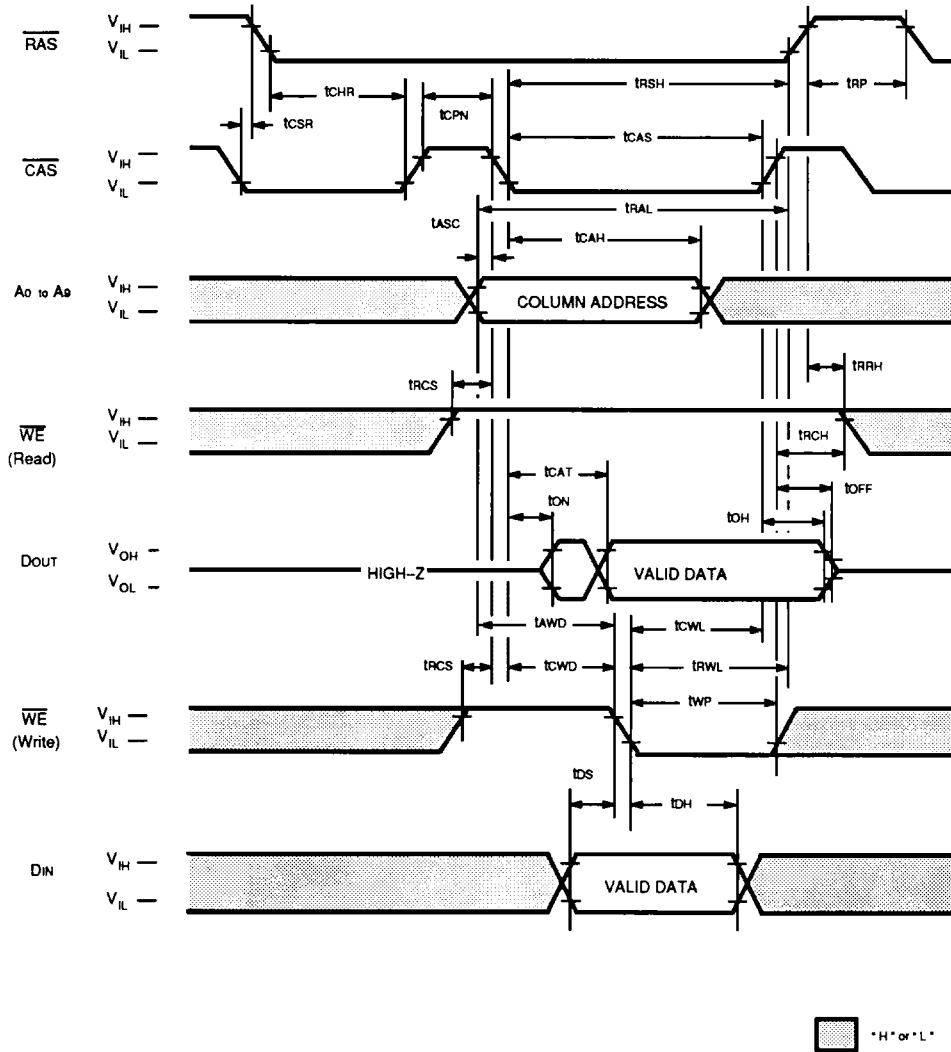


**DESCRIPTION**

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of  $\overline{CAS}$  and cycling  $\overline{RAS}$ . The refresh row address is provided by the on-chip refresh address counter. This eliminates the need for the external row address that is required by DRAMs that do not have  $\overline{CAS}$ -before- $\overline{RAS}$  refresh capability.

□ "H" or "L"

Fig. 13 -  $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$  REFRESH COUNTER TEST CYCLE

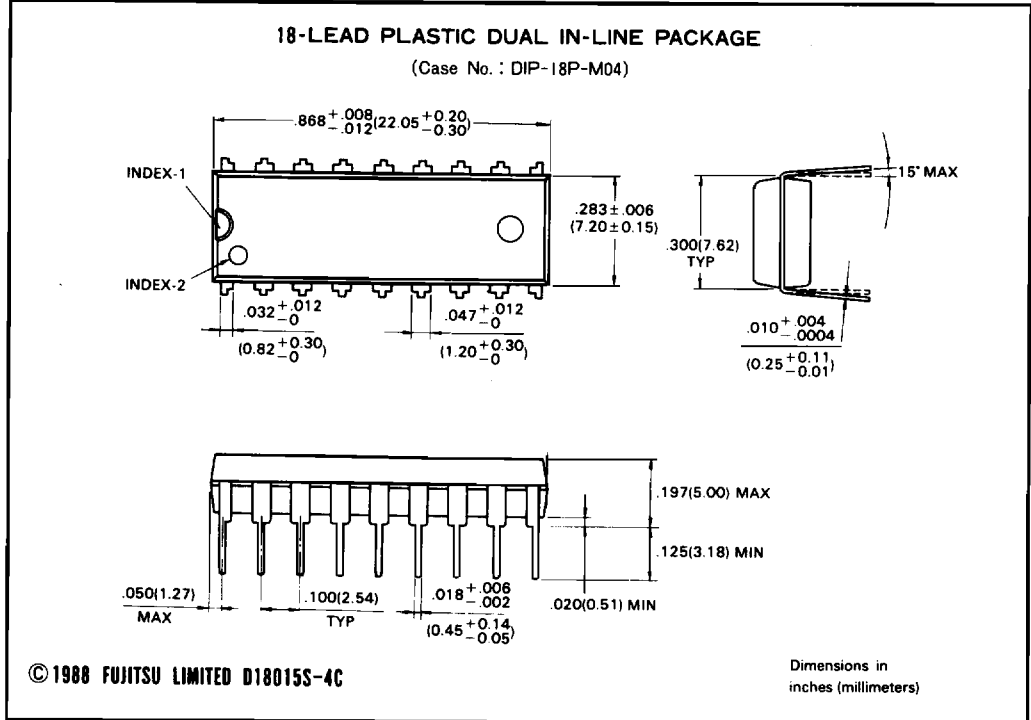


2

MB81C1001-70  
 MB81C1001-80  
 MB81C1001-10  
 MB81C1001-12

## PACKAGE DIMENSIONS

(Suffix: -P)

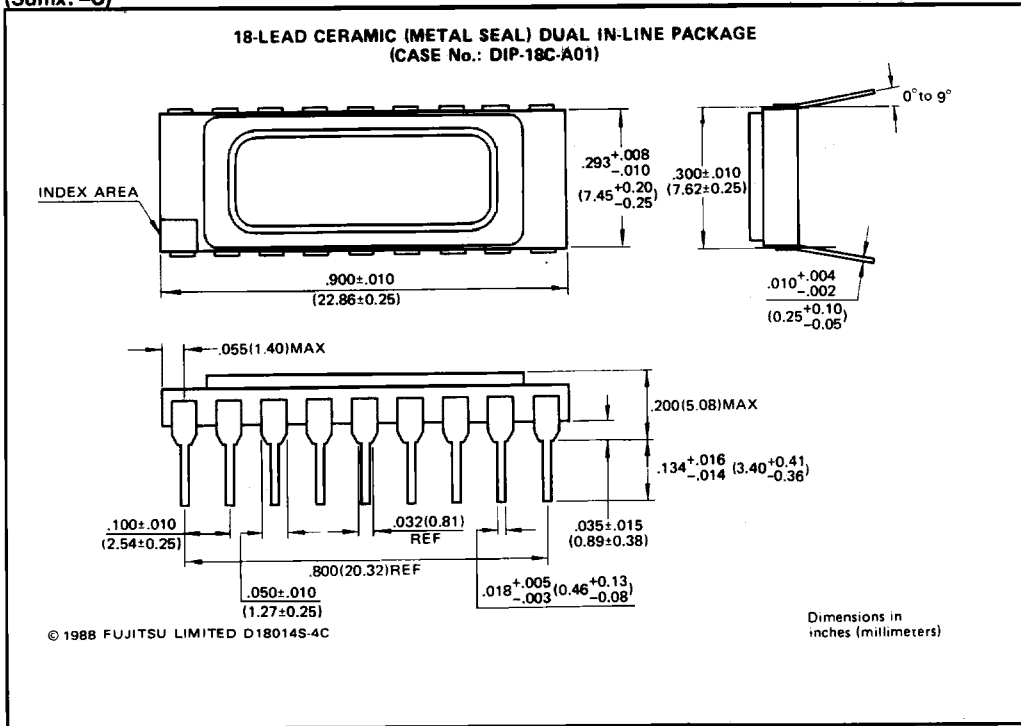


2

MB81C1001-70  
 MB81C1001-80  
 MB81C1001-10  
 MB81C1001-12

# PACKAGE DIMENSIONS (Continued)

(Suffix: -C)

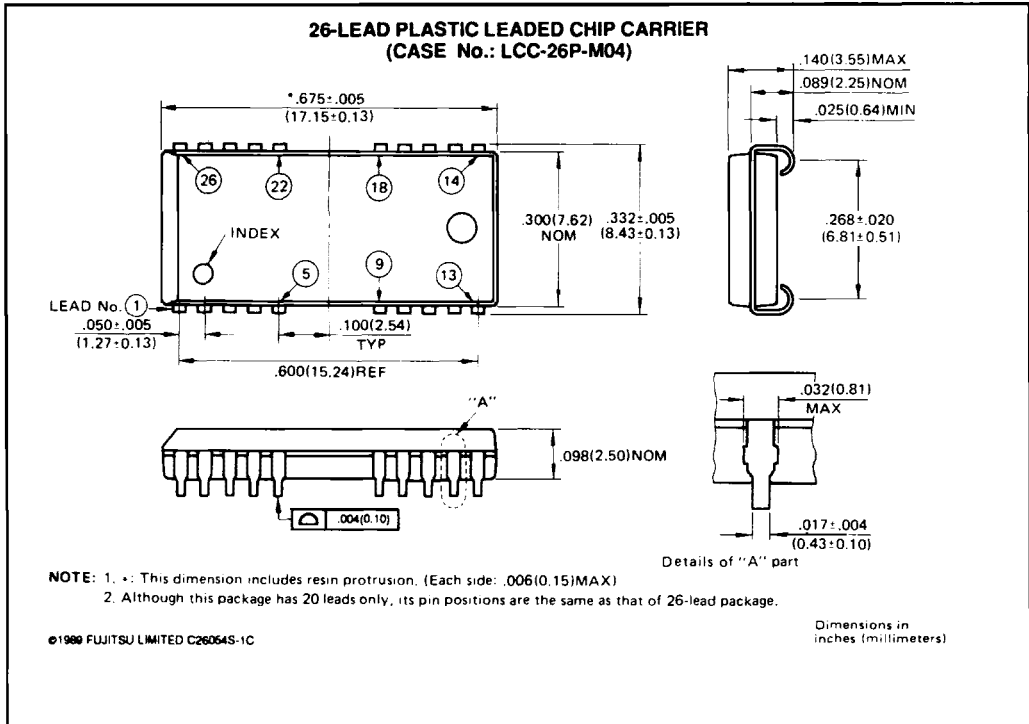


2

MB81C1001-70  
 MB81C1001-80  
 MB81C1001-10  
 MB81C1001-12

## PACKAGE DIMENSIONS (Continued)

(Suffix: -PJ)



2

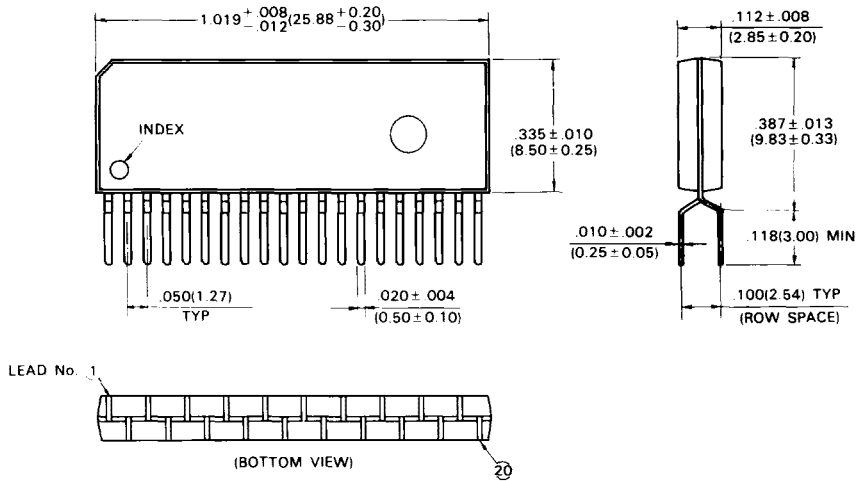
MB81C1001-70  
MB81C1001-80  
MB81C1001-10  
MB81C1001-12

## PACKAGE DIMENSIONS (Continued)

(Suffix: -PSZ)

### 20-LEAD PLASTIC ZIG-ZAG IN-LINE PACKAGE

(Case No. : ZIP-20P-M02)



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Dimensions in  
inches (millimeters)

2

