HM514280A/AL, HM51S4280A/AL Series Preliminary

262,144-Word x 18-Bit Dynamic Random Access Memory

■ DESCRIPTION

The Hitachi HM514280A/AL are CMOS dynamic RAM organized as 262,144-word x 18-bit. HM514280A/AL have realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514280A/AL offer fast page mode as a high speed access mode.

Multiplexed address input permits the HM514280A/AL to be packaged in standard 400 mil 40-pin plastic SOJ, standard 475 mil 40-pin plastic ZIP and standard 400 mil 40-pin plastic TSOPII.

Internal refresh timer enables HM51S4280A/AL self refresh operation.

■ FEATURES

- Single 5V (±10%)
- High Speed
  - Access Time ....70 ns/80 ns/100 ns (max)
- Low Power Dissipation
  - Active Mode ....825 mW/770 mW/688 mW (max)
  - Standby Mode ....11 mW (max)
    1.1 mW (max) (L-Version)
- Fast Page Mode Capability
- 512 Refresh Cycles ....8 ms
  128 ms (L-Version)
- 2 $\overline{\text{CAS}}$ Byte Control
- 2 Variations of Refresh
  - $\overline{\text{RAS}}$ Only Refresh
  - $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- Battery Back-up Operation (L-Version)
- Self-Refresh Operation (HM51S4280A/AL)

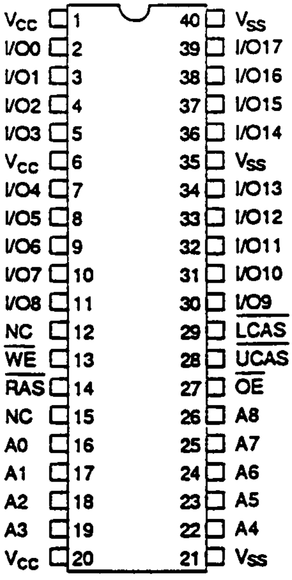
■ ORDERING INFORMATION

Part No.	Access Time	Package
HM514280AJ-7	70 ns	400 mil 40-pin Plastic SOJ (CP-40D)
HM514280AJ-8	80 ns	
HM514280AJ-10	100 ns	
HM514280AZ-7	70 ns	475 mil 40-pin Plastic ZIP (ZP-40)
HM514280AZ-8	80 ns	
HM514280AZ-10	100 ns	
HM514280ATT-7	70 ns	400 mil 40-pin Plastic TSOPII (TTP-40DB)
HM514280ATT-8	80 ns	
HM514280ATT-10	100 ns	
HM514280ARR-7	70 ns	400 mil 40-pin Plastic TSOPII (TTP-40DB)
HM514280ARR-8	80 ns	
HM514280ARR-10	100 ns	
HM514280ALJ-7	70 ns	400 mil 40-pin Plastic SOJ (CP-40D)
HM514280ALJ-8	80 ns	
HM514280ALJ-10	100 ns	
HM514280ALZ-7	70 ns	475 mil 40-pin Plastic ZIP (ZP-40)
HM514280ALZ-8	80 ns	
HM514280ALZ-10	100 ns	
HM514280ALTT-7	70 ns	400 mil 40-pin Plastic TSOPII (TTP-40DB)
HM514280ALTT-8	80 ns	
HM514280ALTT-10	100 ns	
HM514280ALRR-7	70 ns	400 mil 40-pin Plastic TSOPII (TTP-40DB)
HM514280ALRR-8	80 ns	
HM514280ALRR-10	100 ns	

Part No.	Access Time	Package
HM51S4280AJ-7	70 ns	400 mil 40-pin Plastic SOJ (CP-40D)
HM51S4280AJ-8	80 ns	
HM51S4280AJ-10	100 ns	
HM51S4280AZ-7	70 ns	475 mil 40-pin Plastic ZIP (ZP-40)
HM51S4280AZ-8	80 ns	
HM51S4280AZ-10	100 ns	
HM51S4280ATT-7	70 ns	400 mil 40-pin Plastic TSOPII (TTP-40DB)
HM51S4280ATT-8	80 ns	
HM51S4280ATT-10	100 ns	
HM51S4280ARR-7	70 ns	400 mil 40-pin Plastic TSOPII (TTP-40DB)
HM51S4280ARR-8	80 ns	
HM51S4280ARR-10	100 ns	
HM51S4280ALJ-7	70 ns	400 mil 40-pin Plastic SOJ (CP-40D)
HM51S4280ALJ-8	80 ns	
HM51S4280ALJ-10	100 ns	
HM51S4280ALZ-7	70 ns	475 mil 40-pin Plastic ZIP (ZP-40)
HM51S4280ALZ-8	80 ns	
HM51S4280ALZ-10	100 ns	
HM51S4280ALTT-7	70 ns	400 mil 40-pin Plastic TSOPII (TTP-40DB)
HM51S4280ALTT-8	80 ns	
HM51S4280ALTT-10	100 ns	
HM51S4280ALRR-7	70 ns	400 mil 40-pin Plastic TSOPII (TTP-40DB)
HM51S4280ALRR-8	80 ns	
HM51S4280ALRR-10	100 ns	

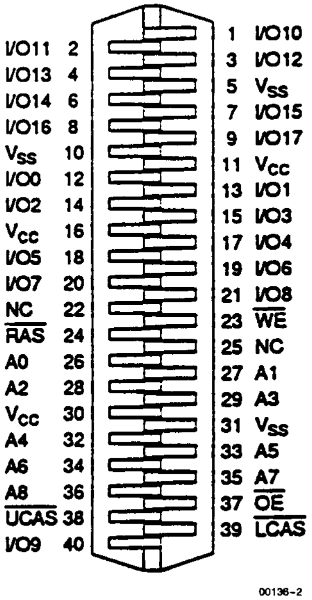
■ PIN ARRANGEMENT

HM514280AJ/ALJ Series
HM51S4280AJ/ALJ Series



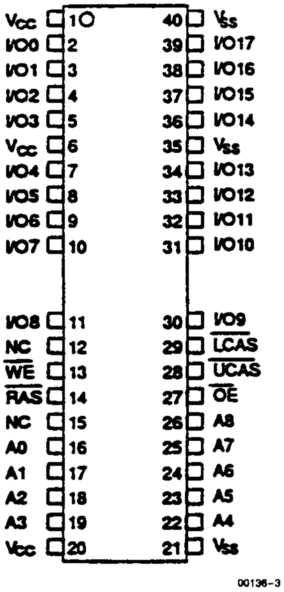
(Top View)

HM514280AZ/ALZ Series
HM51S4860AZ/ALZ Series



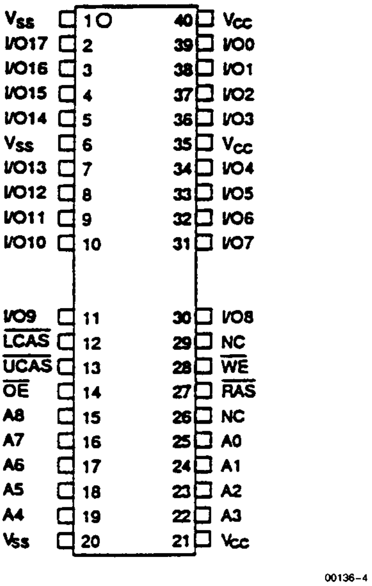
(Bottom View)

HM514280ATT/ALTT Series
HM51S4280ATT/ALTT Series



(Top View)

HM514280ARR/ALRR Series
HM51S4280ARR/ALRR Series

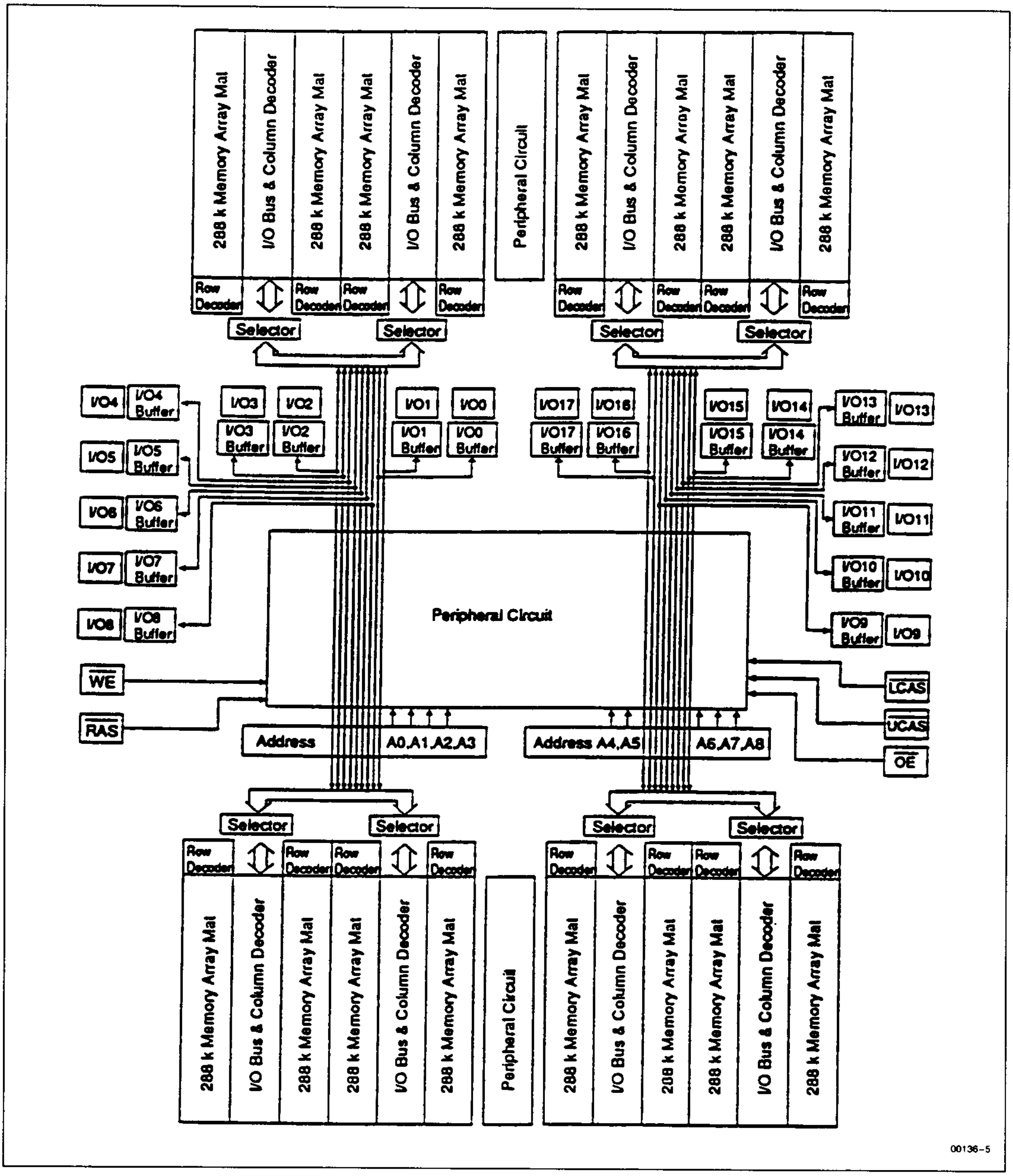


(Top View)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_8	Address Input —Row Address A_0–A_8 —Column Address A_0–A_8 —Refresh Address A_0–A_8
I/O_0–I/O_{17}	Data-in/Data-out
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$, $\overline{LCAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground

■ BLOCK DIAGRAM



TRUTH TABLE

Inputs					I/O		Operation
$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	$I/O_0-I/O_8$	$I/O_9-I/O_{17}$	
H	H	H	H	H	High-Z	High-Z	Standby
L	H	H	H	H	High-Z	High-Z	Refresh
L	L	H	H	L	D_{out}	High-Z	Lower Byte Read
L	H	L	H	L	High-Z	D_{out}	Upper Byte Read
L	L	L	H	L	D_{out}	D_{out}	Word Read
L	L	H	L	H	D_{in}	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	D_{in}	Upper Byte Write
L	L	L	L	H	D_{in}	D_{in}	Word Write
L	L	L	H	H	High-Z	High-Z	
H to L	L	H	—	—	High-Z	High-Z	CBR Refresh or Self Refresh
H to L	H	L	—	—	High-Z	High-Z	
H to L	L	L	—	—	High-Z	High-Z	

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	− 1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	− 1.0 to + 7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to + 70	°C
Storage Temperature	T_{stg}	− 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)[2]

Parameter		Symbol	Min	Typ	Max	Unit	Note
Supply Voltage		V_{SS}	0	0	0	V	
		V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage		V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	(I/O Pin)	V_{IL}	− 1.0	—	0.8	V	1
	(Others)	V_{IL}	− 2.0	—	0.8	V	1

Notes: 1. All voltage referenced to V_{SS}.
2. The supply voltage with all V_{CC} pins must be on the same level.
The supply voltage with all V_{SS} pins must be on the same level.

- **DC Electrical Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	HM514280A/AL-7 HM51S4280A/AL-7		HM514280A/AL-8 HM51S4280A/AL-8		HM514280A/AL-10 HM51S4280A/AL-10		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	150	—	140	—	125	mA	$\overline{RAS}$ Cycling $\overline{LCAS}$ or $\overline{UCAS}$ Cycling t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	2	—	2	—	2	mA	TTL Interface $\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$ = V_{IH}, D_{out} = High-Z	
		—	1	—	1	—	1	mA	CMOS Interface $\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{WE}$ $\overline{OE}$ ≥ V_{CC} − 0.2V, D_{out} = High-Z	
Standby Current (L-Version)		—	200	—	200	—	200	µA	CMOS Interface $\overline{RAS}$, $\overline{LCAS}$,$\overline{OE}$, $\overline{WE}$ $\overline{UCAS}$ ≥ V_{CC} − 0.2V D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	140	—	130	—	110	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH}, $\overline{LCAS}$ or $\overline{UCAS}$ = V_{IL}, D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	140	—	130	—	110	mA	t_{RC} = Min	25
Fast Page Mode Current	I_{CC7}	—	130	—	120	—	110	mA	t_{PC} = Min	1, 3
Self-Refresh Mode Current (HM51S4280A)	I_{CC9}	—	1	—	1	—	1	mA	CMOS Interface $\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$ ≤ 0.2V D_{out} = High-Z	
Self-Refresh Mode Current (HM51S4280AL)		—	200	—	200	—	200	µA	CMOS Interface $\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$ ≤ 0.2V D_{out} = High-Z	
Battery Back-up Current (Standby with CBR Refresh) (L-Version)	I_{CC10}	—	300	—	300	—	300	µA	Standby: CMOS Interface D_{out} = High-Z CBR Refresh: t_{RC} = 250 µs t_{RAS} ≤ 1 µs, $\overline{LCAS}$, $\overline{UCAS}$ = V_{IL} $\overline{WE}$, $\overline{OE}$ = V_{IH}	4
Input Leakage Current	I_{LI}	− 10	10	− 10	10	− 10	10	µA	0V ≤ V_{in} ≤ 6.5V	
Output Leakage Current	I_{LO}	− 10	10	− 10	10	− 10	10	µA	0V ≤ V_{out} ≤ 6.5V D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = − 5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2 mA	

Notes:
1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed ≤ 1 time while $\overline{RAS}$ = V_{IL}.
3. Address can be changed ≤ 1 time while $\overline{LCAS}$ and $\overline{UCAS}$ = V_{IH}.
4. V_{IH} ≥ V_{CC} − 0.2V, 0 ≤ V_{IL} ≤ 0.2V, Address can be changed ≤ 1 time while $\overline{RAS}$ = V_{IL}.
5. All the V_{CC} pins shall be supplied with the same voltage. And all the V_{SS} pins shall be supplied with the same voltage.

- **Capacitance** (T_A = 25°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Output Capacitance (Data-in, Data-out)	$C_{I/O}$	—	10	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ = V_{IH} to disable D_{out}.

- **AC Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)$^{1, 14, 15, 17, 18}$

Test Conditions

- Input rise and fall times: 5 ns
- Input timing reference levels: 0.8V, 2.4V
- Output load: 2 TTL gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM514280A/AL-7 HM51S4280A/AL-7		HM514280A/AL-8 HM51S4280A/AL-8		HM514280A/AL-10 HM51S4280A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	130	—	150	—	180	—	ns	
$\overline{\text{RAS}}$ Precharge Time	t_{RP}	50	—	60	—	70	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t_{RAS}	70	10000	80	10000	100	10000	ns	
$\overline{\text{CAS}}$ Pulse Width	t_{CAS}	20	10000	20	10000	25	10000	ns	23
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	ns	19
Column Address Hold Time	t_{CAH}	15	—	15	—	20	—	ns	19
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t_{RCD}	20	50	20	60	25	75	ns	8
$\overline{\text{RAS}}$ to Column Address Delay Time	t_{RAD}	15	35	15	40	20	55	ns	9
$\overline{\text{RAS}}$ Hold Time	t_{RSH}	20	—	20	—	25	—	ns	
$\overline{\text{CAS}}$ Hold Time	t_{CSH}	70	—	80	—	100	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t_{CRP}	15	—	15	—	15	—	ns	20, 24
$\overline{\text{OE}}$ to D_{in} Delay Time	t_{ODD}	20	—	20	—	25	—	ns	
$\overline{\text{OE}}$ Delay Time from D_{in}	t_{DZO}	0	—	0	—	0	—	ns	
$\overline{\text{CAS}}$ Setup Time from D_{in}	t_{DZC}	0	—	0	—	0	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	8	—	8	—	8	ms	
Refresh Period (L-Version)	t_{REF}	—	128	—	128	—	128	ms	

Read Cycle

Parameter	Symbol	HM514280A/AL-7 HM51S4280A/AL-7		HM514280A/AL-8 HM51S4280A/AL-8		HM514280A/AL-10 HM51S4280A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	70	—	80	—	100	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	ns	3, 4, 13
Access Time from Address	t_{AA}	—	35	—	40	—	45	ns	3, 5, 13
Access Time from $\overline{OE}$	t_{OAC}	—	20	—	20	—	25	ns	23
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	19
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	16, 19
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	ns	16
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	35	—	40	—	45	—	ns	
Output Buffer Turn-off Time	t_{OFF1}	0	15	0	15	0	20	ns	6
Output Buffer Turn-off to $\overline{OE}$	t_{OFF2}	0	15	0	15	0	20	ns	6
$\overline{CAS}$ to D_{in} Delay Time	t_{CDD}	15	—	15	—	20	—	ns	

Write Cycle

Parameter	Symbol	HM514280A/AL-7 HM51S4280A/AL-7		HM514280A/AL-8 HM51S4280A/AL-8		HM514280A/AL-10 HM51S4280A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	ns	10, 19
Write Command Hold Time	t_{WCH}	15	—	15	—	20	—	ns	20
Write Command Pulse Width	t_{WP}	10	—	10	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	—	20	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	20	—	20	—	25	—	ns	21
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	ns	11, 19
Data-in Hold Time	t_{DH}	15	—	15	—	20	—	ns	11, 19
$\overline{CAS}$ to $\overline{OE}$ Delay Time	t_{COD}	—	0	—	0	—	0	ns	23

Read-Modify-Write Cycle

Parameter	Symbol	HM514280A/AL-7 HM51S4280A/AL-7		HM514280A/AL-8 HM51S4280A/AL-8		HM514280A/AL-10 HM51S4280A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Read-Modify-Write Cycle Time	t_{RWC}	180	—	200	—	245	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	95	—	105	—	135	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	45	—	45	—	60	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	60	—	65	—	80	—	ns	10, 13
$\overline{OE}$ Hold Time from $\overline{WE}$	t_{OEH}	20	—	20	—	25	—	ns	

Refresh Cycle

Parameter	Symbol	HM514280A/AL-7 HM51S4280A/AL-7		HM514280A/AL-8 HM51S4280A/AL-8		HM514280A/AL-10 HM51S4280A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{\text{CAS}}$ Setup Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	ns	19
$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle)	t_{CHR}	10	—	10	—	10	—	ns	20
$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Hold Time	t_{RPC}	10	—	10	—	10	—	ns	19
$\overline{\text{CAS}}$ Precharge Time in Normal Mode	t_{CPN}	10	—	10	—	10	—	ns	22

Fast Page Mode Cycle

Parameter	Symbol	HM514280A/AL-7 HM51S4280A/AL-7		HM514280A/AL-8 HM51S4280A/AL-8		HM514280A/AL-10 HM51S4280A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	50	—	55	—	60	—	ns	24
Fast Page Mode $\overline{\text{CAS}}$ Precharge Time	t_{CP}	15	—	15	—	15	—	ns	22, 24
Fast Page Mode $\overline{\text{RAS}}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	ns	12
Access Time from $\overline{\text{CAS}}$ Precharge	t_{ACP}	—	40	—	45	—	50	ns	3, 13, 20
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t_{RHCP}	40	—	45	—	50	—	ns	
Fast Page Mode Read-Modify-Write Cycle $\overline{\text{CAS}}$ Precharge to $\overline{\text{WE}}$ Delay Time	t_{CPW}	65	—	70	—	85	—	ns	
Fast Page Mode Read-Modify-Write Cycle Time	t_{PCM}	95	—	100	—	110	—	ns	

Self-Refresh Mode

Parameter	Symbol	HM51S4280A/AL-7		HM51S4280A/AL-8		HM51S4280A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{\text{RAS}}$ Pulse Width (Self-Refresh)	t_{RASS}	100	—	100	—	100	—	µs	
$\overline{\text{RAS}}$ Precharge Time (Self-Refresh)	t_{RPS}	130	—	150	—	180	—	ns	
$\overline{\text{CAS}}$ Hold Time (Self-Refresh)	t_{CHS}	0	—	0	—	0	—	ns	21

Notes:

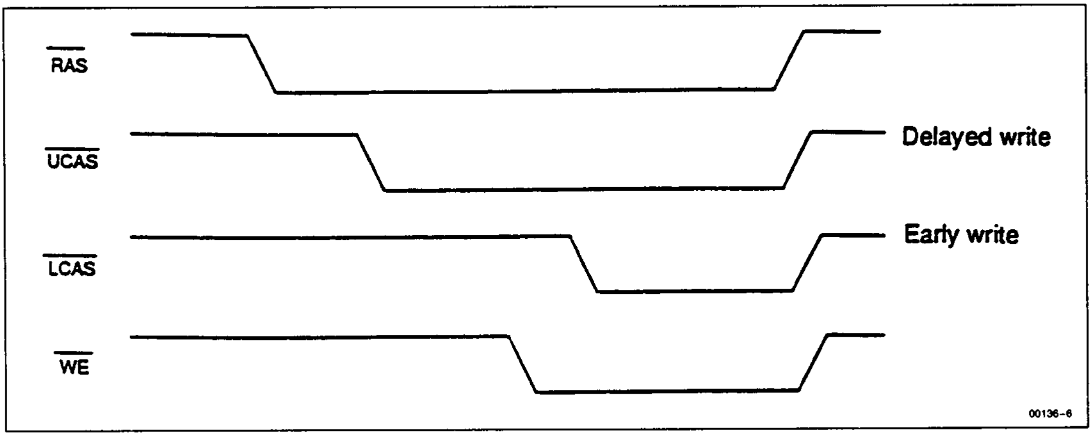
1. AC measurements assume t_T = 5 ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD} t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycle.
12. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100 µs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ refresh cycles is required.
15. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
16. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
17. When both, $\overline{LCAS}$ and $\overline{UCAS}$ go low at the same time, all 16-bits data are written into the device. $\overline{LCAS}$ and $\overline{UCAS}$ cannot be straggered within the same write/read cycles.
18. All the V_{CC} and V_{SS} pins shall be supplied with the same voltages.
19. t_{ASC}, t_{CAH}, t_{RCS}, t_{RCH}, t_{WCS}, t_{WCH}, t_{DS}, t_{DH}, t_{CSR}, and t_{RPC} are determined by the earlier falling edge of $\overline{UCAS}$ or $\overline{LCAS}$.
20. t_{CRP}, t_{CHR}, t_{ACP}, and t_{CPW} are determined by the later rising edge of $\overline{UCAS}$ or $\overline{LCAS}$.
21. t_{CWL} and t_{CHS} should be satisfied by both $\overline{UCAS}$ and $\overline{LCAS}$.
22. t_{CPN}, and t_{CP} are determined by the time that both $\overline{UCAS}$ and $\overline{LCAS}$ are high.
23. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large V_{CC}/V_{SS} line noise, which causes to degrade V_{IH} min/V_{IL} max level.
24. t_{CRP}, t_{PC} and t_{CP} are planned to be improved to match the standard DRAM specifications.
25. If you use distributed CBR refresh mode with 15.6 µs interval in normal read/write cycle, CBR refresh should be executed within 15.6 µs immediately after exiting from and before entering into self refresh mode.
26. If you use $\overline{RAS}$ only refresh or CBR burst refresh mode in normal read/write cycle, 512 cycles of distributed CBR refresh with 15.6 µs interval should be executed within 8 ms immediately after exiting from and before entering into the self refresh mode.
27. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self fresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.

Notes concerning 2$\overline{\text{CAS}}$ control

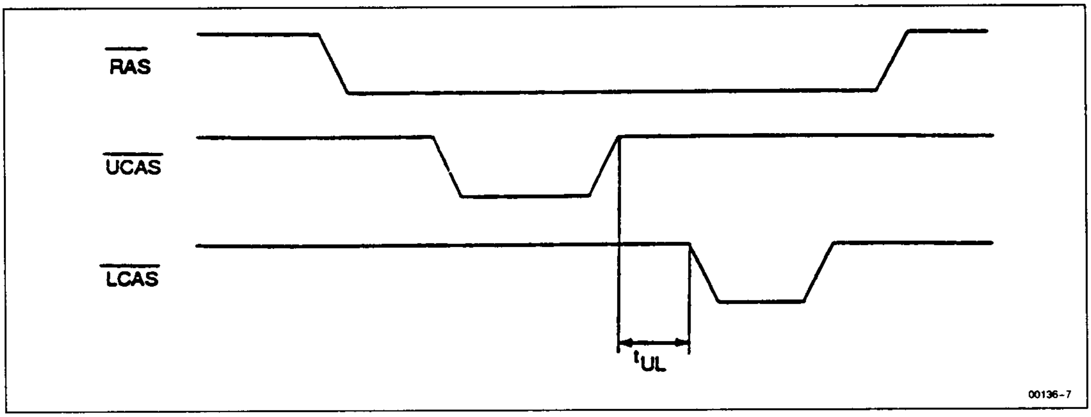
Please do not separate the $\overline{\text{UCAS}}$/$\overline{\text{LCAS}}$ operation timing intentionally. However skew between $\overline{\text{UCAS}}$/$\overline{\text{LCAS}}$ are allowed under the following conditions.

(1) Each of the $\overline{\text{UCAS}}$/$\overline{\text{LCAS}}$ should satisfy the timing specifications individually.

(2) Different operation mode for upper/lower byte is not allowed; such as following.

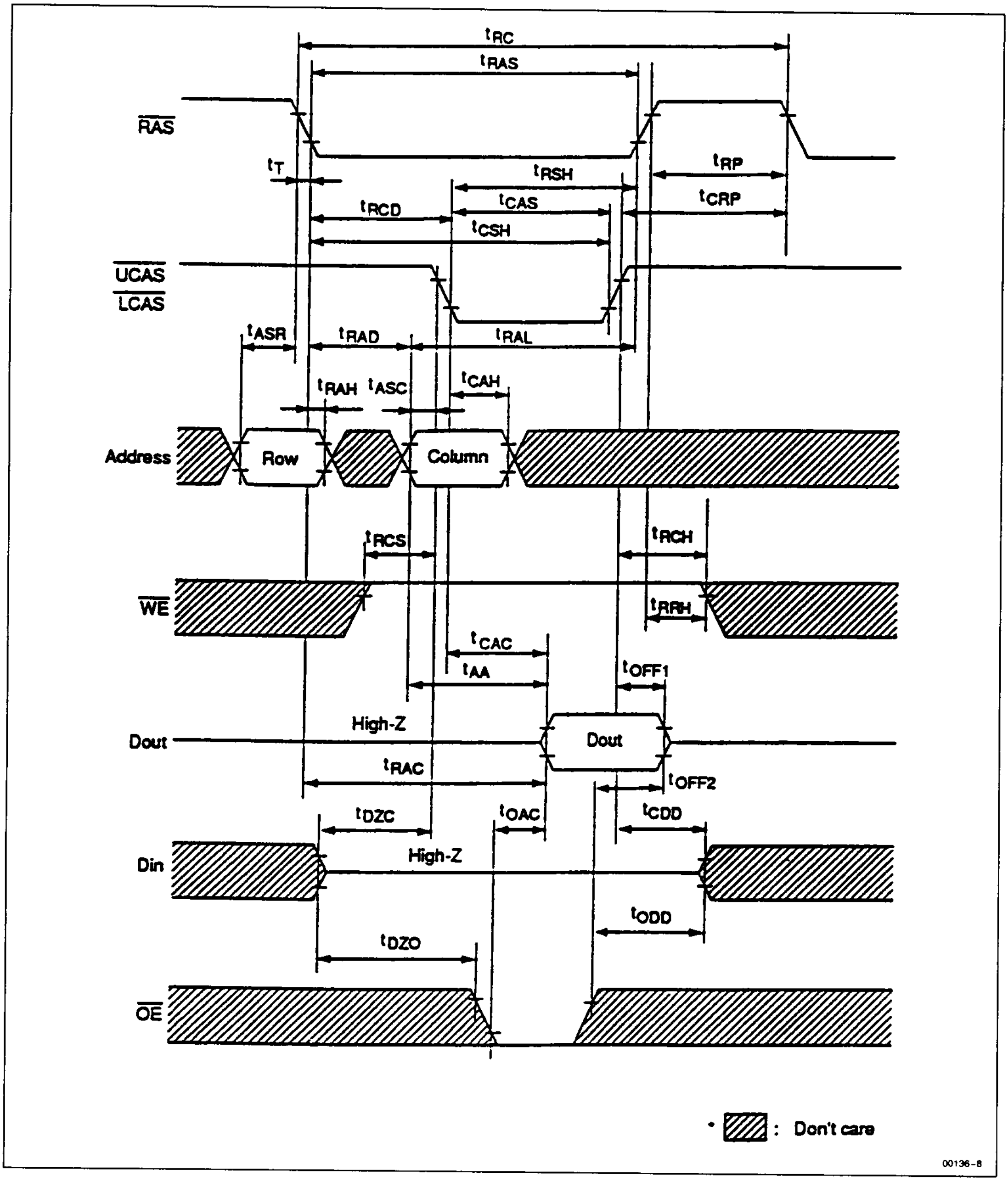


(3) Closely separated upper/lower byte control is not allowed. However when the condition ($t_{CP} \le t_{UL}$) is satisfied, fast page mode can be performed.

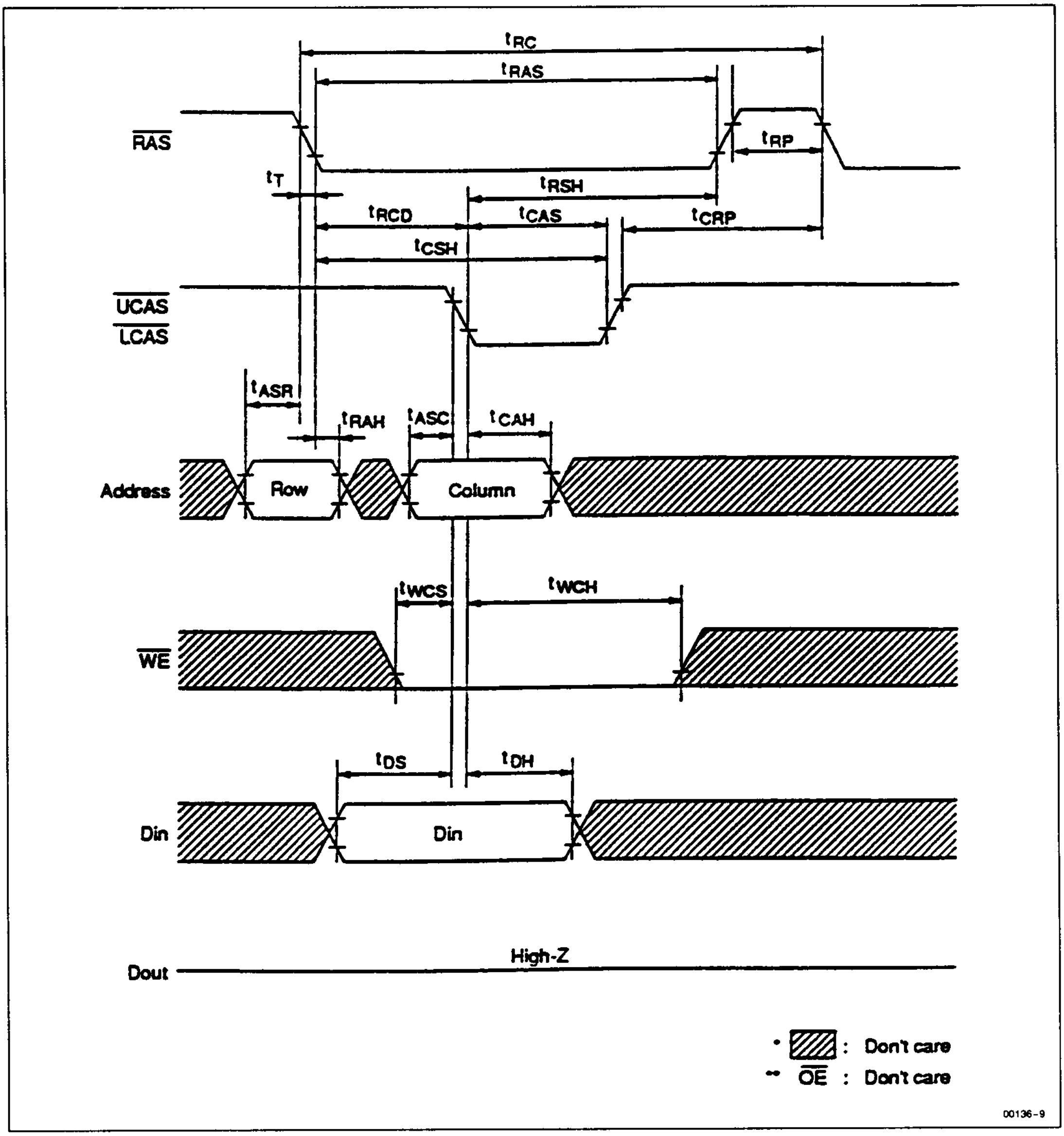


■ TIMING WAVEFORMS

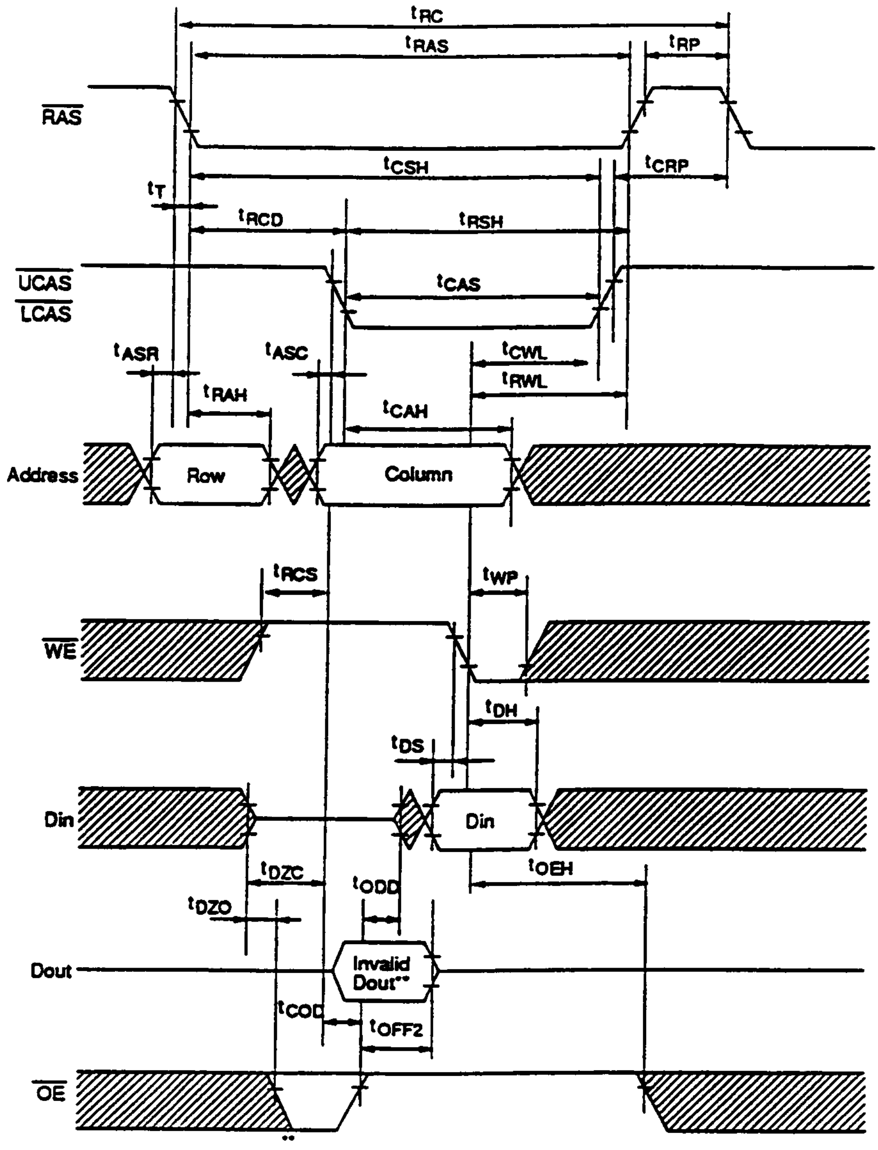
- **Read Cycle**



- **Early Write Cycle**



- **Delayed Write Cycle**

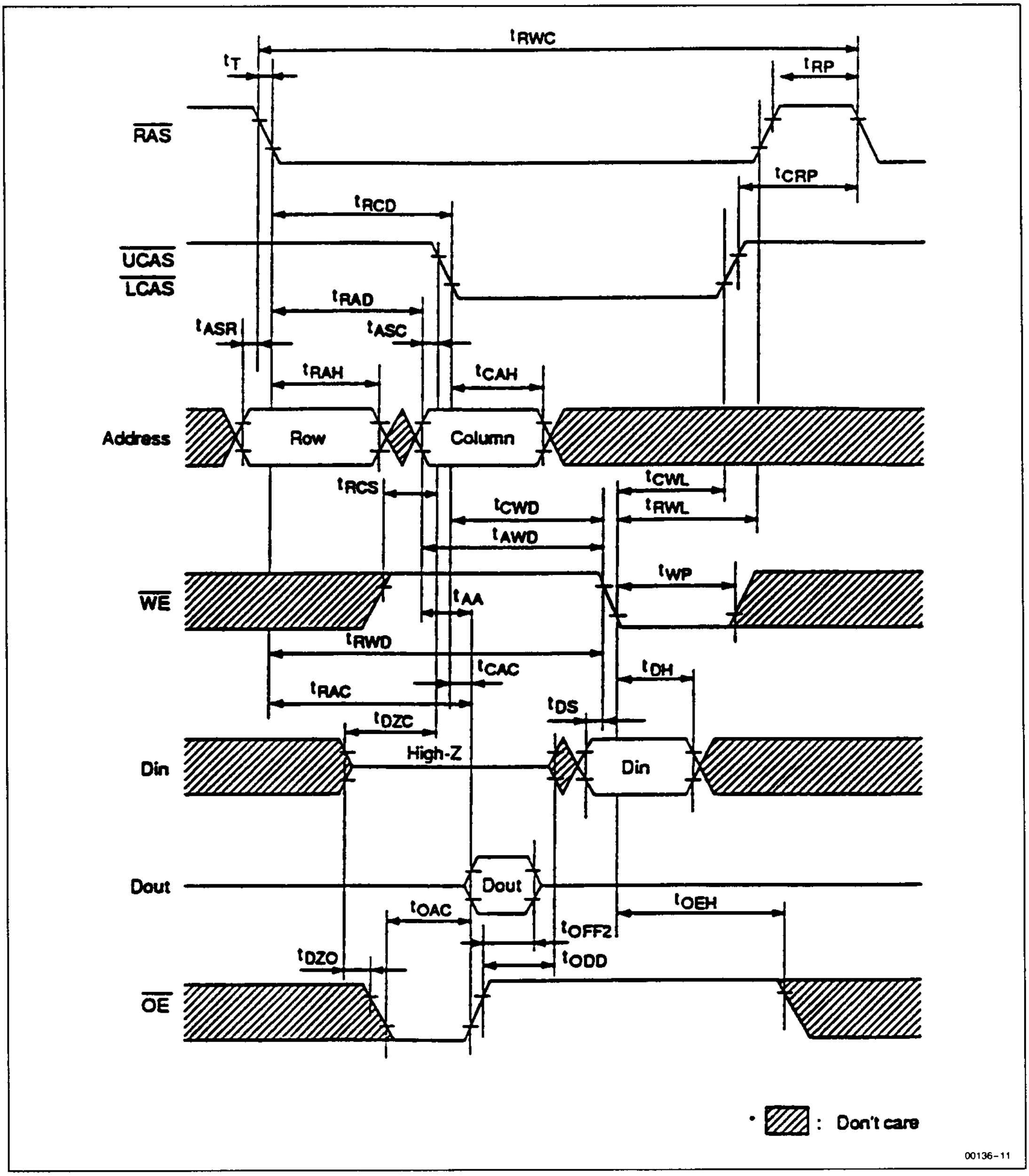


- ▨ : Don't care

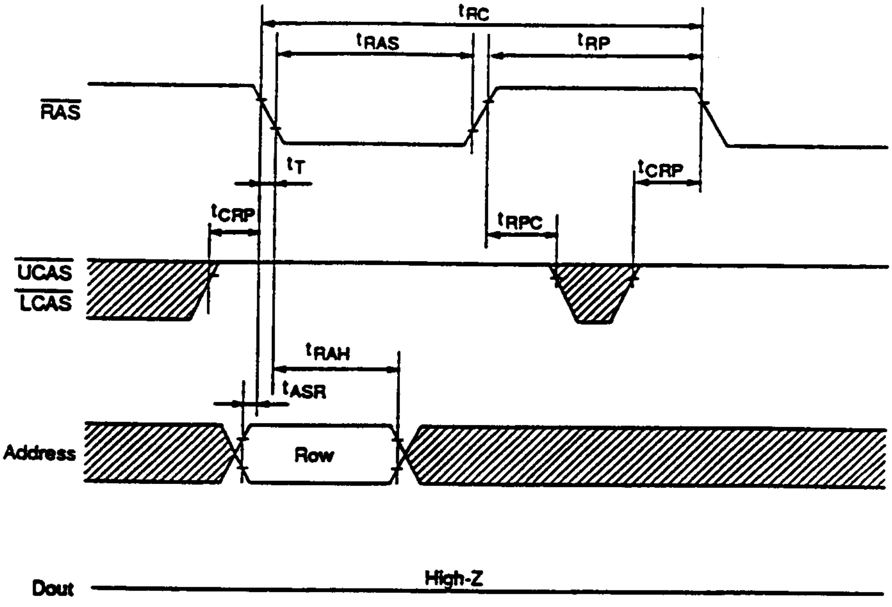
** Invalid Dout comes out, when $\overline{\text{OE}}$ is low level.

00136-10

- **Read-Modify-Write Cycle**



- **$\overline{\text{RAS}}$ Only Refresh Cycle**



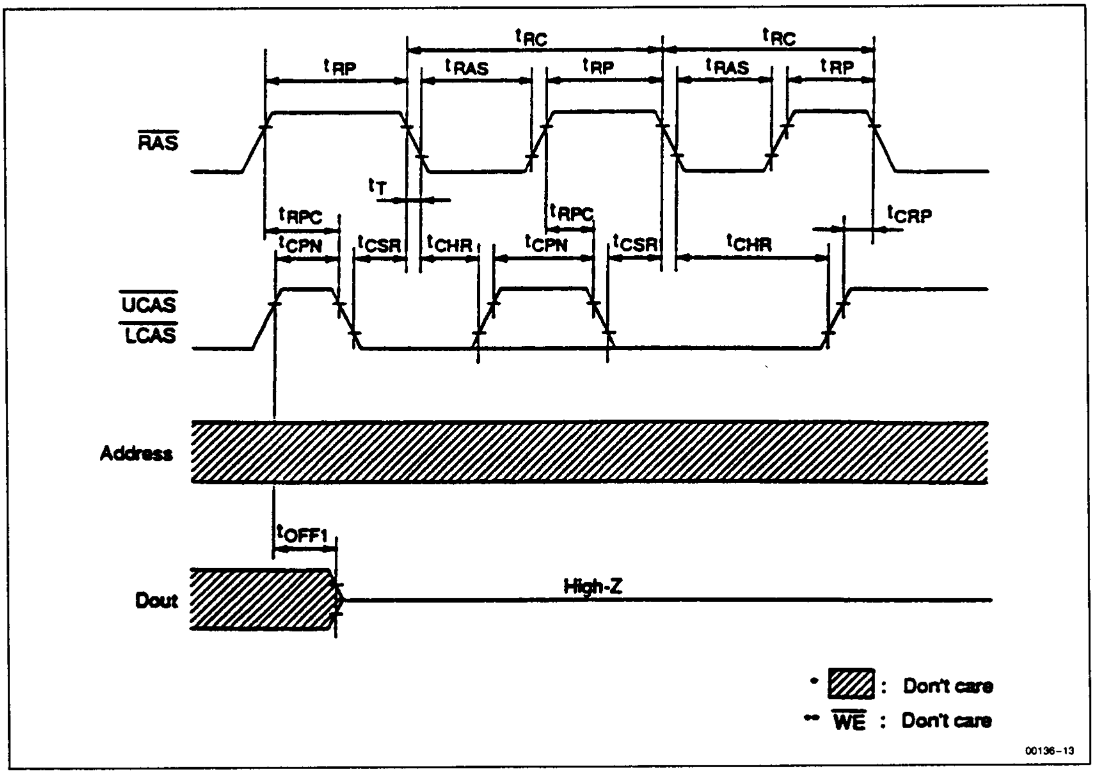
* $\overline{\text{OE}}$, $\overline{\text{WE}}$: Don't care

** ▨ : Don't care

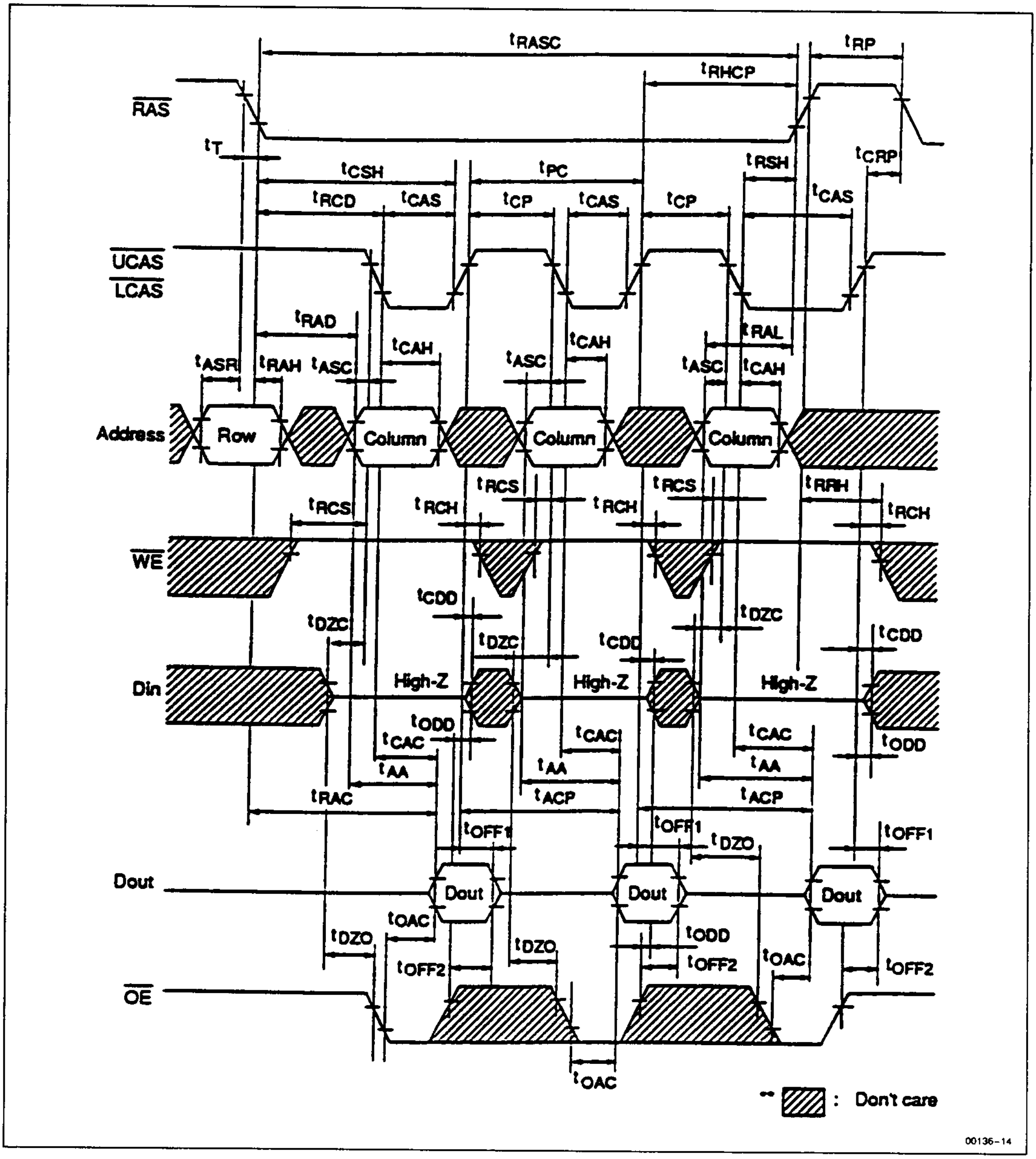
*** Refresh address : A0 – A8 (AX0 – AX8)

00136-12

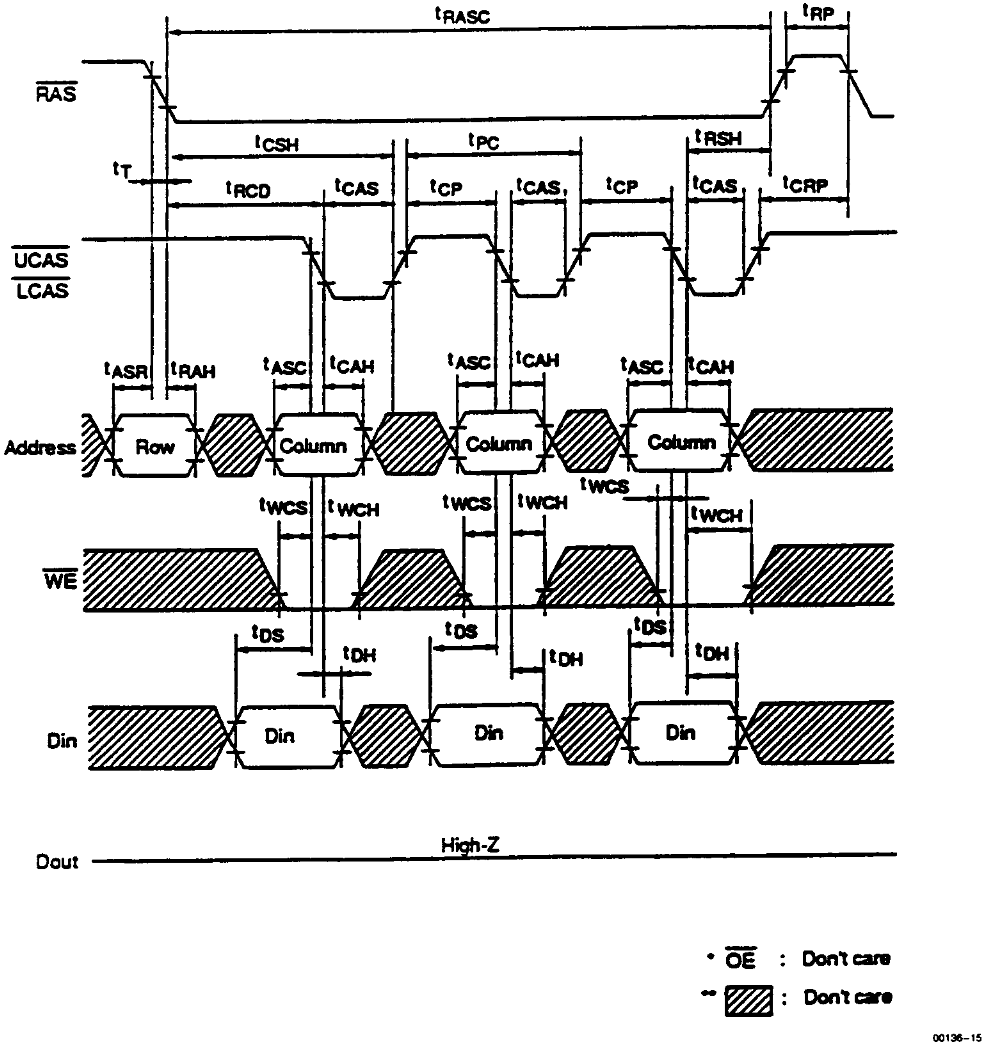
- **$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle**



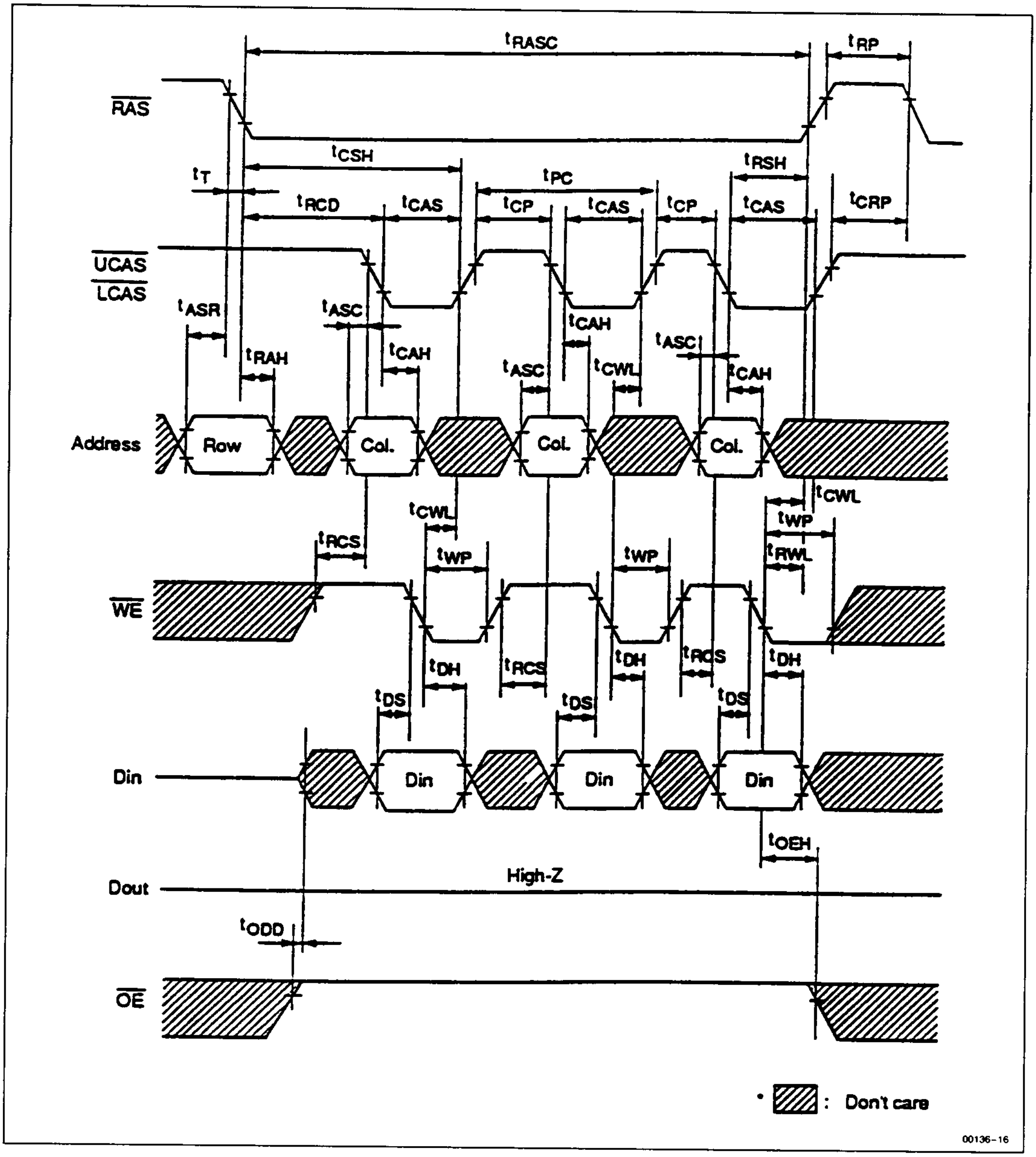
- **Fast Page Mode Read Cycle**



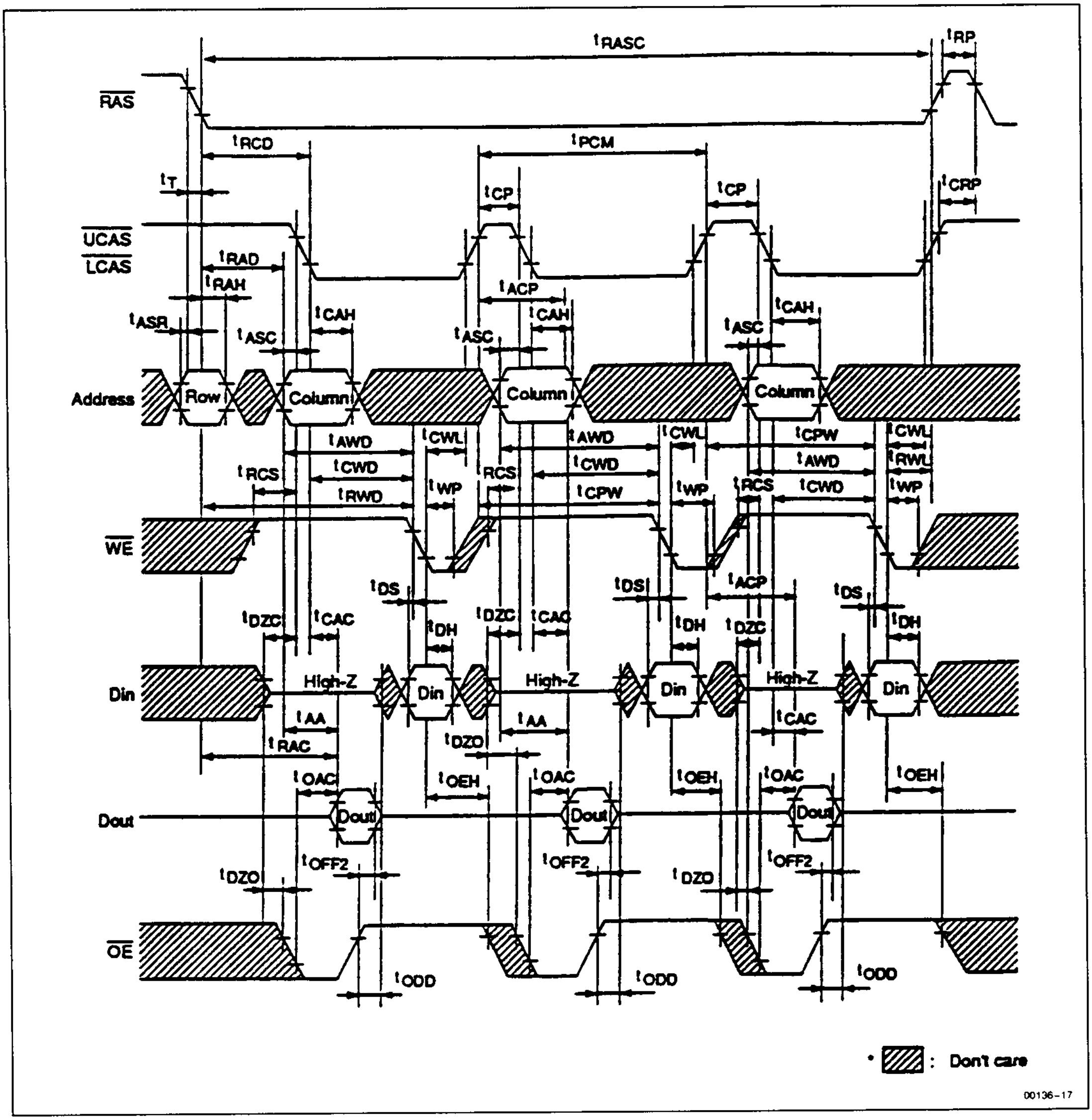
- **Fast Page Mode Early Write Cycle**



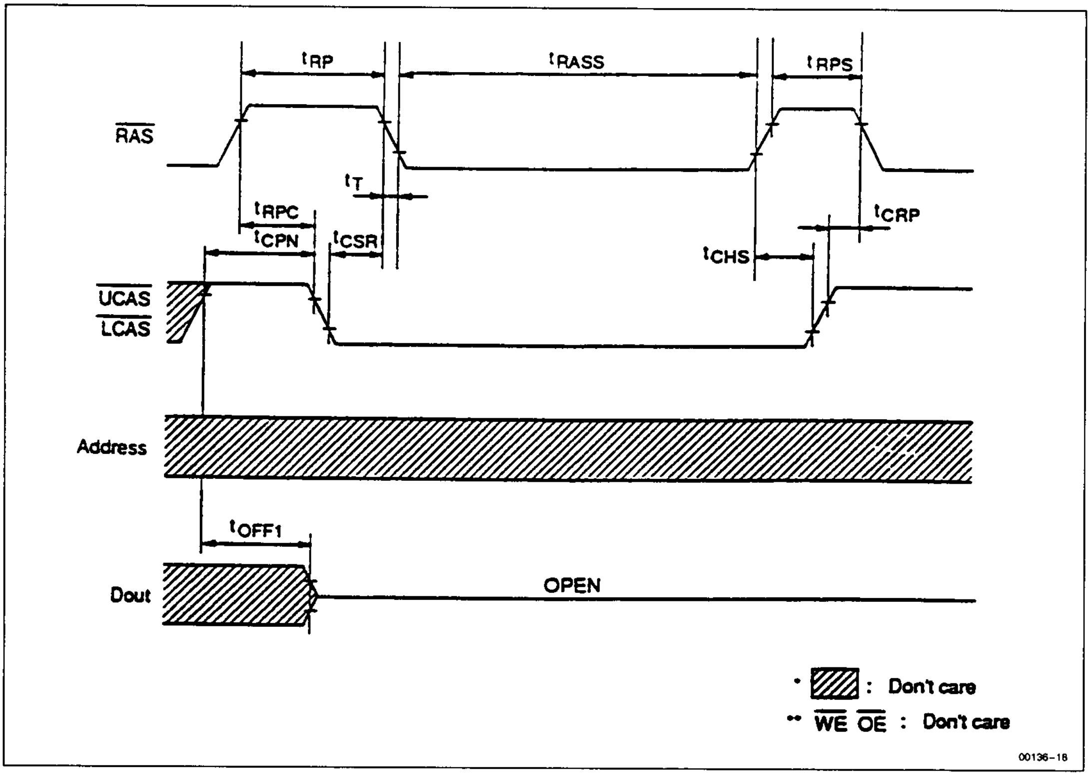
- **Fast Page Mode Delayed Write Cycle**



- **Fast Page Mode Read-Modify-Write Cycle**



- **Self Refresh Cycle**



The low self refresh current is achieved by introducing extremely long internal refresh cycle. Therefore some care needs to be taken on the refresh.

1. Please do not use t_{RASS} timing, 10 μs ≤ t_{RASS} ≤ 100 μs. During this period, the device is in transition state from normal operation mode to self refresh mode. If t_{RASS} ≥ 100 μs, then $\overline{RAS}$ precharge time should use t_{RPS} instead of t_{RP}.
2. If you use $\overline{RAS}$ only refresh or CBR burst refresh mode in normal read/write cycle, 512 cycles of distributed CBR refresh with 15.6 μs interval should be executed within 8 ms immediately after exiting from and before entering into the self refresh mode.
3. If you use distributed CBR refresh mode with 15.6 μs interval in normal read/write cycle, CBR refresh should be executed within 15.6 μs immediately after exiting from and before entering into self refresh mode.
4. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.