IXF6401 Broadband Access Processor

64 Bit, 66 MHz

Datasheet

Product Features

- General Performance
  - — Integrated Asynchronous Transfer Mode (ATM) Optical Carrier (OC)-12c Segmentation and Reassembly (SAR)
  - — Full-duplex, line-rate operation for even 64-byte, small packets
  - — 64-bit architecture
  - — Hardware encapsulation and tagging
  - — Hardware packet formatting
  - — Full source code for device drivers
- Buffer Management
  - — Full scatter/gather Direct Memory Access (DMA)
  - — Extensive transmit and receive buffering
  - — Two-dimensional link-list packet queuing
  - — 64 K internal transmit packet descriptor and packet buffer pools; 36 K receive buffer pool
  - — Multiple buffer sizes and buffer pools
  - — Two and four-bank, structured SDRAM supported
  - — Flow-through and pipelined SSRAM supported
- Interfaces
  - — OC-12c or Quad OC-3c
  - — Glueless, 64-bit SSRAM and SDRAM I/F
  - — PCI 2.1 compliant, 33- or 66-MHz, 32- or 64-bit operation
  - — UTOPIA 1, 2, 3
  - — ATM or POS
- Upper-Layer Assist
  - — LEC ID, ELAN ID, LLC/SNAP, MPOA, and IP encapsulations
  - — LAN, MPOA, MPLS, and IP protocol assist
  - — Programmable header encapsulation or tagging
  - — Packet and VC tagging supported
  - — Concurrent cell-or-packet counter reporting per VC for ease in tracking statistics
  - — Nine transmit and receive report-ring size configurations
  - — Sixteen offset configurations per receive VC per packet and/or per buffer
  - — 0 to 255 bytes offset configurations per VC per packet in transmit direction on byte boundary
- Traffic Shaping and Policing
  - — Up to 64 K VCs supported
  - — Traffic-shaping resources for up to 4 K CBR rates and at least 64 K VBR rates
  - — Granularity for rates down to 1 Kbps
  - — Time-wheel shaper for ABR/UBR, with guaranteed frame rate
  - — Dual Generic Cell Rate Algorithm (GCRA) policing per receive VC
  - — Weighted-fair queuing and dynamic-priority arbitration
- Process Technology
  - — 3.3 V ± 5% tolerant I/Os
  - — 0.35 µm CMOS design
  - — 352-pin EBGA package
  - — Power consumption 6 W @ 66 MHz

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April 2001

- Features
  - AAL Types 0, 1, 3/4, and 5 supported
  - TM 4.0 compliant
  - UBR, CBR, VBR, and ABR flow control supported
  - 64-byte, virtual-channel (VC) descriptors
  - Scalable to OC-48
  - ATM and Packet-over-SONET (POS) UTOPIA 1, 2, and 3 supported
  - PCI 2.1 compliant
- Local Area Network Emulation (LANE) Hardware Assist
  - LANE V1 and V2 packet-header generation
  - LEC ID, ELAN ID, and/or LLC/SNAP encapsulation
  - Separate LANE control buffer pool with 4 K bitmap
  - LANE flush protocol assist
  - Programmable packet holding mode
  - "Wait for Flush" reply message

The power of the IXF6401 Broadband Access Processor is its flexibility, scalability, and efficiency, and its integration of the different network traffic types. The processor's architecture simplifies and speeds OEM development by providing industry-standard interfaces for a 64-bit, 66-MHz PCI bus or 64-bit Synchronous Static Random Access Memory (SSRAM) / Synchronous Dynamic RAM (SDRAM) local-memory bus. Other standard interfaces include Universal Test and Operations Interface (UTOPIA) levels 1, 2, and 3; Asynchronous Transfer Mode (ATM); and Packet-over-SONET (Synchronous Optical Network) interfaces for direct coupling of a broad range of layer-1 physical interfaces.

The IXF6401 processor's 64-bit, 66-MHz local-memory bus acts in concert with the 64-bit, 66-MHz PCI bus to provide up to 8 Gbps of bus bandwidth. An onboard DMA "engine" controls access to and from the PCI and local-memory buses and can run in master or slave mode.

The IXF6401 processor achieves its speed by using extensive, dedicated, and hardware-based state machines. OEMs can use APIs that run on top of the processor's device driver to achieve value-added, differentiated services.

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Revision History

Date	Revision	Description
4/9/01	001	This is the first publication of this document.

1.0 Architectural Overview

The IXF6401 Broadband Access Processor provides a flexible and powerful solution for products designed for broadband Synchronous Optical Network (SONET) networks.

Figure 1 shows how the IXF6401 processor could be incorporated into an Asynchronous Transfer Mode (ATM)/Packets over SONET (POS) solution. Figure 2 is a block diagram of the processor's architecture.

Figure 1. IXF6401 Broadband Access Processor in ATM/POS Application

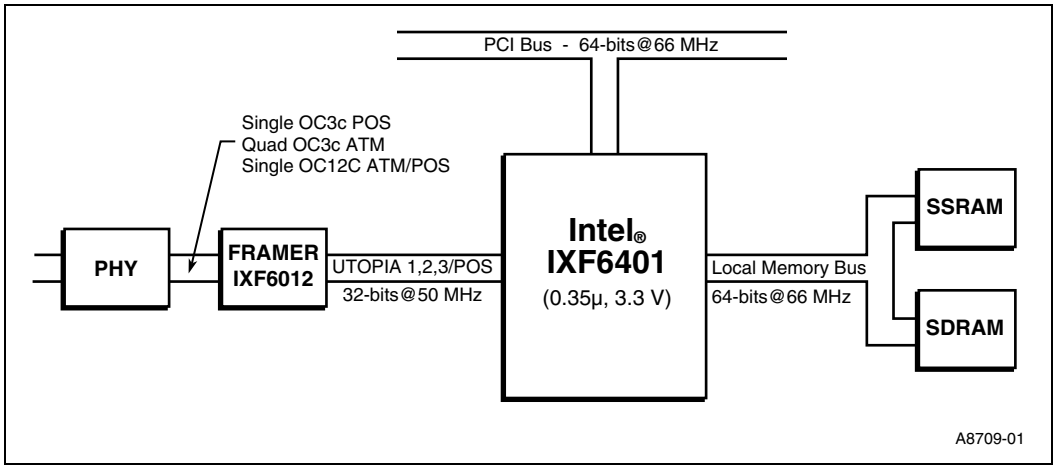
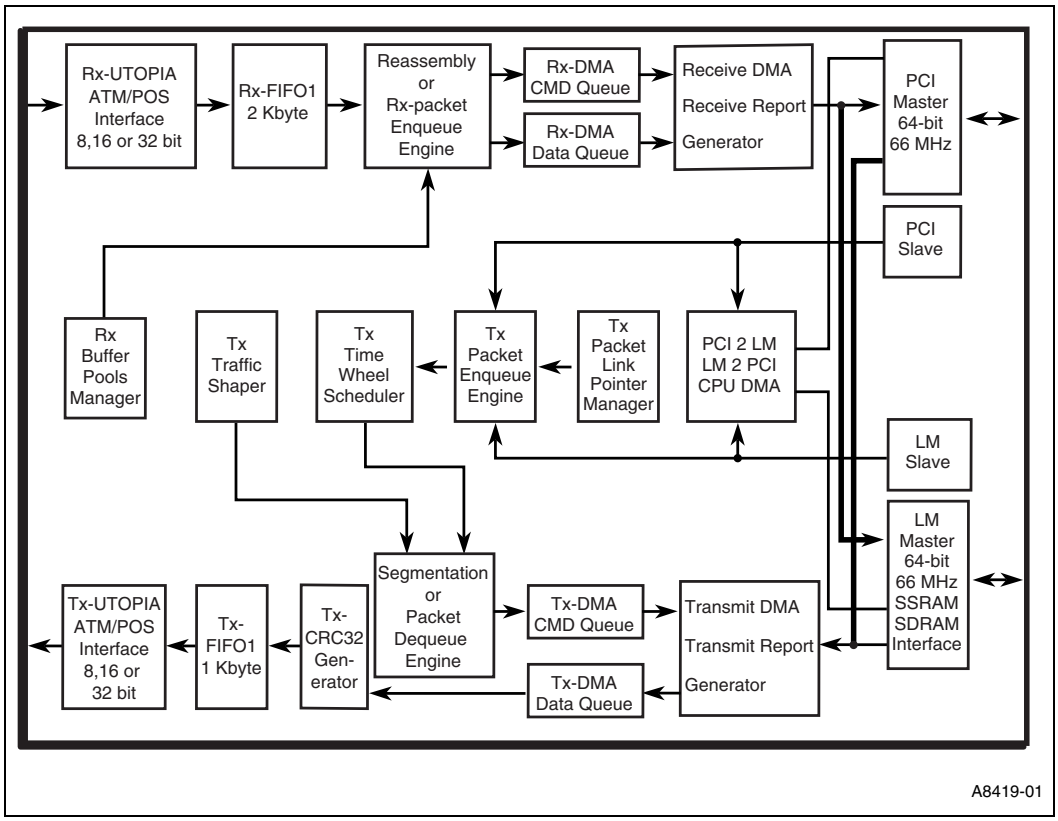


Figure 2. Architectural Block Diagram



1.1 Hardware Packet Processing

The IXF6401 processor performs all relevant layer-2 functions and provides extensive hardware assistance to your CPU, FPGA, or ASIC-based, higher-layer processing engine. ATM segmentation and reassembly (SAR), traffic-shaping, packet-tagging, encapsulation, buffer management, and data transfers between the PCI and local-memory bus via on-chip direct memory access (DMA) are handled by the IXF6401 processor. This frees your higher-layer engine to focus on application layers such as bridging, routing, encryption, network operating system, management, and security.

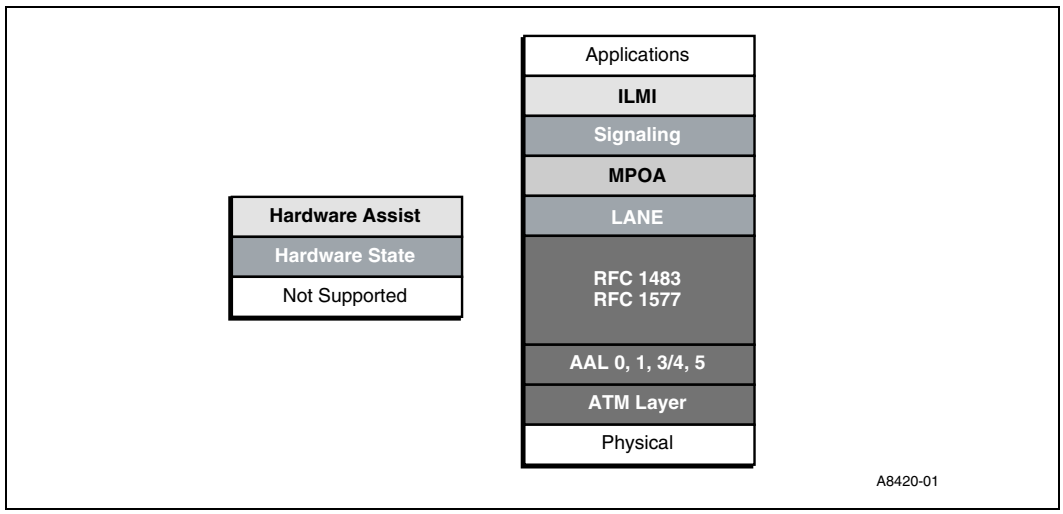
The processor supports several encapsulation methods that accelerate packet processing at layers 2 and 3 and can automate packet-header generation using the LEC ID, ELAN ID, MAC address, or any required bit field. The IXF6401 processor performs LLC/SNAP encapsulation and handles Multiprotocol Over ATM (MPOA), Local Area Network Emulation (LANE), Multiprotocol Label Switching (MPLS), and Internet Protocol (IP) protocols and any custom packet-tagging scheme.

1.2 ATM Processing

In addition to the high-performance features for higher-layer processing, the IXF6401 processor still comprises a full suite of ATM processing functions.

It supports ATM AAL 0, 1, 3/4, and 5 and can deliver true Unspecified Bit Rate (UBR), Constant Bit Rate (CBR), Variable Bit Rate (VBR), and Available Bit Rate (ABR) processing for up to 64 K virtual channels (VCs). The design features full, 64-byte VC descriptors and is multiport, SONET capable.

Figure 3. ATM Functionality



In the ATM mode, the IXF6401 processor provides all of the necessary termination functions currently established by the ATM Forum and Internet Engineering Task Force (IETF):

- ATM Forum User-Network Interface (UNI) 3.1 ATM Adaptation Layer and ATM Layer Specifications
- ATM Forum Traffic Management Specifications, Rev. 4.0
- RFC 1483 (Multiprotocol Encapsulation over ATM Adaptation Layer 5 [AAL 5])
- RFC 1626 (Default IP MTU for Use over ATM AAL 5)
- RFC 1577 (Classical IP and ARP over ATM)
- ATM Forum LANE Specification, Version 1.0
- ATM Forum LANE Version 2.0 - LUNI Baseline Document, Draft 5, February 1997

The IXF6401 processor maximizes both chip-level and system-level throughput. The IXF6401 processor supports 128 VC descriptors in its on-chip cache to virtually eliminate latency for specific VCs (for example, nominated CBR VCs). Adding external, high-speed Synchronous Static Random Access Memory (SSRAM) to the engine's local bus increases total capacity to 64 K VCs.

The IXF6401 processor has a sophisticated buffer-management scheme. All buffer pointer structures (64 K for transmit and 36 K for receive) are internal to the engine, greatly reducing the number of read/write operations performed during lookup, segmentation, and reassembly. Multiple buffer sizes and non-contiguous cell-splitting are fully supported in the hardware.

The IXF6401 processor can build a two-dimensional link list to link packets on a per-VC basis and buffers on a per-packet basis for transmit-packet queuing. This link list not only contains per-packet address and size, but also may contain per-packet encapsulation.

1.3 Traffic Shaping and Policing

The IXF6401 processor provides granular and efficient traffic shaping, making it an ideal fit for Digital Subscriber Line Access Multiplexer (DSLAM), Voice-over-IP (VoIP), and class-of-service sensitive applications. It includes 16 on-chip traffic shapers for CBR/VBR, with a TM-4.0-compliant ABR scheduler with guaranteed “MCR not Zero” hardware support and onboard RM-cell processing.

Within a shaped virtual path (VP), each VC can be independently shaped to rates as low as 1-Kbps increments, giving you extensive control over traffic on a per-VC basis. The IXF6401 processor’s dual, leaky-bucket, and virtual-scheduling algorithms can be implemented on a per-VC or per-VP basis.

The processor has no embedded Reduced Instruction Set Computing (RISC) processor in the path of any per-cell or per-packet transaction that would slow device operation or system throughput. This massive hardware assist offloads the CPU, saving valuable cycles for other critical tasks such as bridging, routing, policy execution, encryption, and security.

1.4 Basic Operation

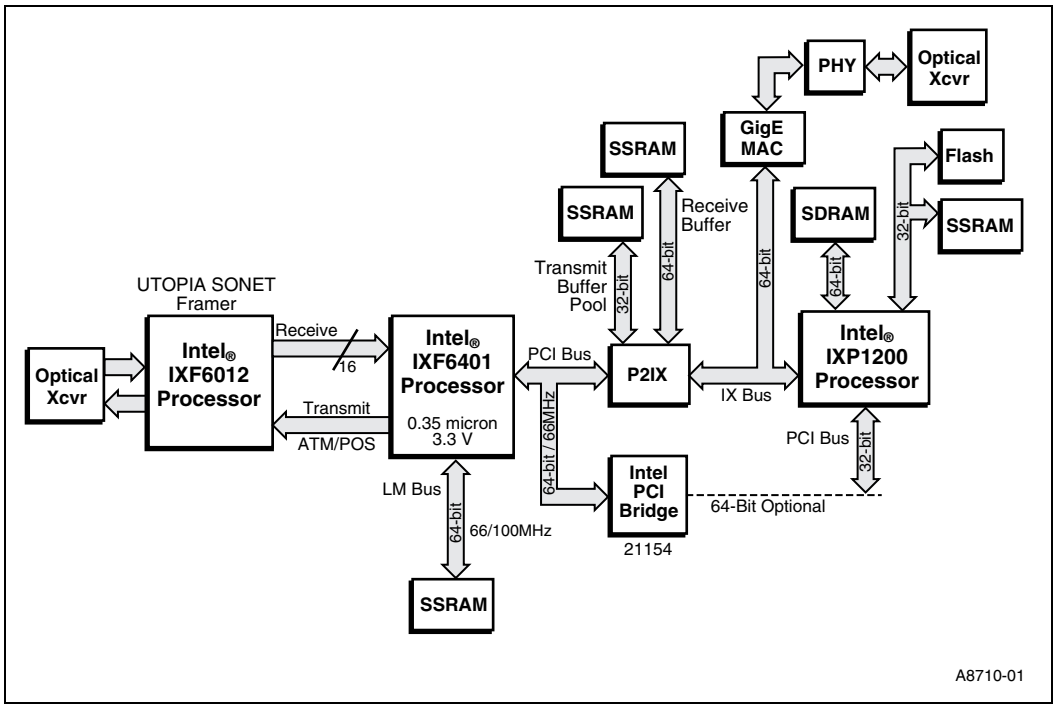
The IXF6401 processor is simple to use. To send a packet to the SONET infrastructure, software issues a 16-byte Add-Packet command that includes tagging and offset options, packet length, other per-packet variables, and a VC descriptor number. The descriptor specifies the target cell header VPI/VCI and traffic-shaping parameters. This may be followed by a series of 8-byte Add-Buffer commands, telling the engine where the payload resides (in local SDRAM or across the PCI bus). This is done in case the packet uses multiple buffers.

From this point, the IXF6401 processor takes control. The packet is linked per VC for CBR, VBR, and ABR connections or the packet is linked on the UBR chain. Once the packet is linked, it is transmitted at the specified rate, per VC descriptor, with the required encapsulation.

The process of associating a packet with a VC descriptor is an application-level function. For example, if your application is routing, IP-route matches will direct packets destined to a remote subnet to a Virtual Path Identifier (VPI) / Virtual Channel Identifier (VCI) defined in a local or centralized table. In LAN emulation or bridging, a similar process occurs, based on the Media Access Control (MAC) / Local Exchange Carrier Identification (LEC ID) address.

This association function is performed outside the IXF6401 processor, typically by a network processor, such as the IXP1200 processor, or a combination of standard CPUs, FPGAs, or ASICs, in either classic centralized or distributed architectures. Figure 4 shows how the IXF6401 processor would be used with the IXP1200 network processor.

Figure 4. IXF6401 Broadband Access Processor Using an IXP1200



The IXF6401 processor can perform any desired combination of operations on individual packets and reliably deliver wire-speed Optical Carrier (OC) 12c performance, even for 64-byte packets. Designs must issue the requisite Add-Packet commands, at whatever rates are required, to achieve target performance levels.

Full support for newly developed ABR service category and multiprotocols, such as TCP/IP over ATM, also are supported. On-chip memory enables cached VC descriptors to be registered and allows extensive cell buffering, which further enhances performance for single-chip OC-12c rate operation.

To handle changes to networking standards, the IXF6401 processor obtains configuration information from the PCI address space or from a tightly coupled, local network processor. With its extensive hardware assist, the IXF6401 processor is able to support multiprotocol data rates of 622 Mbps, full-duplex. That is possible because the higher-layer processor is not in the critical path of any per-cell transaction.

In PCI-host systems, the IXF6401 processor further increases overall end-system performance and manageability by off-loading, from the end-system's main processor, the ATM service-specific software functions, IP over ATM, and network statistical and management functions. This allows the load to be distributed to each local processor, which greatly reduces system-bus bandwidth.

An intelligent DMA interface provides a high-speed transfer mechanism between the processor's local memory and PCI address space. The architecture also provides SSRAM and SDRAM support. In very high-performance applications, part of the memory can be allocated to SSRAM.

Up to 128 Mbytes of addressable memory can be used for packet buffering. The packet-buffer memory can be at the PCI bus or the local-memory bus.

Table 1. Control Structure Memory Requirement

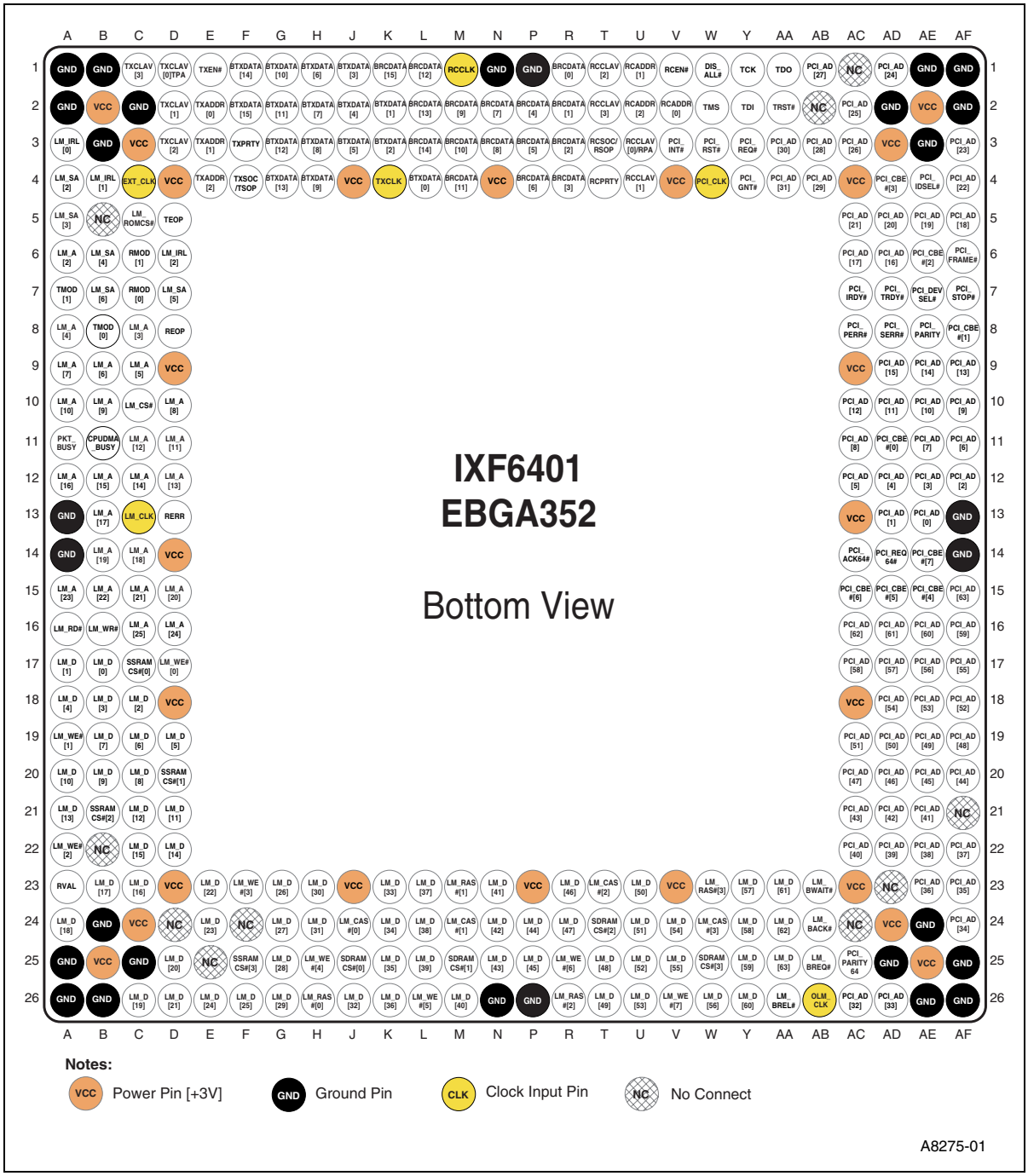
Description	Max Size Total	Byte Length Each	Total Memory Required	Where Kept†
Rc VC descriptor memory for 8 K VC	2^{13}	64	512 Kbytes	LM only
Tx VC descriptor memory for 8 K VC	2^{13}	64	512 Kbytes	LM only
Maximum Tx packet buffer descriptor for 64 K pointers	2^{16}	16	1 Mbyte	LM only
Maximum Rc report ring for 16 K entry	2^{14}	8	128 Kbytes	LM or PCI
Maximum Tx report ring for 16 K entry	2^{14}	8	128 Kbytes	LM or PCI
Maximum OEM cell ring for 1 K entry	2^{10}	64	64 Kbytes	LM or PCI
Maximum RM cell ring for 1 K entry	2^{10}	64	64 Kbytes	LM or PCI

† LM – Local memory consists of either all SDRAM, all SSRAM, or the combination of those two.

2.0 Pinout Information

2.1 IXF6401 Broadband Access Processor Ball Pinout

Figure 5. IXF6401 Processor Ball Configuration



2.2 Pin and Signal-Name Cross References

This section contains the tables listed below.

- Table 1, “PCI Bus Signals” on page 14 — Alphabetical list of PCI bus signals, by signal name, that shows pin locations
- Table 2, “Local Memory Bus Signals” on page 15 — Alphabetical list of local-memory bus signals, by signal name, that shows pin locations
- Table 3, “UTOPIA/POS Bus Signals” on page 15 — Alphabetical list of UTOPIA/POS bus signals, by signal name, that shows pin locations
- Table 4, “JTAG Signals” on page 16 — Alphabetical list of JTAG signals, by signal name, that shows pin locations
- Table 5, “Miscellaneous Signals” on page 16 — List of general-use signals, pins used for power and ground, and pins reserved for ground or power, respectively, including their pin locations
- Table 6, “Signal Descriptions” on page 17 — Alphabetical list of signal names that provides descriptions

The “pin locations” given in the following tables refer to the grid location of the pin, as shown in Figure 5, “IXF6401 Processor Ball Configuration” on page 13.

Table 1. PCI Bus Signals (Sheet 1 of 2)

Signal Name	Pin Locations
PCI_ACK64#	AC14
PCI_AD[63:0]	AF15, AC16, AD16, AE16, AF16, AC17, AD17, AE17, AF17, AD18, AE18, AF18, AC19, AD19, AE19, AF19, AC20, AD20, AE20, AF20, AC21, AD21, AE21, AC22, AD22, AE22, AF22, AE23, AF23, AF24, AD26, AC26, AA4, AA3, AB4, AB3, AB1, AC3, AC2, AD1, AF3, AF4, AC5, AD5, AE5, AF5, AC6, AD6, AD9, AE9, AF9, AC10, AD10, AE10, AF10, AC11, AE11, AF11, AC12, AD12, AE12, AF12, AD13, AE13
PCI_CBE#[7:0]	AE14, AC15, AD15, AE15, AD4, AE6, AF8, AD11
PCI_CLK	W4
PCI_DEVSEL#	AE7
PCI_FRAME#	AF6
PCI_GNT#	Y4
PCI_IDSEL#	AE4
PCI_INT#	V3
PCI_IRDY#	AC7
PCI_PARITY	AE8
PCI_PARITY64	AC25
PCI_PERR#	AC8
PCI_REQ#	Y3
PCI_REQ64#	AD14
PCI_RST#	W3
PCI_SERR#	AD8
PCI_STOP#	AF7

Table 1. PCI Bus Signals (Sheet 2 of 2)

Signal Name	Pin Locations
PCI_TRDY#	AD7

Table 2. Local Memory Bus Signals

Signal Name	Pin Locations
LM_A[25:2]	C16, D16, A15, B15, C15, D15, B14, C14, B13, A12, B12, C12, D12, C11, D11, A10, B10, D10, A9, B9, C9, A8, C8, A6†
LM_D[63:0]	AA25, AA24, AA23, Y26, Y25, Y24, Y23, W26, V25, V24, U26, U25, U24, U23, T26, T25, R24, R23, P25, P24, N25, N24, N23, M26, L25, L24, L23, K26, K25, K24, K23, J26, H24, H23, G26, G25, G24, G23, F26, E26, E24, E23, D26, D25, C26, A24, B23, C23, C22, D22, A21, C21, D21, A20, B20, C20, B19, C19, D19, A18, B18, C18, A17, B17
LM_BACK#	AB24
LM_BREL#	AA26
LM_BREQ#	AB25
LM_BWAIT#	AB23
LM_CAS#[3:0]	W24, T23, M24, J24
LM_CLK	C13
LM_CS#	C10
LM_IRL[2:0]	D6, B4, A3
LM_RAS#[3:0]	W23, R26, M23, H26
LM_RD#	A16
LM_ROMCS#	C5
LM_SA[6:3]	B7, D7, B6, A5
LM_SA[2]	A4††
LM_WE#[7:0]	V26, R25, L26, H25, F23, A22, A19, D17
LM_WR#	B16
OLM_CLK	AB26
SDRAMCS#[3:0]	W25, T24, M25, J25
SSRAMCS#[3:0]	F25, B21, D20, C17

† LM_A[2] (or Pin A6) is not used and must be pulled low.

†† LM_SA[2] is not used. Keep this signal no connect.

Table 3. UTOPIA/POS Bus Signals (Sheet 1 of 2)

Signal Name	Pin Locations
RCDATA[15:0]	K1, L3, L2, L1, M4, M3, M2, N3, N2, P4, P3, P2, R4, R3, R2, R1
TXDATA[15:0]	F2, F1, G4, G3, G2, G1, H4, H3, H2, H1, J3, J2, J1, K3, K2, L4
RCADDR[2:0]	U2, U1, V2
RCCLAV [0]/RPA	U3
RCCLAV[3:1]	T2, T1, U4

Table 3. UTOPIA/POS Bus Signals (Sheet 2 of 2)

Signal Name	Pin Locations
RCCLK	M1
RCEN#	V1
RCPRTY	T4
RCSOC/RSOP	T3
REOP	D8
RERR	D13
RMOD[0]	C7
RMOD[1]	C6
RVAL	A23
TEOP	D5
TMOD[0]	B8
TMOD[1]	A7
TXADDR[2:0]	E4, E3, E2
TXCLAV[0]TPA	D1
TXCLAV[3:1]	C1, D3, D2
TXCLK	K4
TXEN#	E1
TXPRTY	F3
TXSOC/TSOP	F4

Table 4. JTAG Signals

Signal Name	Pin Locations
TCK	Y1
TDI	Y2
TDO	AA1
TMS	W2
TRST#	AA2

Table 5. Miscellaneous Signals (Sheet 1 of 2)

Signal Name	Pin Locations
General-Use Signals	
CPUDMA_BUSY	B11
DIS_ALL#	W1
EXT_CLK	C4
PKT_BUSY	A11

Table 5. Miscellaneous Signals (Sheet 2 of 2)

Signal Name	Pin Locations
Power Pins	
VCC	B2, B25, C3, C24, D4, D9, D14, D18, D23, J4, J23, N4, P23, V4, V23, AC4, AC9, AC13, AC18, AC23, AD3, AD24, AE2, AE25
Ground Pins	
GND	A1, A2, A13, A14, A25, A26, B1, B3, B24, B26, C2, C25, N1, N26, P1, P26, AD2, AD25, AE1, AE3, AE24, AE26, AF1, AF2, AF13, AF14, AF25, AF26
No-Connect Pins	
NC	B5, B22, D24, E25, F24, AB2, AC1, AC24, AD23, AF21

Table 6. Signal Descriptions (Sheet 1 of 6)

Signal Name	Input (I) Output (O)	Description
CPUDMA_BUSY	O	DMA Queue Full.
DIS_ALL#	I	Disable All. This signal disables all output and three-state signals. For normal operation, this signal should be high.
EXT_CLK	I	External Clock. This clock can be used as an external clock source for the traffic shaper.
GND	I	Ground.
LM_A[25:3]	I/O	Local Bus Address. Using the 16-MByte Micron device as an example (MT48LC1M16A1), the SDRAM row address is selected by LM_A[13:3]. The SDRAM column address is represented by LM_A[10:3] because this device has 11 row addresses and eight column addresses. During SSRAM operation, a new address is presented on every clock, if SSRAMCS# is asserted. When the external master is performing a slave transaction, it must hold the address until LM_BWAIT# is deasserted.
LM_A[2]	I/O	LM_A[2] (or Pin A6) is not used and must be pulled low.
LM_BACK#	I	Local Bus Acknowledge. This is the grant signal to the IXF6401 processor bus request. It should remain asserted throughout the transaction. To optimize the performance of the chip, external logic can assert this signal all the time. If an external master is present, however, external logic needs to deassert this signal only when the external master requires the bus by asserting LM_BREL# and LM_BREQ# is deasserted by the IXF6401 processor. After LM_BACK# is deasserted, it must remain deasserted until the external master has completed the transaction.
LM_BREL#	I	Local Bus Release. The external master asserts this signal to indicate that it intends to use the local bus. It deasserts this signal once it detects that LM_BREQ# is deasserted. To improve performance, the external master should not assert this signal until there is a transaction waiting to be performed.
LM_BREQ#	O	Local Bus Request. When asserted, this signal indicates that the IXF6401 processor wants to access the local bus. Once it is asserted, it remains asserted until the external master asserts LM_BREL#. If the IXF6401 processor is idle when LM_BREL# is asserted, the IXF6401 processor deasserts LM_BREQ# in the next clock cycle. If the IXF6401 processor is not idle when LM_BREL# is asserted, the processor deasserts LM_BREQ# two cycles after it finishes the current transaction. The IXF6401 processor deasserts this signal for only one cycle.
LM_BWAIT#	O	Local Bus External Master Wait. During slave access, after the external master asserts LM_CS#, the IXF6401 processor asserts this signal when it is not ready for a data transaction. The IXF6401 processor removes LM_BWAIT# when it is ready for transaction. During slave read access, the data on the local bus is valid the cycle AFTER LM_BWAIT# is deasserted. The external master must hold the data until one cycle after this signal is deasserted, during a slave-write transaction.

Table 6. Signal Descriptions (Sheet 2 of 6)

Signal Name	Input (I) Output (O)	Description
LM_CAS#[3:0]	I/O	Local Bus SDRAM Column Address Strobe Command. When this signal and SDRAMCS# are both asserted while LM_RAS# is deasserted, the column address is selected. The signals remain asserted until the transaction has completed. These signals also are asserted for one cycle during either refresh or mode set. The signals should be connected directly to CAS# of a SDRAM. They are input and shaped during slave external master access of the local SDRAM.
LM_CLK	I	Local Bus Clock. This is the master clock for the local memory bus and the IXF6401 processor.
LM_CS#	I	Local Memory Chip Select. When asserted, the host processor wants to access the processor's internal memory and registers.
LM_D[63:0]	I/O	Local Bus Data. Output during master write or slave read. Input when master read or slave write. When writing to SSRAM or SDRAM, data is valid on every clock, provided any of the memory chip enables are asserted. During SSRAM read access, data is valid one cycle after SSRAMCS# is asserted. Therefore, the first cycle after SSRAMCS# is deasserted, data is still valid. When reading from SDRAM, depending on the CAS latency value, data could be valid three clock cycles after SDRAMCS# is asserted. As a result, data could still be valid for three cycles after SDRAMCS# has been removed. Data is invalid in all other cycles when the IXF6401 processor is in master mode. During slave write, the external device must put the valid data on the data bus in the same cycle that it asserts LM_CS#, and the value of the data must be held for one cycle after LM_BWAIT# is deasserted. During slave read, data is valid one cycle after LM_BWAIT# is deasserted, and it is held until LM_CS# is deasserted by the external device.
LM_IRL[2:0]	O	Local Bus Interrupt. LM_IRL[0] is asserted when any bit in the Error Interrupt register is set. LM_IRL[1] is set when any bit in the Status Interrupt register is asserted. LM_IRL[2] is set when any bit in the Status[2:0] register is set.
LM_RAS#[3:0]	I/O	Local Bus SDRAM Row Address Strobe Command. When this signal and SDRAMCS# are asserted, the row address is selected.
LM_RD#	I/O	Local Bus Read. Asserted when the current transaction performed by the IXF6401 processor is a read instruction to SSRAM. It has the same timing as SSRAMCS#. Please notice that this signal is not used when a master read from SDRAM is performed. This signal is asserted by the external master during a slave read transaction, and external logic should hold the signal until the IXF6401 processor deasserts IM_WAIT#.
LM_ROMCS#	O	Local Bus Expansion ROM Chip Select. If ROM is present, this signal will be asserted during the booting process. PCI Master Access Expansion ROM. Only 16-bit EEPROM is supported by the IXF6401 processor and it should be connected to LM_A[18:3] and LM_D[63:48].
LM_SA[6:3]	O	Local Bus Spare Memory Address. When LM_A[6:3] is used for SDRAM. The LM_SA[6:3] should be used for SSRAM or vice-versa. This signal has the same timing as LM_A. Instead of becoming input during a slave access, however, these pins will be tristated.
LM_SA[2]	O	LM_SA[2] is not used. Keep this signal no connect.

Table 6. Signal Descriptions (Sheet 3 of 6)

Signal Name	Input (I) Output (O)	Description
LM_WE#[7:0]	I/O	Local Bus Write Enable. Output during master read/write and input during slave read/write. LM_WE#[7] controls LM_D[63:56]. LM_WE#[6] controls LM_D[55:48]. LM_WE#[5] controls LM_D[47:40]. LM_WE#[4] controls LM_D[39:32]. LM_WE#[3] controls LM_D[31:24]. LM_WE#[2] controls LM_D[23:16]. LM_WE#[1] controls LM_D[15:8]. LM_WE#[0] controls LM_D[7:0]. LM_WE#[2 *i*] and LM_WE#[2 *i*+1] should be connected to DQML and DQMU of the SDRAM, respectively, where *i* is 0 to 3. When connected to SSRAM, LM_WE#[*i*] should be connected to BW*i*#. LM_WE# has the same timing as local memory chip select when the IXF6401 processor is performing a master write.
LM_WR#	I/O	Local Bus Write. Asserted when the IXF6401 processor accesses SDRAM. It has the same timing as SDRAMCS#. This signal is not asserted during a master write to SSRAM. During slave access, the external master asserts LM_WR# to indicate a write access. The external logic should hold the signal until the IXF6401 processor deasserts IM_WAIT#.
NC	—	No connect.
OLM_CLK	O	Local Memory Clock Output.
PCI_ACK64#	I/O	PCI Bus Acknowledge 64-bit. When asserted, this signal indicates the target is willing to transfer data using 64 bits.
PCI_AD[63:0]	I/O	PCI Bus Multiplexed 64-bit Address/Data. During a data phase, the upper 32 bits are meaningful when both PCI_REQ64# and PCI_ACK# are asserted. During the address phase, only the lower 32 bits are used.
PCI_CBE#[7:0]	I/O	PCI Bus Command and Byte Enable. During an address phase, PCI_CBE# represents a PCI-bus command. During a data phase, it represents a byte enable.
PCI_CLK	I	PCI Bus Clock. Up to 66 MHz.
PCI_DEVSEL#	I/O	PCI Bus Device Select. When driven, this signal indicates that the driving device has decoded its address as the target of the current access.
PCI_FRAME#	I/O	PCI Bus Cycle Frame. This signal is driven by the bus master to indicate the start and end of a transaction.
PCI_GNT#	I	PCI Bus Grant for the IXF6401 processor.
PCI_IDSEL#	I	PCI Bus Initialization Device Select. This signal is used as a chip select during configuration read and write transactions.
PCI_INT#	O	PCI Bus Interrupt Signal. This signal should be connected to INTA# of the PCI connector.
PCI_IRDY#	I/O	PCI Bus Initiator Ready. When asserted, the bus master is ready to complete the current data phase.
PCI_PARITY	I/O	PCI Bus Parity Bit. Sets even parity across PCI_AD[31:0] and PCI_C/BE#[3:0].
PCI_PARITY64	I/O	PCI Bus Parity Double Word. Sets even parity across PCI_AD[63:32] and PCI_C/BE#[7:4].
PCI_PERR#	I/O	PCI Bus Parity Error. This bit is only used for reporting data parity errors during all PCI transactions, except for a Special Cycle.
PCI_REQ#	O	PCI Bus Request. The IXF6401 processor asserts this signal when it is trying to access the PCI bus.
PCI_REQ64#	I/O	PCI Bus Request 64-bit Transfer. When asserted, this signal indicates a 64-bit transaction.
PCI_RST#	I	PCI Bus Reset. This is the master reset signal for the IXF6401 processor.

Table 6. Signal Descriptions (Sheet 4 of 6)

Signal Name	Input (I) Output (O)	Description
PCI_SERR#	O	PCI Bus System Error. This signal is used to report address parity errors, data parity on the Special Cycle command, or any other system error where the result will be catastrophic. PCI_SERR# is an open drain signal.
PCI_STOP#	I/O	PCI Bus Stop. The PCI target asserts this signal to request the bus master to stop the current transaction.
PCI_TRDY#	I/O	PCI Bus Target Ready. This signal is driven by the target to indicate its ability to complete current data phase.
PKT_BUSY	O	Packet Processor Busy. The purpose of this pin is to help external hardware to keep track of whether the IXF6401 processor's four-entry Transmit_ADD_PKT_QUEUE and two-entry ADD_BUFFER_QUEUE are available to accept another command.
RCADDR[2:0]	O	UTOPIA Bus Receive MPHY Address. When address polling is enabled, these signals are the Receive MPHY address. When polling is disabled, these signals are used as RxEn#[3:1].
RCCLAV [0]/RPA	I	ATM: RCCLAV-UTOPIA Bus Receive Cell Available. When asserted, MPHY is ready to transfer a complete cell. POS: Receive Packet Available. When high, indicates the POS framer has at least one packet.
RCCLAV[3:1]	I	UTOPIA Bus Receive Cell Available. When asserted, MPHY is ready to transfer a complete cell.
RCCLK	I	UTOPIA Bus Receive Clock. This is the UTOPIA-bus receive clock.
RCDATA[15:0]	I/O	UTOPIA/POS Receive Data. This bus carries valid ATM cell or POS packet data, when RCEN# is asserted. In 16-bit or 8-bit mode, RCDATA is input only for receive data. In 32-bit mode with receive only, RCDATA will represent receive data [15:0] and TXDATA will represent receive data [31:16].
RCEN#	O	UTOPIA Bus Receive Enable. When asserted, indicates that the IXF6401 processor is ready to accept an ATM cell in the following cycles.
RCPRTY	I	UTOPIA/POS Receive Data Parity. RCPRTY serves as the odd parity over RCDATA on 8/16-bit mode or RCDATA and TXDATA on 32-bit mode.
RCSOC/RSOP	I	ATM: RCSOC-UTOPIA Bus Receive Start of Cell. This signal indicates the current data on RCDATA is the beginning of a new ATM cell. POS: RSOP-Receive Start Of Packet. When high, indicates the beginning of the packet with RCEN# asserted.
REOP	I	Receive End Of Packet. REOP is valid only when RCEN# is asserted. In ATM mode, this pin must be pulled down.
RERR	I	Receive Error. Indicates the packet is not valid due to error(s). In ATM mode, this pin must be pulled down.
RMOD[1] RMOD[0]	I I	Receive module indicates the valid bytes. In the data bus when REOP is asserted. 00 — DATA [31:0] valid 01 — DATA [31:8] valid 10 — DATA [31:16] valid 11 — DATA [31:24] valid In ATM mode, these pins must be pulled low.
RVAL	I	Receive Data Valid. When high, all receive controls and data are valid. In ATM mode, this pin must be pulled up.

Table 6. Signal Descriptions (Sheet 5 of 6)

Signal Name	Input (I) Output (O)	Description
SDRAMCS#[3:0]	I/O	Local Bus SDRAM Chip Select. When asserted, the IXF6401 processor wants to access SDRAM. These signals are asserted two cycles after LM_BACK# is asserted, if there is a transaction pending. They remain asserted until the burst transaction has completed. When these signals are deasserted at the end of the read cycle, it does not mean the data is invalid from then on. These signals are for flow-through only. See “LM_D[63:0]” on page 15 for more information.
SSRAMCS#[3:0]	I/O	Local Bus SSRAM Chip Select. When asserted, the IXF6401 processor wants to access SSRAM. These signals should be connected to CS# of the SSRAMs. Since the processor generates its own burst addresses, ADSP# should be pulled up to high and ADSC# and ADV# should be pulled down to GND. These signals are asserted two cycles after LM_BACK is asserted if there is a transaction pending. They remain asserted until the burst transaction has completed. When these signals are deasserted at the end of the read cycle, it does not mean the data is invalid from then on. See “LM_D[63:0]” on page 15 for more information.
TCK	I	JTAG Input Clock.
TDI	I	JTAG Data Input.
TDO	O	JTAG Data Output.
TEOP	O	Transmit End Of Packet. TEOP is valid only when TXEN# is asserted. In ATM mode, this pin is no connect.
TMOD[1] TMOD[0]	O O	Transmit Module. Indicates the valid bytes in the data bus when TEOP is asserted. 00 — DATA [31:0] valid 01 — DATA [31:8] valid 10 — DATA [31:16] valid 11 — DATA [31:24] valid In ATM mode, these pins are no connect.
TMS	I	JTAG Test Mode Select. Controls the state of the TAP controller in the device.
TRST#	I	JTAG Test Reset. This will reset the TAP controller.
TXADDR[2:0]	O	UTOPIA Bus Transmit MPHY Address. When address polling is enabled, these signals are the MPHY address. When address polling is disabled, these signals are used as TXEN#[3:1].
TXCLAV[0]TPA	I	ATM: UTOPIA Bus Transmit Cell Available. When asserted, this signal indicates that MPHY is ready to accept the transfer of a complete cell. POS: Transmit Packet Available (TPA). When high, indicates the POS framer is ready to take data. When low, indicates the POS framer transmit fifo is full or near full and the IXF6401 processor needs to stop transmitting data.
TXCLAV[3:1]	I	UTOPIA Bus Transmit Cell Available. When asserted, this signal indicates that MPHY is ready to accept the transfer of a complete cell.
TXCLK	I	UTOPIA Bus Transmit Clock. This signal is the UTOPIA bus transmit clock.
TXDATA[15:0]	I/O	UTOPIA/POS transmit data. This bus carries valid ATM cell or POS packet data when TXEN# is asserted. In 16-bit or 8-bit mode, TXDATA is output only for transmit data. In 32-bit mode with transmit only, TXDATA will represent transmit data [15:0] and RCDATA will represent transmit data [31:16].

Table 6. Signal Descriptions (Sheet 6 of 6)

Signal Name	Input (I) Output (O)	Description
TXEN#	O	Transmit Enable. ATM- When asserted, this signal indicates that the current cycle contains a valid packet data. UTOPIA Bus Transmit Enable. When asserted, this signal indicates that the current cycle contains a valid ATM cell.
TXPRTY	O	UTOPIA/POS Transmit Data Parity. TXPRTY serves as the odd parity bit over TXDATA, on 8/16-bit mode, or RCDATA and TXDATA, on 32-bit mode. When FPE (Force Parity Error) is set in the UTOPIA Control register, the IXF6401 processor asserts even parity on this pin.
TXSOC/TSOP	O	ATM: TXSOC- UTOPIA Bus Transmit Start of Cell. When asserted, this signal indicates that the current data on TXDATA is the beginning of a new ATM cell. POS: TSOP-Transmit start of packet. When high, indicates the beginning of the packet when TXEN# is asserted.
VCC	I	Power, 3.3 V.

3.0 Bus-Interface Information

This section provides overview information about the IXF6401 Broadband Access Processor's following bus interfaces:

- PCI Interface — See page 23.
- Local-Memory Interface — See page 24.
- UTOPIA Interface — See page 28.

3.1 PCI Interface

The IXF6401 processor's default clock speed and bus width are 66 MHz and 64-bit. The processor's addressing is always 32-bit. Table 7 lists the other supported clock speeds and bus widths.

Table 7. Supported Clock Speeds and Bus Widths

Clock Speed	Bus Width
33 MHz	32-bit†
33 MHz	64-bit
66 MHz	32-bit†
66 MHz	64-bit
† To use the 32-bit mode, set System Control Register bit (W_B[25]) to 1.	

The configuration cycle/mechanism supported by the processor is: Configuration Mechanism #1, Type 0.

PCI command and cycles to which the processor responds are shown in Table 8.

Table 8. PCI Commands and Cycles

PCI_CBE# [3:0] Bits	Command	PCI Specification
0110	Memory Read	PCI 2.1, page 36
0111	Memory Write	PCI 2.1, page 37
1010	Configuration Read	PCI 2.1, pages 84 - 86
1011	Configuration Write	PCI 2.1, pages 84 - 86

The PCI interface has the following special features:

- Burst length and order — In Master mode, 64 bytes at a time.
- Retry, Disconnect, and Target-Abort — All are supported. (See the PCI 2.1 specification, pages 43 - 47.)

Note: Combining, merging, and collapsing are not supported.

Slave and Master operation are supported by the IXF6401 processor. For master operation:

- You need to include an arbitration protocol that uses PCI_CLK, PCI_REQ#, PCI_GNT#, PCI_FRAME#, and PCI_AD[63:0]. (See the PCI 2.1 specification, page 57.)
- Fast back-to-back transaction — The just-cited signals are used in conjunction with PCI_IRDY# and PCI_TRDY#. (For a timing diagram, see the PCI 2.1 specification, page 61.)

3.2 Local-Memory Interface

3.2.1 General Features

The local-memory interface for the processor always operates in the 64-bit mode at 66 MHz. There is no parity check.

The processor can address up to 256 MBytes of memory space — split between SSRAM (128 Mbytes) and SDRAM (128 Mbytes). Flow through and pipelined SSRAM can be used. The IXF6401 processor always will perform as SDRAM auto-refresh.

Memory access transaction used:

- Size — Bursts can be one-byte, two-byte, four-byte, eight-byte, and linear eight-byte bursts up to 64 bytes per access.
- SDRAM refresh — The IXF6401 processor always provides the address, but it does not have an internal counter to auto-increment the address.

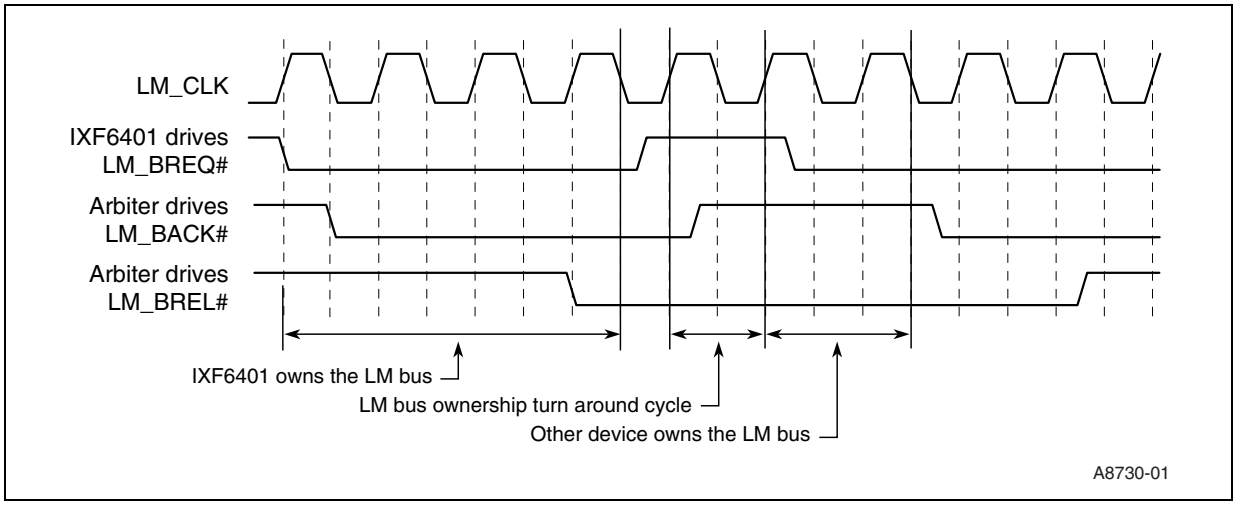
For detailed SSRAM and SDRAM timing information, see the manufacturer's specifications.

3.2.2 Arbitration

The IXF6401 processor does not have a local-memory-bus, on-chip arbiter or a PCI-bus arbiter. The local-memory-bus arbitration is shown in Figure 6.

The PCI arbitration is performed according to PCI specifications.

Figure 6. Local-Memory Arbitration Timing



NOTES:
1. For the processor or host to gain the local bus, the device first must assert either LM_BREQ# or LM_BREL#.
2. The device must wait for LM_BACK# to be asserted and then can start bus operations.
3. The bus request must remain active for the duration of the operation.
4. The bus request should return to inactive at the end of the operation. If the device's grant is removed, it must remain inactive for at least two clock cycles.
5. After detecting the desertion of the bus request of a current bus owner, the external arbitrator will rearbitrate the bus.
6. The bus is granted to the next candidate on a first-come, first-served, round-robin basis.
7. To share the bus bandwidth, limit bursts to less than 64 bytes per transaction.
8. To access the IXF6401 processor's internal registers and on-chip RAM/CAM from the local memory bus, the local-memory-bus CPU asserts the LM_CS# pin after it gains ownership of the bus.
9. For more details on bus timing, see "Local Memory Bus Timing" on page 47.
10. For an illustration of the recommended local-memory clock circuitry, see Table 35 on page 47.

3.2.3 Local Memory Configuration

For information on configuring the local memory, refer to documentation on BIU Master Control Register 1, in the *IXF6401 Broadband Access Processor Developer's Manual* (273453).

3.2.3.1 SDRAM Configuration

For READ and WRITE SDRAM timing, refer to the memory manufacturer's specification(s). The following tables show the configuration settings for the Micron MT48LC8M16A2 SDRAM module.

Table 9. Sample SDRAM Configuration: Bank 0 (Sheet 1 of 2)

SDRAM Pins	IXF6401 Broadband Access Processor Pins 8 Mbits x 16 x 4 Chips			
CLK	LM_CLK†	LM_CLK†	LM_CLK†	LM_CLK†
CKE	VCC	VCC	VCC	VCC
CS#	SDRAMCS0#	SDRAMCS0#	SDRAMCS0#	SDRAMCS0#
† LM_CLK refers to the "delayed" LM_CLK signal. See Figure 20 on page 48.				

Table 9. Sample SDRAM Configuration: Bank 0 (Sheet 2 of 2)

SDRAM Pins	IXF6401 Broadband Access Processor Pins 8 Mbits x 16 x 4 Chips			
RAS#	LM_RAS0#	LM_RAS0#	LM_RAS0#	LM_RAS0#
CAS#	LM_CAS0#	LM_CAS0#	LM_CAS0#	LM_CAS0#
WE#	LM_WR#	LM_WR#	LM_WR#	LM_WR#
DQML	LM_WE0#	LM_WE2#	LM_WE4#	LM_WE6#
DQMH	LM_WE1#	LM_WE3#	LM_WE5#	LM_WE7#
BA0	LM_A15	LM_A15	LM_A15	LM_A15
BA1	LM_A16	LM_A16	LM_A16	LM_A16
A[0:11]	LM_A[3:14]	LM_A[3:14]	LM_A[3:14]	LM_A[3:14]
DQ[0:15]	LM_D[0:15]	LM_D[16:31]	LM_D[32:47]	LM_D[48:63]
† LM_CLK refers to the “delayed” LM_CLK signal. See Figure 20 on page 48.				

Table 10. Sample SDRAM Configuration: Bank 1

SDRAM Pins	IXF6401 Broadband Access Processor Pins 8 Mbits x 16 x 4 Chips			
CLK	LM_CLK†	LM_CLK†	LM_CLK†	LM_CLK†
CKE	VCC	VCC	VCC	VCC
CS#	SDRAMCS1#	SDRAMCS1#	SDRAMCS1#	SDRAMCS1#
RAS#	LM_RAS1#	LM_RAS1#	LM_RAS1#	LM_RAS1#
CAS#	LM_CAS1#	LM_CAS1#	LM_CAS1#	LM_CAS1#
WE#	LM_WR#	LM_WR#	LM_WR#	LM_WR#
DQML	LM_WE0#	LM_WE2#	LM_WE4#	LM_WE6#
DQMH	LM_WE1#	LM_WE3#	LM_WE5#	LM_WE7#
BA0	LM_A15	LM_A15	LM_A15	LM_A15
BA1	LM_A16	LM_A16	LM_A16	LM_A16
A[0:11]	LM_A[3:14]	LM_A[3:14]	LM_A[3:14]	LM_A[3:14]
DQ[0:15]	LM_D[0:15]	LM_D[16:31]	LM_D[32:47]	LM_D[48:63]
† LM_CLK refers to the “delayed” LM_CLK signal. See Figure 20 on page 48.				

3.2.3.2 SSRAM Configuration

For READ and WRITE SSRAM timing, refer to the memory manufacturer’s specification(s). The following tables show the configuration settings for the Micron SSRAM MT58L128L32F and Flow-through Syncburst SRAM.

Note: Buffering may be required due to SSRAM load. Refer to the manufacturer’s load specification.

Table 11. Sample SSRAM Configuration: Banks 0 and 1

SSRAM Pins	IXF6401 Broadband Access Processor Pins			
	Bank 0 (128 Kbits x 32 x 2 Chips)		Bank 1 (128 Kbits x 32 x 2 Chips)	
SA0	LM_SA3	LM_SA3	LM_SA3	LM_SA3
SA1	LM_SA4	LM_SA4	LM_SA4	LM_SA4
SA[3:2]	LM_SA[6:5]	LM_SA[6:5]	LM_SA[6:5]	LM_SA[6:5]
SA[16:4]	LM_A[19:7]	LM_A[19:7]	LM_A[19:7]	LM_A[19:7]
Mode	GND	GND	GND	GND
CLK	LM_CLK†	LM_CLK†	LM_CLK†	LM_CLK†
ADV#	GND	GND	GND	GND
ADSC#	Pull-down	Pull-down	Pull-down	Pull-down
ADSP#	Pull-Up	Pull-Up	Pull-Up	Pull-Up
BWd#	LM_WE3#	LM_WE7#	LM_WE3#	LM_WE7#
BWc#	LM_WE2#	LM_WE6#	LM_WE2#	LM_WE6#
BWb#	LM_WE1#	LM_WE5#	LM_WE1#	LM_WE5#
BWa#	LM_WE0#	LM_WE4#	LM_WE0#	LM_WE4#
BWE#	GND	GND	GND	GND
GW#	Pull-Up	Pull-Up	Pull-Up	Pull-Up
CE#	SSRAMCS0#	SSRAMCS0#	SSRAMCS1#	SSRAMCS1#
CE2#	GND	GND	GND	GND
CE2	Pull-Up	Pull-Up	Pull-Up	Pull-Up
OE#	LM_RD#	LM_RD#	LM_RD#	LM_RD#
DQa, b, c , d	LM_D[0:31]	LM_D[32:63]	LM_D[0:31]	LM_D[32:63]

† LM_CLK refers to the “delayed” LM_CLK signal. See Figure 20 on page 48.

Table 12. Sample SSRAM Configuration: Banks 2 and 3 (Sheet 1 of 2)

SSRAM Pins	IXF6401 Broadband Access Processor Pins			
	Bank 2 (128 Kbits x 32 x 2 Chips)		Bank 3 (128 Kbits x 32 x 2 Chips)	
SA0	LM_SA3	LM_SA3	LM_SA3	LM_SA3
SA1	LM_SA4	LM_SA4	LM_SA4	LM_SA4
SA[3:2]	LM_SA[6:5]	LM_SA[6:5]	LM_SA[6:5]	LM_SA[6:5]
SA[16:4]	LM_A[19:7]	LM_A[19:7]	LM_A[19:7]	LM_A[19:7]
Mode	GND	GND	GND	GND
CLK	LM_CLK†	LM_CLK†	LM_CLK†	LM_CLK†
ADV#	GND	GND	GND	GND
ADSC#	Pull-down	Pull-down	Pull-down	Pull-down

† LM_CLK refers to the “delayed” LM_CLK signal. See Figure 20 on page 48.

Table 12. Sample SSRAM Configuration: Banks 2 and 3 (Sheet 2 of 2)

SSRAM Pins	IXF6401 Broadband Access Processor Pins			
	Bank 2 (128 Kbits x 32 x 2 Chips)		Bank 3 (128 Kbits x 32 x 2 Chips)	
ADSP#	Pull-Up	Pull-Up	Pull-Up	Pull-Up
BWd#	LM_WE3#	LM_WE7#	LM_WE3#	LM_WE7#
BWc#	LM_WE2#	LM_WE6#	LM_WE2#	LM_WE6#
BWb#	LM_WE1#	LM_WE5#	LM_WE1#	LM_WE5#
BWa#	LM_WE0#	LM_WE4#	LM_WE0#	LM_WE4#
BWE#	GND	GND	GND	GND
GW#	Pull-Up	Pull-Up	Pull-Up	Pull-Up
CE#	SSRAMCS2#	SSRAMCS2#	SSRAMCS3#	SSRAMCS3#
CE2#	GND	GND	GND	GND
CE2	Pull-Up	Pull-Up	Pull-Up	Pull-Up
OE#	LM_RD#	LM_RD#	LM_RD#	LM_RD#
DQa, b, c , d	LM_D[0:31]	LM_D[32:63]	LM_D[0:31]	LM_D[32:63]
† LM_CLK refers to the “delayed” LM_CLK signal. See Figure 20 on page 48.				

3.3 UTOPIA Interface

For the Universal Test and Operations Interface for ATM (UTOPIA) interface, the supported clock rate is 37.5 to 50 MHz, to meet the OC-12 (4 x OC-3) line rate.

UTOPIA levels support:

- Level 1 (8-bit)
- Level 2 (16-bit)
- Level 3 (32-bit)
  - — Full duplex requires two IXF6401 processors.
  - — If the IXF6401 processor is programmed for UTOPIA III receive-mode only, the TXDATA signal will carry the upper word [31:16] of the receive data.
  - — If the IXF6401 processor is programmed for UTOPIA III transmit-mode only, RCDATA[15:0] is the upper 16 bits of the transmit data.

For information on configuring the local memory, refer to documentation on UTOPIA Control Register 1, in the *IXF6401 Broadband Access Processor Developer’s Manual* (273453).

3.3.1 UTOPIA I

In UTOPIA I (8-bit), 53 octet cells are transferred.

Table 13. UTOPIA-I Bit Settings

Transmit / Receive Time	Bit 7 .. Bit 0
↓	Header 1
	Header 2
	Header 3
	Header 4
	UDF / HEC
	Payload 1
	...
	Payload 48

3.3.2 UTOPIA II

In UTOPIA II (16-bit), 54 octet cells are transferred.

Table 14. UTOPIA-II Bit Settings

Transmit / Receive Time	Bit 15	Bit 0
↓	Header 1	Header 2
	Header 3	Header 4
	UDF1-HEC	UDF2-HEC
	Payload 1	Payload 2
	...	...
	Payload 47	Payload 48

3.3.3 UTOPIA III

In UTOPIA III (32-bit), 52 octet cells are transferred. There is no HEC support.

Table 15. UTOPIA-III Bit Settings

Transmit / Receive Time	Bit 31 ...	... Bit 16	Bit 15 ...	... Bit 0
↓	Header 1	Header 2	Header 3	Header 4
	Payload 1	Payload 2	Payload 3	Payload 4
	Payload 5	Payload 6	Payload 7	Payload 8
	...	...	...	...
	...	...	...	...
	Payload 45	Payload 46	Payload 47	Payload 48

3.3.4 UTOPIA Modes

Table 16. UTOPIA Modes

UTOPIA Mode	IXF6401	IXF6402
Direct Status	Support – Rev B	Supported
Direct Mode	Not supported	Supported
Address Polling	Not supported	Not Supported

3.3.5 POS Mode

IXF6401 processor can support either one OC-3 port or one OC-12 port in the POS mode.

4.0 Package Information

4.1 Mechanical Specifications

Figure 7. 352-Pin Ball Grid Array

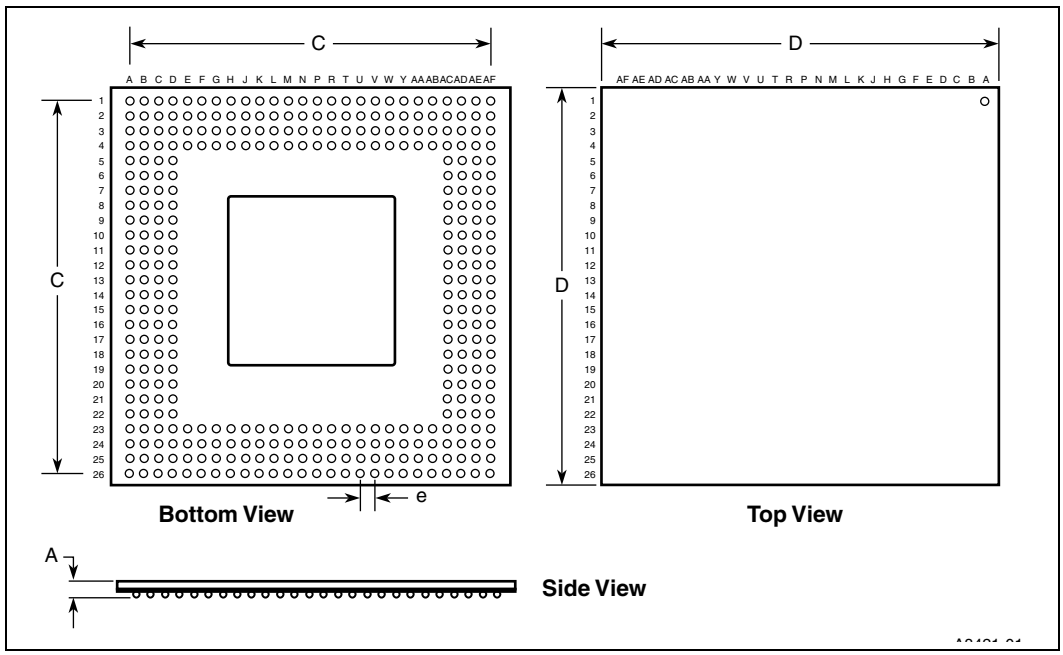


Table 17. Mechanical Dimensions

Description	Parameter	Value	Units
Maximum Mounted Package Height	A	1.4	mm
Ball Footprint	C	31.75	mm
Body Size	D	35 x 35	mm
Ball Pitch	e	1.27	mm
Ball Matrix		26 x 26	
Number of Rows		4	
Number of Columns		4	

4.2 Thermal Specifications

The IXF6401 Broadband Access Processor consumes 6 W of power when operating at 66 MHz. The processor's thermal design power (TDP) level is given in Table 30, "Power Dissipation Requirements for Thermal Design" on page 42.

The processor's Enhanced Ball Grid Array (EBGA) package dissipates the majority of its heat into the environment via the metal cap that is attached to the die.

To ensure proper operation and reliability of the IXF6401 processor, the thermal solution must maintain the case temperature at or below the values specified in Table 18. Considering the power dissipation levels and typical system ambient environment of 0° C to 70° C, system or component-level thermal enhancements will be required if the case temperature exceeds the referenced table's maximum temperatures.

Table 18. EBGA Thermal Absolute Maximum Rating

Parameter	Maximum
T_{case}	85° C

Note: A heat sink is strongly recommended when the processor is operating at 66 MHz.

To dissipate the highest possible thermal power, good system airflow is critical. Airflow is determined by the size and number of fans, vents and/or ducts along with the placement of these elements, in relation to the components and the airflow channels within the system. Noise constraints may limit the size and/or types of fans, vents and/or ducts that can be used in a particular design.

To develop a reliable, cost-effective thermal solution, all of the above variables must be considered. Thermal characterization and simulation should be carried out at the entire system level, accounting for the thermal requirements of each component.

4.2.1 Die Temperature

Case temperature is a function of the local ambient temperature and the internal temperature of the component under evaluation. Since a local ambient temperature is not directly specified for the IXF6401 processor, the only restriction is that the maximum case temperature (T_{case}) is not exceeded.

4.2.2 Package Temperatures

As an aid in determining the optimum airflow and heat sink combination for IXF6401 processor, Table 19 and Table 20 are provided below. The tables show T_{case} as a function of airflow and ambient temperature, at the Thermal Design Power level.

These tables may be used to evaluate prospective thermal solutions.

Table 19. T_{case} as a Function of Ambient Temperature and Airflow: Without Heat Sink

Ambient Temperature (° C)	T_{case} Temperature at Thermal Design Power Level (° C)				
70	130	116	109	106	103
55	115	101	94	91	88
35	95	81	74	71	68
0	60	46	39	36	33
Airflow Linear Feet per Minute	**0**	**100**	**200**	**300**	**400**

Note: Table 19 uses the same notes as Table 20.

Table 20. T_{case} as a Function of Ambient Temperature and Airflow: Using a Heat Sink

Ambient Temperature (° C)	T_{case} Temperature at Thermal Design Power Level (° C)				
70	119	103	95	91	89
55	104	88	80	76	74
35	84	68	60	56	54
0	49	33	25	21	19
Airflow Linear Feet per Minute	**0**	**100**	**200**	**300**	**400**

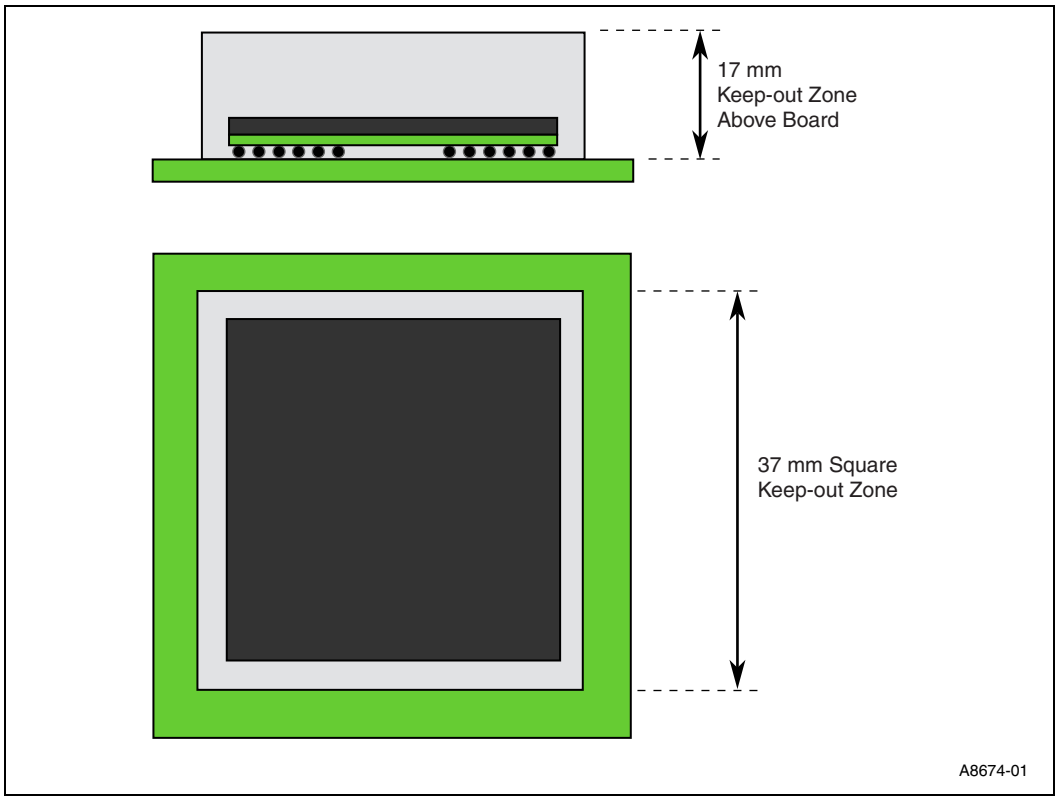
NOTES:
1. The shaded table cells indicate airflow and ambient conditions that will exceed the allowable case temperature.
2. The heat sink case in Table 20 assumes the default thermal solution (see “Thermal Solutions” on page 33).
3. The board used for this evaluation was a four-layer, standard JESEC printed circuit board.
4. The T_{case} maximum temperature, with no heat sink is 122° C. The PSI-JT changes dramatically for a package with a heat sink. The T_{case} maximum temperature, with a heat sink, is 121° C.
5. All data is simulated and is not validated against physical examples.
6. An Airflow Linear Feet per Minute value of zero is defined as a natural-convection environment.

4.2.3 Thermal Solutions

If sufficient airflow cannot be supplied to the component and motherboard, one method frequently used to improve thermal performance is to increase the surface area of the component by attaching a metallic heat sink to the component’s heat spreader, connected to the top of the case. To maximize the heat transfer, maximizing the surface area of the heat sink can reduce the thermal resistance from the heat sink to the air.

Though each design may have unique mechanical volume and height restrictions or implementation requirements, the height, width, and depth constraints typically placed on the IXF6401 processor are shown in Figure 8.

Figure 8. EBGA Heat Sink Volume Restrictions

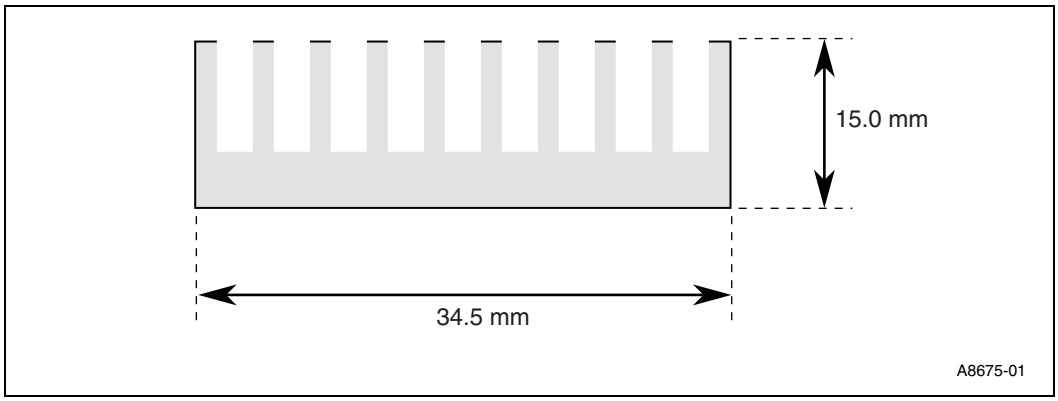


For those who have no control over their end user's thermal environment or for those who wish to bypass the thermal modeling and evaluation process, a default thermal solution has been developed for the IXF6401 processor. That thermal solution will replicate the performance, defined in Table 19 and Table 20, with the processor operating at the thermal design power level.

If implementing the default thermal solution does not bring the case temperature within the values listed in Table 18, additional cooling will be needed. This is achieved by improving airflow to the component and applying thermal enhancements.

If airflow improvements are not implemented or successful, the default thermal solution for the IXF6401 processor is the use of an extruded heat sink. Figure 9 on page 35 is a drawing of the heat sink. Possible sources for extruded heat sinks are listed in "Thermal-Solution Vendors" on page 37.

Figure 9. EBGA Extruded Heat Sink Measurements



4.2.3.1 System Requirements for Thermal Efficiency

General printed-circuit-board design guidelines are listed below as recommendations for maximizing the thermal performance of the EBGA package.

- When connecting ground (thermal) vias to the ground plane(s), do not use thermal-relief patterns. Thermal-relief patterns are designed to limit heat transfer between the vias and the copper planes and constrict the heat flow path from the component to the ground planes in the printed circuit board.
- When the package is in a still-air environment and without a heat sink, the primary heat path for conducting heat out of the PBGA package is through the vias directly under the die, internal planes, and the ground planes of the printed circuit board. Increasing the number of ground planes in the printed circuit board, and increasing the thickness of those copper planes, increases heat conduction and lowers the package's temperature. Since the primary path of heat dissipation for the IXF6401 processor EBGA package is through the top metallic heat spreader, printed circuit boards using 1.0-ounce copper thickness are acceptable.
- Since the board temperature also has an effect on the thermal performance of the package, avoid placing the IXF6401 processor adjacent to high-power dissipation devices.
- For maximum thermal performance, locate the components in the main stream of the airflow path, if airflow exists. Avoid placing the components downstream, behind larger devices or devices with heat sinks that obstruct the airflow or supply excessively heated air.

The preceding guidelines are not all-inclusive and are listed to give the designer known good-design practices to maximize the thermal performance of the components.

The top view of the recommended printed-circuit-board layout, for the 35-mm, 352-ball EBGA is shown in Figure 7 on page 31.

Figure 10. Recommended and Discouraged Via Connections (Top View)

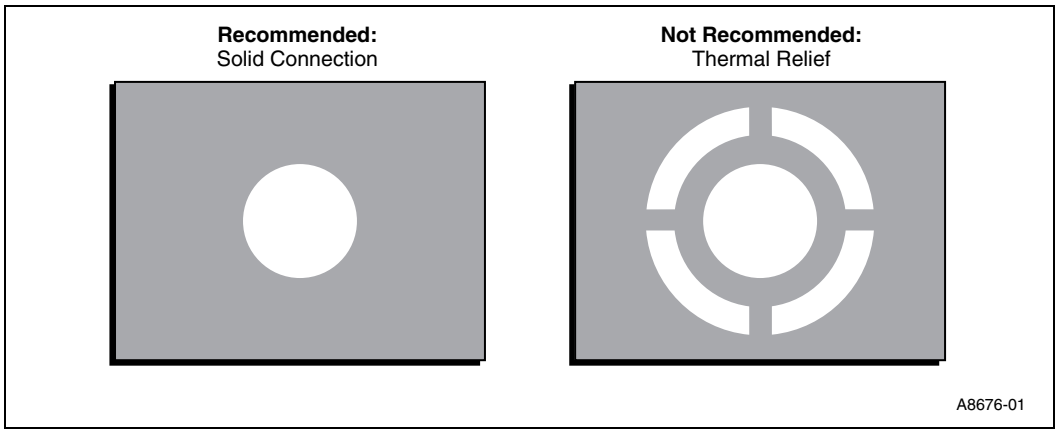
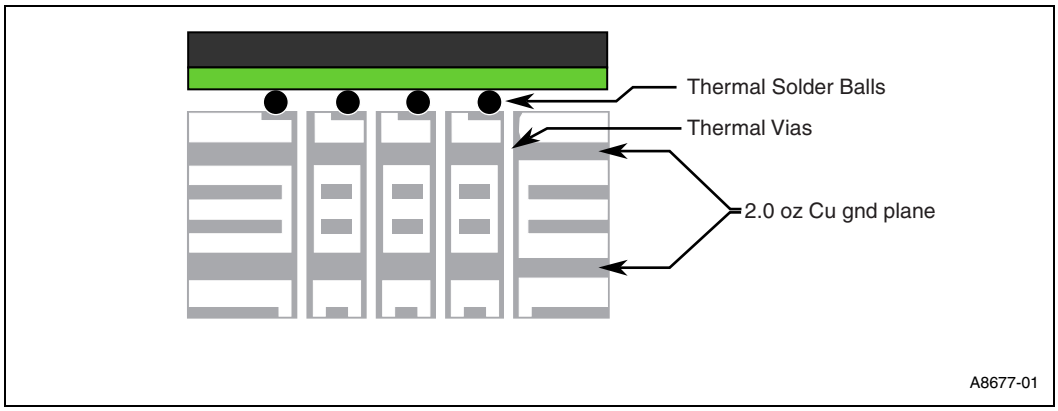


Figure 11. Recommended Printed-Circuit-Board Stack Up (Cross-Sectional View)



4.2.3.2 Recommendations for Thermal Solutions

When the clock for the IXF6401 processor is running at 66 MHz or higher, a passive heat sink is strongly recommended. See “Thermal-Solution Vendors” on page 37 for a list of possible vendors.

4.2.4 Thermal-Solution Vendors

Table 21 provides a vendor list as a reference to our customers. This list should not be considered recommendations or product endorsements by Intel®.

Table 21. Thermal-Solution Vendor List

Heat Sink	
Aavid Thermalloy Corporate headquarters: 80 Commercial St. Concord, NH 03301 Telephone: (603) 224-9988 Other worldwide offices. Visit their Web site for contact information: http://www.aavid.com	ChipCoolers*, Inc. Heatsinks 333 Strawberry Field Road Warwick, RI 02886 Telephone: (401) 739-7600 or (800) 227-0254 Web site: http://www.chipcoolers.com E-mail: sales@chipcoolers.com
Sumitomo Corporation International, group headquarters: Osaka: 5-33, Kitahama 4-chome, Chuo-ku, Osaka 540-8666 Tokyo: 2-2, Hitotsubashi 1-chome, Chiyoda-ku, Tokyo 100-8601 Sumitomo Corporation of America Americas headquarters: 600 Third Ave. New York, NY 10016-2001 Telephone: (212) 207-0700 Other worldwide offices. Visit their Web site for contact information: http://www.sumitomocorp.com	
Clips	
Chip Coolers* Inc. (See listing under “Heat Sink”)	
Adhesives	
Loctite Corporation Americas headquarters: 1001 Trout Brook Crossing Rocky Hill, CT 06067-3910 Telephone: (860) 571-5100 Other worldwide offices. Visit their Web site for contact information: http://www.loctite.com	Parker Hannifin Corp. Chomerics Division World headquarters: 77 Dragon Court Woburn, MA 01888-4014 Telephone: (781) 935-4850 Other worldwide offices. Visit their Web site for contact information: http://www.chomerics.com E-mail address: mailbox@chomerics.com

4.3 Ordering Information

Figure 12 shows the markings on the IXF6401 Broadband Access Processor. Table 22 shows gives the details for the figure's codes.

Figure 12. IXF6401 Broadband Access Processor Markings

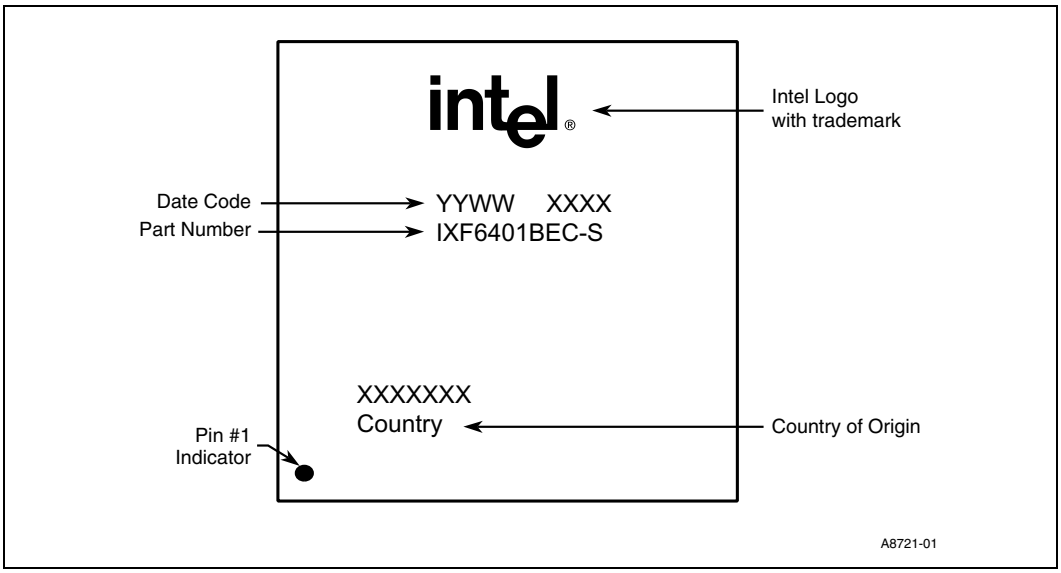


Table 22. IXF6401 Broadband Access Processor Date and Part-Number Codes

Code	Description(s)
Date Codes	
YY	Two-digit designation for year
WW	Two-digit designation for work week
Part-Number Codes	
IXF6401	Designates the IXF6401 Broadband Access Processor
B	The die revision and stepping
E	Indicates the Enhanced Ball Grid Array Package (352 balls)
C	Operating temperature range C = 0 to 70° C
S	Speed grade 7 = 66.6 MHz
Country	Country of manufacture

5.0 Electrical Specifications

5.1 Absolute Maximum Ratings

Warning: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only.

Table 23. Absolute Maximum Ratings

Parameter	Maximum Rating
Case temperature under bias	0° C to 85° C
Storage temperature	–65° C to 150° C
Ambient temperature (Power ON)	0° C to 70° C
Junction temperature	125° C
Voltage on any pin	–0.3 V to V_{cc}+0.3 V (with respect to GND)
DC input Voltage	–0.5 V to 7.0 V

5.2 Operating Conditions

Warning: Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

Table 24. Operating Conditions

Parameter	Minimum	Maximum
Supply voltage, I/O V_{cc}	3.3 V – 5%	3.3 V + 5%
Ambient temperature	0° C	70° C

5.3 DC Specifications

This section contains the tables listed below.

- Table 25, "DC Characteristics (Single-PHY,155 Mbps, 622 Mbps)" on page 40 — The DC characteristics for UTOPIA Level 2 Version 1.0
- Table 26, "DC Characteristics for (Multi-PHY, 622 Mbps)" on page 40
- Table 27, "DC Characteristics for UTOPIA Level 3 Baseline Text" on page 41
- Table 28, "DC Characteristics for PCI" on page 41
- Table 29, "DC Characteristics for LM" on page 42
- Table 30, "Power Dissipation Requirements for Thermal Design" on page 42

Table 25. DC Characteristics (Single-PHY,155 Mbps, 622 Mbps)

Symbol	Parameters	Test Conditions	Min	Max	Units	Notes
VIL	Input LOW Voltage		-0.3 V	+0.8 V	V	1
VIH	Input HIGH Voltage		+2.0 V	V_{cc} + 0.3 V	V	2
VOH	Output or bidirectional HIGH Voltage	IOH > -4 mA	+2.4 V		V	3
VOL	Output or bidirectional LOW Voltage	IOL > +4 mA		+0.5 V	V	4
IOH	Output current at HIGH Voltage	VOH > +2.4 V	-4 mA		mA	5
IOL	Output current at HIGH Voltage	VOL < +0.5 V	+4 mA		mA	6
IIH	Input current at HIGH Voltage					7
IIL	Input current at LOW Voltage					7

Note: Table 25 uses the same notes as Table 26.

Table 26. DC Characteristics for (Multi-PHY, 622 Mbps)

Symbol	Parameters	Test Conditions	Min	Max	Units	Notes
VIL	Input LOW Voltage		-0.3 V	+0.8 V	V	1
VIH	Input HIGH Voltage		+2.0 V	V_{cc} + 0.3 V	V	2
VOH	Output or bidirectional HIGH Voltage	IOH > –8 mA	+2.4 V		V	3
VOL	Output or bidirectional LOW Voltage	IOL > +8 mA		+0.5 V	V	4
IOH	Output current at HIGH Voltage	VOH > +2.4 V	-4 mA		mA	5
IOL	Output current at HIGH Voltage	VOL < +0.5 V	+4 mA		mA	6
IIH	Input current at HIGH Voltage					7
IIL	Input current at LOW Voltage					7

NOTES:
1. A device with VIL, min. $\leq$ –0.3 V is compliant to this specification.
2. A device with VIH, max. $\geq$ VDD + 0.3 V is compliant with this specification.
3. Negative current flows out of the considered node (out of the PHY/ATM layer device pin). A device with VOH, min. $\geq$ +2.4 V (and IOH $\geq$ –4 mA) is compliant with this specification.
4. Positive current flows into the considered node (into PHY/ATM layer device pin). A device with VOL, max. $\leq$ +0.5 V (and IOL $\geq$ +4 mA) is compliant with this specification.
5. Negative current flows out of the considered node (out of the PHY/ATM layer device pin). IOH, min. defines the minimal required IOH value for the driver.
   A device with IOH, min. $\geq$ –4 mA (and VOH $\geq$ +2.4 V) is compliant to this specification.
6. Positive current flows into the considered node (into the PHY/ATM layer device pin). IOL, min. defines the minimal required IOL value for the driver.
7. To allow several technologies, no values for IIH and IIL are specified. An input can sink and source.

Table 27. DC Characteristics for UTOPIA Level 3 Baseline Text

Symbol	Parameters	Test Conditions	Min	Max	Units	Notes
VOH	High-Level Output Voltage	Test Condition	2.4 V		V	
VOH	High-Level Output Voltage	IOH = –8 mA	2.0 V		V	
	Normal Switching Point					
VIL	Low-Level Input Voltage			0.8	V	
VOL	Low-Level Input Voltage			0.4	V	
IIN	Input Current-Input Only	Vin = 0 or Vin = Vdd		+5	µA	
	Input Current-I/O Terminals			+15		

Table 28. DC Characteristics for PCI

Symbol	Parameters	Test Conditions	Min	Max	Units	Notes
VCC	Supply Voltage		3.0 V	3.6 V	V	
VIH	Input HIGH Voltage		0.5 V_{cc}	V_{cc} +0.5	V	
VIL	Input LOW Voltage		–0.5 V	0.3 V_{cc}	V	
VIPU	Input LOW Voltage		0.7 V_{cc}		V	1
IIL	Input Leakage Current	0 < Vin < V_{cc}		+10	µA	2
VOH	Output HIGH Voltage	Iout = –500 µA	0.9 V_{cc}		V	
VOL	Output LOW Voltage	Iout = 1,500 µA		0.1 V_{cc}	V	
CIN	Input Pin Capacitance			10	pF	3
CCLK	CLK Pin Capacitance		5	12	pF	
CIDSEL	IDSEL Pin Capacitance			8	pF	4
LPIN	Pin Inductance			20	nH	5

NOTES:
1. This specification should be guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Applications sensitive to static power utilization should assure that the input buffer is conducting minimum at this input voltage.
2. Input leakage currents include hi-Z output leakage for all bidirectional buffers with three-state outputs.
3. Absolute maximum pin capacitance for the PCI input is 10 pF (except for CLK) with an exception granted to motherboard-only devices, which could be up to 16 pF, in order to accommodate PGA packaging. This would mean in general that components for expansion boards would need to use alternatives to ceramic PGA packaging, i.e., SGA.
4. Lower capacitance in this input-only pin allows for non-resistive coupling.
5. This is a recommendation, not an absolute requirement.

Table 29. DC Characteristics for LM

Symbol	Parameters	Test Conditions	Min	Max	Units	Notes
VCC	Supply Voltage		0.3 V	3.6 V	V	
VIH	Input HIGH Voltage		0.5 V_{cc}	V_{cc}+ 0.5	V	
VIL	Input LOW Voltage		–0.5 V	0.3 V_{cc}	V	
IIL	Input Leakage Current	0 < Vin < Vcc		±10	µA	
VOH	Output HIGH Voltage	Iout = 500 µA	0.9 V_{cc}		V	
VOL	Output LOW Voltage	Iout = –1,500 µA		0.1 V_{cc}	V	

Figure 13. Tval (min) and Slew Rate

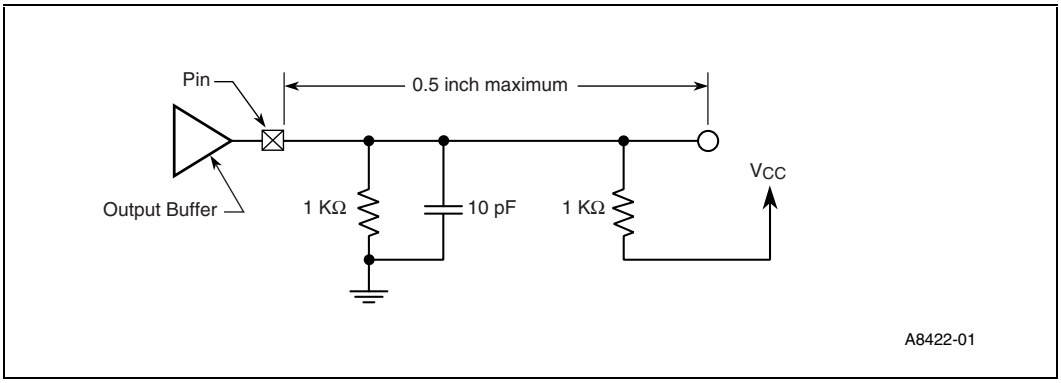


Table 30. Power Dissipation Requirements for Thermal Design

Parameter	Typical†	Maximum††	Unit	Frequency
Thermal design power	TBD	6	Watts	66.6 MHz
Active power†††	4.5	TBD	Watts	66.6 MHz

NOTES:

† This value is an estimate of the typical power dissipation in a system. The value is expected to be the average value that will be measured in a system, using a typical device at the specified voltage and running typical applications. This value is dependent upon the specific system configuration. Typical power specifications are not tested.

†† Systems must be designed to thermally dissipate the maximum thermal design power (TDP) unless the system uses thermal feedback to limit the processor's maximum power. The maximum thermal design power is determined using a worst-case instruction mix and takes into account the thermal time constant of the package. The given value is an estimate.

††† Active power is the average power measured in a system, using a typical device that is running typical applications under normal operating conditions at nominal V_{cc} and room temperature.

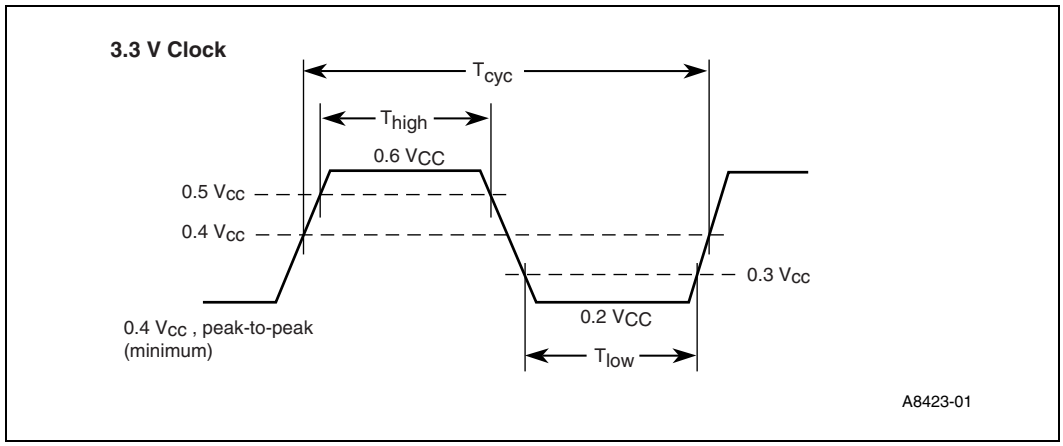
5.4 Timing Specifications

5.4.1 Clock Timing

The clock waveform must be delivered to each 66-Mhz PCI component in the system. In the case of add-in boards, compliance with clock specification is measured at the add-in board component, not at the connector slot.

Figure 14 shows the clock waveform and required measurement points for 3.3-V signaling environments.

Figure 14. 3.3 V Clock Waveform



5.4.2 Clock Specifications

Table 31. 33-MHz/66-MHz Timing Parameters

Symbol	Parameter	66 MHz		33 MHz		Units	Notes
		Min	Max	Min	Max		
Tcyc	Clock cycle time	15	30	30		ns	1, 3
Thigh	Clock high time	6		11		ns	
Tlow	Clock low time	6		11		ns	
	Clock slew rate	1.5	4	1	4	V/ns	2

NOTES:
1. In general, all 66.6-MHz PC components must work with a clock frequency of up to 66.6 MHz. Device operational parameters at frequencies under 33 MHz must conform to the specifications in Chapter 4 of the PCI specification, rev 2.1.
2. The clock frequency may be changed at any time during the operation of the system as long as the clock edges remain “clean” (monotonic) and the minimum cycle and high and low times are not violated. The clock maybe stopped only in a low state. A variance on this specification is allowed for components designed for use on the system planar only. For clock frequency between 33 MHz and 66.6 MHz, the clock frequency may not change except in conjunction with a PCI reset.
3. Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to-peak portion of the clock waveform as shown in Figure 31. Clock slew rate is measured by the slew rate circuit shown in Figure 13, “Tval (min) and Slew Rate” on page 42. The minimum clock rate must not be violated for any single clock cycle, i.e., accounting for all system jitter.

5.4.3 PCI Timing Parameters

Table 32. 33-MHz and 66-MHz Timing Parameters

Symbol	Parameter	66 MHz		33 MHz		Units	Notes
		Min	Max	Min	Max		
Tval	PCI_CLK to signal valid delay – bused signals	2	6	2	11	ns	1, 2, 3
Tval(ptp)	PCI_CLK to signal valid delay – point-to-point signals	2	6	2	12	ns	1, 2, 3
Ton	Float to active delay	2		2		ns	1, 5
Toff	Active to Float delay		14		28	ns	1, 5
Tsu	Input setup time to PCI_CLK – bused signals	3				ns	3, 4
Tsu(ptp)	Input setup time to PCI_CLK – point-to-point signals	5		10 12		ns	3, 4
Th	Input Hold time from PCI_CLK	0		0		ns	4
Trst	RESET active time after Power stable	1		1		ms	
Trst-clk	RESET active time after PCI_CLK stable	100		100		µs	
Trst-off	RESET active to output float delay		40		40	ns	
Trrsu	PCI_REQ64# to PCI_RST# setup time	10 Tcyc		10 Tcyc		ns	
Trrh	PCI_RST# to PCI_REQ64# HOLD time	0	50	0	50	ns	

NOTES:
1. See the timing measurement conditions in Figure 15 and Figure 16. It is important that all driven signal transitions drive to their Voh or Vol level within one Tcyc.
2. Minimum times are measured at the package pin with the load circuit shown in Figure 17 on page 46 and Figure 18 on page 46. Maximum times are measured with the load circuit shown in Figure 17 on page 46 and Figure 18 on page 46.
3. PCI_REQ64# and PCI_GNT# are point-to-point signals and have different input setup times than do bused signals. The PCI_REQ64# and PCI_GNT# signals have a setup time of 5 ns at 66.6 Mhz. All other signals are bused. See the timing measurement conditions in chapter four of the PCI specification.
4. PCI_RST# is asserted and deasserted asynchronously with respect to PCI_CLK. All output drivers must be floated when PCI_RST# is active.
5. For the purposes of active/float timing measurements, the HI-Z or “off” state is defined as when the total current delivered through the component pin is less than or equal to the current leakage specification.

Figure 15. Output Timing Measurement Conditions

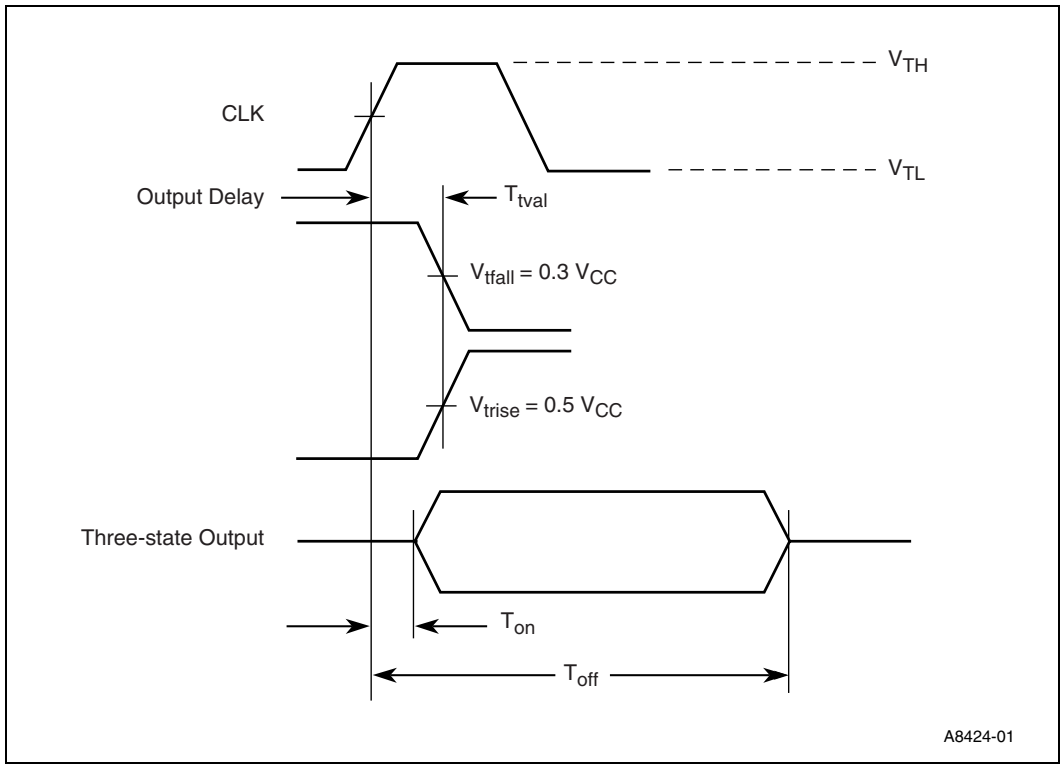


Figure 16. Input Timing Measurement Conditions

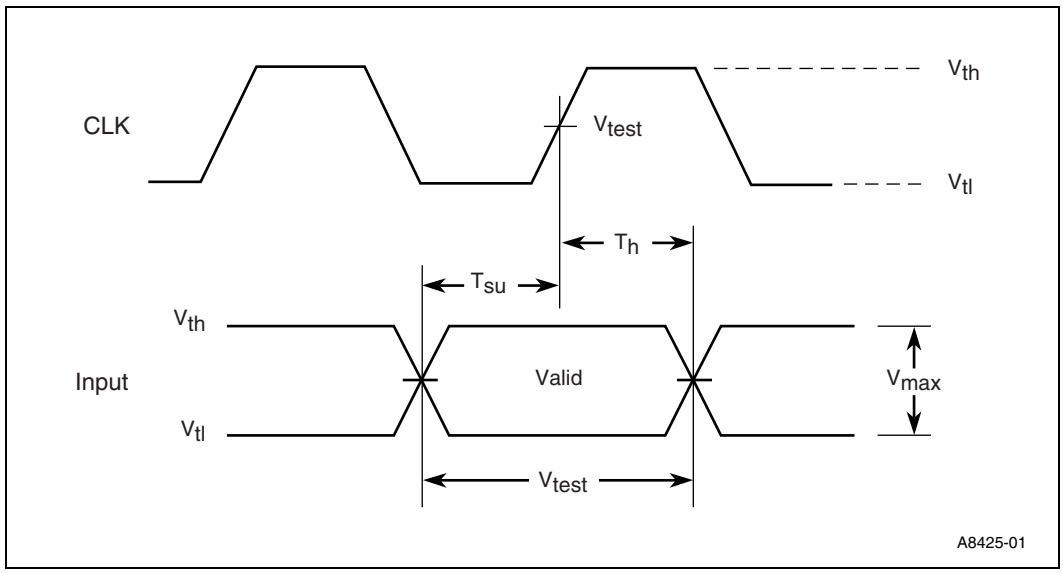


Figure 17. Tval (max) Rising Edge

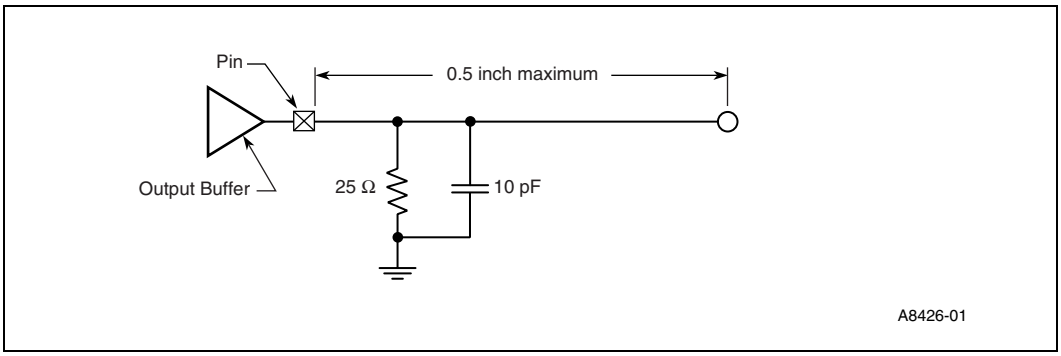
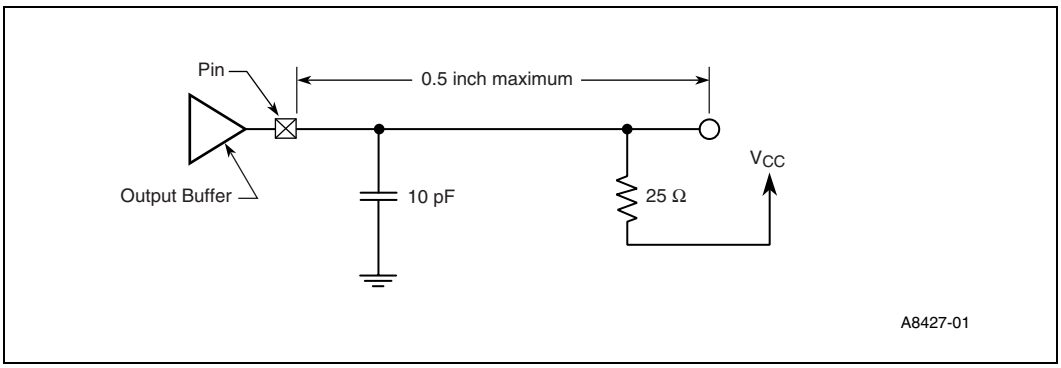


Figure 18. Tval (max) Falling Edge



5.4.4 UTOPIA Timing Parameters

The IXF6401 processor's UTOPIA interface is fully compliant with the ATM Forum specifications. The following timing description is an extract from the ATM Form UTOPIA Level 2 Specification, Version 1.0 of June 1995 (af-phy-0039.0000).

Table 33. Transmit Timing

16-bit Data Bus, UTOPIA-II 50-MHz at Cell Interface, Single/Multi-PHY

Signal Name	Input (I) Output (O)	Item	Description	Min	Max
TXCLK	I	f1 tT2 tT3 tT4	TXCLK frequency (nominal) TXCLK duty cycle TXCLK peak-to-peak jitter TXCLK rise/fall time	0 40%	50 MHz 60% 5% 2 ns
TXDATA[15:0], TXPRTY, TXSOC, TXEN#	O	tT5 tT6	Output delayed	4 ns	13 ns
TXFULL#/ TXCLAV	I	tT7 tT8	Input setup to TXCLK Input hold from TXCLK	4 ns 1 ns	

Table 34. Receive Timing

16-bit Data Bus, UTOPIA-II 50-MHz at Cell Interface, Single/Multi-PHY

Signal Name	Input (I) Output (O)	Item	Description	Min	Max
RCCLK	I	f1 tT2 tT3 tT4	RCCLK frequency (nominal) RCCLK duty cycle RCCLK peak-to-peak jitter TXCLK rise/fall time	0 40%	50 MHz 60% 5% 2 ns
RXEN#	O	tT5 tT6	Output delayed	4 ns	13 ns
RCDATA[15:0], RCPRTY, RCSOC, RCEMPTY#/ RCCLAV	I	tT7 tT8	Input setup to RCCLK Input hold from RCCLK	4 ns 1 ns	

5.4.5 Local Memory Bus Timing

Table 35. Local Memory Bus Timing Parameters

Symbol	Parameter	66 MHz		33 MHz		Units	Notes
		Min	Max	Min	Max		
Tcyc	Clock cycle time	15				ns	1, 2
Thigh	Clock high time	6	9			ns	
Tlow	Clock low time	6	9			ns	
Tsetup	Input setup	1				ns	
Thold	Input hold	4				ns	
Tdly	Output delay	4	13			ns	
Thigh-z	High impedance delay	5	14			ns	

NOTES:
1. See the timing measurement conditions in Figure 14. It is important that all driven signal transitions drive to their Voh or Vol level within one Tcyc.
2. Minimum times are measured at the package pin with the load circuit shown in Figure 17 on page 46 and Figure 18 on page 46. Maximum times are measured with the load circuit shown in Figure 17 on page 46 and Figure 18 on page 46.

Figure 19. Local Memory Bus Timing Specifications

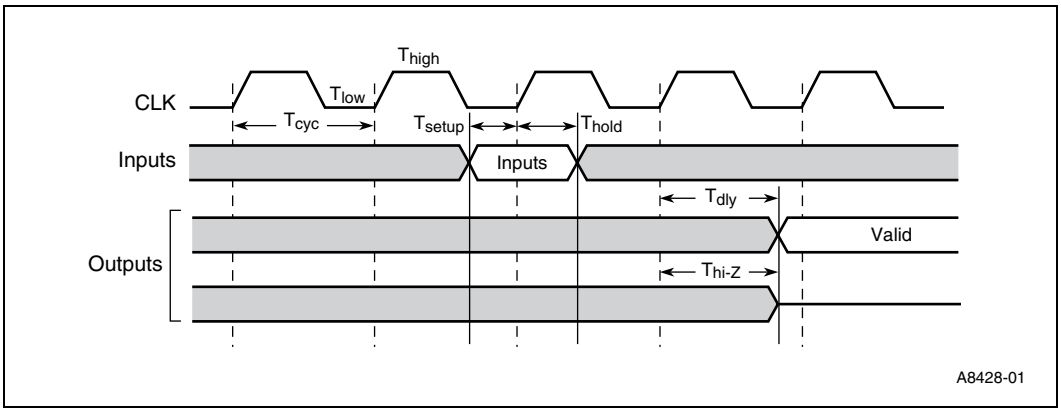


Figure 20. Recommended Local Memory Clock Circuitry