OKI semiconductor

MSM28C16A

2K-Word x 8-Bit CMOS E²PROM

GENERAL DESCRIPTION

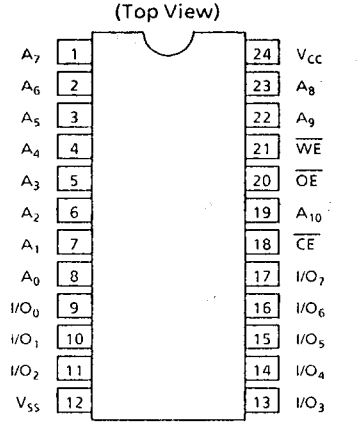
The MSM28C16ARS is a CMOS electrically erasable and programmable read only memory (E²PROM) with a capacity of 2,048 words x 8 bits using a single 5V power supply. Its timing is similar to that of a static RAM. Byte data written in programming mode starts when the $\overline{WE}$ and $\overline{CE}$ signals are set to low level for 100 ns. The address and data bus information are latched in the IC, and the system is released for other tasks during the write cycle. Writing in the MSM28C16A starts after automatic erasure of the selected byte, and the erase/write cycle finishes within 10 ms.

FEATURES

- Single 5V power supply
- High-speed access: 200 ns max.
- Byte write cycle: 10 ms max.
- Internal address and data latch in write cycle
- Automatic erasure before writing
- Automatic ending of write operation
- Built-in protective function for false writing
- TTL compatible input/output
- Pin arrangement in compliance with JEDEC Standard
- Compatible with Xicor 2816A

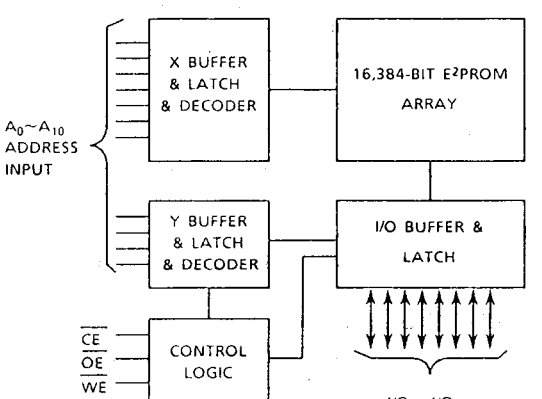
PIN CONFIGURATION

(Top View)



A_0~A_{10} :ADDRESS INPUT
I/O_0~I/O_7 :DATA I/O
$\overline{CE}$:CHIP ENABLE
$\overline{OE}$:OUTPUT ENABLE
$\overline{WE}$:WRITE ENABLE
V_{CC} : +5V
V_{SS} :GROUND

FUNCTION BLOCK DIAGRAM



9

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
V_{IH}	X	X	Standby and Write inhibit	High Z	Standby
V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
V_{IL}	V_{IH}	⎍	Byte Write ($\overline{WE}$ controlled)	D_{IN}	Active
⎍	V_{IH}	V_{IL}	Byte Write ($\overline{CE}$ controlled)	D_{IN}	Active
V_{IL}	V_{IH}	V_{IH}	Write Inhibit	High Z	
V_{IL}	V_{IL}	V_{IL}	Write Inhibit	High Z	

Note) X: Don't care (V_{IH} or V_{IL})

DEVICE OPERATION

READ

The data in the MSM28C16A can be read by setting $\overline{WE}$ to high (H), $\overline{CE}$ to low (L) and $\overline{OE}$ to L. The data becomes valid upon lapse of t_{AA} after the address change, t_{CE} after $\overline{CE}$ setting to L, or t_{OE} after $\overline{OE}$ setting to L, whichever is the latest. The I/O pin remains in a high impedance state to prevent data bus contention in the system when $\overline{OE}$ or $\overline{CE}$ is set to H.

WRITE

The write cycle starts when $\overline{WE}$ and $\overline{CE}$ are set to L and $\overline{OE}$ is set to H. The address input is latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ (Whichever is later). The I/O pin data is latched on the first rising edge of $\overline{WE}$ or $\overline{CE}$. The address and data are latched in 100 ns using the TTL level write signal. When the data latch ends, the MSM28C16A automatically erases the selected byte and writes the new data within 10 ms.

DATA POLLING

DATA polling is provided to indicate the completion of a write cycle. While the write operation is in progress, attempts to read the last byte written output the complement of that data on I/07. Once the write cycle is completed, all I/Os produce true data during a read cycle.

STANDBY

The power consumption decreases greatly by setting $\overline{CE}$ to TTL H level.

ENDURANCE

The MSM28C16A is designed for applications that require up to 10,000 write cycles per byte.

DATA PROTECTION

Four functions are incorporated to prevent false writing at the time of power up, power down, or power noise.

1. V_{CC} LEVEL DETECTION

   The write cycle to the device is automatically inhibited when V_{CC} drops below 3.0V.

2. TIME DELAY

The MSM28C16A automatically inhibits any write operation for the period between 5 ms and 20 ms after V_{CC} reaches V_{WI} level at power up.
This allows sufficient time for the system to set $\overline{WE}$ or $\overline{CE}$ to the H level before writing starts.

3. $\overline{OE}$ GATING

The MSM28C16A inhibits any write operation when $\overline{OE}$ is at the L level.

4. $\overline{WE}$ NOISE PROTECTION

The write cycle does not start for a write pulse shorter than 20 ns.

ABSOLUTE MAXIMUM RATINGS (Note 1)

(Ta = 25°C)

Rating	Symbol	Value	Unit	Condition
Power Supply Voltage	V_{CC}	− 0.3 to 7	V	Referenced to V_{SS}
Input Voltage (Note 2)	V_I	− 0.3 to V_{CC} + 0.3	V	Referenced to V_{SS}
Output Voltage (Note 2)	Vo	− 0.3 to V_{CC} + 0.3	V	Referenced to V_{SS}
Power Dissipation	P_D	1	W	Per package
Operating Temperature	Topr	0 to 70	°C	−
Storage Temperature	Tstg	− 55 to 150	°C	−

Note 1) The stress from exceeding the absolute maximum rating causes permanent damage to the device. These are stress ratings only and do not mean functional operations of the device. They are by no means above the operating characteristics in the data sheet. Leaving the device for a long time in the absolute maximum rating state may adversely affect device reliability.

Note 2) The device has a special circuit to protect the internal circuit from damage caused by static electricity, but do not use it beyond the maximum ratings for safety.

ELECTRICAL CHARACTERISTICS

DC OPERATING CHARACTERISTICS

(VCC = 5V ± 10%, Ta = 0°C~70°C)

Parameter	Symbol	Test Condition	Limits		Unit
			Min	Max	
Input Low Voltage	V_{IL}		− 0.3	0.8	V
Input High voltage	V_{IH}		2.0	V_{CC} + 0.3	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA	−	0.4	V
Output High Voltage	V_{OH}	I_{OH} = − 400μA	2.4	−	V
V_{CC} Voltage for Write Inhibit	V_{WI}		3.0	4.0	V
Input Leakage Current	I_{LI}	V_{IN} = 0 ~ V_{CC}	− 10	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 0 ~ V_{CC}	− 10	10	μA
V_{CC} Power Current	I_{CCA}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, Io = 0mA t_{RC} = 200ns V_{CC} = MAX	−	30	mA
Standby Current	I_{CCS}	$\overline{CE}$ = V_{CC} − 0.2V V_{CC} = MAX	−	0.1	mA
	I_{CCS1}	$\overline{CE}$ = V_{IH}, V_{CC} = MAX	−	1	mA

CAPACITANCE

(Ta = + 25°C, f = 1.0MHz, V_{CC} = 5V)

Parameter	Symbol	Test Condition	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	10	pF
Input Capacitance	C_{IN}	V_{IN} = 0V	6	pF

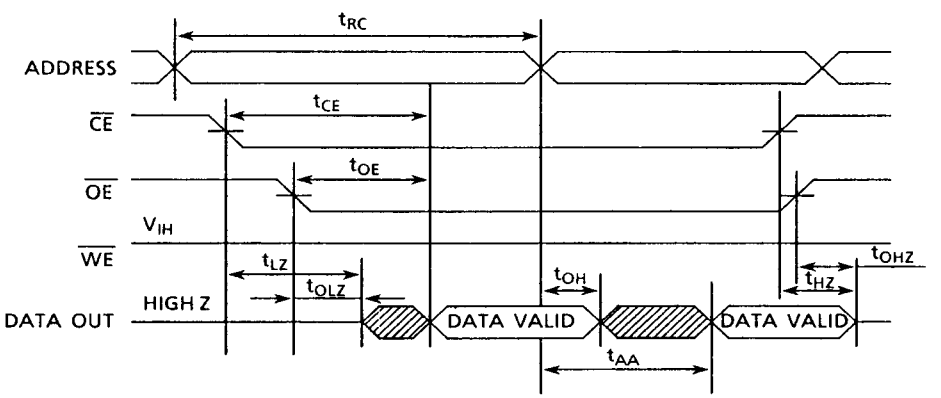
AC CHARACTERISTICS

READ OPERATION

(V_{CC} = 5V ± 10%, Ta = 0°C~70°C)

Parameter	Symbol	MSM28C16A-20		Unit
		Min	Max	
Read Cycle Time	t_{RC}	200	-	ns
Address Access Time	t_{AA}	-	200	ns
$\overline{CE}$ Access Time	t_{CE}	-	200	ns
$\overline{OE}$ Access Time	t_{OE}	-	80	ns
$\overline{CE}$ to Output in Low Z	t_{LZ}	10	-	ns
$\overline{CE}$ to Output in High Z	t_{HZ}	10	50	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	10	-	ns
$\overline{OE}$ to Output in High Z	t_{OHZ}	10	50	ns
Output Hold Time	t_{OH}	20	-	ns

READ CYCLE



AC Test Conditions	Input Pulse Levels	0.6 to 2.4 Volts
	Input Rise/Fall Times	5 ns
	Timing Reference Levels	INPUT : 1.5V, OUTPUT : 0.8V & 2.0V
	Output Load	1 TTL Gate and C_L = 100 pF

9

WRITE

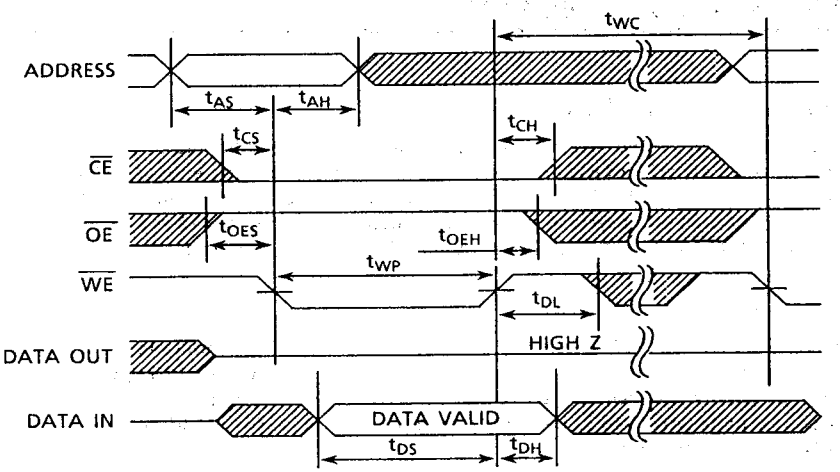
(V_{CC} = 5V ± 10%, Ta = 0°C ~ 70°C)

Parameter	Symbol	Limits		Unit
		Min	Max	
Write Cycle Time	t_{WC}	–	10	ms
Address Setup Time	t_{AS}	10	–	ns
Address Hold Time	t_{AH}	70	–	ns
Chip Enable or Write Setup Time	t_{CS}	0	–	ns
Chip Enable or Write Hold Time	t_{CH}	0	–	ns
Chip Enable Pulse Width	t_{CW}	100	–	ns
Output Enable Setup Time	t_{OES}	10	–	ns
Output Enable Hold Time	t_{OEH}	10	–	ns
Write Enable Pulse Width (Note 1)	t_{WP}	100	–	ns
Data Latch Time	t_{DL}	50	–	ns
Data Setup Time	t_{DS}	50	–	ns
Data Hold Time	t_{DH}	10	–	ns
Write Inhibit Time on Power Up	t_{INIT}	5	20	ms

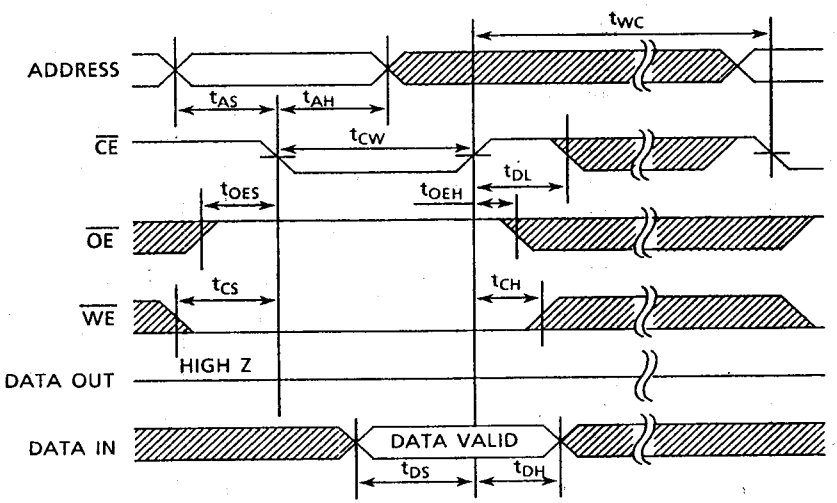
Note 1) $\overline{WE}$ is protected from noise. The write cycle does not start for a write pulse shorter than 20 ns.

WRITE CYCLE

CONTROLLED BY $\overline{WE}$



CONTROLLED BY $\overline{CE}$



9