# QUADRUPLE 2-INPUT OR GATE

The HEF4071B is a positive logic quadruple 2-input OR gate. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

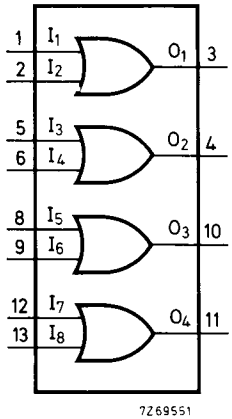


Fig. 1 Functional diagram.

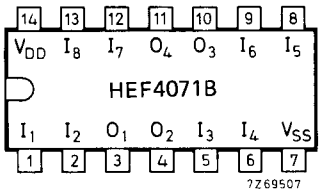


Fig. 2 Pinning diagram.

HEF4071BP : 14-lead DIL; plastic (SOT-27).
HEF4071BD: 14-lead DIL; ceramic (cerdip) (SOT-73).
HEF4071BT : 14-lead mini-pack; plastic (SO-14; SOT-108A).

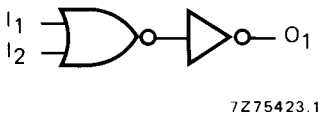


Fig. 3 Logic diagram (one gate).

**FAMILY DATA**

**$I_{DD}$ LIMITS category GATES**

see Family Specifications

## A.C. CHARACTERISTICS

$V_{SS}$ = 0 V; $T_{amb}$ = 25 °C; $C_L$ = 50 pF; input transistion times ⩽ 20 ns

| | $V_{DD}$ V | symbol | typ. | max. | | typical extrapolation formula |
|---|---|---|---|---|---|---|
| Propagation delays | | | | | | |
| $I_n \rightarrow O_n$ | 5 | | 55 | 115 | ns | 28 ns + (0,55 ns/pF) $C_L$ |
| HIGH to LOW | 10 | $t_{PHL}$ | 25 | 50 | ns | 15 ns + (0,23 ns/pF) $C_L$ |
| | 15 | | 20 | 35 | ns | 12 ns + (0,16 ns/pF) $C_L$ |
| | 5 | | 45 | 90 | ns | 18 ns + (0,55 ns/pF) $C_L$ |
| LOW to HIGH | 10 | $t_{PLH}$ | 20 | 45 | ns | 9 ns + (0,23 ns/pF) $C_L$ |
| | 15 | | 15 | 30 | ns | 7 ns + (0,16 ns/pF) $C_L$ |
| Output transition times | | | | | | |
| | 5 | | 60 | 120 | ns | 10 ns + (1,0 ns/pF) $C_L$ |
| HIGH to LOW | 10 | $t_{THL}$ | 30 | 60 | ns | 9 ns + (0,42 ns/pF) $C_L$ |
| | 15 | | 20 | 40 | ns | 6 ns + (0,28 ns/pF) $C_L$ |
| | 5 | | 60 | 120 | ns | 10 ns + (1,0 ns/pF) $C_L$ |
| LOW to HIGH | 10 | $t_{TLH}$ | 30 | 60 | ns | 9 ns + (0,42 ns/pF) $C_L$ |
| | 15 | | 20 | 40 | ns | 6 ns + (0,28 ns/pF) $C_L$ |

| | $V_{DD}$ V | typical formula for P (μW) | where |
|---|---|---|---|
| Dynamic power dissipation per package (P) | 5 | 1150 $f_i$ + Σ($f_o C_L$) x $V_{DD}^2$ | $f_i$ = input freq. (MHz)<br>$f_o$ = output freq. (MHz)<br>$C_L$ = load capacitance (pF)<br>Σ($f_o C_L$) = sum of outputs<br>$V_{DD}$ = supply voltage (V) |
| | 10 | 4800 $f_i$ + Σ($f_o C_L$) x $V_{DD}^2$ | |
| | 15 | 19 700 $f_i$ + Σ($f_o C_L$) x $V_{DD}^2$ | |