

**DESCRIPTION**

Series 55450B/75450B dual peripheral drivers are a family of versatile devices designed for use in systems that employ TTL or DTL logic. The 55450B/75450B family is functionally interchangeable with and replaces the 75450 family and the 75450A family devices manufactured previously. The speed of the 55450B/75450B family is equal to that of the 75450 family and a test to ensure freedom from latch-up has been added. Diode-clamped inputs simplify circuit design. Typical applications include high-speed logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, line drivers, and memory drivers. Series 55450B drivers are characterized for operation over the full military temperature range of -55°C to 125°C; Series 75450B drivers are characterized for operation from 0°C to 70°C.

The 55450B and 75450B are unique general-purpose devices each featuring two standard Series 54/74 TTL gates and two uncommitted, high-current, high-voltage n-p-n transistors. These devices offer the system designer the flexibility of tailoring the circuit to the application.

The 55451B/75451B, 55452B/75452B, 55453B/75453B, and 55454B/75454B are dual peripheral AND, NAND, OR, and NOR drivers, respectively, (assuming positive logic) with the output of the logic gates internally connected to the bases of the n-p-n output transistors.

**FEATURES**

- 300mA output current capability
- High voltage outputs
- No output latch up at 20V
- High speed switching
- Circuit flexibility for varied applications
- TTL or DTL compatible diode-clamped inputs
- Standard supply voltages

**TRUTH TABLE** (55/75450B and 55/75451B)

A	B	Y
L	L	L (on state)
L	H	L (on state)
H	L	L (on state)
H	H	H (off state)

**TRUTH TABLE** (55/75452B)

A	B	Y
L	L	H (off state)
L	H	H (off state)
H	L	H (off state)
H	H	L (on state)

**TRUTH TABLE** (55/75453B)

A	B	Y
L	L	L (on state)
L	H	H (off state)
H	L	H (off state)
H	H	H (off state)

**TRUTH TABLE** (55/75454B)

A	B	Y
L	L	H (off state)
L	H	L (on state)
H	L	L (on state)
H	H	L (on state)

**PIN CONFIGURATIONS**

**F,N PACKAGE**

ORDER PART NO.  
55/775450B

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**T PACKAGE**

Pin 4 is in electrical contact with the case

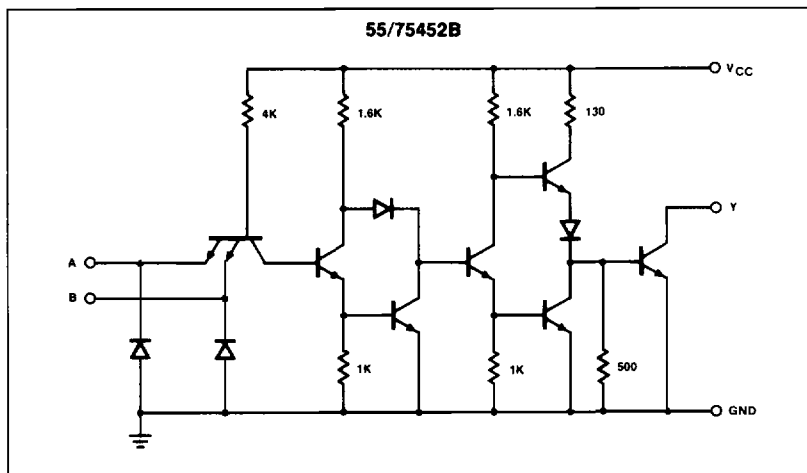
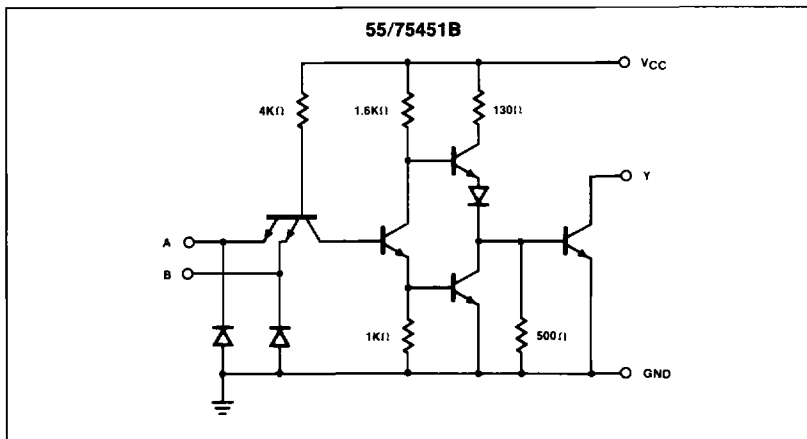
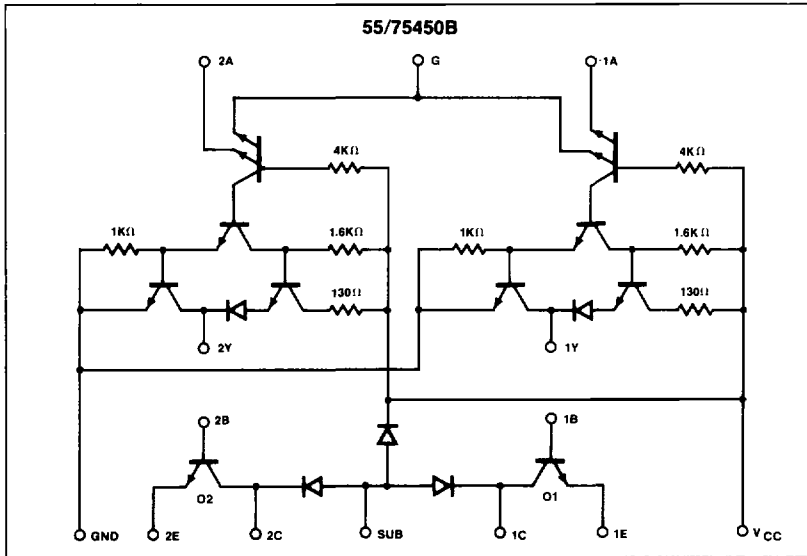
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55/75451B  
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55/75454B

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**N PACKAGE**

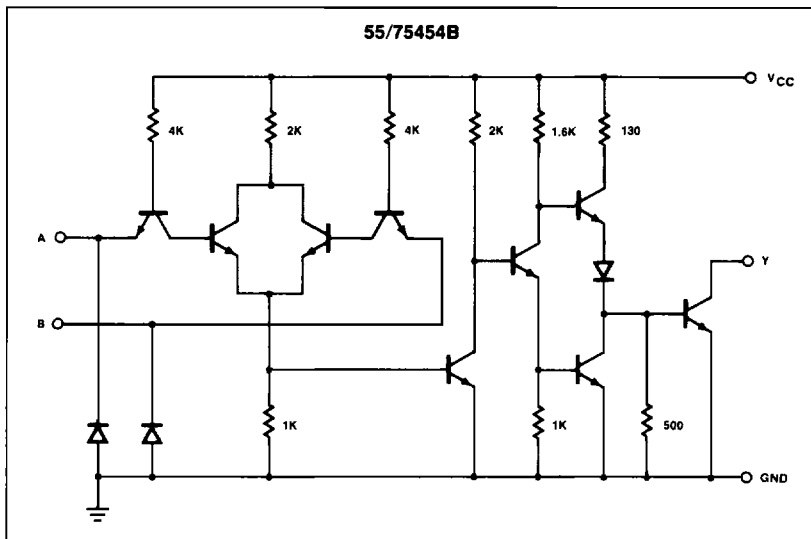
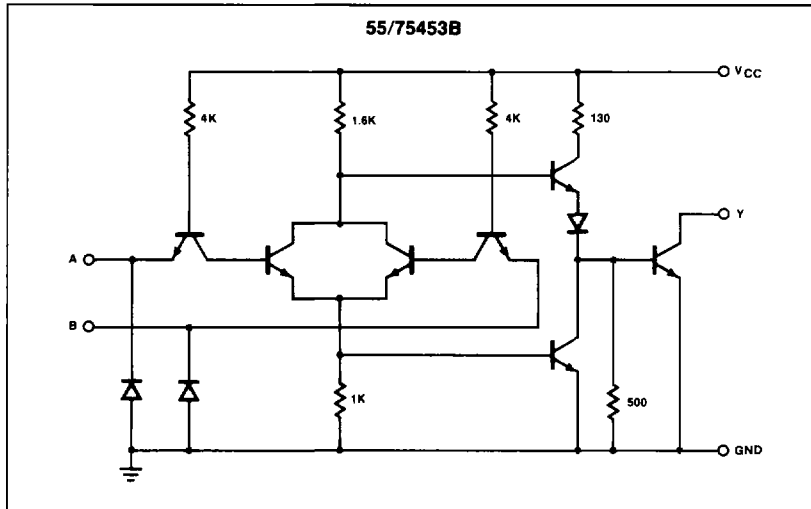
positive logic Y = AB

EQUIVALENT SCHEMATICS



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EQUIVALENT SCHEMATICS



**ABSOLUTE MAXIMUM RATINGS**  $T_A = 25^\circ\text{C}$  unless otherwise specified.

PARAMETER	55450B	75450B	55454B	75454B	UNIT
			55453B 55452B 55451B	75453B 75452B 75451B	
Supply voltage, $V_{CC}^1$	7	7	7	7	V
Input voltage	5.5	5.5	5.5	5.5	V
Interemitter voltage <sup>2</sup>	5.5	5.5	5.5	5.5	V
$V_{CC}$ -to-substrate voltage	35	35			V
Collector-to-substrate voltage	35	35			V
Collector-base voltage	35	35			V
Collector-emitter voltage <sup>3</sup>	30	30			V
Emitter-base voltage	5	5			V
Output voltage <sup>4</sup>			30	30	V
Collector current <sup>5</sup>	300	300			mA
Output current <sup>5</sup>			300	300	mA
Continuous total dissipation at (or below) $25^\circ\text{C}$ free-air temperature <sup>6</sup>	800	800	800	800	mW
Operating free-air temperature range	-55 to 125	0 to 70	-55 to 125	0 to 70	$^\circ\text{C}$
Storage temperature range	-65 to 150	-65 to 150	-65 to 150	-65 to 150	$^\circ\text{C}$
Lead temperature 1/16 inch from case for 60 seconds F or T package	300	300	300	300	$^\circ\text{C}$
Lead temperature 1/16 inch from case for 10 seconds N package	260	260	260	260	$^\circ\text{C}$

NOTES

- Voltage values are with respect to network ground terminal unless otherwise specified.
- This is the voltage between two emitters of a multiple-emitter transistor.
- This value applies when the base-emitter resistance ( $R_{BE}$ ) is equal to or less than  $500\Omega$ .
- This is the maximum voltage which should be applied to any output when it is in the off state.
- Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.
- For operation above  $25^\circ\text{C}$  free-air temperature, refer to Dissipation Derating Curve, Figure 20. This rating for the T package requires a heat sink that provides a thermal resistance from case to free-air,  $R_{\theta CA}$ , of not more than  $95^\circ\text{C/W}$ .

**DC ELECTRICAL CHARACTERISTICS**  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{V}$  unless otherwise specified.

PARAMETER	TEST CONDITIONS	55450B			75450B			UNIT
		Min	Typ	Max	Min	Typ	Max	
$V_{(BR)CBO}$ Collector-base break-down voltage	$I_C = 100\mu\text{A}$ , $I_E = 0$	35			35			V
$V_{(BR)CER}$ Collector-emitter breakdown voltage	$I_C = 100\mu\text{A}$ , $R_{BE} = 500\Omega$	30			30			V
$V_{(BR)EBO}$ Emitter-base breakdown voltage	$I_E = 100\mu\text{A}$ , $I_C = 0$	5			5			V
$h_{FE}$ Static forward current transfer ratio	$V_{CE} = 3\text{V}$ , $I_C = 100\text{mA}$	25			25			
$h_{FE}$ Static forward current transfer ratio	$V_{CE} = 3\text{V}$ , $I_C = 300\text{mA}$	30			30			
$h_{FE}$ Static forward current transfer ratio	$V_{CE} = 3\text{V}$ , $I_C = 100\text{mA}$	10						
$h_{FE}$ Static forward current transfer ratio	$V_{CE} = 3\text{V}$ , $I_C = 300\text{mA}$	15						
$h_{FE}$ Static forward current transfer ratio	$V_{CE} = 3\text{V}$ , $I_C = 100\text{mA}$				20			
$h_{FE}$ Static forward current transfer ratio	$V_{CE} = 3\text{V}$ , $I_C = 300\text{mA}$				25			
$V_{BE}$ Base-emitter voltage	$I_B = 10\text{mA}$ , $I_C = 100\text{mA}$		0.85	1.2		0.85	1	V
$V_{BE}$ Base-emitter voltage	$I_B = 30\text{mA}$ , $I_C = 300\text{mA}$		1.05	1.4		1.05	1.2	V
$V_{CE(SAT)}$ Collector-emitter saturation voltage	$I_B = 10\text{mA}$ , $I_C = 100\text{mA}$		0.25	0.5		0.25	0.4	V
$V_{CE(SAT)}$ Collector-emitter saturation voltage	$I_B = 30\text{mA}$ , $I_C = 300\text{mA}$		0.5	0.8		0.5	0.7	V



**DC ELECTRICAL CHARACTERISTICS** (Cont'd)  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{V}$  unless otherwise specified.

PARAMETER		TEST CONDITIONS	55450B			75450B			UNIT
			Min	Typ	Max	Min	Typ	Max	
$V_{IH}$	High-level input voltage		2		0.8	2		0.8	V
$V_{IL}$	Low-level input voltage								V
$V_I$	Input clamp voltage	$V_{CC} = 4.5\text{V } I_I = -12\text{mA}$			1.5				V
$V_i$	Input clamp voltage	$V_{CC} = 4.75\text{V } I_I = -12\text{mA}$						1.5	V
$V_{OH}$	High-level output voltage	$V_{CC} = 4.5\text{V } V_{IL} = 0.8\text{V}$ $I_{OH} = -400\mu\text{A}$	2.4	3.3					V
$V_{OH}$	High-level output voltage	$V_{CC} = 4.75\text{V } V_{IL} = 0.8\text{V}$ $I_{OH} = -400\mu\text{A}$				2.4	3.3		V
$V_{OL}$	Low-level output voltage	$V_{CC} = 4.5\text{V } V_{IH} = 2\text{V}$ $I_{OL} = 16\text{mA}$		0.22	0.5				V
$V_{OL}$	Low-level output voltage	$V_{CC} = 4.75\text{V } V_{IH} = 2\text{V}$ $I_{OL} = 16\text{mA}$				0.22	0.4		V
$I_I$	Input current at maximum input voltage	InputA $V_{CC} = 5.5\text{V } V_I = 5.5\text{V}$ InputG			1 2				mA
$I_i$	Input current at maximum input voltage	InputA $V_{CC} = 5.25\text{V } V_I = 5.5\text{V}$ InputG						1 2	mA
$I_H$	High level input current	InputA $V_{CC} = 5.5\text{V } V_I = 2.4\text{V}$ InputG			40 80				$\mu\text{A}$
$I_H$	High level input current	InputA $V_{CC} = 5.25\text{V } V_I = 2.4\text{V}$ InputG						40 80	$\mu\text{A}$
$I_{IL}$	Low-level input current	InputA $V_{CC} = 5.5\text{V } V_I = 0.4\text{V}$ InputG			-1.6 -3.2				mA
$I_{IL}$	Low-level input current	InputA $V_{CC} = 5.25\text{V } V_I = 0.4\text{V}$ InputG						-1.6 -3.2	mA
$I_{OS}$	Short-circuit output current <sup>2</sup>	$V_{CC} = 5.5\text{V}$	-18		-55				mA
$I_{OS}$	Short-circuit output current <sup>2</sup>	$V_{CC} = 5.25\text{V}$				-18		-55	mA
$I_{CCH}$	Supply current, outputs high	$V_{CC} = 5.5\text{V } V_I = 0$		2	4				mA
$I_{CCH}$	Supply current, outputs high	$V_{CC} = 5.25\text{V } V_I = 0$				2	4		mA
$I_{CCL}$	Supply current, outputs low	$V_{CC} = 5.5\text{V } V_I = 5\text{V}$		6	11				mA
$I_{CCL}$	Supply current, outputs low	$V_{CC} = 5.25\text{V } V_I = 5\text{V}$				6	11		mA

NOTES

1. Electrical characteristics over recommended operating free-air temperature range (unless otherwise specified).
2. Not more than one output should be shorted at a time

**DC ELECTRICAL CHARACTERISTICS** (Cont'd)  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{V}$  unless otherwise specified.

PARAMETER	TEST CONDITIONS	55451			75451			UNIT
		Min	Typ	Max	Min	Typ	Max	
$V_{IH}$ $V_{IL}$	High-level input voltage Low-level input voltage	2		0.8	2		0.8	V V
$V_i$ $V_i$	Input clamp voltage Input clamp voltage			-1.5			1.5	V V
$I_{OH}$ $I_{OH}$	High-level output current High-level output current			300			100	$\mu\text{A}$ $\mu\text{A}$
$V_{OL}$ $V_{OL}$	Low-level output voltage Low-level output voltage		0.25 0.5	0.5 0.8		0.25 0.5	0.4 0.7	V V
$I_i$ $I_i$	Input current at maximum input voltage Input current at maximum input voltage			1			1	mA mA
$I_{IH}$ $I_{IH}$	High level input current High level input current			40			40	mA $\mu\text{A}$
$I_{IL}$ $I_{IL}$	Low level input current Low-level input current		-1	-1.6		-1	-1.6	mA mA
$I_{CCH}$ $I_{CCH}$	Supply current, outputs high Supply current, outputs high		7	11		7	11	mA mA
$I_{CCL}$ $I_{CCL}$	Supply current, outputs low Supply current, outputs low		52	65		52	65	mA mA

**DC ELECTRICAL CHARACTERISTICS** (Cont'd)  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{V}$  unless otherwise specified.

PARAMETER	TEST CONDITIONS	55452			75452			UNIT
		Min	Typ	Max	Min	Typ	Max	
$V_{IH}$ $V_{IL}$	High-level input voltage Low-level input voltage	2		0.8	2		0.8	V V
$V_i$ $V_i$	Input clamp voltage Input clamp voltage			-1.5			-1.5	V V
$I_{OH}$ $I_{OH}$	High-level output current High-level output current			300			100	$\mu\text{A}$ $\mu\text{A}$
$V_{OL}$ $V_{OL}$	Low-level output voltage Low-level output voltage		0.25 0.5	0.5 0.8		0.25 0.5	0.4 0.7	V V
$I_i$ $I_i$	Input current at maximum input voltage Input current at maximum input voltage			1			1	mA mA
$I_{IH}$ $I_{IH}$	High-level input current High-level input current			40			40	$\mu\text{A}$ $\mu\text{A}$
$I_{IL}$ $I_{IL}$	Low-level input current Low-level input current		-1	-1.6		-1	-1.6	mA mA
$I_{CCH}$ $I_{CCH}$	Supply current, outputs high Supply current, outputs high		11	14		11	14	mA mA
$I_{CCL}$ $I_{CCL}$	Supply current, outputs low Supply current, outputs low		56	71		56	71	mA mA

**DC ELECTRICAL CHARACTERISTICS** (Cont'd)  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{V}$  unless otherwise specified.

PARAMETER	TEST CONDITIONS	55453			75453			UNIT
		Min	Typ	Max	Min	Typ	Max	
$V_{IH}$ $V_{IL}$	High-level input voltage Low-level input voltage	2		0.8	2		0.8	V V
$V_I$ $V_I$	Input clamp voltage Input clamp voltage			-1.5			-1.5	V V
$I_{OH}$ $I_{OH}$	High-level output current High-level output current			300			100	$\mu\text{A}$ $\mu\text{A}$
$V_{OL}$ $V_{OL}$	Low-level output voltage Low-level output voltage		0.25 0.5	0.5 0.8		0.25 0.5	0.4 0.7	V V
$I_I$ $I_I$	Input current at maximum input voltage Input current at maximum input voltage			1			1	$\text{mA}$ $\text{mA}$
$I_{IH}$ $I_{IH}$	High-level input current High-level input current			40			40	$\mu\text{A}$ $\mu\text{A}$
$I_{IL}$ $I_{IL}$	Low-level input current Low-level input current		-1	-1.6		-1	-1.6	$\text{mA}$ $\text{mA}$
$I_{CCH}$ $I_{CCH}$	Supply current, outputs high Supply current, outputs high		8	11		8	11	$\text{mA}$ $\text{mA}$
$I_{CCL}$ $I_{CCL}$	Supply current, outputs low Supply current, outputs low		54	68		54	68	$\text{mA}$ $\text{mA}$

**DC ELECTRICAL CHARACTERISTICS** (Cont'd)  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{V}$  unless otherwise specified.

PARAMETER	TEST CONDITIONS	55454			75454			UNIT
		Min	Typ	Max	Min	Typ	Max	
$V_{IH}$ $V_{IL}$	High-level input voltage Low-level input voltage	2		0.8	2		0.8	V V
$V_I$ $V_I$	Input clamp voltage Input clamp voltage			-1.5			-1.5	V V
$I_{OH}$ $I_{OH}$	High-level output current High-level output current			300			100	$\mu\text{A}$ $\mu\text{A}$
$V_{OL}$ $V_{OL}$	Low-level output voltage Low-level output voltage		0.25 0.5	0.5 0.8		0.25 0.5	0.4 0.7	V V V
$I_I$ $I_I$	Input current at maximum input voltage Input current at maximum input voltage			1			1	$\text{mA}$ $\text{mA}$
$I_{IH}$ $I_{IH}$	High-level input current High-level input current			40			40	$\mu\text{A}$ $\mu\text{A}$
$I_{IL}$ $I_{IL}$	Low-level input current Low-level input current		-1	-1.6		-1	-1.6	$\text{mA}$ $\text{mA}$
$I_{CCH}$ $I_{CCH}$	Supply current, outputs high Supply current, outputs high		13	17		13	17	$\text{mA}$ $\text{mA}$
$I_{CCL}$ $I_{CCL}$	Supply current, outputs low Supply current, outputs low		61	79		61	79	$\text{mA}$ $\text{mA}$

**AC ELECTRICAL CHARACTERISTICS**  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{V}$  unless otherwise specified.

PARAMETER	TEST CONDITIONS	55/75450B			UNIT
		Min	Typ	Max	
<b>TTL GATES</b>					
$t_{PLH}$ Propagation delay time, low-to-high output	$C_L = 15\text{pF}$ , $R_L = 400\Omega$		12	22	ns
$t_{PHL}$ Propagation delay time, high-to-low level output			8	15	ns
<b>OUTPUT TRANSISTORS</b>					
$t_d$ Delay time	$I_C = 200\text{mA}$ , $I_{B(1)} = 20\text{mA}$ , $I_{B(2)} = -40\text{mA}$ , $V_{BE(OFF)} = -1\text{V}$ , $C_L = 15\text{pF}$ , $R_L = 50\Omega$		8	15	ns
$t_r$ Rise time			12	20	ns
$t_s$ Storage time			7	15	ns
$t_f$ Full time			6	15	ns
<b>GATES AND TRANSISTORS COMBINED</b>					
$t_{PLH}$ Propagation delay time, low-to-high level output	$I_C \approx 200\text{mA}$ , $C_L = 15\text{pF}$ , $R_L = 50\Omega$		20	30	ns
$t_{PHL}$ Propagation delay time, high-to-low level output			20	30	ns
$t_{TLH}$ Transition time, low-to-high level output			7	12	ns
$t_{THL}$ Transition time, high-to-low level output			9	15	ns
$V_{OH}$ High-level output voltage after switching	$V_S = 20\text{V}$ , $I_C \approx 300\text{mA}$ , $R_{BE} = 500\Omega$	$V_S - 6.5$			mV

**AC ELECTRICAL CHARACTERISTICS**  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{V}$  unless otherwise specified.

PARAMETER	TEST CONDITIONS	55451/75451			55452/75452			UNIT
		Min	Typ	Max	Min	Typ	Max	
$t_{PLH}$ Propagation delay time, low-to-high level output	$I_O \approx 200\text{mA}$ , $C_L = 15\text{pF}$ , $R_L = 50\Omega$		18	25		26	35	ns
$t_{PHL}$ Propagation delay time, high-to-low level output	$I_O \approx 200\text{mA}$ , $C_L = 15\text{pF}$ , $R_L = 50\Omega$		18	25		24	35	ns
$t_{TLH}$ Transition time, low-to-high level output	$I_O \approx 200\text{mA}$ , $C_L = 15\text{pF}$ , $R_L = 50\Omega$		5	8		5	8	ns
$t_{THL}$ Transition time, High-to-low level output	$I_O \approx 200\text{mA}$ , $C_L = 15\text{pF}$ , $R_L = 50\Omega$		7	12		7	12	ns
$V_{OH}$ High-level output voltage after switching	$V_S = 20\text{V}$ , $I_O \approx 300\text{mA}$	$V_S - 6.5$			$V_S - 6.5$			mV

NOTE

Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

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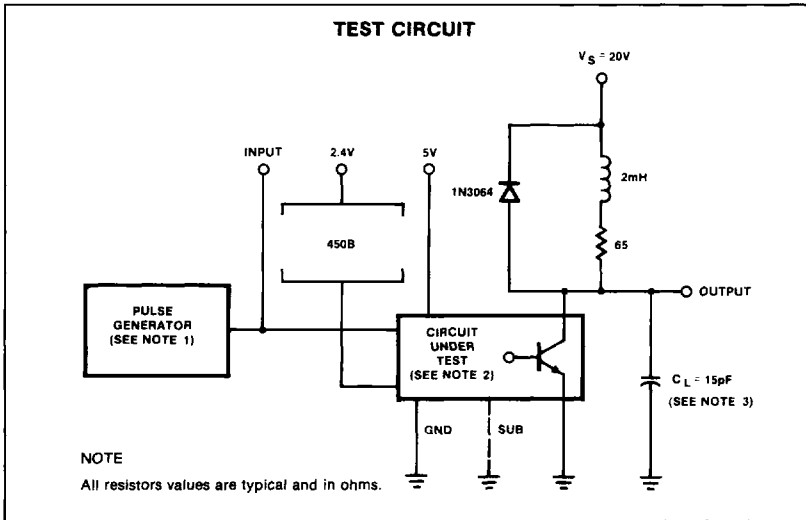


**AC ELECTRICAL CHARACTERISTICS** (Cont'd)  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{V}$  unless otherwise specified.

PARAMETER	TEST CONDITIONS	55453/75453			55454/75454			UNIT
		Min	Typ	Max	Min	Typ	Max	
$t_{PLH}$ Propagation delay time, low-to-high level output	$I_O \approx 200\text{mA}$ , $C_L = 15\text{pF}$ , $R_L = 50\Omega$		18	25		27	35	ns
$t_{PHL}$ Propagation delay time, high-to-low level output	$I_O \approx 200\text{mA}$ , $C_L = 15\text{pF}$ , $R_L = 50\Omega$		16	25		24	35	ns
$\tau_{LH}$ Transition time, low-to-high level output	$I_O \approx 200\text{mA}$ , $C_L = 15\text{pF}$ , $R_L = 50\Omega$		5	8		5	8	ns
$\tau_{HL}$ Transition time, High-to-low level output	$I_O \approx 200\text{mA}$ , $C_L = 15\text{pF}$ , $R_L = 50\Omega$		7	12		7	12	ns
$V_{OH}$ High-level output voltage after switching	$V_S = 20\text{V}$ , $I_O \approx 300\text{mA}$	$V_S - 6.5$			$V_S - 6.5$			mV

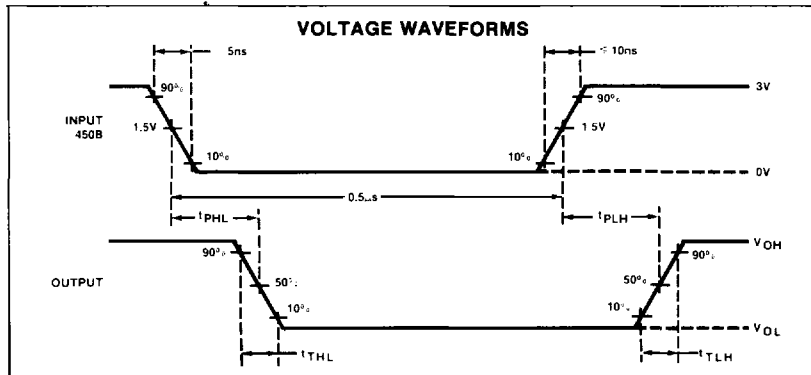
NOTE  
Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

**LATCH-UP TEST OF COMPLETE DRIVERS**



- NOTES
1. The pulse generator has the following characteristics:  $\text{PRR} = 12.5\text{kHz}$ ,  $Z_{OUT} = 50\Omega$ .
  2. When testing 55450B or 75450B, connect output Y to transistor base with a 500- $\Omega$  resistor from there to ground, and ground to substrate terminal.
  3.  $C_L$  includes probe and jig capacitance.

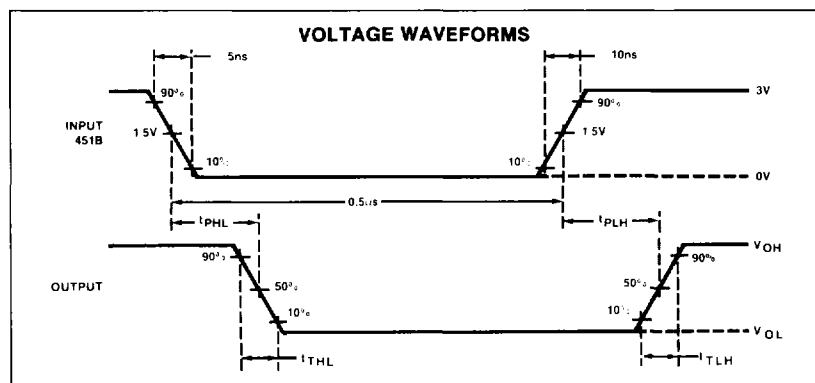
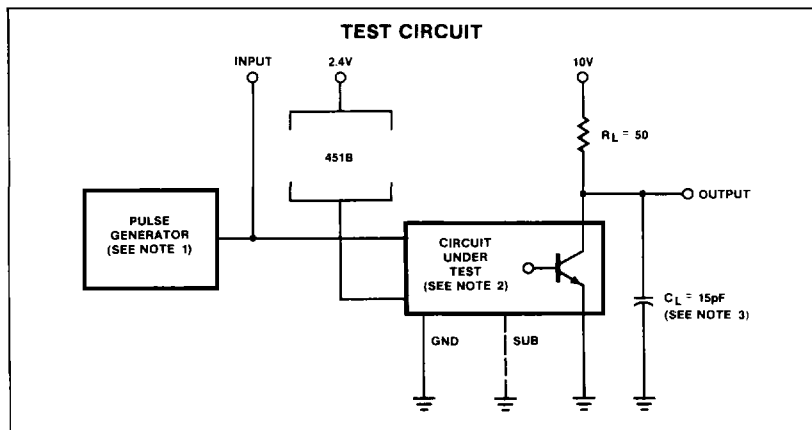
LATCH-UP TEST OF COMPLETE DRIVERS (Cont'd)



NOTES

1. The pulse generator has the following characteristics: PRR = 12 kHz,  $Z_{OUT} = 50\Omega$ .
2. When testing 55450B or 75450B, connect output Y to transistor base with a 500- $\Omega$  resistor from there to ground, and ground to substrate terminal.
3.  $C_L$  includes probe and jig capacitance.

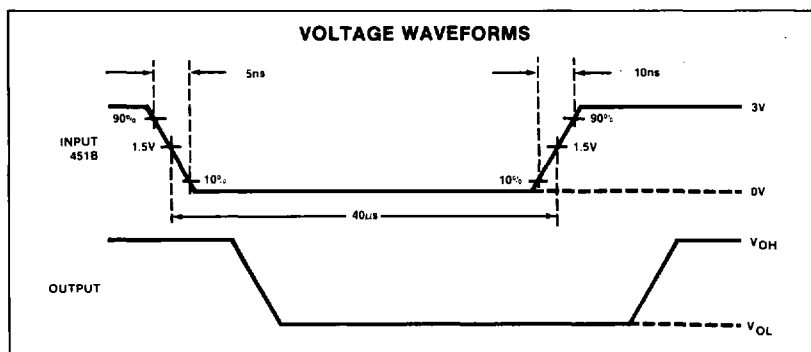
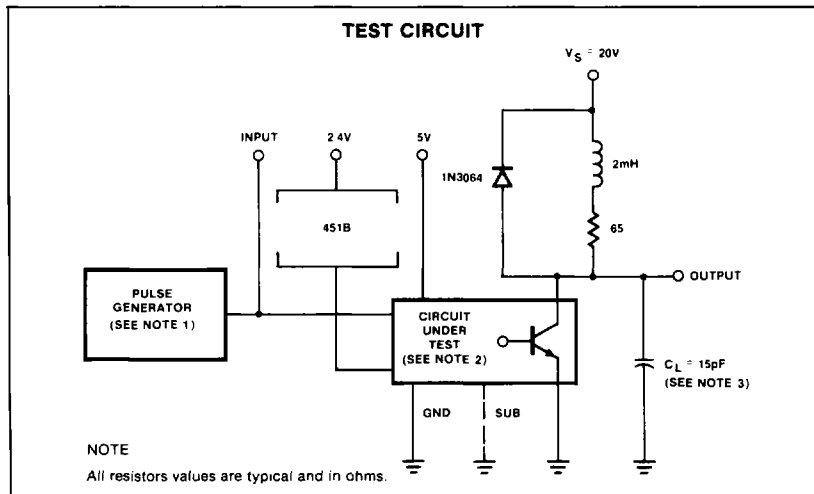
SWITCHING TIMES OF COMPLETE DRIVERS



NOTES

1. The pulse generator has the following characteristics: PRR = 1MHz,  $Z_{OUT} \approx 50\Omega$ .
2. When testing 55451B or 75451B, connect output Y to transistor base and ground the substrate terminal.
3.  $C_L$  includes probe and jig capacitance.

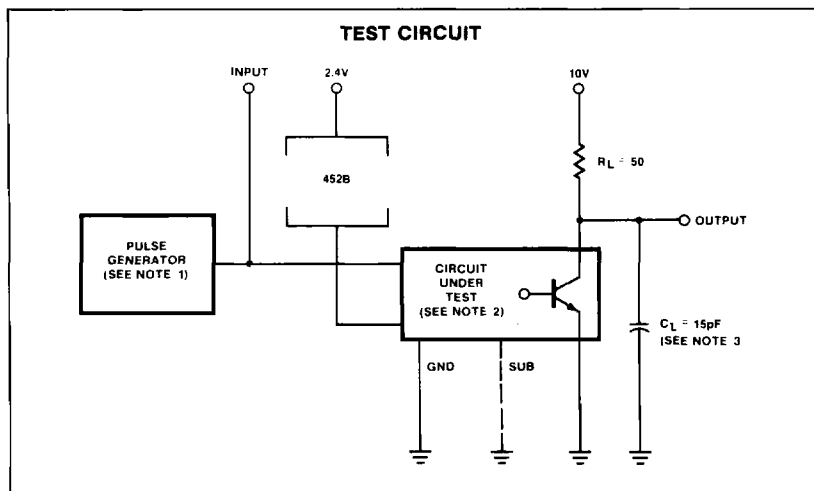
**LATCH-UP TEST OF COMPLETE DRIVERS**



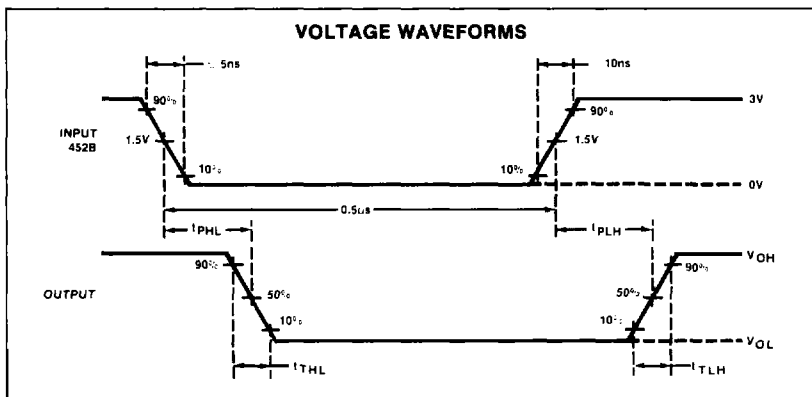
**NOTES**

1. The pulse generator has the following characteristics: PRR = 12.5kHz,  $Z_{out} = 50\Omega$ .
2. When testing 55451B or 75451B, connect output Y to transistor base with a 500- $\Omega$  resistor from there to ground, and ground the substrate terminal.
3.  $C_L$  includes probe and jig capacitance.

**SWITCHING TIMES OF COMPLETE DRIVERS**



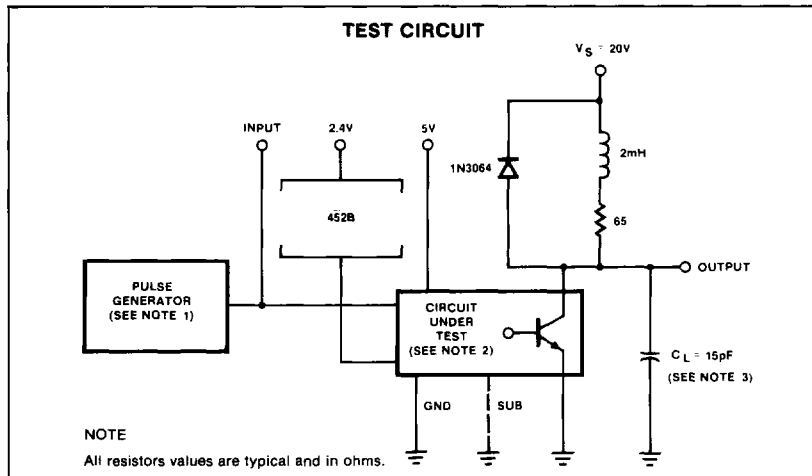
**SWITCHING TIMES OF COMPLETE DRIVERS (Cont'd)**



**NOTES**

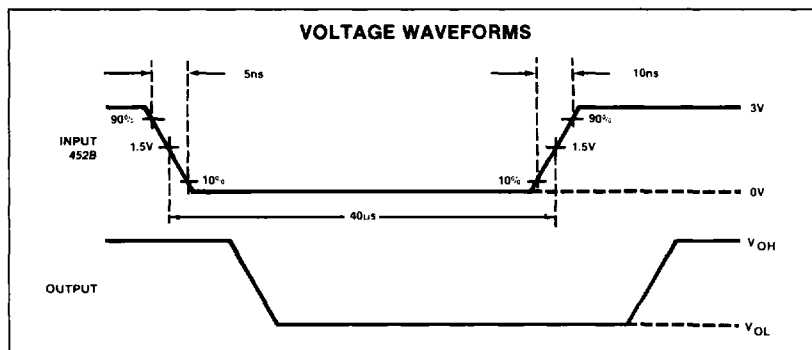
1. The pulse generator has the following characteristics: PRR = 1MHz,  $Z_{OUT} \approx 50\Omega$ .
2. When testing 55452B or 75452B, connect output Y to transistor base and ground the substrate terminal.
3.  $C_L$  includes probe and jig capacitance.

**LATCH-UP TEST OF COMPLETE DRIVERS**



**NOTE**

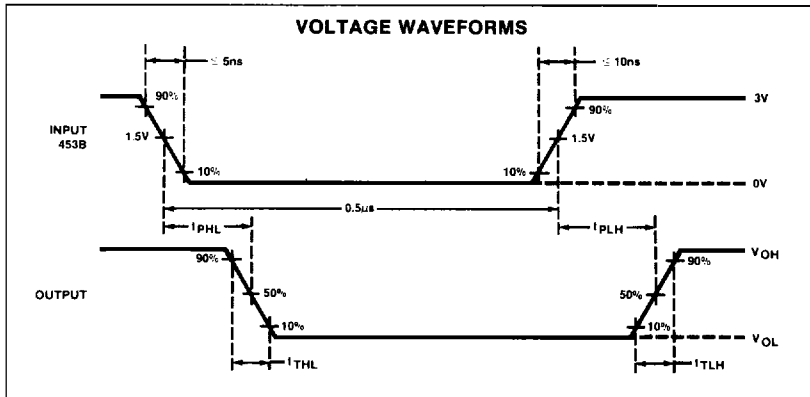
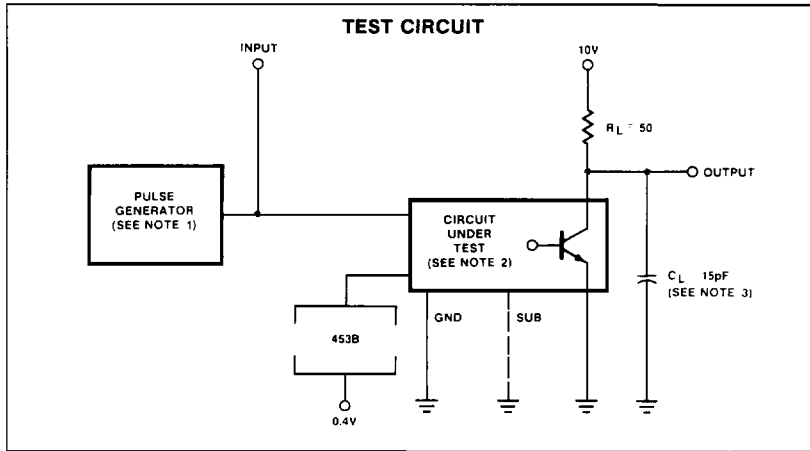
All resistors values are typical and in ohms.



**NOTES**

1. The pulse generator has the following characteristics: PRR = 12.5kHz,  $Z_{OUT} = 50\Omega$ .
2. When testing 55452B or 75452B, connect output Y to transistor base with a 500- $\Omega$  resistor from there to ground, and ground the substrate terminal.
3.  $C_L$  includes probe and jig capacitance.

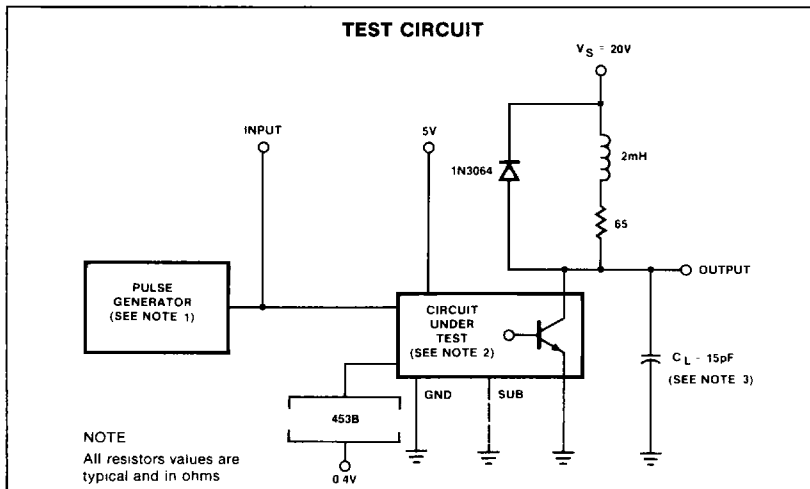
**SWITCHING TIMES OF COMPLETE DRIVERS**



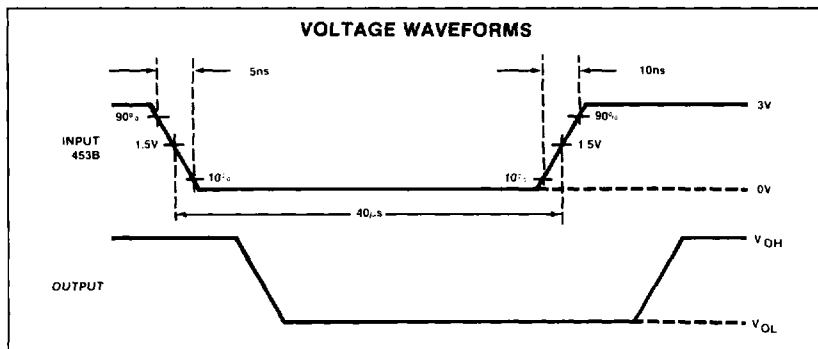
**NOTES**

1. The pulse generator has the following characteristics: PRR = 1MHz,  $Z_{out} \approx 50\Omega$ .
2. When testing 55453B or 75453B, connect output Y to transistor base and ground the substrate terminal.
3.  $C_L$  includes probe and jig capacitance

**LATCH-UP TEST OF COMPLETE DRIVERS**



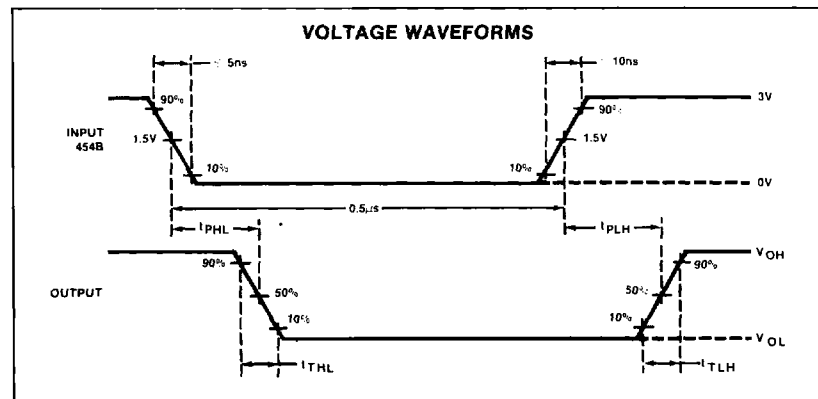
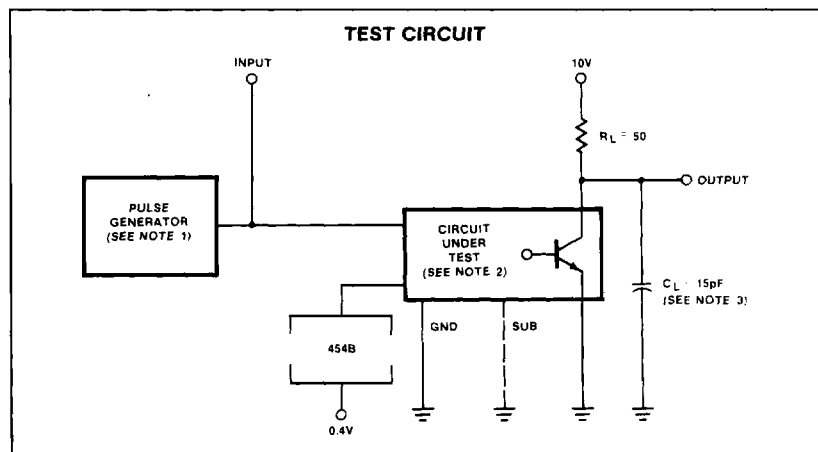
LATCH-UP TEST OF COMPLETE DRIVERS (Cont'd)



NOTES

1. The pulse generator has the following characteristics: PRR = 12.5kHz,  $Z_{OUT} = 50\Omega$
2. When testing 55453B or 75453B, connect output Y to transistor base with a 500- $\Omega$  resistor from there to ground, and ground the substrate terminal.
3.  $C_L$  includes probe and jig capacitance.

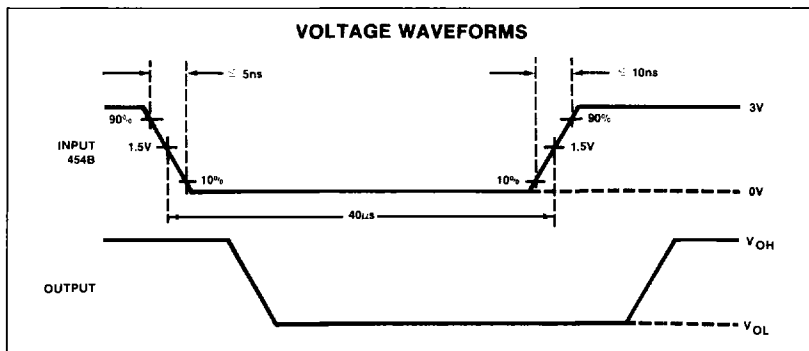
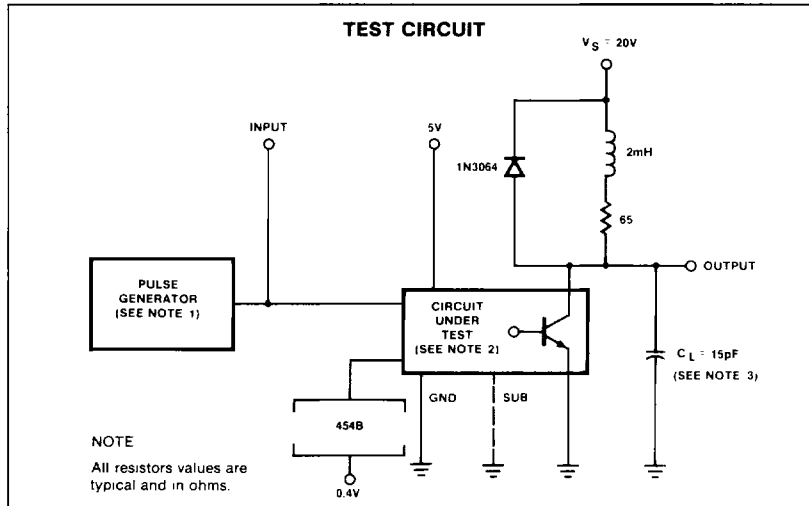
SWITCHING TIMES OF COMPLETE DRIVERS



NOTES

1. The pulse generator has the following characteristics. PRR = 1MHz,  $Z_{OUT} = 50\Omega$ .
2. When testing 55454B or 75454B, connect output Y to transistor base and ground the substrate terminal.
3.  $C_L$  includes probe and jig capacitance

LATCH-UP TEST OF COMPLETE DRIVERS

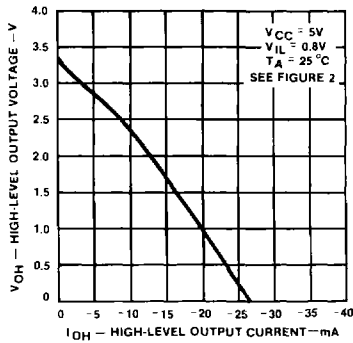


NOTES

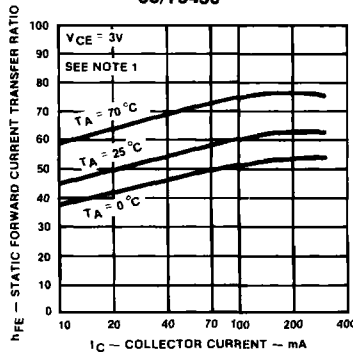
1. The pulse generator has the following characteristics: PRR = 12.5kHz,  $Z_{OUT} = 50\Omega$
2. When testing 55454B or 75454B, connect output Y to transistor base with a 500- $\Omega$  resistor from there to ground, and ground the substrate terminal.
3.  $C_L$  includes probe and jig capacitance.

TYPICAL PERFORMANCE CHARACTERISTICS

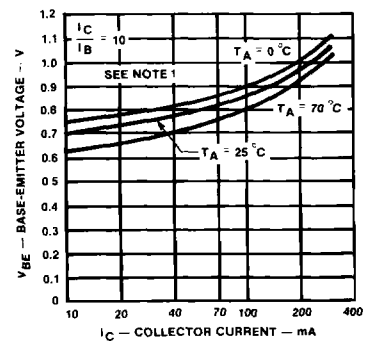
TTL GATE HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT  
55/75450



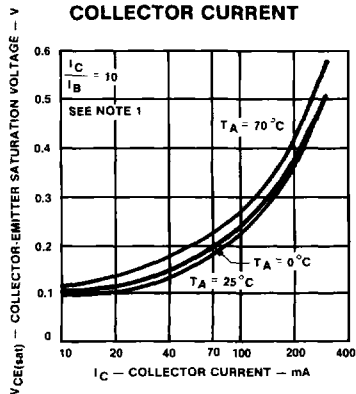
TRANSISTOR STATIC FORWARD CURRENT TRANSFER RATIO vs COLLECTOR CURRENT  
55/75450



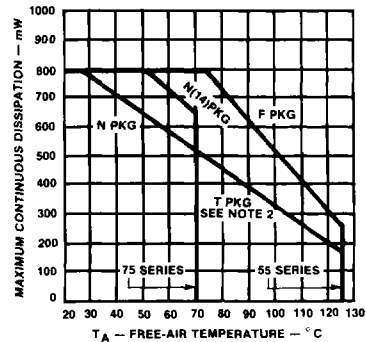
TRANSISTOR BASE-EMITTER VOLTAGE vs COLLECTOR CURRENT  
55/75450



TRANSISTOR COLLECTOR-EMITTER SATURATION VOLTAGE vs COLLECTOR CURRENT



DISSIPATION DERATING CURVE



NOTE

1. These parameters must be measured using pulse techniques.  $t_w = 300\mu s$ , duty cycle  $\leq 2\%$ .
2. This rating for the T Package requires a heat sink that provides a thermal resistance from case to free-air,  $R_{\theta CA}$ , of not more than  $95^\circ C/W$ .