SOT-3 Device
STM-1/STS-3/STS-3c Overhead Terminator
TXC-03003

DATA SHEET
Preliminary

FEATURES

- Full overhead processing, compliant with ANSI and ITU-T standards
- Transmit and receive pointer generation with respect to external clock and frame signals
- Byte-parallel data, clock and frame on the line side
- Byte-parallel data, clock, C1J1, SPE, parity bit (odd) and path overhead indication on the terminal side
- SDH/SONET alarm detection
- Serial link from SOT-3 provides vital alarm signals for path-protected ring applications
- Downstream AIS sent using the E1 byte
- Performance monitoring: B1, B2 and B3 coding violations, FEBE and pointer justification counts
- Separate address and data busses for the microprocessor I/O (pin-selectable as either Intel or Motorola compatible)
- Receive and transmit overhead bytes available via on-chip RAM and a serial I/O port

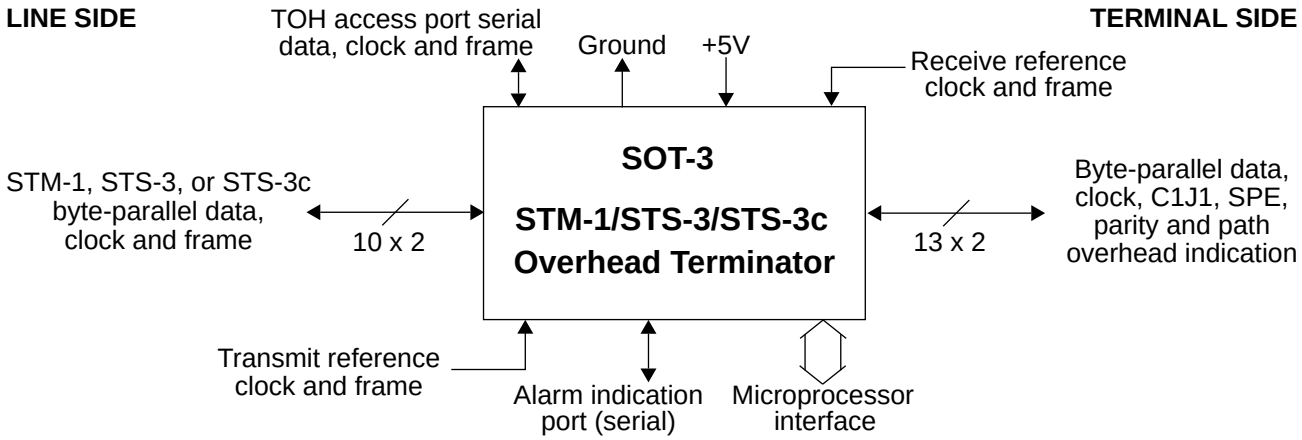
DESCRIPTION

This SOT-3 SDH/SONET overhead terminator is a highly versatile, programmable device which performs section, line and path overhead processing for STM-1/STS-3/STS-3c signals. The SOT-3 device performs pointer generation (with internal pointer justification) with respect to external clock timing in both the transmit and receive directions. It automatically adjusts pointers to account for differences between the input clock and frame, and the reference clock and frame. All overhead bytes are provided in the SOT-3 memory map with access via the microprocessor port or serial I/O port.

The SOT-3 device sends downstream AIS information via the E1 byte in order to meet system timing requirements. It also provides a serial alarm indication port for use in path-protected ring architectures. In the transmit direction, overhead bytes may be multiplexed into the signal from either the memory map or from the external serial interface.

APPLICATIONS

- Supports Telecom Bus and dual ring mode applications
- Add/drop multiplexer
- Digital cross-connect
- High speed data communication
- Supports ATM mapping into SONET/SDH



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TranSwitch Corporation • 8 Progress Drive • Shelton, CT 06484 • USA • Tel: 203-929-8810 • Fax: 203-926-9453

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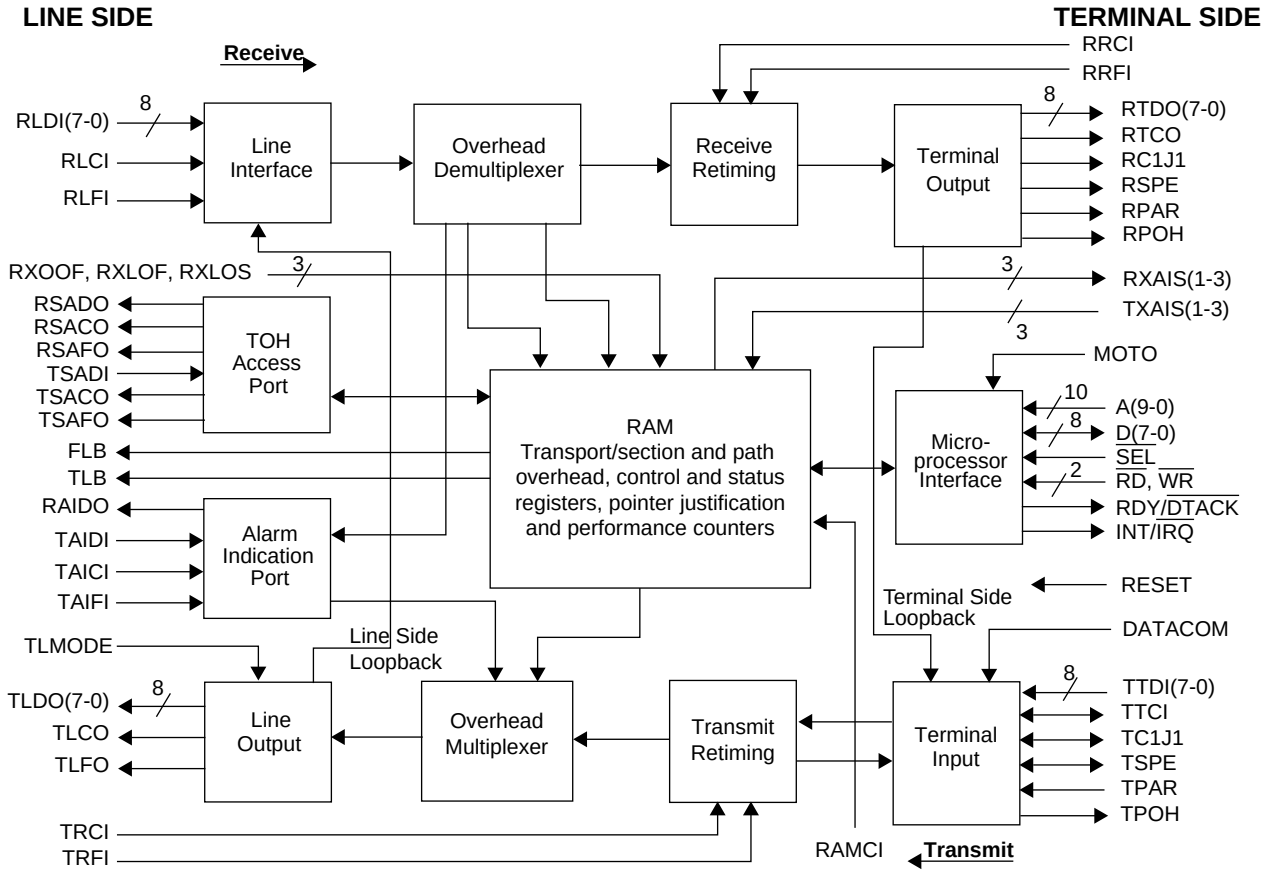


Figure 1. Block Diagram

BLOCK DIAGRAM DESCRIPTION

A simplified block diagram of the SOT-3 device is shown in Figure 1.

On the receive line side, the Line Interface block terminates the STM-1/STS-3/STS-3c input signals, which are derived from an external line interface device, such as the TranSwitch SYN155, TXC-02301B. The external line interface device performs the functions of descrambling/scrambling, B1 checking/generating, and serial/parallel conversion in the receive and transmit directions. The receive line side interface signals consist of byte-parallel data (RLDI), a 19.48 MHz clock input signal (RLCI) and a framing signal (RLFI). External alarm inputs from the line interface device consist of an out of frame alarm (RXOOF), loss of frame alarm (RXLOF) and loss of signal alarm (RXLOS).

The Overhead Demultiplexer block writes the 81 STM-1 section overhead or STS-3/STS-3c transport overhead bytes, and the 9/27 path overhead bytes (after pointer tracking), to RAM locations from which stable values may be read by the microprocessor. The Overhead Demultiplexer block also monitors the incoming signal and detects line AIS, loss of pointer, path AIS, loss of multiframe, yellow alarm (path Remote Defect Indication, RDI) for the STM-1/STS-3c signal and individual STS-1s in the STS-3 signal, and the B2 and B3 parity errors and pointer movements for counting. Hardware interrupt capability is provided, with a software interrupt pointer and alarm indications placed in RAM locations for the microprocessor to read.

The Receive Retiming block provides pointer justification for the STM-1 AU-4 or STS-3/STS-3c SPE, using an external timebase. The payload is justified to an external timebase consisting of a framing pulse (RRFI) and

clock reference (RRCI). For normal operation, the STM-1/STS-3c signal AU-4 (SPE) consists of 2349 bytes (path overhead plus payload), and for an STS-3 signal, three 783-byte SPEs (three STS-1s).

The Terminal Output block provides an interface for byte-parallel data (RTDO), a 19.44 MHz clock output (RTCO), a composite signal that identifies the location of the first C1 byte and the J1 byte(s) (RC1J1), a payload active signal (RSPE), an odd parity bit (RPAR), and a path overhead indication (RPOH). The data bytes provided at the terminal interface consist of the A1 and A2 framing pattern, the H1, H2, and H3 pointer bytes, the three E1 orderwire bytes (used to convey an AIS indication downstream), and 8 STM-1/STS-3c or 24 STS-3 (plus H4 during VTAIS/TUAIS) POH bytes plus payload bytes. For all other overhead bytes, the data byte contents are set equal to zero.

On the transmit terminal side, the Terminal Input block provides the interface for normal operation, consisting of a byte-parallel data input (TTDI), clock input (TTCI), a composite input signal that identifies the location of the first C1 byte and the J1 byte(s) (TC1J1), a payload input signal (TSPE), and an odd parity bit (TPAR). For the data communication mode, the clock signal, the C1J1 signal, and the payload signal become outputs and a path overhead indication output (TPOH) is also provided. The output signals establish a timebase for sourcing data packets into the payload. For either normal or data communication operation, the data bytes that must be at the interface are the 2322 STM-1 TUG-3 or STS-3c SPE, or 2340 STS-3 SPE bytes. The path overhead may accompany the payload, or may be multiplexed into the transmit signal from the RAM. The extraction of AIS indications from the E1 bytes is optional.

The Transmit Retiming block performs a pointer calculation for the transmit signal with respect to the external clock reference (TRCI), and framing pulse (TRFI). The payload consists of 261 bytes per subframe for STM-1/STS-3c operation, or three payloads of 87 bytes per subframe each for STS-3 operation.

Section overhead bytes for the STM-1 signal and transport bytes for the STS-3/STS-3c signal are multiplexed with the retimed payload by the Overhead Multiplexer block. All transport overhead bytes are inserted from the RAM. Control bits are provided in RAM to select whether the RAM locations are written by the microprocessor interface or by the Transport Overhead Serial Access Port (TOH Access Port block). These control bits select the K1 and K2 bytes, orderwire and datacom channels, the F1 and Z bytes, unused bytes, and other bytes (A1, A2, C1, H1, and H2 bytes).

The Line Output block provides the source for the transmit line STM-1/STS-3/STS-3c signal. The interface consists of a byte-parallel data output signal (TLDO), a clock signal (TLCO), and a framing pulse (TLFO). The output frame phase and clock signals are derived from the external reference clock signal (TRCI) and framing pulse (TRFI).

The Transport Overhead Serial Access Port (TOH Access Port block) provides a bit-serial interface to the 81 section (transport) overhead bytes in the STM-1/STS-3/STS-3c signal. Its receive side interface consists of serial output data (RSADO), clock output (RSACO), and a framing pulse (RSAFO); it provides real-time access to all received transport overhead bytes. The clock and framing pulse are also used for the receive Alarm Indication Port. The transmit side interface of the TOH Access Port consists of bit serial input data (TSADI) that carries the states of the 81 overhead bytes in an STM-1/STS-3/STS-3c signal, clock output (TSACO), and framing pulse (TSAFO). Control bits are provided for selecting whether the RAM locations are written by the microprocessor or by the TOH Access Port.

The SOT-3 device also supports the ring architecture. The Alarm Indication Port (AIP) provides a way of notifying a paired SOT-3 device of the status of alarms for an STM-1/STS-3c signal, or for individual STS-1s in the STS-3 signal. The AIP interface consists of a serial data output (RAIDO), clock output (RSACO), and framing pulse (RSAFO). The transmit interface consists of a bit serial transmit data input (TAIDI), clock signal (TAICI), and framing pulse (TAIFI).

The SOT-3 device supports either an Intel or Motorola formatted microprocessor bus interface. The Microprocessor Interface block interface consists of separate 10-bit address leads and 8-bit data leads, together with other microprocessor control leads, including Ready or Data Transfer Acknowledge (RDY/$\overline{\text{DTACK}}$). In addition, software and hardware interrupt capability is provided.

PIN DIAGRAM

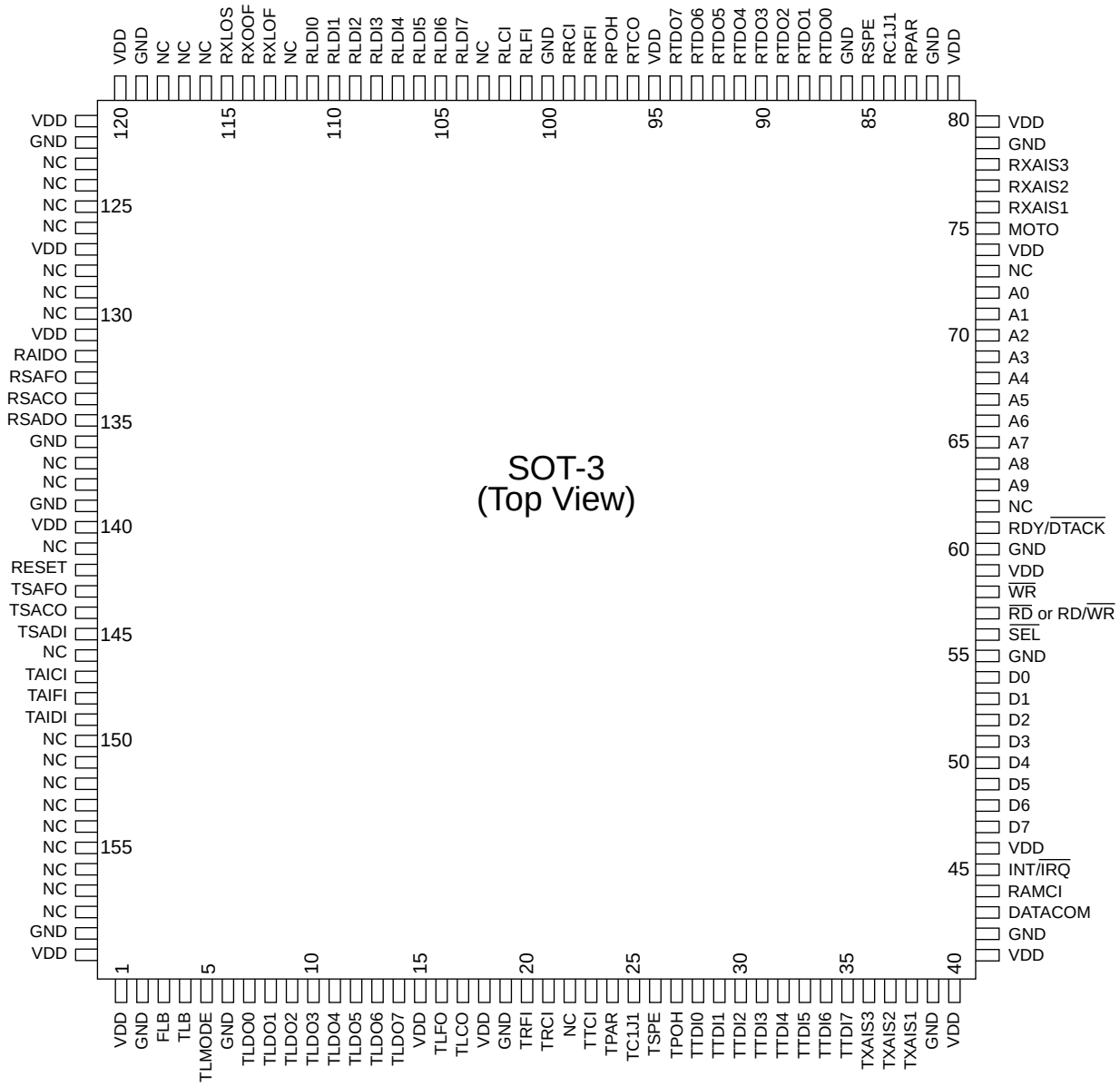


Figure 2. Pin Diagram

PIN DESCRIPTIONS

Power Supply, Ground and No Connect

Symbol	Pin No.	I/O/P*	Type	Name/Function
VDD	1,15,18,40,41, 46,59,74,80, 81,95,120,121, 127,131,140,160	P		**VDD:** + 5-volt supply voltage, +/- 5%
GND	2,6,19,39,42, 55,60,79,82, 86,100,119, 122,136,139,159	P		**Ground.**
NC	22,62,73,103, 112,116-118, 123-126, 128-130, 137, 138,141, 146, 150-158			**No Connect:** NC pins are not to be connected, not even to another NC pin, but must be left floating. Connection of these pins may impair performance or cause damage to the device. (NC pins may have internal connections within the device. They may be assigned functions in future versions of the device such that connection would prevent backwards compatibility.)

*Note: I = Input; O = Output; P = Power

Microprocessor Bus Interface

Symbol	Pin No.	I/O/P	Type *	Name/Function
RAMCI	44	I	CMOS	**RAM Clock Input:** Clock input for the internal RAM. This clock must be synchronous with TRCI (pin 21).
INT/$\overline{\text{IRQ}}$	45	O	TTL4mA	**Interrupt:** Intel mode: A high on this output pin signals an interrupt request to the microprocessor. Motorola mode: A low on this output pin signals an interrupt request to the microprocessor.
D(7-0)	47-54	I/O	TTL8mA	**Data Bus:** These bidirectional data lines are used for transferring data between the SOT-3 RAM and microprocessor. D7 is defined as the most significant bit.
$\overline{\text{SEL}}$	56	I	TTLp	**Select:** A low enables data transfers between the microprocessor and SOT-3 RAM during a read/write bus cycle.
$\overline{\text{RD}}$ or RD/$\overline{\text{WR}}$	57	I	TTL	**Read or Read/Write:** Intel mode: An active low signal generated by the microprocessor for reading the SOT-3 RAM. Motorola mode: An active high signal generated by the microprocessor for reading the SOT-3 RAM. A low is used to write to SOT-3 RAM locations.

* See Input, Output and I/O Parameters section below for Type Definitions.

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{WR}$	58	I	TTL	**Write:** Intel mode: An active low signal generated by the microprocessor for writing to SOT-3 RAM. Motorola mode: Not used, left floating.
MOTO	75	I	TTL	**Motorola/Intel Processor Select:** A high selects a Motorola microprocessor compatible bus interface. A low selects an Intel microprocessor compatible bus interface.
RDY/ $\overline{DTACK}$	61	O (tristate)	OD8mA/ TTL8mA	**Ready or Data Transfer Acknowledge:** Intel mode: A high is an acknowledgment from the addressed RAM location that the transfer can be completed. A low indicates the SOT-3 cannot complete the transfer cycle, and that microprocessor wait states must be generated. Motorola mode: During a read bus cycle, a low signal indicates the information on the data bus is valid. During a write bus cycle, a low signal acknowledges the acceptance of data.
A(9-0)	63-72	I	TTL	**Address Bus:** These active high address line inputs are used by the microprocessor to select a SOT-3 RAM location for a read/write data transfer when the Select lead is low. A9 is defined as the most significant bit.

Receive Line Side Interface

Symbol	Pin No.	I/O/P	Type	Name/Function
RLFI	101	I	CMOS	**Receive Line Frame In:** An active high framing pulse that occurs at the time of the third A2 byte of the STM-1/STS-3/STS-3c received data signal on RLDI.
RLCI	102	I	CMOS	**Receive Line Clock In:** This input clock has a nominal frequency of 19.44 MHz. Data (RLDI) and the framing signal (RLFI) are clocked in on the rising edges of this clock.
RLDI(7-0)	104-111	I	CMOS	**Receive Line Data In:** STM-1/STS-3/STS-3c byte-parallel data. RLDI7 is defined as the most significant bit.
RXLOF	113	I	TTL	**Receive Loss Of Frame In:** An external active high signal received from the SYN155 device or other line interface circuit that indicates a loss of frame alarm. The status of this alarm is provided in the SOT-3 RAM.
RXOOF	114	I	TTL	**Receive Out Of Frame In:** An external active high signal received from the SYN155 device or other line interface circuit that indicates an out of frame alarm. The status of this alarm is reported in the SOT-3 RAM.

Symbol	Pin No.	I/O/P	Type	Name/Function
RXLOS	115	I	TTL	**Receive Loss Of Signal In:** An external active high signal received from the SYN155 device or other line interface circuit that indicates a loss of signal. This signal is “OR”ed with the output of the internal SOT-3 Receive Loss Of Signal detector for an alarm indication (see bit 6 (RLOS) in status register locations 3D0H, 3D1H).

Transmit Reference Timing

Symbol	Pin No.	I/O/P	Type	Name/Function
TRFI	20	I	CMOS	**Transmit Reference Frame In:** A reference framing pulse input that the SOT-3 uses to synchronize the output frame timing. This is an optional signal which, when used, would normally occur every 125 microseconds. When not used, it must be disabled by use of TLMODE (pin 5) as follows: When TLMODE = 0, set TRFI = 1. When TLMODE = 1, set TRFI = 0.
TRCI	21	I	CMOS	**Transmit Reference Clock In:** Reference clock input that has a nominal frequency of 19.44 MHz. Used for transmit retiming and for sourcing the transmit data (TLDO) and clock out (TLCO) signals. This signal can be inverted by using the TLMODE input (pin 5).

Transmit Line Side Interface

Symbol	Pin No.	I/O/P	Type	Name/Function
TLDO(7-0)	14-7	O	CMOS2mA	**Transmit Line Data Out:** STM-1/STS-3/STS-3c byte-parallel data. Data is clocked out on the falling edge of the transmit line clock out (TLCO) if TLMODE = 1. Otherwise, it is clocked out on the rising edge. TLDO7 is defined as the most significant bit.
TLFO	16	O	CMOS2mA	**Transmit Line Frame Out:** A positive framing pulse that occurs during the third A2 byte time of the transmitted data (TLDO). This signal can be inverted by using the TLMODE input (pin 5).
TLCO	17	O	CMOS2mA	**Transmit Line Clock Out:** Output clock, derived from TRCI, that is used for clocking out the byte-parallel TLDO data after retiming.This signal can be inverted by using the TLMODE input (pin 5).

Receive Reference Timing

Symbol	Pin No.	I/O/P	Type	Name/Function
RRFI	98	I	CMOS	**Receive Reference Frame In:** An active high framing pulse reference that occurs every 125 microseconds. It can be used by the SOT-3 device to locate the outgoing terminal side framing. If it is not used, it must be grounded.
RRCI	99	I	CMOS	**Receive Reference Clock In:** An input clock that has a nominal frequency of 19.44 MHz. Used for receive retiming, and for sourcing the receive terminal side output signals.

Terminal Side Receive Interface

Symbol	Pin No.	I/O/P	Type	Name/Function
RPAR	83	O	CMOS2mA	**Receive Terminal Parity:** Odd parity status bit that is calculated over the receive terminal side data RTDO(7-0), RSPE, and RC1J1 signals.
RC1J1	84	O	CMOS2mA	**Receive C1J1 Indication:** A composite synchronization signal which contains active high pulses in the location of the first C1 byte in the transport overhead and in the location(s) of the J1 byte(s) within the payload. The receive SPE indication (RSPE) is low during C1 and high during J1. For STM-1/STS-3c signals, there is one J1 pulse. For STS-3 signals, there are three J1 pulses.
RSPE	85	O	CMOS2mA	**Receive SPE Indication:** RSPE is high during STM-1 AU-4 and STS-3/STS-3c SPE byte times (261 byte times per subframe). This signal is low during the time that corresponds to the STM-1 section overhead and AU-4 pointer bytes and the STS-3 transport overhead bytes (nine byte times per subframe).
RTDO(7-0)	94-87	O	CMOS2mA	**Receive Terminal Data Out:** Byte-parallel STM-1/STS-3/STS-3c data. Data is clocked out on the falling edge of the Receive Terminal Clock Out (RTCO). Data bytes are present for the A1, A2, three E1s, three H1s and H2s, H4 during VTAIS/TUAIS, and 261 STM-1 AU-4 or STS-3/STS-3c SPE (path overhead bytes plus payload) byte times. During other byte times, the data bytes are set equal to zero. RTDO7 is defined as the most significant bit.
RTCO	96	O	CMOS2mA	**Receive Terminal Clock Out:** Output clock, derived from RRCI, that has a nominal frequency of 19.44 MHz and is used for clocking out the byte-parallel data after retiming, and the RC1J1, RSPE, and RPAR signals.

Symbol	Pin No.	I/O/P	Type	Name/Function
RPOH	97	O	CMOS2mA	**Receive Terminal Path Overhead Indication:** RPOH is high during STM-1/STS-3/STS-3c path overhead byte times. For STM-1/STS-3c signals, RPOH will be high for one byte per subframe. For STS-3 signals, RPOH will be high for three bytes per subframe. RPOH is low during VTAIS alarm conditions.

Terminal Side Transmit Interface

Symbol	Pin No.	I/O/P	Type	Name/Function
TTCI	23	I/O	CMOS2mA	**Transmit Terminal Clock In:** Transmit STM-1/STS-3 byte rate clock that has a nominal frequency of 19.44 MHz. In normal operation, byte-parallel data TTDI(7-0) and the other transmit terminal input signals are clocked into the SOT-3 device on the rising edge of this clock. In the data communication mode, this clock becomes an output clock and is used for sourcing data (TTDI) into the SOT-3 device.
TPAR	24	I	CMOS	**Terminal Parity Input:** Odd parity input bit in which parity has been calculated over the transmit data byte, TSPE, and TC1J1 signals. The SOT-3 device compares this input value against an internally generated value. If the comparison does not match, the BERR alarm bit is set. TPAR is not used in the data communication mode. The J1 pulse within the T1C1J1 signal is ignored if it is coincident with a parity error. The C1 pulse is not ignored.
TC1J1	25	I/O	TTL2mA	**Transmit C1J1 Indication:** An input synchronization signal which contains active high pulses in the location of the first C1 byte in the transport overhead and in the location(s) of the J1 byte(s) within the payload. The transmit SPE indication (TSPE) must be low during C1 and high during J1. For STM-1/STS-3c signals, there is one J1 pulse. For STS-3 signals, there are three J1 pulses. In the data communication operating mode, this signal becomes an output. See TPAR above for effect of a parity error.
TSPE	26	I/O	TTL2mA	**Transmit SPE Indication:** In normal operation, TSPE is an active high input signal that occurs during STM-1 AU-4 or STS-3/STS-3c SPE byte times (261 byte times per row.) It is low during the time that corresponds to the STM-1 section overhead and AU pointer bytes and the STS-3/STS-3c transport overhead bytes (nine byte times per row). In the data communication operating mode, this signal becomes an output.

Symbol	Pin No.	I/O/P	Type	Name/Function
TPOH	27	O	CMOS2mA	**Transmit Terminal Path Overhead Indication:** Used only in the data communication mode, TPOH is high during STM-1/STS-3/STS-3c path overhead byte times. For STM-1/STS-3c signals, TPOH will be high for one byte per subframe. For STS-3 signals, TPOH will be high for three bytes per subframe.
TTDI(7-0)	35-28	I	CMOS	**Transmit Terminal Data In:** Byte-parallel STM-1/ STS-3/STS-3c data input. During normal or data communication operation, data bytes are present for 260 STM-1 TUG-3 or STS-3/STS-3c SPE byte times. The E1 bytes carrying an AIS indication are optional. The path overhead may accompany the payload. No other data bytes are required. TTDI7 is defined as the most significant bit.

Transport Overhead Byte Access Interface

Symbol	Pin No.	I/O/P	Type	Name/Function
RSAFO	133	O	TTL4mA	**Receive TOH Serial Access Port Frame Out:** An active high framing pulse that identifies the most significant bit in the C1 byte of the RSADO serial data stream. This framing pulse is also used to identify the location of the first bit of the Receive Alarm Indication Port Data Out (RAIDO) signal.
RSACO	134	O	TTL4mA	**Receive TOH Serial Access Port Clock Out:** A gapped clock which has an average rate of 5.184 MHz. The clock is generated by dividing the RLCI input clock by three and the gap is one clock cycle out of every five cycles. This permits a serial clock to be derived from the byte rate clock. Data (RSADO) and framing (RSAFO) are clocked out on the falling edge of this clock. This clock is also used to clock out the Receive Alarm Indication Port Data Out (RAIDO) signal.
RSADO	135	O	TTL4mA	**Receive TOH Serial Access Data Out:** Serial bit stream that carries the received line side section overhead bytes plus the AU-4 pointer in an STM-1 signal or the 81 transport overhead bytes in an STS-3 frame.
TSAFO	143	O	TTL4mA	**Transmit TOH Serial Access Port Frame Out:** An active high framing pulse that identifies the most significant bit in the C1 byte of the TSADI serial data stream. Used for identifying the location of the 81 overhead bytes to be accepted into the SOT-3.

Symbol	Pin No.	I/O/P	Type	Name/Function
TSACO	144	O	TTL4mA	**Transmit TOH Serial Access Port Clock Out:** A gapped output clock which has an average rate of 5.184 MHz. The clock is generated by dividing the TRCI input clock by three, and the gap is one clock cycle for every five cycles. This permits a serial clock to be derived from a byte rate clock. Data (TSADI) is clocked in on the rising edge of this clock.
TSADI	145	I	TTL	**Transmit TOH Serial Access Port Data In:** Serial bit stream that carries the states of the section overhead bytes plus the AU-4 pointer in the STM-1 or the 81 transport overhead bytes received from the line in an STS-3/STS-3c frame.

Controls

Symbol	Pin No.	I/O/P	Type	Name/Function
FLB	3	O	TTL4mA	**Facility Loopback Control Out:** An active high control signal provided by the SOT-3 device via the processor for enabling the facility loopback feature in the SYN155 (TXC-02301B) or other line interface circuit.
TLB	4	O	TTL4mA	**Terminal Loopback Control Out:** An active high control signal provided by the SOT-3 via the processor for enabling the terminal loopback feature in the SYN155 (TXC-02301B) or other line interface circuit.
TLMODE	5	I	TTLp	**Transmit Line Interface Invert:** Causes the TRFI, TRCI, TLFO and TLCO signal functions to be inverted in polarity. See Note 1.
DATACOM	43	I	TTL	**Data Communication Mode:** An active high select for the data communication operating mode. In the transmit direction, the SOT-3 device provides the transmit clock (TTCI), C1J1 signal, SPE, POH, and framing pulse for sourcing terminal data (TTDI) into the SOT-3.
RESET	142	I	TTL	**SOT-3 Reset:** An active high signal which returns the performance monitor and parity counters to preset values. The reset must be used after power is applied and all four input clocks are stable. The signal must be held high for a minimum duration of 1 microsecond and then returned to low.

Note 1: See Figures 4 and 5 for details of operation with TLMODE set to 1 (high) and 0 (low).

AIS Port Indications

Symbol	Pin No.	I/O/P	Type	Name/Function
RXAIS1	76	O	TTL	**Receive AIS Indication (1) Output:** Active high AIS indication for STM-1/STS-3c and STS-1 No. 1 of STS-3. Asserted when one of the following alarms occurs: receive loss of signal (RLOS), internal loss of clock (RLOC), loss of frame (RLOF), line AIS detected (RLAIS), loss of pointer (RLOP) for STM-1/ STS-3c or STS-1 No. 1, path AIS detected (RPAIS) conditional on bits 3 and 4 (PTE0, PTE1) in 3E1H not equal to 0, 0, or loss of multiframe detected (RLOM1) for STM-1/STS-3c or STS-1 No. 1 of STS-3 conditional on bit 3 in 3E3H (LM2AIS) equal to one and PTE0, PTE1 not equal to 0, 0.
RXAIS2	77	O	TTL	**Receive AIS Indication (2) Output:** AIS indication for STS-1 No. 2 of STS-3 (similar to RXAIS1, above).
RXAIS3	78	O	TTL	**Receive AIS Indication (3) Output:** AIS indication for STS-1 No. 3 of STS-3 (similar to RXAIS1, above).
TXAIS1	38	I	TTL	**Transmit AIS Control (1) Input:** A high causes the introduction of line AIS or path AIS into the transmitted STM-1/STS-3c or STS-3 (STS-1 No. 1) signal conditional on bit 2 and bit 0 in 3E0H. Bit 2 (TRPAIS) in 3E0H must be one for enabling path AIS. Bit 0 (TRLAIS) in 3E0H must be one for enabling line AIS.
TXAIS2	37	I	TTL	**Transmit AIS Control (2) Input:** AIS control input for STS-1 No. 2 of STS-3 (similar to TXAIS1, above).
TXAIS3	36	I	TTL	**Transmit AIS Control (3) Input:** AIS control input for STS-1 No. 3 of STS-3 (similar to TXAIS1, above).

Alarm Indication Port Interface

Symbol	Pin No.	I/O/P	Type	Name/Function
RAIDO	132	O	TTL	**Receive Alarm Indication Port Data Out:** An output that provides the status of receive alarms for ring applications. The RAIDO interface is connected to the TAIDI port of the mate SOT-3 device. The data is a serial stream of 40 bits that is transmitted once per frame. The output has the following bit sequence, starting with bit 39, the first bit transmitted: Bit No. — Indication 39 — Send Yellow(1) 38 — Send FERF (line RDI) 37 — APS new 36-21 — Debounced K1K2 bytes 20-17 — FEBE(1) count, LSB in bit 17 16 — Not used - low 15 — Send Yellow(2) 14 — Send FERF (line RDI) 13 — APS new 12 — Not used-low 11-8 — FEBE(2) count, LSB in bit 8 7 — Send Yellow(3) 6 — Send FERF (line RDI) 5 — APS new 4 — Not used-low 3-0 — FEBE(3) count, LSB in bit 0 Send Yellow(n) alarm (path RDI) is inserted into the transmit line signal if any one of seven conditions occurs (e.g, Loss of Signal, Loss of Clock, Loss of Frame). Refer to the description of Transmit Path Yellow Control in the Control Register Descriptions section of this data sheet for all seven conditions. The letter n represents the STS-1 number. Send FERF is equal to loss of signal (RLOS), loss of frame (LOF), or line AIS. APS new is an indication that a new value of K1K2 has been received for three consecutive frames. K1K2 (bits 36-21) are the latest bytes persisting for at least three frames. FEBE(n) is equal to the last four bits of the B3(n) error count. Data is clocked out on the falling edge of the Receive TOH Clock (RSACO). The receive TOH framing signal (RSAFO) occurs during the first bit (No. 39) of the alarm indication port data stream.

Symbol	Pin No.	I/O/P	Type	Name/Function
TAICI	147	I	TTL	**Transmit Alarm Indication Port Clock In:** Normally connected to the Receive TOH Serial Access Port Clock Out signal (RSACO) of the other SOT-3 device in a ring configuration. This is a gapped clock which has an average rate of 5.184 MHz. Data (TAIDI) and framing (TAIFI) are clocked into the SOT-3 on the rising edges of this clock. TAICI is not monitored for loss of clock.
TAIFI	148	I	TTL	**Transmit Alarm Indication Port Frame In:** Normally connected to the Receive TOH Serial Access Port Frame out signal (RSAFO) pin of the other SOT-3 device in a ring configuration. Requires an active high framing pulse that identifies the first bit of the alarm indication port data stream.
TAIDI	149	I	TTL	**Transmit Alarm Indication Port Data In:** Normally connected to the Receive Alarm Indication Port Data Out signal (RAIDO) pin of the other SOT-3 device when two devices are used together in a ring configuration. The input alarms are used to generate FERF, yellow and FEBE alarm indications, and APS information, in the transmitted STM-1/STS-3 line signal. The alarm indication states are clocked into the SOT-3 device on the rising edges of the Transmit TOH Clock (RSACO).

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min *	Max *	Unit
Supply voltage	V_{DD}	-0.3	+7.0	V
DC input voltage	V_{IN}	-0.5	V_{DD} + 0.5	V
Continuous power dissipation	P_C		1	Watts
Ambient operating temperature	T_A	-40	85	^oC
Operating junction temperature	T_J		150	^oC
Storage temperature range	T_S	-55	150	^oC

*Note: Operating conditions outside the min-max ranges specified may cause permanent device failure. Exposure to conditions near the min or max limits for extended periods may impair device reliability.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal resistance - junction to ambient		54	56	$^oC/W$	

POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	4.75	5.0	5.25	V	
I_{DD}			180	mA	
P_{DD}			945	mW	Inputs switching

INPUT, OUTPUT AND I/O PARAMETERS

Input Parameters For TTL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	µA	$V_{DD} = 5.25$
Input capacitance		3.5		pF	

Input Parameters For TTLp

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current		0.5	1.4	mA	$V_{DD} = 5.25$; Input = 0 volts
Input capacitance		3.5		pF	

Note: Input has a 9k (nominal) internal pull-up resistor.

Input Parameters For CMOS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	3.15			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			1.65	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	µA	$V_{DD} = 5.25$
Input capacitance		3.5		pF	

Output Parameters For TTL4mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	$V_{DD} = 4.75$; $I_{OH} = -2.0$
V_{OL}			0.4	V	$V_{DD} = 4.75$; $I_{OL} = 4.0$
I_{OL}			4.0	mA	
I_{OH}			-2.0	mA	
t_{RISE}	2.5	5.5	10.0	ns	$C_{LOAD} = 15pF$
t_{FALL}	1.0	2.0	4.0	ns	$C_{LOAD} = 15pF$

Output Parameters For CMOS2mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 4.75; I_{OH} = -2.0
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 2.0
I_{OL}			2.0	mA	
I_{OH}			-2.0	mA	
t_{RISE}	2.5	5.5	9.9	ns	C_{LOAD} = 15pF
t_{FALL}	2.0	3.9	8.0	ns	C_{LOAD} = 15pF

Input/Output Parameters For TTL8mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	mA	V_{DD} = 5.25
Input capacitance		3.5		pF	
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 4.75; I_{OH} = -4.0 mA
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 8.0 mA
I_{OL}			8.0	mA	
I_{OH}			-4.0	mA	
t_{RISE}	1.9	4.5	8.0	ns	C_{LOAD} = 25pF
t_{FALL}	0.8	1.5	3.1	ns	C_{LOAD} = 25pF

Input/Output Parameters For CMOS2mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	3.15			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			1.65	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	µA	V_{DD} = 5.25
Input capacitance		3.5		pF	
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 4.75; I_{OH} = -2.0 mA
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 2.0 mA
I_{OL}			2.0	mA	
I_{OH}			-2.0	mA	
t_{RISE}	2.5	5.5	9.9	ns	C_{LOAD} = 15pF
t_{FALL}	2.0	3.9	8.0	ns	C_{LOAD} = 15pF

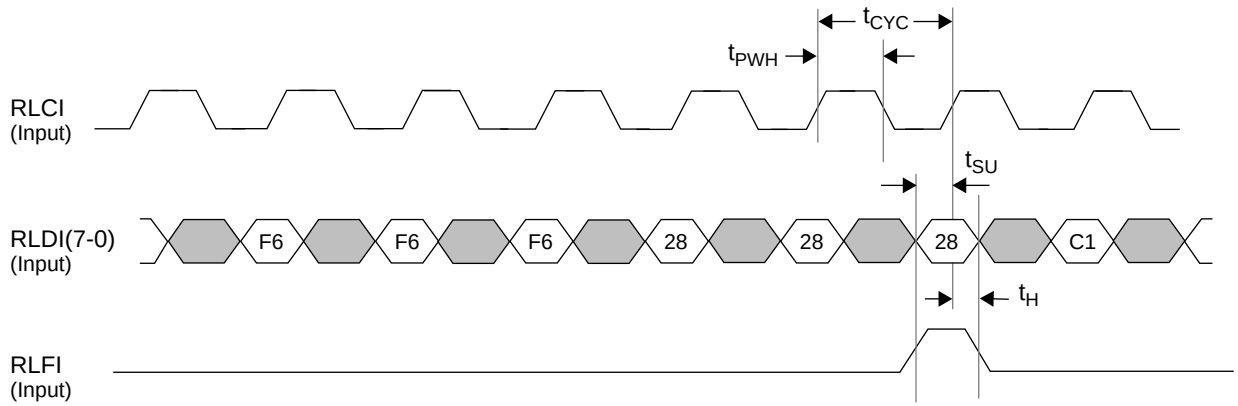
Input/Output Parameters For TTL2mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	µA	$V_{DD} = 5.25$
Input capacitance		3.5		pF	
V_{OH}	V_{DD} - 0.5			V	$V_{DD} = 4.75$; $I_{OH} = -2.0$ mA
V_{OL}			0.4	V	$V_{DD} = 4.75$; $I_{OL} = 2.0$ mA
I_{OL}			2.0	mA	
I_{OH}			-2.0	mA	
t_{RISE}	2.5	5.5	9.9	ns	$C_{LOAD} = 15$pF
t_{FALL}	2.0	3.9	8.0	ns	$C_{LOAD} = 15$pF

TIMING CHARACTERISTICS

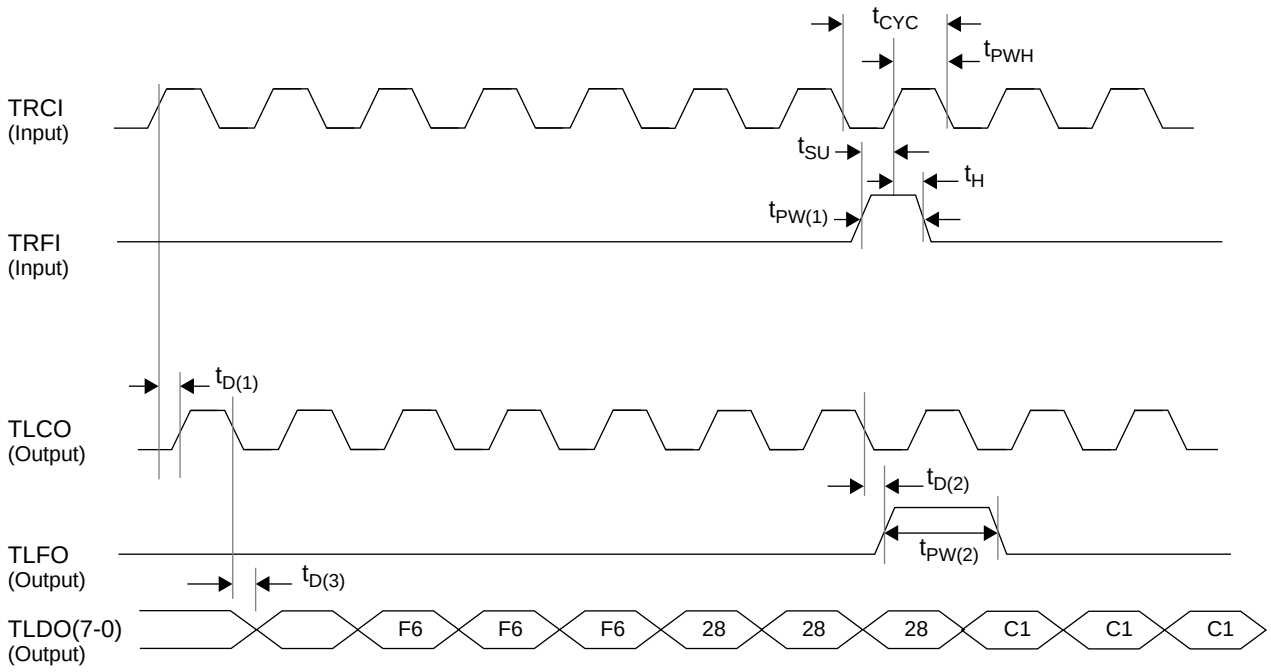
Detailed timing diagrams for the SOT-3 device are illustrated in Figures 3 through 16, with values of the timing intervals following each figure. All output times are measured with a maximum 25 pF load capacitance. Timing parameters are measured at $(V_{OH} - V_{OL})/2$ or $(V_{IH} - V_{IL})/2$ as applicable.

Figure 3. Line Side Receive Timing



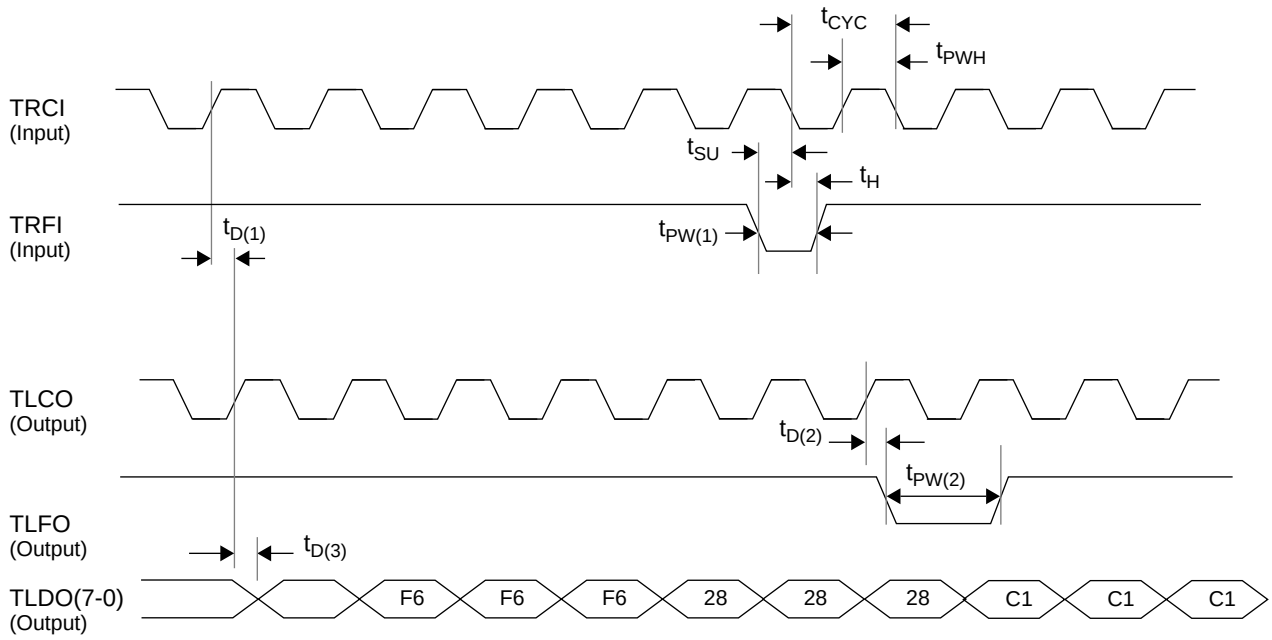
Parameter	Symbol	Min	Typ	Max	Unit
RLCI clock period	t_{CYC}	50	51.44		ns
RLCI duty cycle (t_{PWH}/t_{CYC})	--	45		55	%
RLDI/RLFI set-up time to RLCI↑	t_{SU}	7			ns
RLDI/RLFI hold time after RLCI↑	t_H	3			ns

Figure 4. Line Side Transmit Timing with TLMODE (Pin 5) Tied High



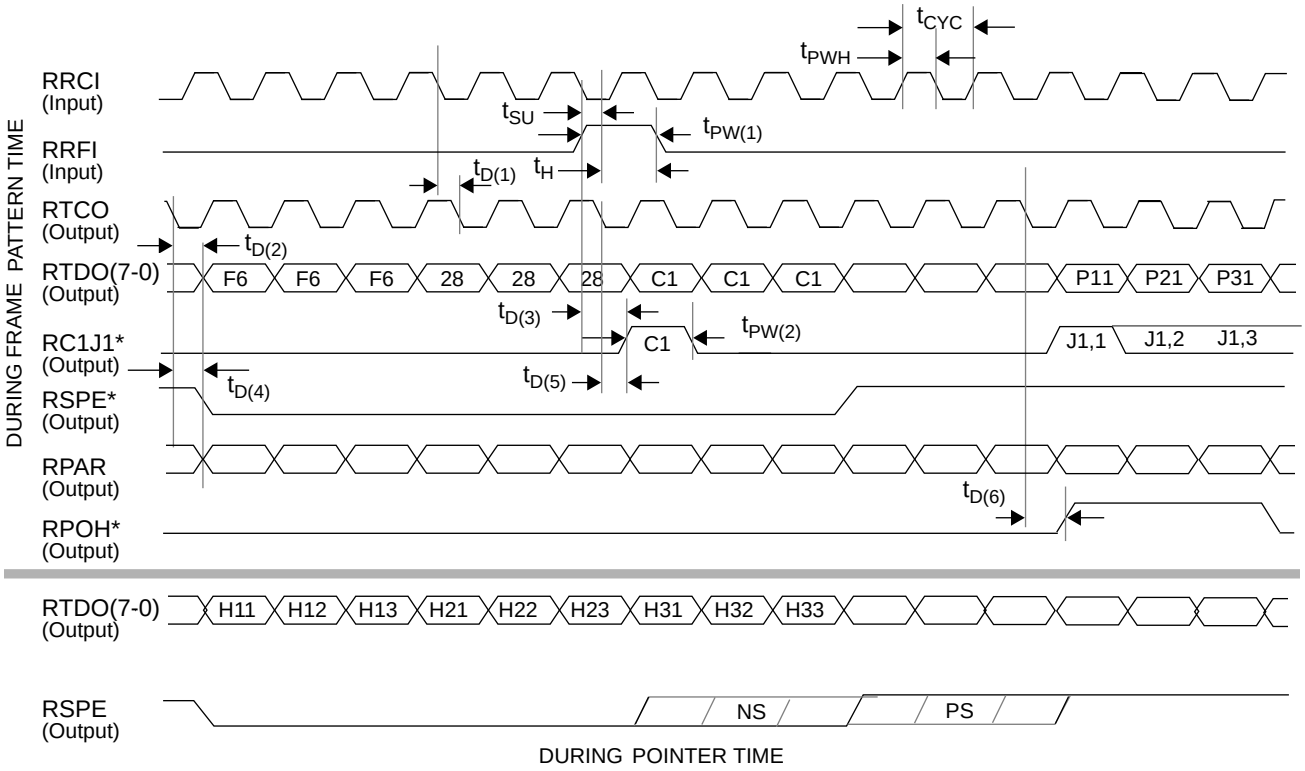
Parameter	Symbol	Min	Typ	Max	Unit
TRCI clock period	t_{CYC}	50	51.44		ns
TRCI duty cycle (t_{PWH}/t_{CYC})	--	45		55	%
TRFI set-up time to TRCI↑	t_{SU}	7			ns
TRFI hold time after TRCI↑	t_H	3			ns
TLCO delay after TRCI↑	$t_{D(1)}$	6	15	30	ns
TLFO delay after TLCO↓	$t_{D(2)}$	-2	0	5	ns
TLDO delay after TLCO↓	$t_{D(3)}$	-2	0	5	ns
TRFI pulse width	$t_{PW(1)}$	40			ns
TLFO pulse width	$t_{PW(2)}$	40	t_{CYC}		ns

Figure 5. Line Side Transmit Timing with TLMODE (Pin 5) Tied Low



Parameter	Symbol	Min	Typ	Max	Unit
TRCI clock period	t_{CYC}	50	51.44		ns
TRCI duty cycle (t_{PWH}/t_{CYC})	--	45		55	%
TRFI set-up time to TRCI↓	t_{SU}	7			ns
TRFI hold time after TRCI↓	t_H	3			ns
TLCO delay after TRCI↑	$t_{D(1)}$	6	15	30	ns
TLFO delay after TLCO↑	$t_{D(2)}$	-2	0	5	ns
TLDO delay after TLCO↑	$t_{D(3)}$	-2	0	5	ns
TRFI pulse width	$t_{PW(1)}$	40			ns
TLFO pulse width	$t_{PW(2)}$	40	t_{CYC}		ns

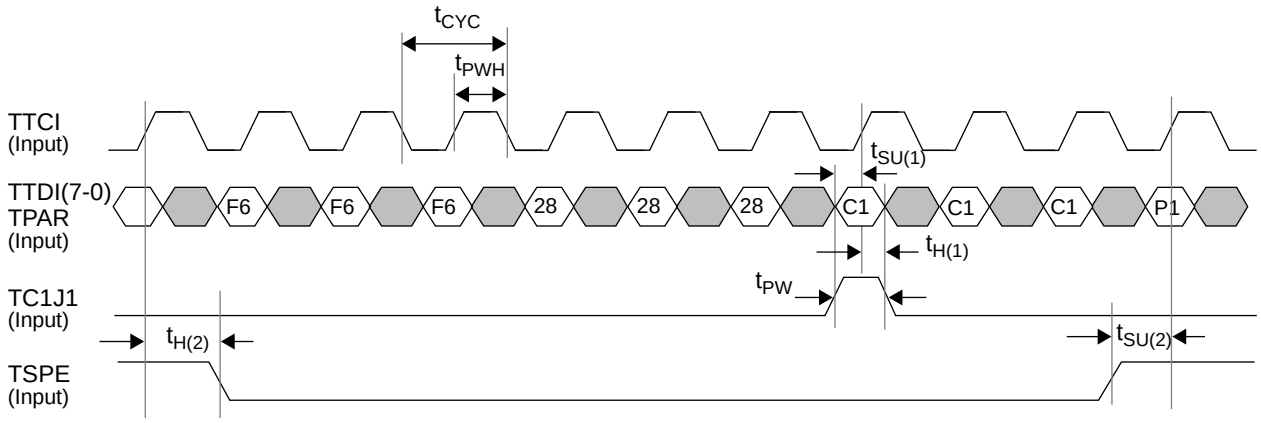
Figure 6. Terminal Side Receive Timing



Parameter	Symbol	Min	Typ	Max	Unit
RRCI clock period	t_{CYC}	50	51.44		ns
RRCI duty cycle (t_{PWH}/t_{CYC})	--	45		55	%
RRFI set-up time to RRCI↑	t_{SU}	7			ns
RRFI hold time after RRCI↑	t_H	3			ns
RTCO↓ delay after RRCI↓	$t_{D(1)}$	6	15	30	ns
RTDO delay after RTCO↓	$t_{D(2)}$	-2	0	5	ns
RC1J1 C1 pulse delay after RRFI↑	$t_{D(3)}$	0		40	ns
RSPE, RPAR delay after RTCO↓	$t_{D(4)}$	-2	0	5	ns
RC1J1 C1 pulse delay after RTCO↓	$t_{D(5)}$	-2	0	5	ns
RPOH delay after RTCO↓	$t_{D(6)}$	-2	0	5	ns
RRFI pulse width	$t_{PW(1)}$	40			ns
RC1J1 C1 pulse width	$t_{PW(2)}$	40	t_{CYC}	3 t_{CYC}	ns

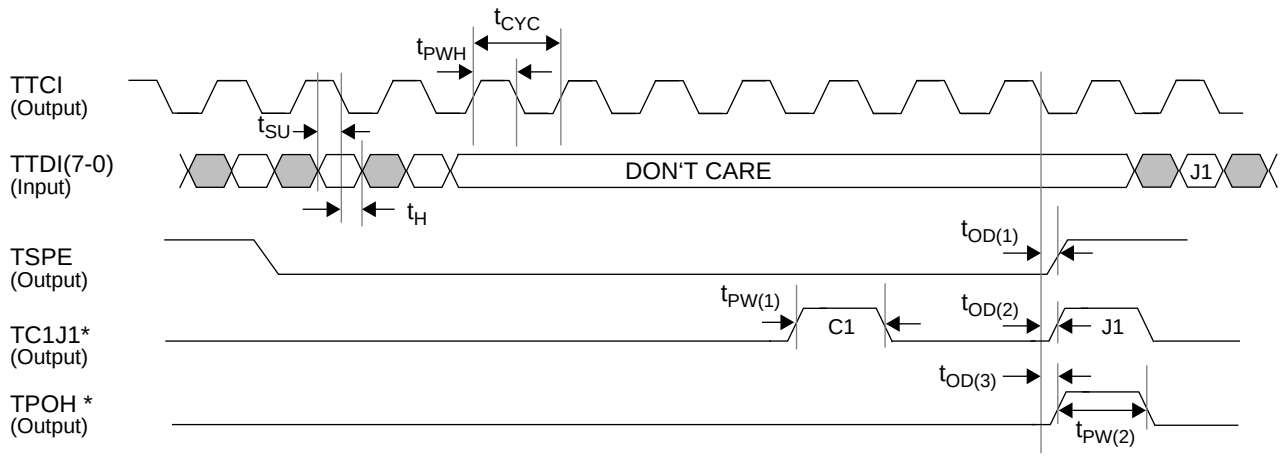
*Note: The location of the J1, SPE and POH indications will change with the pointer value(s). In the STM-1 or STS-3c mode, there will be a single J1 pulse. In the STS-3 mode, there will be three J1 locations, one for each STS-1. If the pointer values of 2 or 3 of the STS-1s are the same, the NRZ character of the STS-3 output causes the adjacent pulses to be a single entity as illustrated by the dotted line in the RC1J1 waveform above. The pointer value illustrated is 522 (Decimal). If the pointer values of the three STS-1s are different the STS-3 output will be RZ, yielding three J1 pulses.

Figure 7. Transmit Terminal Side Timing



Parameter	Symbol	Min	Typ	Max	Unit
TTCI clock period	t_{CYC}	50	51.44		ns
TTCI duty cycle (t_{PWH}/t_{CYC})	--	45		55	%
TTDI/TPAR/TC1J1 set-up time to TTCI↑	$t_{SU(1)}$	7			ns
TTDI/TPAR/TC1J1 hold time after TTCI↑	$t_{H(1)}$	3			ns
TC1J1 pulse width	t_{PW}	40			ns
TSPE set-up time to TTCI↑	$t_{SU(2)}$	7			ns
TSPE hold time after TTCI↑	$t_{H(2)}$	3			ns

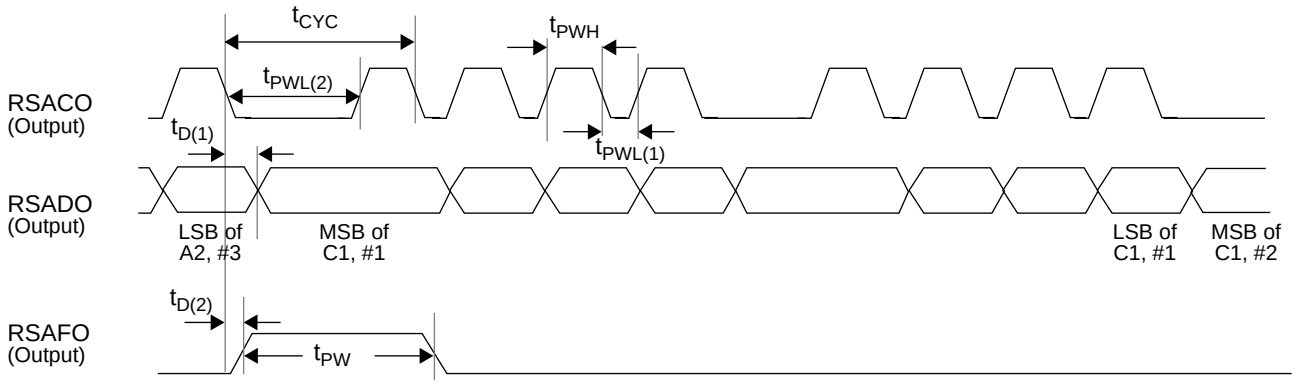
Figure 8. Transmit Terminal Side Timing in Data Communication Mode



Parameter	Symbol	Min	Typ	Max	Unit
TTCI clock period	t_{CYC}	50	51.44		ns
TTCI duty cycle (t_{PWH}/t_{CYC})	--	45		55	%
TTDI set-up time to TTCI↓	t_{SU}	19			ns
TTDI hold time after TTCI↓	t_H	0			ns
TC1J1 pulse width	$t_{PW(1)}$	40	t_{CYC}	3 t_{CYC}	ns
TPOH pulse width	$t_{PW(2)}$	40	t_{CYC}	3 t_{CYC}	ns
TSPE output delay after TTCI↓	$t_{OD(1)}$	-2	0	5	ns
TC1J1 output delay after TTCI↓	$t_{OD(2)}$	-2	0	5	ns
TPOH output delay after TTCI↓	$t_{OD(3)}$	-2	0	5	ns

* Note: TPOH occurs every subframe during the transport path overhead byte time, and J1 occurs once per frame.

Figure 9. TOH Serial Access Port Receive Timing

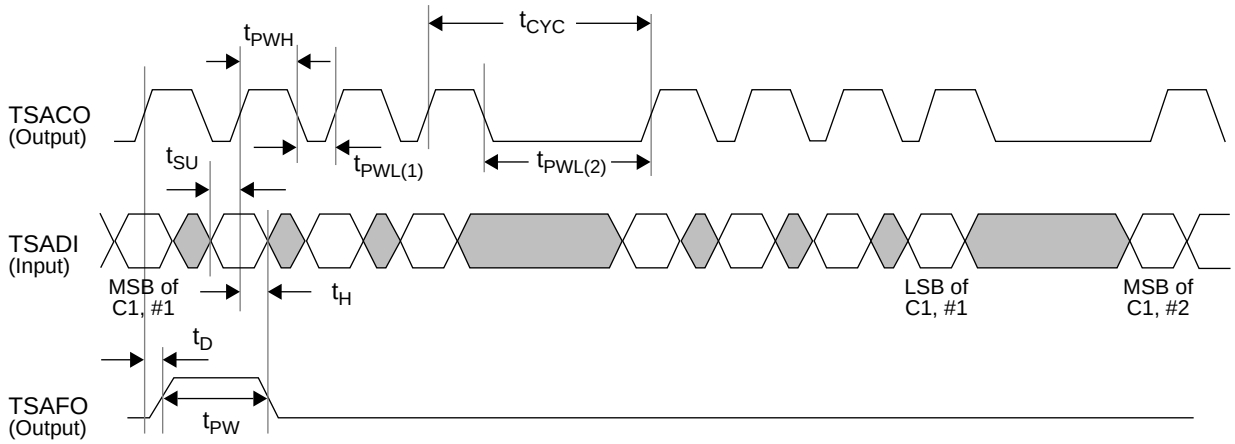


Parameter	Symbol	Min	Typ	Max	Unit
RSACO clock period	t_{CYC}	3 t_{CYC}*	**	6 t_{CYC}*	ns
RSACO high time	t_{PWH}		2 t_{CYC}*		ns
RSACO low time (non-gap time)	$t_{PWL(1)}$		1 t_{CYC}*		ns
RSACO low time (gap time)	$t_{PWL(2)}$		4 t_{CYC}*		ns
RSADO delay after RSACO↓	$t_{D(1)}$	-2	0	5	ns
RSAFO delay after RSACO↓	$t_{D(2)}$	-2	0	5	ns
RSAFO pulse width	t_{PW}		6 t_{CYC}*		ns

*t_{CYC} is equal to one RLCI clock period (51.44 ns, nominal).

**Long term average RSACO clock period is 5/4(t_{CYC} x 3), or 192.9 ns, nominal.

Figure 10. TOH Serial Access Port Transmit Timing

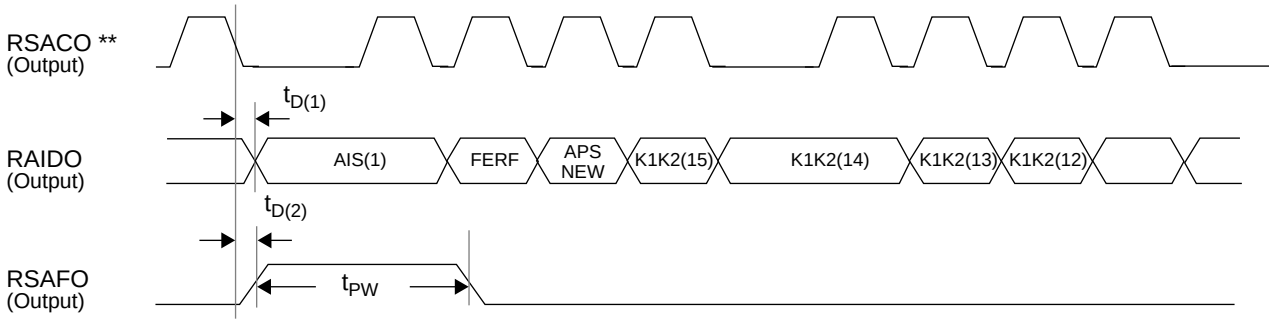


Parameter	Symbol	Min	Typ	Max	Unit
TSACO clock period	t_{CYC}	3 t_{CYC}*	**	6 t_{CYC}*	ns
TSACO high time	t_{PWH}		2 t_{CYC}*		ns
TSACO low time (non-gap time)	$t_{PWL(1)}$		1 t_{CYC}*		ns
TSACO low time (gap time)	$t_{PWL(2)}$		4 t_{CYC}*		ns
TSADI set-up time to TSACO↑	t_{SU}	7			ns
TSADI hold time after TSACO↑	t_H	3			ns
TSAFO delay after TSACO↑	t_D	-2	0	5	ns
TSAFO pulse width	t_{PW}		3 t_{CYC}*		ns

* t_{CYC} is equal to one TRCI clock period (51.44 ns, nominal).

**Long term average TSACO clock period is 5/4(t_{CYC} x 3), or 192.9 ns, nominal.

Figure 11. Alarm Indication Port Receive Timing

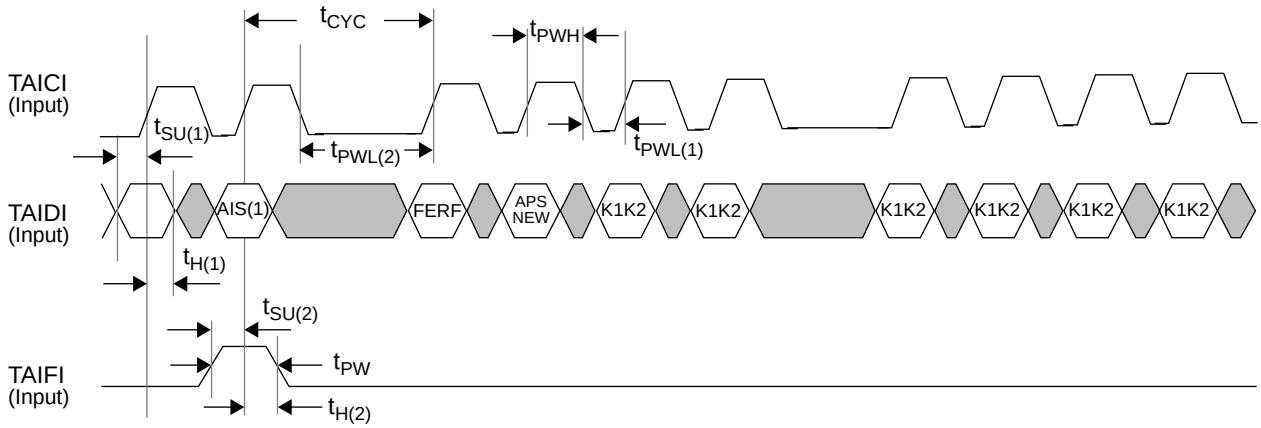


Parameter	Symbol	Min	Typ	Max	Unit
RAIDO delay after RSACO↓	$t_{D(1)}$	-2	0	5	ns
RSAFO delay after RSACO↓	$t_{D(2)}$	-2	0	5	ns
RSAFO pulse width	t_{PW}		6 t_{CYC}*		ns

*t_{CYC} is equal to one RLCI clock period (51.44 ns, nominal).

**Timing characteristics of RSACO are shown in Figure 9.

Figure 12. Alarm Indication Port Transmit Timing

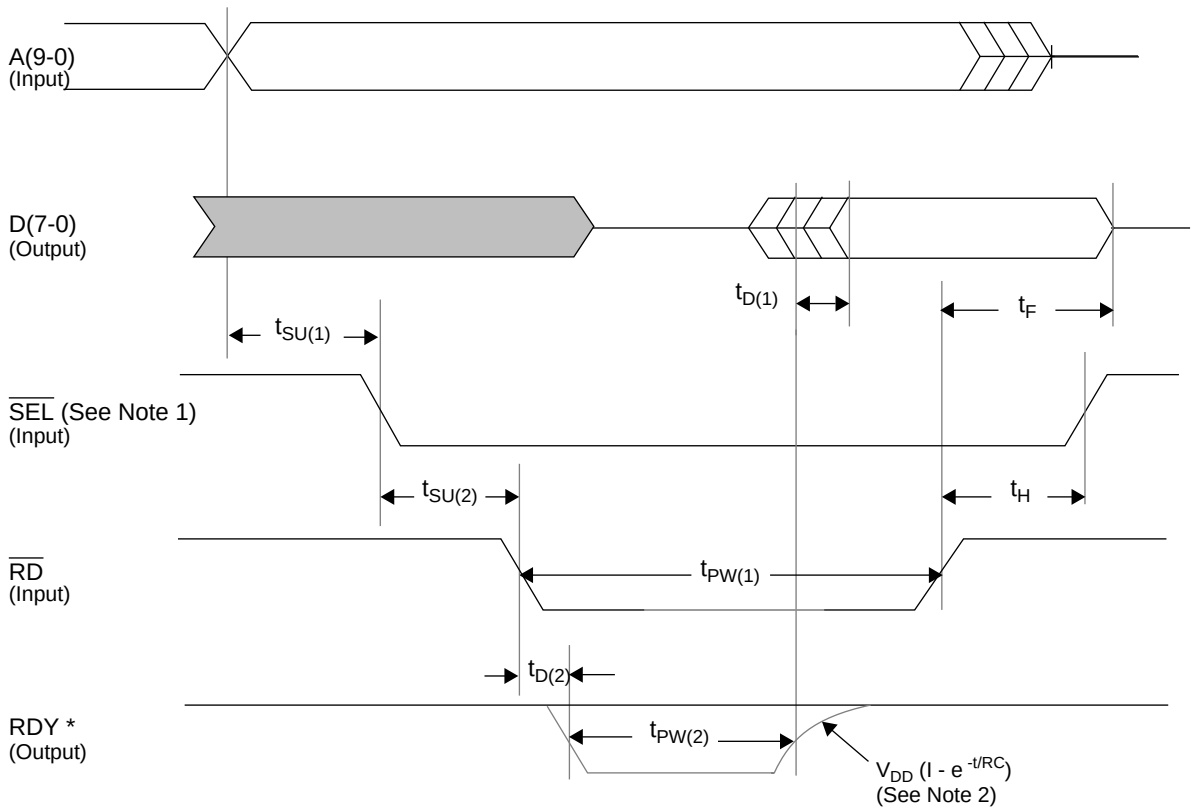


Parameter **	Symbol	Min	Typ	Max	Unit
TAICI clock period	t_{CYC}	3 t_{CYC}*		6 t_{CYC}*	ns
TAICI high time	t_{PWH}		2 t_{CYC}*		ns
TAICI low time (non-gap time)	$t_{PWL(1)}$		1 t_{CYC}*		ns
TAICI low time (gap time)	$t_{PWL(2)}$		4 t_{CYC}*		ns
TAIDI set-up time to TAICI↑	$t_{SU(1)}$	7			ns
TAIDI hold time after TAICI↑	$t_{H(1)}$	3			ns
TAIFI set-up time to TAICI↑	$t_{SU(2)}$	7			ns
TAIFI hold time after TAICI↑	$t_{H(2)}$	3			ns
TAIFI pulse width	t_{PW}		3 t_{CYC}*		ns

* t_{CYC} is equal to one TRCI clock period (51.44 ns, nominal) from the SOT-3 device that is sourcing the Alarm Indication Port signals.

** In applications using the Alarm Indication Port, TAICI, TAIDI and TAIFI of one SOT-3 device would normally be connected to RSACO, RAIDO, and RSAFO, respectively, of another SOT-3 device. Timing characteristics of these signals are shown in Figure 11.

Figure 13. Microprocessor Interface Bus Timing: Read Cycle - Intel Mode



Parameter	Symbol	Min	Typ	Max	Unit
A(9-0) address set-up time to $\overline{SEL}\downarrow$	$t_{SU(1)}$			0	ns
D(7-0) data output valid delay after RDY$\uparrow$	$t_{D(1)}$	0			ns
D(7-0) data output float time after $\overline{RD}\uparrow$	t_F	1	3	5	ns
$\overline{SEL}$ set-up time to $\overline{RD}\downarrow$	$t_{SU(2)}$	20			ns
$\overline{RD}$ pulse width	$t_{PW(1)}$	40			ns
$\overline{SEL}$ hold time after $\overline{RD}\uparrow$	t_H	0			ns
RDY delay after $\overline{RD}\downarrow$*	$t_{D(2)}$	1	3	5	ns
RDY pulse width*	$t_{PW(2)}$	0		617**	ns

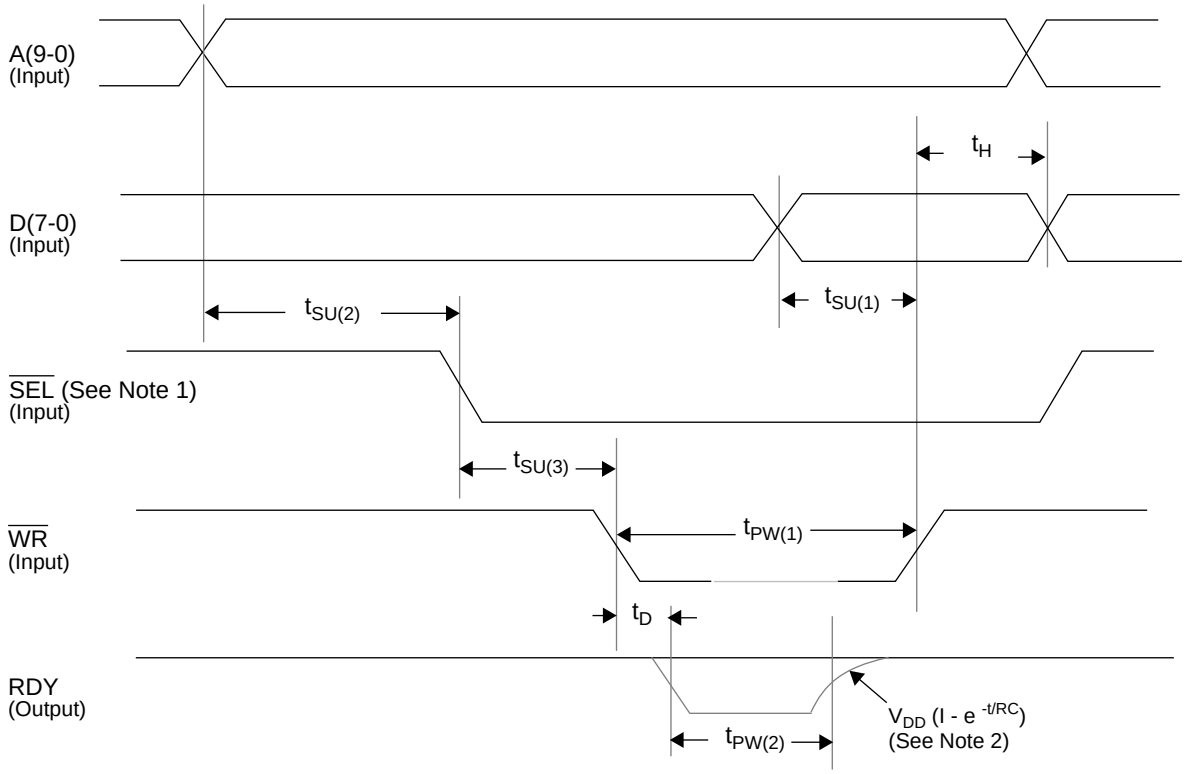
* RDY goes low when the address being written to corresponds to a RAM location but remains high when externally pulled-up during status or control register access.

**Assuming a 19.44 MHz clock at RAMCI.

Note 1: $\overline{SEL}$ must be active low for $\overline{RD}$ to be valid, and $t_{SU(2)}$ must be as specified. If the SOT-3 is the only device on the bus, $\overline{SEL}$ can be grounded.

Note 2: Open Drain rise time is dependent upon external pull-up resistor (R) and load capacitance (C).

Figure 14. Microprocessor Interface Bus Timing: Write Cycle - Intel Mode



Parameter	Symbol	Min	Typ	Max	Unit
A(9-0) address set-up time to $\overline{SEL}\downarrow$	$t_{SU(2)}$	20			ns
D(7-0) data input valid set-up time to $\overline{WR}\uparrow$	$t_{SU(1)}$	20			ns
D(7-0) data input hold time after $\overline{WR}\uparrow$	t_H		1	3	ns
$\overline{SEL}$ set-up time to $\overline{WR}\downarrow$	$t_{SU(3)}$	0			ns
$\overline{WR}$ pulse width	$t_{PW(1)}$	40			ns
RDY delay after $\overline{WR}\downarrow$*	t_D	1	3	5	ns
RDY pulse width*	$t_{PW(2)}$	0		617**	ns

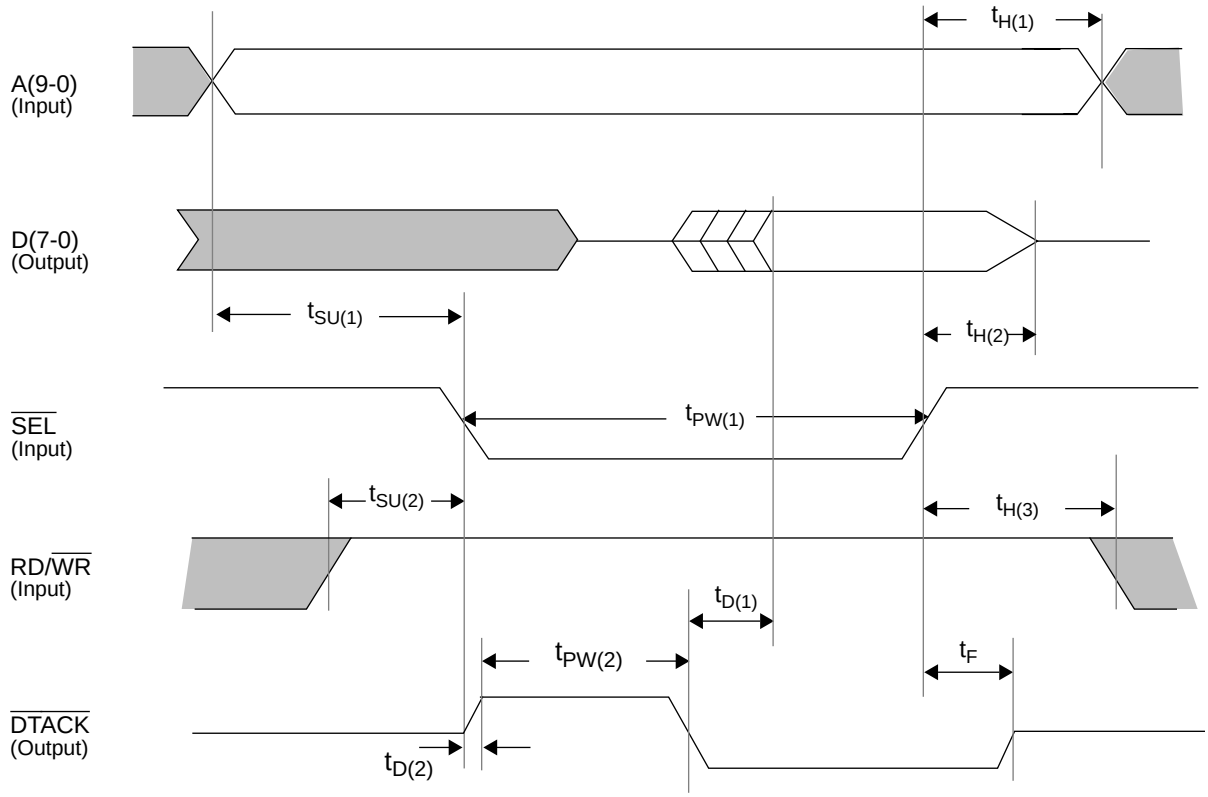
* RDY goes low when the address being written to corresponds to a RAM location but remains high when externally pulled-up during status or control register access.

**Assuming a 19.44 MHz clock at RAMCI.

Note 1: If the address, A(9-0), is valid 20 nanoseconds before $\overline{WR}$ becomes active low, and if the SOT-3 is the only device on the bus, then $\overline{SEL}$ can be grounded.

Note 2: Open Drain rise time is dependent upon external pull-up resistor (R) and load capacitance (C).

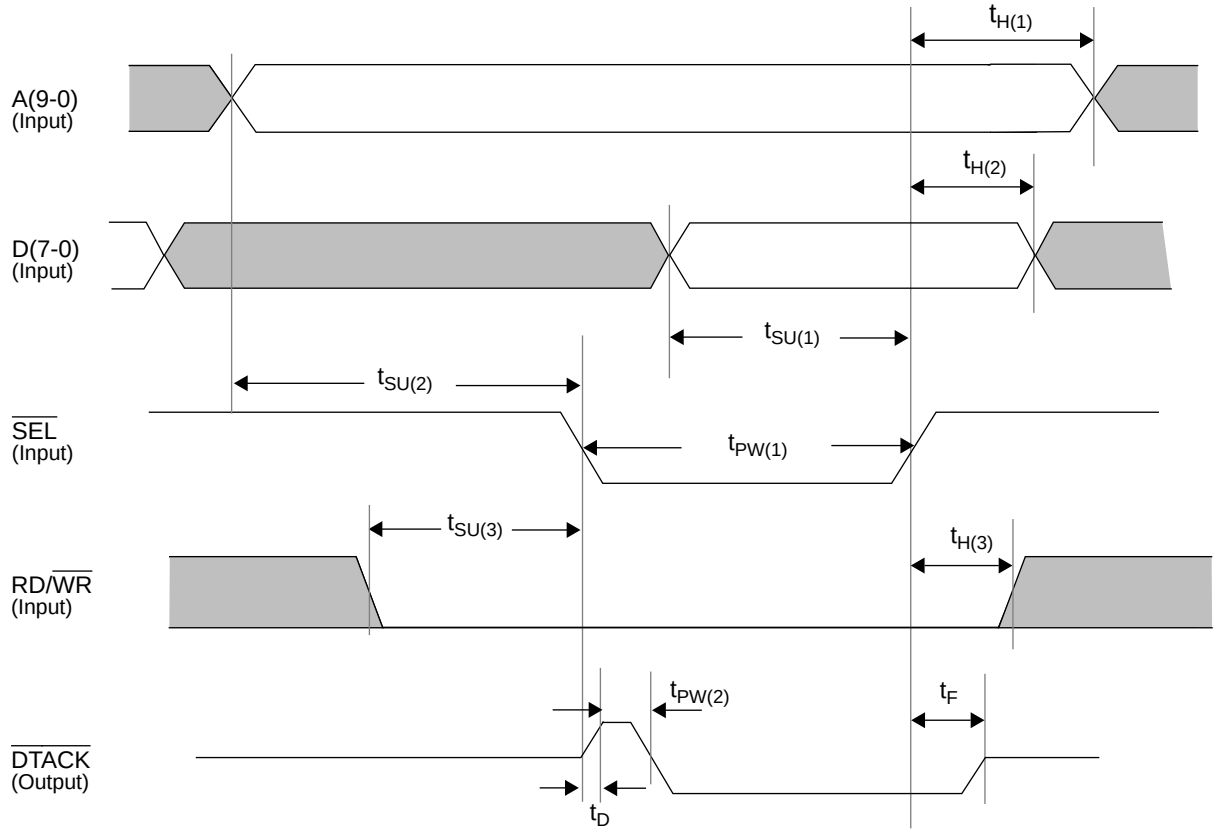
Figure 15. Microprocessor Interface Bus Timing: Read Cycle - Motorola Mode



Parameter	Symbol	Min	Typ	Max	Unit
A(9-0) address valid set-up time to $\overline{SEL}\downarrow$	$t_{SU(1)}$	20			ns
A(9-0) address hold time after $\overline{SEL}\uparrow$	$t_{H(1)}$	0			ns
D(7-0) data output delay after $\overline{DTACK}\downarrow$	$t_{D(1)}$	0			ns
D(7-0) data output hold time after $\overline{SEL}\uparrow$	$t_{H(2)}$	1	3	5	ns
RD/$\overline{WR}$ set-up time to $\overline{SEL}\downarrow$	$t_{SU(2)}$		3	5	ns
$\overline{SEL}$ pulse width	$t_{PW(1)}$	40			ns
RD/$\overline{WR}$ hold time after $\overline{SEL}\uparrow$	$t_{H(3)}$	0			ns
$\overline{DTACK}$ delay after $\overline{SEL}\downarrow$	$t_{D(2)}$	1	3	5	ns
$\overline{DTACK}$ float time after $\overline{SEL}\uparrow$	t_F	1	3	5	ns
$\overline{DTACK}$ pulse width	$t_{PW(2)}$	0		617*	ns

*Assuming a 19.44 MHz clock at RAMCI.

Figure 16. Microprocessor Interface Bus Timing: Write Cycle - Motorola Mode



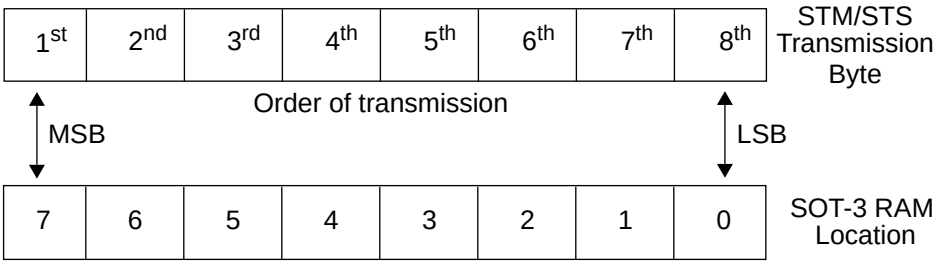
Parameter	Symbol	Min	Typ	Max	Unit
A(9-0) address valid set-up time to $\overline{SEL}\downarrow$	$t_{SU(2)}$	20			ns
A(9-0) address hold time after $\overline{SEL}\uparrow$	$t_{H(1)}$	0			ns
D(7-0) data input valid set-up time to $\overline{SEL}\uparrow$	$t_{SU(1)}$	20			ns
D(7-0) data input hold time after $\overline{SEL}\uparrow$	$t_{H(2)}$		1	3	ns
RD/$\overline{WR}$ set-up time to $\overline{SEL}\downarrow$	$t_{SU(3)}$		3	5	ns
RD/$\overline{WR}$ hold time after $\overline{SEL}\uparrow$	$t_{H(3)}$	0			ns
$\overline{SEL}$ pulse width	$t_{PW(1)}$	40			ns
$\overline{DTACK}$ float time after $\overline{SEL}\uparrow$	t_F	1	3	5	ns
$\overline{DTACK}$ delay after $\overline{SEL}\downarrow$	t_D	1	3	5	ns
$\overline{DTACK}$ pulse width	$t_{PW(2)}$	0		617*	ns

*Assuming a 19.44 MHz clock at RAMCI.

OPERATION

RANDOM ACCESS MEMORY (RAM)

The SOT-3 device's RAM is used for control and status information, pointer justification and performance monitor counters, STS-3/STS-3c transport (STM-1 section) and path overhead bytes, and for multiplexing overhead bytes into the transmitted STM-1/STS-3/STS-3c signal. All address locations are given in Hexadecimal (H). The relationship between the bits of an STM/STS transmission byte (e.g., C1) and the bits of the corresponding SOT-3 RAM location is as illustrated below:



On the receive side of the SOT-3 device, all incoming STS-3/STS-3c transport overhead (STM-1 section overhead) and path overhead bytes are written to locations in RAM. Three separate 64-byte locations are allocated for the path trace message(s) received in the J1 byte(s). Counters for B1, B2 and B3 errors and INC, DEC and NDF pointer justifications are also available in RAM. Real time access to the transport overhead is available via the TOH Serial Access Port.

On the transmit side of the SOT-3 device, all STS-3/STS-3c transport overhead (STM-1 section overhead) bytes are inserted into the outgoing data path from the RAM, with the exception of the pointer bytes. It is possible to insert the H1 and H2 pointer bytes from the RAM by using the TRPTR control bit, but this has no effect on the location of the payload. The TOH RAM locations that are inserted into the data path are either written by the microprocessor or the TOH Serial Access Port. Microprocessor control bits perform the selection. Transmitted path overhead bytes can be inserted from the RAM when in the path terminating mode, or they are retransmitted from the incoming terminal bytes. Path terminating options allow H4 or the F2 and the Z bytes to always be sourced from the terminal.

Microprocessor control bits are used to set the SOT-3 operating modes and loopback operation, and to select the source of overhead bytes multiplexed into the transmitted signal.

Status bits report the condition of alarms from the receive side, the transmit side and from the alarm indication port. Unlatched bit positions provide access to the transient alarm signal. Latched bit positions stay high until cleared by a read operation.

Software interrupt on alarms is provided, as well as an optional hardware interrupt. Writing to the interrupt mask locations controls which alarms cause interrupts. If one of the interrupt mask bits is set to one, and the corresponding status bit goes high, a one is written to bit 7 (SINT) in 3D7H. If bit 7 (HINT) in 3F3H is also a one, then a hardware interrupt to the microprocessor occurs.

A special 16-bit read operation is performed to allow uninterrupted access to certain two-byte values, without the danger of one byte changing while the other byte is being read. The B1, B2 and B3 error counters, the FEBE counters, and the debounced K1-K2 bytes from the receive side and from the Alarm Indication Port all require a 16-bit read operation. To perform a 16-bit read, the low order byte (e.g., B1 error counter, bits 7-0) is read from its location. This causes the high order byte (e.g., B1 error counter, bits 15-8) to be immediately copied into the shared high order byte hold location 3FFH. If the contents of 3FFH are not read next to complete the 16-bit read operation, then the high order byte that it is holding may be lost due to over-writing if another 16-bit read is initiated.

INTERRUPT CONTROL

When the SOT-3 device is operating for STM-1 or STS-3c, certain interrupt bits must be masked by writing a zero to them. The SOT-3 status bits and interrupt mask bits have four sets of the error bits for the following alarms:

RPAIS(1,2,3)	Receive Path AIS
RLOP(1,2,3)	Receive Loss of Pointer
RLOM(1,2,3)	Receive Loss of Multi-frame
RYEL(1,2,3)	Receive Path Yellow

Since the STS-1 No. 2 and No. 3 bits for STS-3 are unused in STM-1/STS-3c they could be employed for other purposes or retain a default value, so they must be masked in the interrupt mask bits table in order to avoid unwarranted interrupts. The masked bits are those with a 2 or 3 as the designator number. If the SOT-3 is used for STS-3, these mask bits can be set to one to enable the interrupt.

The SOT-3 is not sensitive to payload contents. Therefore, for bulk STM-1 or STS-3c payloads where there is no need for a multi-frame indicator, all RLOM interrupt mask bits must be set to zero to avoid a spurious interrupt.

FAULT INFORMATION IN E1 BYTES OF RECEIVE TERMINAL OUTPUT

The receive terminal side E1 bytes of the signals at the RTDO(0-7) output pins provide fault information. All three E1 bytes contain FFH for any of the RLAIS, RLOC, RLOF or RLOS fault conditions, and the E1n byte contains FFH for the condition RLOPn or the compound condition PTE1, PTE0 are not equal to 00 and (RPAISn or (RLOMn and LM2AIS)), where n=1-3. The E1n bytes are 00H for all other conditions, including RFERF.

TERMINAL BUS PARITY

When the SOT-3 is operated against a terminal side bus with other TranSwitch products, bus parity is included, both into and from the SOT-3 terminal side. The SOT-3 can find bus parity errors on its terminal side input and records such errors in BERR (bit 4, address 3D6,3D7).

Parity is determined over all bits on the bus. In particular, there is an ADD pulse on the bus when data is being put onto the bus by an add/drop device. The SOT-3 does not see the ADD pulse, and it consequently records parity errors. There are two solutions:

1. Mask the BERR bit with a zero in the interrupt mask location for BERR.
2. Since the effect of the ADD pulse is to invert the parity bit, the circuit in Figure 17 can be used.

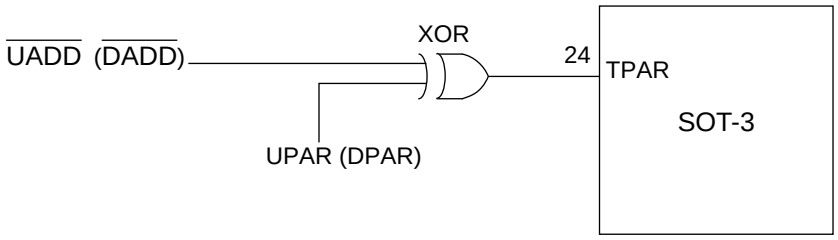


Figure 17. External Circuit to Include the ADD Pulse for Parity

The exclusive-or (XOR) circuit serves to invert the TPAR input to the SOT-3 when the $\overline{\text{UADD}}$ ($\overline{\text{DADD}}$) pulse is present. The truth table is:

$\overline{\text{UADD}}$ ($\overline{\text{DADD}}$)	UPAR (DPAR)	TPAR	
0	0	0	Parity Passed Through
0	1	1	
1	0	1	Parity Inverted
1	1	0	

THROUGHPUT DELAY

The following table gives the extremes of the SOT-3 throughput delay. The delay is a function of pointer change activity and jitter which in turn affect the fill of internal FIFOs in the SOT-3.

Direction	Minimum		Maximum	
	µsec	Bytes	µsec	Bytes
Rx, line to terminal	1.76	34	2.36	46
Tx, terminal to line	3.0	58	3.6	70

OUTPUT DURING SPE LOW

The 125-microsecond frame for STM-1/STS-3/STS-3c is divided into 9 subframes. During the overhead times of these subframes, the RSPE output (pin 85) of the SOT-3 is low, and some data is included on 3 of the 9 subframes during this time.

Subframe 1: Framing Bytes (A1A1A1A2A2A2) with the remaining 3 bytes being 00H. The C1 Byte (immediately following the third A2 byte) is denoted by a pulse on the output C1J1 lead.

Subframe 2: The K2 byte (only) is on the byte output if it is enabled via the software bit map.

Subframe 3: All bytes are 00H.

Subframe 4: All pointer bytes are on the byte output: H11, H12, H13, H21, H22, H23, H31, H32 and H33. Note: the H3 bytes are data if a pointer decrement is made.

Subframe 5-9: All bytes are 00H.

MEMORY MAP FOR RAM LOCATIONS

Receive Overhead RAM Addresses

Transport (Section) Overhead										Path Overhead		
A1 000	**A1** 01B	**A1** 036	**A2** 001	**A2** 01C	**A2** 037	**C11** 002	**C12/N1** 01D	**C13/N2** 038		**J11** 080-0BF	**J12** 0C0-0FF	**J13** 100-13F
B1 003	**M1** 01E	**M2** 039	**E1** 004	**M3** 01F	**U1** 03A	**F1** 005	**N3** 020	**N4** 03B		**B31** 060	**B32** 068	**B33** 070
D1 006	**M4** 021	**M5** 03C	**D2** 007	**M6** 022	**U2** 03D	**D3** 008	**U3** 023	**U4** 03E		**C21** 061	**C22** 069	**C23** 071
H11 009	**H12** 024	**H13** 03F	**H21** 00A	**H22** 025	**H23** 040	**H31** 00B	**H32** 026	**H33** 041		**G11** 062	**G12** 06A	**G13** 072
B21 00C	**B22** 027	**B23** 042	**K1** 00D	**U5** 028	**U6** 043	**K2** 00E	**U7** 029	**U8** 044		**F21** 063	**F22** 06B	**F23** 073
D4 00F	**U9** 02A	**U10** 045	**D5** 010	**U11** 02B	**U12** 046	**D6** 011	**U13** 02C	**U14** 047		**H41** 064	**H42** 06C	**H43** 074
D7 012	**U15** 02D	**U16** 048	**D8** 013	**U17** 02E	**U18** 049	**D9** 014	**U19** 02F	**U20** 04A		**Z31** 065	**Z32** 06D	**Z33** 075
D10 015	**U21** 030	**U22** 04B	**D11** 016	**U23** 031	**U24** 04C	**D12** 017	**U25** 032	**U26** 04D		**Z41** 066	**Z42** 06E	**Z43** 076
Z11 018	**Z12** 033	**Z13** 04E	**Z21** 019	**Z22** 034	**Z23** 04F	**E2** 01A	**N5** 035	**N6** 050		**Z51** 067	**Z52** 06F	**Z53** 077

Note: The above addresses are read-only.

STM-1/STS-3/STS-3c Transmit Overhead RAM Locations

Transport (Section) Overhead										Path Overhead		
A1 140	**A1** 15B	**A1** 176	**A2** 141	**A2** 15C	**A2** 177	**C11** 142	**C12/N1** 15D	**C13/N2** 178		**J11** 1C0-1FF	**J12** 200-23F	**J13** 240-27F
B1 143	**M1** 15E	**M2** 179	**E1** 144	**M3** 15F	**U1** 17A	**F1** 145	**N3** 160	**N4** 17B		**B31** 1A8	**B32** 1B0	**B33** 1B8
D1 146	**M4** 161	**M5** 17C	**D2** 147	**M6** 162	**U2** 17D	**D3** 148	**U3** 163	**U4** 17E		**C21** 1A9	**C22** 1B1	**C23** 1B9
H11 149	**H12** 164	**H13** 17F	**H21** 14A	**H22** 165	**H23** 180	**H31** 14B	**H32** 166	**H33** 181		**G11** 1AA	**G12** 1B2	**G13** 1BA
B21 14C	**B22** 167	**B23** 182	**K1** 14D	**U5** 168	**U6** 183	**K2** 14E	**U7** 169	**U8** 184		**F21** 1AB	**F22** 1B3	**F23** 1BB
D4 14F	**U9** 16A	**U10** 185	**D5** 150	**U11** 16B	**U12** 186	**D6** 151	**U13** 16C	**U14** 187		**H41** 1AC	**H42** 1B4	**H43** 1BC
D7 152	**U15** 16D	**U16** 188	**D8** 153	**U17** 16E	**U18** 189	**D9** 154	**U19** 16F	**U20** 18A		**Z31** 1AD	**Z32** 1B5	**Z33** 1BD
D10 155	**U21** 170	**U22** 18B	**D11** 156	**U23** 171	**U24** 18C	**D12** 157	**U25** 172	**U26** 18D		**Z41** 1AE	**Z42** 1B6	**Z43** 1BE
Z11 158	**Z12** 173	**Z13** 18E	**Z21** 159	**Z22** 174	**Z23** 18F	**E2** 15A	**N5** 175	**N6** 190		**Z51** 1AF	**Z52** 1B7	**Z53** 1BF

Note: The above addresses are read-write, except when sourced by the TOH Access Port.

Control Bits

Address (Hex)	Mode*	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
3E0	R/W	EXDCOW	EXAPS	EXF1Z	EXUN	EXABH	TRPAIS	TRFERF	TRLAIS
3E1	R/W	RTLOOP	TAIS	CCITT	PTE1	PTE0	RING	VTAIS	TRLOOP
3E2	R/W	TLB	TCAT2	TCAT1	TCAT0	FLB	LCAT2	LCAT1	LCAT0
3E3	R/W	TRPTR	E12AIS	TRPYEL	FRENB	LM2AIS	SDVTAIS	FIFORST	Reserved

*Note: R = Read; W = Write; R/W = Read/Write.

Status Bits

Address (Hex)	Mode	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
3D0	R	RLOC	RLOS	ROOF	RLOF	RLAIS	RPAIS3	RPAIS2	RPAIS1
3D1	R/W(L)*	RLOC	RLOS	ROOF	RLOF	RLAIS	RPAIS3	RPAIS2	RPAIS1
3D2	R	RAPS	RLOP3	RLOP2	RLOP1	RFERF	RLOM3	RLOM2	RLOM1
3D3	R/W(L)	RAPS	RLOP3	RLOP2	RLOP1	RFERF	RLOM3	RLOM2	RLOM1
3D4	R	RNAPS	RYEL3	RYEL2	RYEL1	RFIFO	TFIFO	Unused	APNAPS
3D5	R/W(L)	RNAPS	RYEL3	RYEL2	RYEL1	RFIFO	TFIFO	Unused	APNAPS
3D6	R	Reserved	TLOC	TLOS	BERR	UPLOC	SDYEL3	SDYEL2	SDYEL1
3D7	R/W(L)	SINT	TLOC	TLOS	BERR	UPLOC	SDYEL3	SDYEL2	SDYEL1

*Note: L = latched. Latched Bits are cleared on read.

Interrupt Mask Bits

Address (Hex)	Mode	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
3F0	R/W	RLOC	RLOS	ROOF	RLOF	RLAIS	RPAIS3	RPAIS2	RPAIS1
3F1	R/W	RAPS	RLOP3	RLOP2	RLOP1	RFERF	RLOM3	RLOM2	RLOM1
3F2	R/W	RNAPS	RYEL3	RYEL2	RYEL1	RFIFO	TFIFO	Unused	APNAPS
3F3	R/W	HINT	TLOC	TLOS	BERR	UPLOC	SDYEL3	SDYEL2	SDYEL1

Pointer Justification Counters

INC Count	DEC Count	NDF Count
051 054 057	052 055 058	053 056 059

16-Bit Registers

B1 Count	B2 Count	B3 Count	Path FEBE Count	dbK1K2	dbK1K2AP	High Byte
192	194	198 19A 19C	19E 1A0 1A2	196	1A4	3FF

Note: Address listed is low order count byte or K1 byte (except for High Byte). The corresponding high order count byte or K2 byte is located in the next higher address, but is not to be accessed directly, only via the shared High Byte in location 3FF Hex.

DESCRIPTIONS OF OVERHEAD IN RAM

Receive Transport/Section Overhead Locations

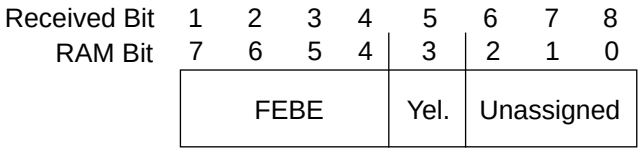
Address	Bit	Symbol	Description
000 01B 036	7-0	A1	**Framing Pattern:** Three A1 and A2 bytes are dedicated in each STM-1/ STS-3/STS-3c signal for framing. Each A1 framing pattern is equal to F6 Hex. The A1 bytes terminate in the SOT-3, without frame alignment performed, and are regenerated for the terminal side signal.
001 01C 037	7-0	A2	**Framing Pattern:** Three A1 and A2 bytes are dedicated in each STM-1/ STS-3/STS-3c signal for framing. Each A2 framing pattern is equal to 28 Hex. The A2 bytes terminate in the SOT-3, without frame alignment performed, and are regenerated for the terminal side signal.
002	7-0	C11	**STM-1/STS-1 Identifier:** The number in this location identifies the STM-1 position from the higher order demultiplexed signal. For an STS-3/STS-3c signal, this number represents the STS-1 No. 1 order of appearance in the higher order demultiplexed signal.
01D	7-0	C12/N1	**STS-1 Indication/National Use:** For an STM-1 signal, this byte is assigned for national use. For an STS-3/STS-3c signal, the number in this location represents the STS-1 No. 2 order of appearance in the higher order demultiplexed signal.
038	7-0	C13/N2	**STS-1 Indication/National Use:** For an STM-1 signal, this byte is assigned for national use. For an STS-3/STS-3c signal, the number in this location represents the STS-1 No. 3 order of appearance in the higher order demultiplexed signal.
003	7-0	B1	**B1 Error Indications:** The received B1 byte carries parity error indications when the SOT-3 is connected to a TranSwitch SYN155. Any ones in this byte indicate a Bit Interleaved Parity-8 (BIP-8) error in that particular bit location. The error indications (up to eight received per frame) are added to the 16-bit B1 counter (B1 Count, low order byte in location 192 Hex).
004	7-0	E1	**Orderwire Channel:** This channel provides a voice communication channel. For an STM-N signal, the orderwire channel is defined for STM-N No. 1. For an STS-N signal, the orderwire channel is defined for STS-1 No. 1.
005	7-0	F1	**User Channel:** This byte is reserved for user purposes. For an STM-N signal, the user channel is defined for the STM-1 No. 1. For an STS-N signal, the user channel is defined for STS-1 No. 1.
006 007 008	7-0	D1 D2 D3	**Section Data Communication Channel:** For an STM-N signal, the section data communication channel is defined for STM-1 No. 1. For an STS-3/STS-3c signal, these three bytes are allocated for section data communication, and are considered one 192 kbit/s message-based channel for alarms, maintenance, and other communication needs. They are defined for STS-1 No. 1.

Address	Bit	Symbol	Description
009 00A 00B	7-0	H11 H21 H31	**Payload Pointer and Action Byte:** The payload pointer carried in the H11 and H21 bytes indicates the location of the byte where the STM-1 AU-4, STS-1 No. 1 SPE and the STS-3c SPE begin. The H31 byte is used for frequency justification purposes. For an STM-1/STS-3c signal, this is the only pointer value that is tracked.
024 025 026	7-0	H12 H22 H32	**Payload Pointer and Action Byte:** The payload pointer carried in the H12 and H22 bytes indicates the location of the byte where the STS-1 No. 2 begins. The H32 byte is used for frequency justification purposes. For an STM-1 signal, the received H12, H22 value is 9BFFH. For an STS-3c signal, the received H12,H22 value is 93FFH.
03F 040 041	7-0	H13 H23 H33	**Payload Pointer and Action Byte:** The payload pointer carried in the H13 and H23 bytes indicates the location of the byte where the STS-1 No. 3 begins. The H33 byte is used for frequency justification purposes. For an STM-1 signal, the received H13, H23 value is 9BFFH. For an STS-3c signal, the received H13,H23 value is 93FFH.
00C 027 042	7-0	B21 B22 B23	**Line/Multiplexer BIP-24:** For an STM-1/STS-3/STS-3c signal, these three bytes are the received Bit Interleaved Parity-24 (BIP-24) value. B2 parity is checked by computing even parity over all bits of the frame, except for the first three rows of the section overhead bytes, and comparing the calculated value against the BIP-24 value received in the next frame. The number of errors detected (up to 24) is added to a single 16-bit counter (B2 Count, low order byte in location 194 Hex).
00D 00E	7-0	K1 K2	**Automatic Protection Switching Bytes:** Beside APS information, these bytes are also monitored for receive line AIS, receive line FERF, and protection switching byte failure and recovery. K1 and K2 values that persist for three or more frames are written to separate RAM locations (dbK2, location 196 Hex).
00F 010 011 012 013 014 015 016 017	7-0	D4 D5 D6 D7 D8 D9 D10 D11 D12	**Line Data Communication Channel:** For an STM-N signal, the line data communication channel is defined for STM-N No. 1. For an STS-3/STS-3c signal, these nine bytes are allocated for line data communication, and are considered one 576 kbit/s message-based channel for alarms, maintenance, and other communication needs. They are defined for STS-1 No. 1.
01A	7-0	E2	**Orderwire Channel:** This channel provides a voice communication channel. For an STM-N signal, the orderwire channel is defined for STM-N No. 1. For an STS-3/STS-3c signal, the orderwire channel is defined for STS-1 No. 1.
018 033 04E 019 034 04F	7-0	Z11 Z12 Z13 Z21 Z22 Z23	**Growth Bytes:** These six bytes are allocated for functions not yet fully defined.

Address	Bit	Symbol	Description
020 03B 035 050	7-0	N3 N4 N5 N6	**National Use:** These bytes are assigned for national use.
01E 039 01F 021 03C 022	7-0	M1 M2 M3 M4 M5 M6	**Media Specific Use.**
03A 03D 023 03E 028 043 029 044 02A 045 02B 046 02C 047 02D 048 02E 049 02F 04A 030 04B 031 04C 032 04D	7-0	U1 U2 U3 U4 U5 U6 U7 U8 U9 U10 U11 U12 U13 U14 U15 U16 U17 U18 U19 U20 U21 U22 U23 U24 U25 U26	**Unused bytes:** These bytes are not assigned in STM/STS signals but are still available in RAM.

STM-1/STS-3/STS-3c: STS-1 No.1 Receive Path Overhead RAM Locations

Address	Bit	Symbol	Description
080-0BF	7-0	J11	**Path Trace:** The path trace is a repetitive 64-byte fixed length message. The incoming message is stored in the RAM locations in a rotating fashion. There is no specified starting point, so any incoming J1 byte is written into the next sequential RAM location.

Address	Bit	Symbol	Description
060	7-0	B31	**Path BIP-8:** The value in this location is the received B3 parity byte. For error monitoring, parity is checked by computing even parity over all bits of the STM-1 AU-4 (261 columns), STS-1 SPE (87 columns), or STS-3c SPE (261 columns), and comparing the calculated value against the B31 value received in the next frame. Errors (up to eight per frame) are added to a 16-bit B31 counter (B3 Count, low order byte in location 198 Hex). The detection of B3 errors also causes a Far End Block Error (FEBE) to be sent when the transmitter is operating in a path terminating mode (bits 3 and 4 in location 3E1 Hex are set to 0, 1 or 1, 0).
061	7-0	C21	**Path Signal Label:** This byte indicates the construction of the AU-4 (STM) or SPE (STS).
062	7-0	G11	**Path Status:** This location provides the received FEBE indication, yellow (path FERF, path RDI) alarm status, and unassigned bit states as shown below:  The FEBE count (up to eight per frame) is added to a 16-bit FEBE counter (low order byte in location 19E Hex).
063	7-0	F21	**Path User Channel:** This byte provides user information between path elements.
064	7-0	H41	**Multiframe Indicator:** The SOT-3 supports floating VT mappings/multiframed TU. The multiframe indicator is carried in bits 0 and 1 (the 7th and 8th bits received) of the H4 byte, while the other bits (7-2) are set to one. The multiframe indication consists of a 00, 01,10,11 pattern repeating every 500 microseconds. The SOT-3 monitors the received H4 pattern for loss of multiframe. No correction is made to the H4 multiframe signal for the terminal side interface, except during VTAIS.
065 066 067	7-0	Z31 Z41 Z51	**Path Growth:** These three bytes are reserved for specific applications, or future growth.

STS-3: STS-1 No. 2 Receive Path Overhead RAM Locations (unused for STM-1/STS-3c)

Address	Bit	Symbol	**Description** (see also STS-1 No. above)
0C0- 0FF	7-0	J12	**Path Trace:** Repetitive 64-byte fixed length message which is stored in the RAM locations in a rotating fashion.
068	7-0	B32	**Path BIP-8:** Calculated BIP-8 errors (up to eight per frame) are added to the 16-bit B32 counter (low order byte in 19AH).
069	7-0	C22	**Path Signal Label.**

Address	Bit	Symbol	**Description** (see also STS-1 No. above)
06A	7-0	G12	**Path Status:** Provides the received FEBE indication and yellow alarm status as shown in G11 above. The FEBE count is added to the 16-bit FEBE counter (low order byte in 1A0H).
06B	7-0	F22	**Path User Channel.**
06C	7-0	H42	**Multiframe Indicator.**
06D 06E 06F	7-0	Z32 Z42 Z52	**Path Growth.**

STS-3: STS-1 No. 3 Receive Path Overhead RAM Locations (unused for STM-1/STS-3c)

Address	Bit	Symbol	**Description** (see also STS-1 No. 1 above)
100- 13F	7-0	J13	**Path Trace:** Repetitive 64-byte fixed length message which is stored in the RAM locations in a rotating fashion.
070	7-0	B33	**Path BIP-8:** Calculated BIP-8 errors (up to eight per frame) are added to the 16-bit B33 counter (low order byte in 19CH).
071	7-0	C23	**Path Signal Label.**
072	7-0	G13	**Path Status:** Provides the received FEBE indication and yellow alarm status as shown in G11 above. The FEBE count is added to the 16-bit FEBE counter (low order byte in 1A2H).
073	7-0	F23	**Path User Channel.**
074	7-0	H43	**Multiframe Indicator.**
075 076 077	7-0	Z33 Z43 Z53	**Path Growth.**

Transmit Transport/Section Overhead RAM Locations

Address	Bit	Symbol	Description
140 15B 176	7-0	A1	**Framing Pattern:** Three A1 and A2 bytes are dedicated in each STM-1/STS-3/STS-3c signal for framing. Each A1 framing pattern is equal to F6 Hex. The A1 bytes from the terminal terminate in the SOT-3, without frame alignment, and are regenerated for the line side signal. When bit 3 (EXABH) in 3E0H is set to zero the framing pattern is written from the TOH access port.
141 15C 177	7-0	A2	**Framing Pattern:** Three A1 and A2 bytes are dedicated in each STM-1/STS-3/STS-3c signal for framing. Each A2 framing pattern is equal to 28 Hex. The A2 bytes from the terminal terminate in the SOT-3, without frame alignment, and are regenerated for the line side signal. When bit 3 (EXABH) in 3E0H is set to zero the framing pattern is written from the TOH access port.
142	7-0	C11	**STM-1/STS-1 Identifier:** C11 identifies the STM-1 position in a higher order multiplexed signal. For an STS-3/STS-3c signal, C11 represents the STS-1 No. 1 order of appearance in the higher order multiplexed signal. Bit 4 (EXUN) in 3E0H controls whether this location is written by the microprocessor or the TOH Access Port.

Address	Bit	Symbol	Description
15D	7-0	C12/N1	**STS-1 Indication/National Use:** For an STM-1 signal, this byte is assigned for national use. For an STS-3/STS-3c signal, C12 represents the STS-1 No. 2 order of appearance in the higher order multiplexed signal. Bit 4 (EXUN) in 3E0H controls whether this location is written by the microprocessor or the TOH Access Port.
178	7-0	C13/N2	**STS-1 Indication/National Use:** For an STM-1 signal, this byte is assigned for national use. For an STS-3/STS-3c signal, C13 represents the STS-1 No. 3 order of appearance in the higher order multiplexed signal. Bit 4 (EXUN) in 3E0H controls whether this location is written by the microprocessor or the TOH Access Port.
143	7-0	B1	**B1 Error Insertion Mask:** These bits represent parity errors to be inserted into the B1 byte when the SOT-3 is connected to a TranSwitch SYN155 device. The error indications are generated by writing one or more ones corresponding to the columns in which the errors are to be generated. The transmitted B1 byte is exclusive-or gated with the calculated B1 byte prior to scrambling in the SYN155 device. The errors are sent until this location is set to 00H. Bit 3 (EXABH) in 3E0H controls whether this location is written by the microprocessor or the TOH Access Port.
144	7-0	E1	**Orderwire Channel:** E1 is part of the transmitted voice channel. Bit 7 (EXDCOW) in 3E0H controls whether this location is written by the microprocessor or the TOH Access Port.
145	7-0	F1	**User Channel:** F1 provides a user channel in an STM-1 or STS-3: STS-1 No. 1 signal. Bit 5 (EXF1Z) in 3E0H controls whether this location is written by the microprocessor or the TOH Access Port.
146 147 148	7-0	D1 D2 D3	**Section Data Communication Channel:** These three bytes are allocated for section data communication, and are considered one 192 kbit/s message-based channel for alarms, maintenance, and other communication needs. Bit 7 (EXDCOW) in 3E0H controls whether these locations are written by the microprocessor or the TOH Access Port.
149 14A 164 165 17F 180	7-0	H11 H21 H12 H22 H13 H23	**Payload Pointer Bytes:** The pointer bytes are normally recalculated and inserted directly into the transmit line data path. They can be inserted from the RAM by writing a one to bit 7 (TRPTR) in 3E3H. The value of the pointer bytes, when they are inserted from the RAM, has no effect on the location of the SPE. Bit 3 (EXABH) in 3E0H controls whether these locations are written by the microprocessor or the TOH Access Port. In STM-1/STS-3c mode the H12, H22, H13 and H23 bytes are automatically overwritten with the corresponding concatenation indicators, which are 9BFFH for STM-1 or 93FFH for STS-3 or STS-3c.
14B 166 181	7-0	H31 H32 H33	**Pointer Action Bytes:** The H3 bytes are normally set to 00H unless the internal retiming of the SOT-3 generates a decrement. The decrement causes the corresponding H3 byte to contain SPE data.
14C 167 182	7-0	B21 B22 B23	**B2 Error Insertion Mask:** B2 error indications are generated by writing ones in the columns in which the errors are to be generated. These three bytes are exclusive-or gated with the calculated B2 bytes prior to transmission. The errors are sent until each byte location is set to 00H. Bit 3 (EXABH) in 3E0H controls whether these locations are written by the microprocessor or the TOH Access Port.

Address	Bit	Symbol	Description
14D 14E	7-0	K1 K2	**Automatic Protection Switching Bytes:** Bit 6 (EXAPS) in 3E0H controls whether these locations are written by the microprocessor or the TOH Access Port.
14F 150 151 152 153 154 155 156 157	7-0	D4 D5 D6 D7 D8 D9 D10 D11 D12	**Line Data Communication Channel:** These nine bytes (D4 - D12) are allocated for line data communication, and are considered one 576 kbit/s message-based channel for alarms, maintenance, and other communication needs. Bit 7 (EXDCOW) in 3E0H controls whether these locations are written by the microprocessor or the TOH Access Port.
15A	7-0	E2	**Orderwire Channel:** E2 is part of the transmitted voice channel. Bit 7 (EXDCOW) in 3E0H controls whether this location is written by the microprocessor or the TOH Access Port.
158 173 18E 159 174 18F	7-0	Z11 Z12 Z13 Z21 Z22 Z23	**Growth Bytes:** Bit 5 (EXF1Z) in 3E0H controls whether these locations are written by the microprocessor or the TOH Access Port.
160 17B 175 190	7-0	N3 N4 N5 N6	**National Use:** Bit 4 (EXUN) in 3E0H controls whether these locations are written by the microprocessor or the TOH Access Port.
15E 179 15F 161 17C 162	7-0	M1 M2 M3 M4 M5 M6	**Media Specific Use:** Bit 4 (EXUN) in 3E0H controls whether these locations are written by the microprocessor or the TOH Access Port.

Address	Bit	Symbol	Description
17A 17D 163 17E 168 183 169 184 16A 185 16B 186 16C 187 16D 188 16E 189 16F 18A 170 18B 171 18C 172 18D	7-0	U1 U2 U3 U4 U5 U6 U7 U8 U9 U10 U11 U12 U13 U14 U15 U16 U17 U18 U19 U20 U21 U22 U23 U24 U25 U26	**Unused Bytes:** Bit 4 (EXUN) in 3E0H controls whether these locations are written by the microprocessor or the TOH Access Port.

STM-1/STS-3/STS-3c: STS-1 No. 1 Transmit Path Overhead RAM Locations

Address	Bit	Symbol	Description
1C0- 1FF	7-0	J11	**Path Trace:** The path trace is a repetitive 64-byte fixed length message that uses the J11 byte. The contents of this message are user-programmable and should be terminated with a CR/LF, and padded with ASCII NULL characters. NULL characters are normally substituted when no message is sent.
1A8	7-0	B31	**Path B3 Error Mask:** The bit locations set to one represent the columns in the B3 byte in which errors are generated. The three B3 bytes in the RAM are exclusive-or gated with the calculated B3 bytes prior to transmission. The errors are sent until these byte locations are set to 00H.
1A9	7-0	C21	**Path Signal Label:** The C2 byte is used to indicate the construction of the AU-4 (STM) or SPE (STS).

Address	Bit	Symbol	Description
1AA	7-0	G11	**Path Status:** The bit relationship between the transmitted G11 byte and this RAM location is shown below: Transmitted Bit 1 2 3 4 5 6 7 8 RAM Bit 7 6 5 4 3 2 1 0 FEBE | Yel. | Unassigned The transmitted FEBE count, and the state of the path yellow (path FERF, path RDI) alarm are determined by the alarm indication port input signals when the ring mode is enabled (bit 2 in 3E1H is a one) and from the receive line input when disabled. To prevent the possible loss of a FEBE count from the receiver because of clock differences, an internal synchronization circuit is used. When bit 3 of this location is written with a one, path yellow (FERF) will be transmitted until the bit is set to zero, regardless of the receive conditions.
1AB	7-0	F21	**Path User channel:** F2 provides user information between path elements.
1AC	7-0	H41	**Not Used:** The multiframe indicator must accompany the payload. The microprocessor can read/write this location.
1AD 1AE 1AF	7-0	Z31 Z41 Z51	**Path Growth:** These three bytes are reserved for specific applications, or future growth.

STS-3: STS-1 No. 2 Transmit Path Overhead RAM Locations (unused for STM-1/STS-3c)

Address	Bit	Symbol	**Description** (see also STS No. 1 above)
200- 23F	7-0	J12	**Path Trace:** Sixty-four RAM locations allocated for J12.
1B0	7-0	B32	**Path B3 Error Mask.**
1B1	7-0	C22	**Path Signal Label.**
1B2	7-0	G12	**Path Status:** Transmits the FEBE count and yellow alarm status as in G11 above.
1B3	7-0	F22	**Path User Channel.**
1B4	7-0	H42	**Not Used:** Microprocessor does have read/write access.
1B5 1B6 1B7	7-0	Z32 Z42 Z52	**Path Growth.**

STS-3: STS-1 No. 3 Transmit Path Overhead RAM Locations (unused for STM-1/STS-3c)

Address	Bit	Symbol	**Description** (see also STS No. 1 above)
240-27F	7-0	J13	**Path Trace:** Sixty-four RAM locations allocated for J13.
1B8	7-0	B33	**Path B3 Error Mask.**
1B9	7-0	C23	**Path Signal Label.**
1BA	7-0	G13	**Path Status:** Transmits the FEBE count and yellow alarm status as in G11 above.
1BB	7-0	F23	**Path User Channel.**
1BC	7-0	H43	**Not Used:** Microprocessor does have read/write access
1BD 1BE 1BF	7-0	Z33 Z43 Z53	**Path Growth.**

REGISTER DESCRIPTIONS

Control Register 0

Address (Hex)	Bit	Symbol	Description	
			Bit Equal to 1 (High)	Bit Equal to 0 (Low)
3E0	7	EXDCOW	**External Data Communications & Orderwire Byte Select:** Transmit TOH RAM locations for data communication bytes (D1-D12) and orderwire bytes (E1-E2) are written by the TOH Access Port once every 125 microseconds. See Notes 1, 2.	Transmit TOH RAM locations D1-D12 and E1-E2 are written by the microprocessor. See Note 2.
3E0	6	EXAPS	**External APS Byte Select:** Transmit TOH RAM locations for APS bytes (K1-K2) are written by the TOH Access Port once every 125 microseconds. See Notes 1, 2.	Transmit TOH RAM locations K1-K2 are written by the microprocessor. See Note 2.
3E0	5	EXF1Z	**External F1 & Z Byte Select:** Transmit TOH RAM locations for the F1 and six Z bytes are written by the TOH Access Port once every 125 microseconds. See Notes 1, 2.	Transmit TOH RAM locations for the F1 and six Z bytes are written by the microprocessor. See Note 2.
3E0	4	EXUN	**External Unused Byte Select:** Transmit TOH RAM locations for the C11, C12/N1, C13/N2 bytes and all M, N and U bytes are written by the TOH Access Port once every 125 microseconds (see the STM-1/STS-3/STS-3c Transmit Overhead RAM Locations table in the Operation section). See Notes 1, 2.	Transmit TOH RAM locations for the C11, C12/N1, C13/N2 bytes and all M, N and U bytes are written by the microprocessor. See Note 2.
3E0	3	EXABH	**External A1, A2, B1, B2, H1, H2 & H3 Byte Select:** Transmit TOH RAM locations for the A1, A2, B1, B2, H1, H2 and H3 bytes are written by the TOH Access Port once every 125 microseconds. H1 and H2 values will have no effect on the location of the transmitted payload. The microprocessor is not prohibited from writing to all the Transmit TOH RAM locations.	Transmit TOH RAM locations for the B1, B2, H1, H2 and H3 bytes are written by the microprocessor. See Note 2.

Note 1: The microprocessor is not prohibited from writing to these locations.

Note 2: If EXABH=0, the transmit TOH RAM locations for the A11, A12 and A13 bytes are written with F6H, and the locations for the A21, A22 and A23 bytes are written with 28H, once every 125 microseconds. The microprocessor is not prohibited from writing to these locations.

Address (Hex)	Bit	Symbol	Description	
			Bit Equal to 1 (High)	Bit Equal to 0 (Low)
3E0	2	TRPAIS	**Transmit Path AIS Enable:** Path AIS (all ones in the pointer bytes and the payload) is introduced into the transmit line signal on any of the following conditions: - A one in bit 6 (TAIS) of 3E1H - Transmit loss of signal (TLOS) - Transmit loss of clock (TLOC) - High signal at the TXAISn pin (AIS generated in STS-1 No. n) - A one in bit 6 (E12AIS) of 3E3H and a majority of ones received in the transmit terminal E1n byte (AIS generated in STS-1 No. n). See Note 1.	Introduction of path AIS into the transmit line signal is disabled.
3E0	1	TRFERF	**Transmit Line FERF (Line RDI) Mode Control:** Line Far End Receiver Failure (110 in transmitted bit 2-0 of K2) is introduced into the transmit line signal when: - There is a one in bit 2 (RING) of 3E1H and a send FERF indication at the transmit Alarm Indication Port, or - Ring mode is disabled and receive loss of signal, loss of frame, loss of clock or line AIS are detected (i.e., RLOS, RLOF, RLOC or RLAIS in locations 3D0H and 3D1H).	The K2 byte is multiplexed into the transmit line signal from the RAM without modification.
3E0	0	TRLAIS	**Transmit Line AIS Enable:** Line AIS (all ones signal, except for A1, A2, C1, B1, E1, F1, and D1-D4) is introduced into the transmit line signal on any of the following conditions: - A one in bit 6 (TAIS) of 3E1H - Transmit loss of signal (TLOS) - Transmit loss of clock (TLOC) - High signal at any TXAIS pin - A one in bit 6 (E12AIS) in 3E3H and a majority of ones received in the transmit terminal E11 byte. See Note above for TRPAIS	Introduction of line AIS into the transmit line signal is disabled.

Note 1: During a path AIS condition, the H1, H2 pointer bytes for the path are set to FFFFH. During a line AIS condition, all three H1, H2 byte pairs are set to FFFFH, overriding any individual path indications. When exit from a line and/or path condition causes an H1, H2 byte pair to leave the FFFFH state, then a New Data Flag (NDF=1001) is sent in byte H1 with the first new pointer (9NNNH) and a normal NDF (0110) is sent with subsequent repetitions of this new pointer (6NNNH), where the first pointer number nibble (N) includes the two SS-bits.

Control Register 1

Address (Hex)	Bit	Symbol	Description	
			Bit Equal to 1 (High)	Bit Equal to 0 (Low)
3E1	7	RTLOOP	**Receive-to-Transmit Loopback Enable:** Terminal loopback is enabled. Transmit terminal data input (TTDI) is disabled. The receive terminal data, clock, C1J1 and SPE signals are internally connected to the transmit terminal input. The receive terminal outputs are still active. Terminal loopback is not valid in data communication mode.	Terminal loopback is disabled.
3E1	6	TAIS	**Transmit AIS Control:** AIS is introduced into the transmit line signal conditional on bits 2 and 0 of location 3E0H (TRPAIS, TRLAIS).	Transmit AIS introduction is caused by alarm indications (see TRPAIS, TRLAIS, bits 2 and 0 of location 3E0H).
3E1	5	CCITT	**CCITT Mode Select:** Transmit line side SS-bits (5th and 6th transmitted bits of H1) are set to 10. Receive loss of pointer circuit expects to see 10 in SS-bits. See Note 1.	Transmit Line side SS-bits set to 00. Receive loss of pointer circuit ignores SS-bits.
3E1	4	PTE1	**Path Terminating Equipment Mode Controls:** PTE1 and PTE0 are used to control the path terminating mode on both the receive and transmit paths. If the receive side is path terminating, then path AIS or loss of multiframe (conditional on bit 3 (LM2AIS) in 3E3H) causes VTAIS at the terminal output. If the transmit side is not path terminated, all transmitted POH bytes are sourced externally, from the terminal input. The transmit side path terminating mode sources POH bytes from the RAM with several options available for the F2 and Z bytes and FEBE introduction.	
3E1	3	PTE0		

PTE(1-0)	Description
00	All TX POH bytes external, including the three B3 parity bytes. RX side not path terminated.
01	TX H4, F2, Z3, Z4 and Z5 bytes external. Path FEBE introduced by the SOT-3 device and the three B3 bytes are calculated by the SOT-3 device. RX side path terminated.
10	TX H4 external, other POH bytes from RAM. Path FEBE introduced by the SOT-3 device and the three B3 bytes are calculated by the SOT-3 device. RX side path terminated.
11	TX H4 external, path FEBE introduced by the microprocessor and the three B3 bytes are calculated by the SOT-3 device. RX side path terminated.

Note 1: The former CCITT organization is now known as ITU-T (see Standards Documentation Sources section).

Address (Hex)	Bit	Symbol	Description	
			Bit Equal to 1 (High)	Bit Equal to 0 (Low)
3E1	2	RING	**Protected Ring Mode Control:** Transmit line FEBE and FERF (line RDI) and path yellow (path RDI) indications are caused by the Alarm Indication Port.	Transmit line FEBE, FERF and path yellow indications are caused by the receive line input.
3E1	1	VTAIS	**Virtual Tributary AIS Mode Control:** Terminal side VTAIS (valid pointer, valid H4 multiframe indicator, and all ones in the payload bytes) is sent on any the following receive side conditions: - Loss of signal (RLOS) - Loss of clock (RLOC) - Loss of frame (RLOF) - Line AIS (RLAIS) - Loss of pointer (RLOPn) - Path AIS (RPAISn) and path terminated (see PTE1,PTE0) - Loss of multiframe (LOMn) and a one in bit 3 (LM2AIS) in 3E3H and path terminated - A one in bit 2 (SDVTAIS) of 3E3H	Introduction of terminal side VTAIS is disabled.
3E1	0	TRLOOP	**Transmit-to-Receive Loopback Enable:** Line side loopback is enabled. The receive line data input (RLDI) is disabled and the transmit line data, clock and frame signals are internally connected to the receive line inputs. The transmit line outputs are still active.	Line side loopback is disabled.

Control Register 2

Address (Hex)	Bit	Symbol	Description	
			Bit Equal to 1 (High)	Bit Equal to 0 (Low)
3E2	7	TLB	**Terminal Loopback Output Control:** Causes a high signal at the TLB pin.	Causes a low signal at the TLB pin.
3E2	6	TCAT2	**Terminal-Side Concatenation Mode Controls:** The following are valid states of the TCAT bits (see Note 1):	
3E2	5	TCAT1		
3E2	4	TCAT0		
3E2	3	FLB	**Facility Loopback Output Control:** Causes a high signal at the FLB pin.	Causes a low signal at the FLB pin.
3E2	2	LCAT2	**Line-Side Concatenation Mode Controls:** The following are valid states of the LCAT bits (see Note 1):	
3E2	1	LCAT1		
3E2	0	LCAT0		

Operating Mode	TCAT2	TCAT1	TCAT0
STM-1/STS-3c	1	1	0
STS-3	0	0	0

Operating Mode	LCAT2	LCAT1	LCAT0
STM-1/STS-3c	1	1	0
STS-3	0	0	0

Note 1: When setting the terminal in STS-3 mode (TCATn=000) and the line in STS-3c mode (LCATn=110) the incoming J1 bytes must be within four byte times of each other.

Control Register 3

Address (Hex)	Bit	Symbol	Description	
			Bit Equal to 1 (High)	Bit Equal to 0 (Low)
3E3	7	TRPTR	**Transmit Pointer Control:** Transmit line H1 and H2 bytes are multiplexed in from the RAM (written by the microprocessor or the TOH Access Port). H1 and H2 values have no effect on the location of the payload.	Transmit line H1 and H2 bytes are recalculated according to payload location and are inserted into the outgoing data path.
3E3	6	E12AIS	**E1-to-AIS Control Mode Select:** A majority of ones in the transmit terminal E1 byte(s) causes AIS to be introduced into the outgoing line signal, conditional on bits 2 and 0 (TRLAIS, TRPAIS) in 3E0H.	The transmit terminal E1 byte(s) has no effect on the introduction of transmit AIS.

Address (Hex)	Bit	Symbol	Description	
			Bit Equal to 1 (High)	Bit Equal to 0 (Low)
3E3	5	TRPYEL	**Transmit Path Yellow Control:** A yellow alarm (path RDI) condition [bit 3 (fifth bit transmitted) of G1 is a one] is inserted into the transmit line signals on any of the following conditions: -Loss of signal (RLOS) -Loss of clock (RLOC) -Loss of frame (RLOF) -Line AIS (RLAIS) -Loss of pointer (RLOPn) - Path AIS (RPAISn) and path terminated (see PTE1,PTE0) -Loss of multiframe (LOMn) and a one in bit 3 (LM2AIS) in 3E3H and path terminated.	A yellow alarm is only transmitted by writing a one to bit 3 of the G1 byte in RAM, and writing bits 3 and 4 (PTE0, PTE1) in location 3E1H to be not equal to 0, 0.
3E3	4	FRENB	**FIFO Reset Enable:** Transmit and receive FIFOs are automatically reset on underflow or overflow.	The FIFOs are not reset on underflow or overflow.
3E3	3	LM2AIS	**Receive-Loss-of-Multiframe-to-VTAIS Generation Control:** Terminal side VTAIS (valid pointer, valid H4 multiframe indicator, and all ones in the payload bytes) is generated on the detection of Loss of Multiframe (RLOMn) provided bit 1 (VTAIS) in 3E1H is a one and the receive side is path terminating (i.e., PTE1, PTE0 bits in 3E1H are not equal to 0, 0).	Receive Loss of Multiframe (RLOMn) has no effect on the generation of terminal side VTAIS.
3E3	2	SDVTAIS	**Send Terminal VTAIS Mode Control:** Terminal side VTAIS (valid pointer, valid H4 multiframe indicator, and all ones in the payload bytes) is generated if bit 1 (VTAIS) in 3E1H is a one.	Terminal side VTAIS is generated based on receive alarms (see VTAIS bit).
3E3	1	FIFORST	**FIFO Reset:** Resets both the transmit and receive FIFOs to an approximately half full condition. For test purposes only.	Transmit and receive FIFO function normally.
3E3	0	Reserved	Not valid.	This bit must be set to zero.

STATUS REGISTER DESCRIPTIONS

Status Register 0

Address (Hex) (Note 1)	Bit	Symbol	Name	Conditions	
				Enter	Exit
3D0, 3D1	7	RLOC	Receive Loss of Clock	No transitions on RLCI for 1,000 +/- 500ns.	Any transition on RLCI.
3D0, 3D1	6	RLOS	Receive Loss of Signal	A high signal on the RXLOS pin, or no data transitions on RLDI for 125µs and RXOOF pin is low. See Note 2.	RXLOS pin is low and any transition on RLDI.
3D0, 3D1	5	ROOF	Receive Out of Frame	A high signal on the RXOOF pin.	A low signal on the RXOOF pin.
3D0, 3D1	4	RLOF	Receive Loss of Frame	A high signal on the RXLOF pin.	A low signal on the RXLOF pin.
3D0, 3D1	3	RLAIS	Receive Line AIS	Bits 2,1 and 0 (received bits 6,7 and 8) of receive line K2 are all ones for five consecutive frames.	Bits 2-0 of receive line K2 are not all ones for five consecutive frames.
3D0, 3D1	2	RPAIS3	Receive Path AIS (STS-3:STS-1 No. 3)	Receive line H13-H23 bytes are FFFFH for three consecutive frames.	Valid new data flag in receive line H13-H23 or a valid pointer for three consecutive frames.
3D0, 3D1	1	RPAIS2	Receive Path AIS (STS-3:STS-1 No. 2)	Receive line H12-H22 bytes are FFFFH for three consecutive frames.	Valid new data flag in receive line H12-H22 or a valid pointer for three consecutive frames.
3D0, 3D1	0	RPAIS1	Receive Path AIS (STM-1, STS-3c or STS-3:STS-1 No. 1)	Receive line H11-H21 bytes are FFFFH for three consecutive frames.	Valid new data flag in receive line H11-H21 or a valid pointer for three consecutive frames.

Note 1: For all status registers, even addresses are unlatched bits and odd addresses are latched bits. Latched bits are cleared on read.

Note 2: This behavior implies that RLOS being high does not always indicate an SDH/SONET loss of signal alarm.

Status Register 1

Address (Hex)	Bit	Symbol	Name	Conditions	
				Enter	Exit
3D2, 3D3	7	RAPS	Receive APS failure	In a period of 12 frames, no three consecutive frames contain identical receive line K1-K2 bytes.	Identical receive line K1-K2 bytes are received for three consecutive frames.
3D2, 3D3	6	RLOP3	Receive Loss of Pointer (STS-3:STS-1 No. 3)	For eight consecutive frames, the receive line H13-H23 bytes contain a new data flag or an invalid pointer. Refer to Note 1.	Receive line H13-H23 has a valid pointer for three consecutive frames, or a one in bit 2 (LCAT2) in 3E2H.
3D2, 3D3	5	RLOP2	Receive Loss of Pointer (STS-3:STS-1 No. 2)	For eight consecutive frames, the receive line H12-H22 bytes contain a new data flag or an invalid pointer. Refer to Note 1.	Receive line H12-H22 has a valid pointer for three consecutive frames, or a one in bit 1 (LCAT1) in 3E2H.
3D2, 3D3	4	RLOP1	Receive Loss of Pointer (STM-1, STS-3c or STS-3:STS-1 No. 1)	For eight consecutive frames, the receive line H11-H21 bytes contain a new data flag or an invalid pointer. Refer to Note 1. The pointer is also invalid if bit 5 (CCITT) in 3E1H is a one and the SS-bits (5th and 6th bits of H11) are not equal to 10.	Receive line H11-H21 has a valid pointer for three consecutive frames.
3D2, 3D3	3	RFERF	Receive Far End Receiver Failure	Bits 2-0 (receive bits 6-8) of the receive line K2 byte are equal to 110 for five consecutive frames.	Bits 2-0 of the receive line K2 byte are not equal to 110 for five consecutive frames.
3D2, 3D3	2	RLOM3	Receive Loss of Multi-frame (H4) (STS-3:STS-1 No.3)	Bits 1-0 (received bits 7-8) of the receive line H43 byte are not equal to the previous bits 1-0 of H43 plus one (modulo 4) for four consecutive frames.	Bits 1-0 of the receive line H43 byte are received in the order 00,01,10,11 for four consecutive frames.
3D2, 3D3	1	RLOM2	Receive Loss of Multi-frame (H4) (STS-3:STS-1 No. 2)	Bits 1-0 (received bits 7-8) of the receive line H42 byte are not equal to the previous bits 1-0 of H42 plus one (modulo 4) for four consecutive frames.	Bits 1-0 of the receive line H42 byte are received in the order 00,01,10,11 for four consecutive frames.

Note 1: NDF is reported for the following values: 1001 (the specified value for a New Data Flag) and the following single bit error values: 1000, 0001, 1101, 1011. All other values are not NDFs and are processed as normal pointer values.

Address (Hex)	Bit	Symbol	Name	Conditions	
				Enter	Exit
3D2, 3D3	0	RLOM1	Receive Loss of Multi-frame (H4) (STM-1, STS-3c or STS-3:STS-1 No 1)	Bits 1-0 (received bits 7-8) of the receive line H41 byte are not equal to the previous bits 1-0 of H41 plus one (modulo 4) for four consecutive frames.	Bits 1-0 of the receive line H41 byte are received in the order 00,01,10,11 for four consecutive frames.

Status Register 2

Address (Hex)	Bit	Symbol	Name	Conditions	
				Enter	Exit
3D4, 3D5	7	RNAPS	Receive New APS bytes	A new value is detected in three consecutive frames for the receive line K1-K2 bytes.	Receive line K1-K2 bytes unchanged for more than three frames or no value persisting for three frames.
3D4, 3D5	6	RYEL3	Receive Yellow (STS-3:STS-1 No. 3)	Bit 3 (received bit 5) of the receive line G13 byte is a one for 10 consecutive frames.	Bit 3 of the receive line G13 byte is a zero for 10 consecutive frames.
3D4, 3D5	5	RYEL2	Receive Yellow (STS-3:STS-1 No. 2)	Bit 3 (received bit 5) of the receive line G12 byte is a one for 10 consecutive frames.	Bit 3 of the receive line G12 byte is a zero for 10 consecutive frames.
3D4, 3D5	4	RYEL1	Receive Yellow (STM-1, STS-3c or STS-3:STS-1 No. 1)	Bit 3 (received bit 5) of the receive line G11 byte is a one for 10 consecutive frames.	Bit 3 of the receive line G11 byte is a zero for 10 consecutive frames.
3D4, 3D5	3	RFIFO	Receive FIFO error	Overflow or underflow condition in the receive side FIFO. Also FIFO misalignment if STM-1/ STS-3c mode is selected.	No error condition exists in the receive FIFO.
3D4, 3D5	2	TFIFO	Transmit FIFO error	Overflow or underflow condition in the transmit side FIFO. Also FIFO misalignment if STM-1/ STS-3c mode is selected.	No error condition exists in the transmit FIFO.
3D4, 3D5	1	Unused			
3D4, 3D5	0	APNAPS	New APS byte from Alarm Indication Port	A high signal received over the Alarm Indication Port in the position used for new APS indication.	A low signal received over the Alarm Indication Port in the position used for new APS indication.

Status Register 3

Address (Hex)	Bit	Symbol	Name	Conditions	
				Enter	Exit
3D6	7	Reserved			
3D7	7	SINT	Software Interrupt	One or more ones in the interrupt mask locations and a corresponding alarm is detected.	A µP read and the alarm causing the interrupt clears, or its corresponding bit in the interrupt mask is set to zero.
3D6, 3D7	6	TLOC	Transmit Loss of Clock	No transitions on TTCI pin for 1,000 +/- 500ns.	Any transition on TTCI.
3D6, 3D7	5	TLOS	Transmit Loss of Signal	No transitions on TTDI for 125 µs.	Any transition on TTDI.
3D6, 3D7	4	BERR	Bus Parity Error (Transmit Terminal Input)	Internally generated odd parity, calculated over TTDI, TSPE and TC1J1, does not match terminal parity input pin (TPAR).	Internally generated parity matches input parity.
3D6, 3D7	3	UPLOC	µP Loss of Clock	No transitions on RAMCI pin for 1,000 +/- 500ns.	Any transition on RAMCI.
3D6, 3D7	2	SDYEL3	Send Path Yellow (STS-3:STS-1 No. 3)	A high signal at the Alarm Indication Port (TAIDI pin) in the position for Send Yellow (3). This indicates that the mate SOT-3 has detected one of the seven alarm conditions listed for TRPYEL, bit 5 in 3E3H.	A low at the Alarm Indication Port in the position for Send Yellow (3).
3D6, 3D7	1	SDYEL2	Send Path Yellow (STS-3:STS-1 No. 2)	A high signal at the Alarm Indication Port (TAIDI pin) in the position for Send Yellow (2). This indicates that the mate SOT-3 has detected one of the seven alarm conditions listed for TRPYEL, bit 5 in 3E3H.	A low at the Alarm Indication Port in the position for Send Yellow (2).
3D6, 3D7	0	SDYEL1	Send Path Yellow (STM-1, STS-3c or STS-3:STS-1 No. 1)	A high signal at the Alarm Indication Port (TAIDI pin) in the position for Send Yellow (1). This indicates that the mate SOT-3 has detected one of the seven alarm conditions listed for TRPYEL, bit 5 in 3E3H.	A low at the Alarm Indication Port in the position for Send Yellow (1).

POINTER JUSTIFICATION COUNTER DESCRIPTIONS

Address	Bit	Symbol	**Description** (Note 1)
051 054 057	7-0	INC Count	**Positive Justification (INC) Counters:** Each RAM location is an eight-bit counter which counts the number of positive (increment) pointer movements in the receive line input. Location 051H counts INCs in the STM-1/STS-3/STS-3c: STS-1 No. 1 signal. Location 054H counts INCs in STS-1 No. 2, and 057H is for STS-1 No. 3. Bit 0 is the least significant bit in the counters. Each counter is frozen during the following associated alarm conditions: RLOC, RLOS, RLOF, RLAIS, RLOP, and RPAIS.
052 055 058	7-0	DEC Count	**Negative Justification (DEC) Counters:** Each RAM location is an eight-bit counter which counts the number of negative (decrement) pointer movements in the receive line input. Location 052H counts DECs in the STM-1/STS-3/STS-3c: STS-1 No. 1 signal. Location 055H counts DECs in STS-1 No. 2, and 058H is for STS-1 No. 3. Bit 0 is the least significant bit in the counters. Each counter is frozen during the following associated alarm conditions: RLOC, RLOS, RLOF, RLAIS, RLOP, and RPAIS.
053 056 059	7-0	NDF Count	**New Data Flag (NDF) Counters:** Each RAM location is an eight-bit counter which counts the number of NDFs (received bits 1-4 of H1) in the receive line input. Refer to Note 2. Location 053H counts NDFs in the STM-1/STS-3/STS-3c: STS-1 No. 1 signal. Location 056H counts NDFs in STS-1 No. 2, and 059H is for STS-1 No.3. Bit 0 is the least significant bit. Each counter is frozen during the following associated alarm conditions: RLOC, RLOS, RLOF, RLAIS, RLOP, and RPAIS.

Note 1: These are non-saturating counters that are set to FEH during SOT-3 reset (pin 142) and are not reset on read.

Note 2: NDF is reported for the following values: 1001 (the specified value for a New Data Flag) and the following single bit error values: 1000, 0001, 1101, 1011. All other values are not NDFs and are processed as normal pointer values.

16-BIT REGISTER DESCRIPTIONS

Address*	Bit	Symbol	Description
192	7-0	B1 Count	**B1 Error Counter:** This 16-bit counter is updated from the error indications received in the B1 byte of the receive line signal from the SYN155 device. Errors are represented by a one in one or more columns of the byte, with up to eight error indications per frame. The high order byte is copied into location 3FFH when the low order byte is read from 192H. Bit 0 is the least significant bit in the byte. This counter is frozen during the following alarm conditions: RLOC, RLOS, and RLOF.
194	7-0	B2 Count	**B2 Error Counter:** This 16-bit counter counts the number of error indications that occur when the incoming B2 bytes in the receive line signal and the three calculated values do not match. The high order byte is copied into location 3FFH when the low order byte is read from 194H. Bit 0 is the least significant bit in the counter. This counter is frozen during the following alarm conditions: RLOC, RLOS, RLOF and RLAIS.
198 19A 19C	7-0	B3 Count	**B3 Error Counters:** These three 16-bit counters count the number of B31, B32 and B33 error indications that occur when the incoming B3 bytes of the receive line signal and the three calculated values do not match. Location 198H counts B3 errors in the STM-1/STS-3/STS-3c: STS-1 No. 1 SPE. Location 19A counts B3 errors in the STS-1 No. 2 SPE, and 19C is for STS-1 No. 3. Bit 0 is the least significant bit in each of the three counters. The high order byte is copied into location 3FFH when the respective low order byte is read. Each counter is frozen during the following associated alarm conditions: RLOC, RLOS, RLOF, RLAIS, RLOP, and RPAIS.
19E 1A0 1A2	7-0	FEBE Count	**FEBE Counters:** These three 16-bit counters count the number of G11, G12 and G13 FEBE indications in the incoming G1 byte (received bits 1-4) of the receive line input. Location 19E counts the FEBEs from the STM-1/STS-3/STS-3c: STS-1 No. 1 G11 byte. Location 1A0 counts the FEBEs from STS-1 No. 2 G12 byte, and 1A2 is for STS-1 No. 3 G13 byte. Bit 0 is the least significant bit in each of the three counters. The high order byte is copied into location 3FFH when the respective low order byte is read. Each counter is frozen during the following associated alarm conditions: RLOC, RLOS, RLOF, RLAIS, RLOP, and RPAIS.
196	7-0	dbK1K2	**Received Debounced K1-K2 Bytes:** After a new K1-K2 value is received at the receive line input for three consecutive frames, a debounce indication occurs (RNAPS) and the new persistent K1 and K2 bytes are stored. When the debounced K1 value is read from 196H, the debounced K2 value is copied into location 3FFH.
1A4	7-0	dbK1-K2AP	**Debounced K1-K2 Bytes From Alarm Indication Port:** After a new K1-K2 value is received at the mate SOT-3 for three consecutive frames, a debounce indication is sent over the Alarm Indication Port (APNAPS) along with the new K1-K2 bytes. The debounced K1-K2 continues to be sent until a new persistent value is detected. When the debounced K1 value is read from 1A4H, the debounced K2 value is copied into location 3FFH.
3FF	7-0	High Byte	**Shared High Byte:** This RAM location is used on a shared basis for the high byte in a 16-bit read operation. The B1, B2, B3 and FEBE counters, and the debounced K1-K2 values from both the receive side and the Alarm Indication Port, are accessed with 16-bit reads using this location for access to the high order byte.

* Note: The above 16-bit counters are non-saturating, are set to FFE0H during SOT-3 reset (pin 142) and do not reset on read. The address listed is the low order byte (except 3FF Hex).

PACKAGE INFORMATION

The SOT-3 device is packaged in a 160-pin plastic quad flat package suitable for socket or surface mounting. All linear dimensions shown are in millimeters and are nominal unless otherwise indicated.

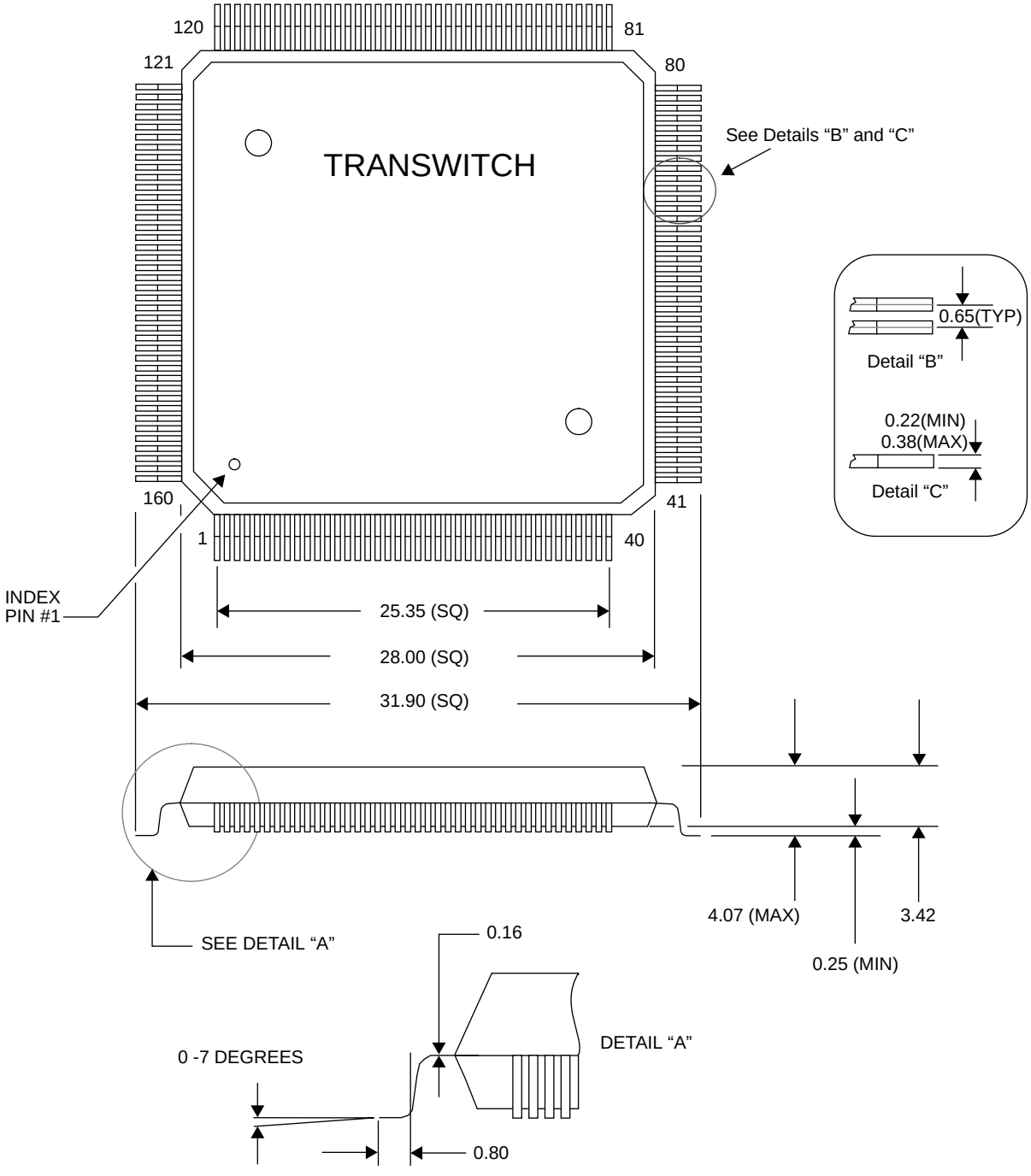


Figure 18. SOT-3 160-Pin Plastic Quad Flat Package

ORDERING INFORMATION

Part Number: TXC-03003-AIPQ	160-Pin Plastic Quad Flat Pack

RELATED PRODUCTS

TXC-02301B, SYN155 VLSI Device (155-Mbit/s Synchronizer, Data Output). Provides complete STS-3/STM-1 frame synchronization on incoming 155 Mbit/s signals in a single low power CMOS unit.

TXC-02302B, SYN155C VLSI Device (155-Mbit/s Synchronizer, Clock and Data Output). This device is similar to the SYN155. It has both clock and data outputs on the line side.

TXC-04002, ADMA-E1 VLSI Device (2 Mbit/s to TU-12 Async Mapper-Desync). Designed for add/drop multiplexer, terminal multiplexer, and dual and single unidirectional ring applications. Connects with the SOT-3 to form an STM-1 add/drop or terminal system.

TXC-21061, SOT-3/SYN155/ADMA-E1 Evaluation Board. A complete, ready-to-use single board test system that demonstrates the functions and features of the ADMA-E1, SOT-3, and SYN155 VLSI devices. Includes on-board microprocessor, RS-232 interface, and MS-DOS compatible PC software. The PC software provides full access to the ADMA-E1 and SOT-3 devices for control and monitoring.

TXC-05501, SARA-S VLSI Device (ATM/SMDS Segmentation Controller). Simultaneously segments up to 8000 packets into ATM/SMDS cells.

TXC-05601, SARA-R VLSI Device (ATM/SMDS Reassembly Controller). Simultaneously reassembles ATM/SMDS cells back into up to 8000 packets.

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute (ANSI)
11 West 42nd Street
New York, New York 10036

Tel: 212-642-4900
Fax: 212-302-1286

Bellcore (U.S.A.):

Bellcore
Attention - Customer Relations
8 Corporate Place, RM 184A
Piscataway, NJ 08854-4156

Tel: 800-521-2673 (In U.S.A. or Canada only)
Tel: 908-699-5800
Fax: 908-336-2559 or 908-336-2692

ITU-T (International):

Publication Services of International Telecommunication Union (ITU)
Telecommunication Standardization Bureau (T)
Contact: ITU Sales Service Department
Place des Nations
CH 1211
Geneve 20, Switzerland

Tel: 41-22-730-5285 or 41-22-730-5111
Fax: 41-22-730-5194

TTC (Japan):

TTC Standard Publishing Group of the
Telecommunications Technology Committee
2nd Floor, Hamamatsucho - Suzuki Building,
1 2-11, Hamamatsu-cho, Minato-ku, Tokyo

Tel: 81-3-3432-1551
Fax: 81-3-3432-1553

LIST OF DATA SHEET CHANGES

This change list identifies those areas within this updated SOT-3 Data Sheet that have technical differences relative to the superseded SOT-3 Data Sheet:

Updated SOT-3 Data Sheet: Edition 4, March 1995

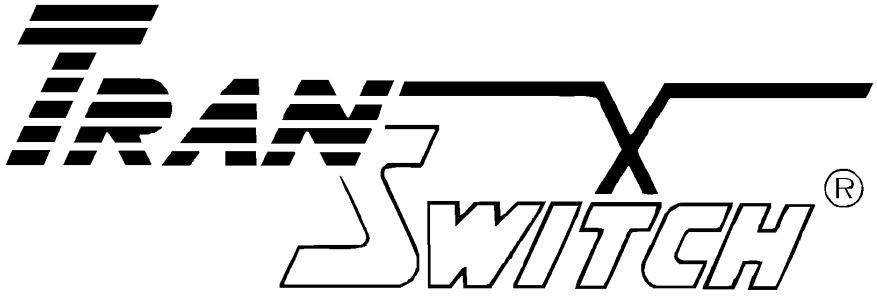
Superseded SOT-3 Data Sheet: Edition 3, July 1993

The page numbers indicated below of this updated data sheet include changes relative to the superseded data sheet.

Page Number of Updated Data Sheet	Summary of the Change
1	Changed edition number and date.
1	Made changes to items 1, 3, 4, 5 and 9 of Feature List.
1	Modified Description section.
1	Modified figure.
2-65	Added edition number and date.
2	Added Table of Contents and List of Figures.
3	Modified Figure 1.
3-4	Modified Block Diagram Description section.
5	Changed all the SPARE pins to NC pins and changed pin 57 from $\overline{RD}$ to $\overline{RD}$ or RD/$\overline{WR}$.
6-15	Modified Pin Descriptions section.
16	Changed Min for Symbol T_S and the note.
19	Added Input/Output Parameters For TTL2mA table.
20-21	Modified the figures.
22	Modified Figure 5 and added Typ to $t_{PW(2)}$ of the table.
23	Modified Figure 6, the table and the note.
24	Modified Figure 7 and the associated table.
25	Modified Figure 8 and the associated table.
26-27	Modified the figures and Parameter column for $t_{PWL(1)}$.
28	Modified Figure 11 and the second note.
29-31	Modified the figures, the table and the notes.

Page Number of Updated Data Sheet	Summary of the Change
32-33	Modified the figures and the tables.
34-61	Modified Operation section.
62	Modified Package Information section.
64	Added Standards Documentation Sources.
65-66	Added List of Data Sheet Changes.
69	Added Documentation Update Registration Form.

- NOTES -



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