256Mbit GDDR SDRAM

Revision 1.3
April 2007

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Revision History

Revision	Month	Year	History
0.0	July	2005	- Target Spec - Defined Target Specification
0.1	September	2005	- Preliminary Spec
0.2	November	2005	- Changed CL from 4clk to 3clk of -LC40 - Added current spec - Added IBIS data
1.0	January	2006	- Final Spec - Deleted -LC33/36/60 spec.
1.1	April	2006	- Deleted CL4 option in MRS table according to deleting high frequency bin(-LC33/36).
1.2	April	2006	- Added CL2.5 option(-LC50 can support 166MHz@CL 2.5) - Changed VDD(min) spec from 2.5V to 2.35V.
1.3	April	2007	- Corrected typo on page 14.

4M x 16Bit x 4 Banks Graphic Double Data Rate Synchronous DRAM with Bi-directional Data Strobe and DLL

1.0 FEATURES

- 2.35V ~ 2.7V power supply for device operation
- 2.35V ~ 2.7V power supply for I/O interface
- SSTL_2 compatible inputs/outputs
- 4 banks operation
- MRS cycle with address key programs
  - -. Read latency 2.5, 3 (clock)
  - -. Burst length (2, 4 and 8)
  - -. Burst type (sequential & interleave)
- All inputs except data & DM are sampled at the positive going edge of the system clock
- Differential clock input
- No Write-Interrupted by Read Function
  (WIR function can be supported only for 200/166MHz)
- 2 DQS's (1DQS / Byte)
- Data I/O transactions on both edges of Data strobe
- DLL aligns DQ and DQS transitions with Clock transition
- Edge aligned data & data strobe output
- Center aligned data & data strobe input
- DM for write masking only
- Auto & Self refresh
- 64ms refresh period (8K cycle)
- 66pin TSOP-II lead free package(RoHS Compliant)
- Maximum clock frequency up to250MHz
- Maximum data rate up to 500Mbps/pin

2.0 ORDERING INFORMATION

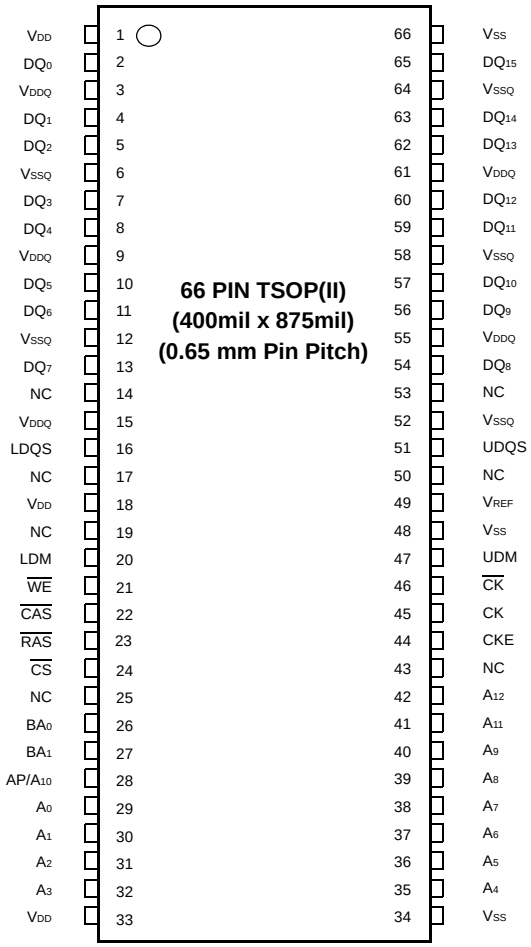
Part NO.	Max Freq.	Max Data Rate	Interface	VDD & VDDQ	Package
K4D551638H-LC40	250MHz	500Mbps/pin	SSTL_2	2.35V ~ 2.7V	66pin TSOP-II
K4D551638H-LC50	200MHz	400Mbps/pin			

3.0 GENERAL DESCRIPTION

FOR 4M x 16Bit x 4 Bank GDDR SDRAM

The K4D551638H is 268,435,456 bits of hyper synchronous data rate Dynamic RAM organized as 4 x 4,194,304 words by 16 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous features with Data Strobe allow extremely high performance up to 1.1GB/s/chip. I/O transactions are possible on both edges of the clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the device to be useful for a variety of high performance memory system applications.

4.0 PIN CONFIGURATION (Top View)



PIN DESCRIPTION

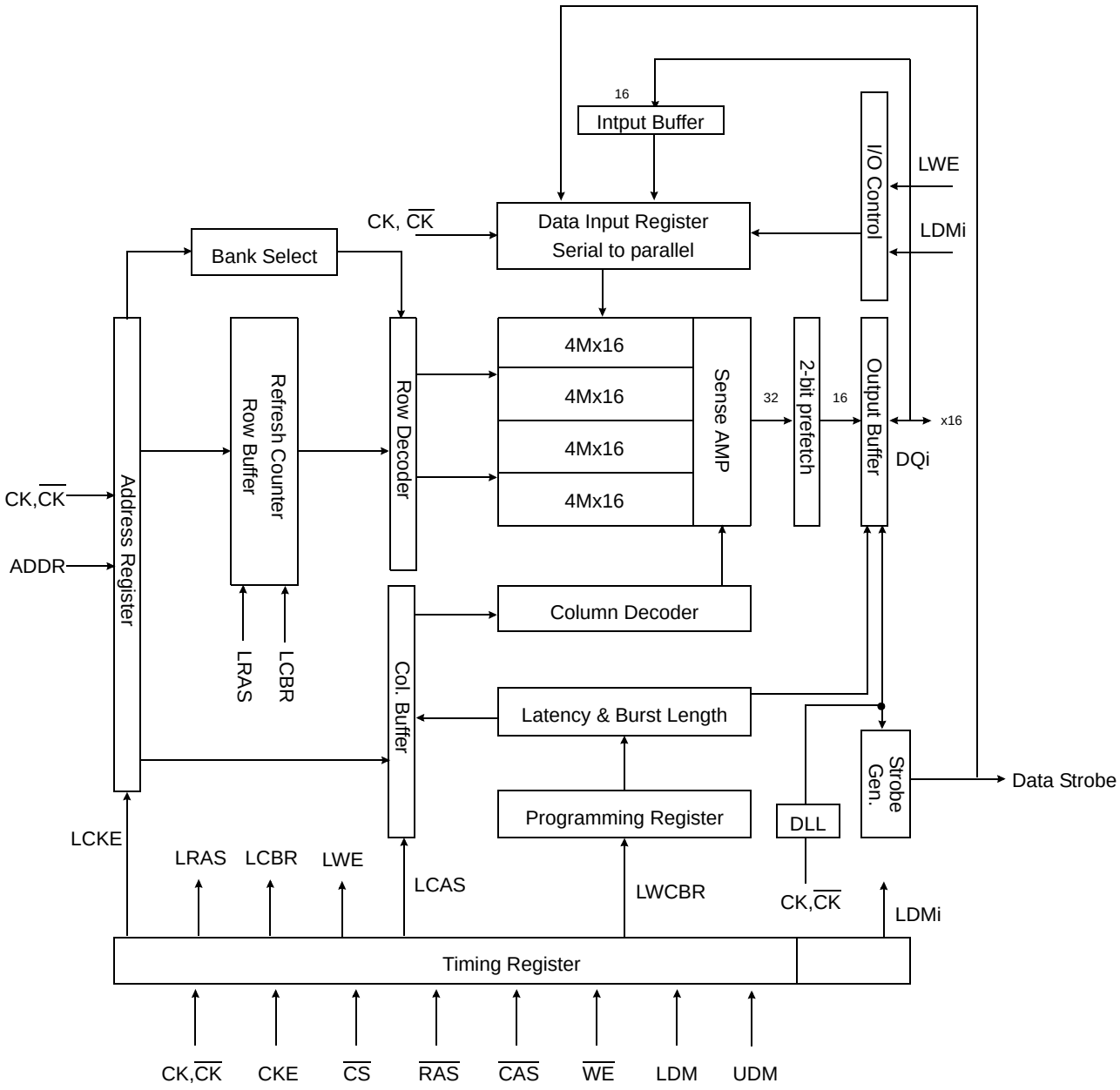
CK,$\overline{CK}$	Differential Clock Input	BA_0, BA_1	Bank Select Address
CKE	Clock Enable	A_0 ~A_{12}	Address Input
$\overline{CS}$	Chip Select	DQ_0 ~ DQ_{15}	Data Input/Output
$\overline{RAS}$	Row Address Strobe	V_{DD}	Power
$\overline{CAS}$	Column Address Strobe	V_{SS}	Ground
$\overline{WE}$	Write Enable	V_{DDQ}	Power for DQ's
L(U)DQS	Data Strobe	V_{SSQ}	Ground for DQ's
L(U)DM	Data Mask	NC	No Connection
RFU	Reserved for Future Use	VREF	Reference voltage

5.0 INPUT/OUTPUT FUNCTIONAL DESCRIPTION

Symbol	Type	Function
CK, $\overline{CK}$*1	Input	The differential system clock Input. All of the inputs are sampled on the rising edge of the clock except DQ's and DM's that are sampled on both edges of the DQS.
CKE	Input	Activates the CK signal when high and deactivates the $\overline{CK}$ signal when low. By deactivating the clock, CKE low indicates the Power down mode or Self refresh mode.CKE is synchronous for Power down entry and exit, and for Self refresh entry. CKE is asynchronous for Self refresh exit, and for output disable. CKE must be maintained high through Read and Write accesses. Input buffers, excluding CK, $\overline{CK}$ and CKE are disbled during Power down. Input buffers, excluding CKE are disabled during Self refresh. CKE is an SSTL_2 input, but will detect a LVCMOS low level after Vdd is applied upon 1st power up. After Vref has become stable during the power on and intialization sequence, it must be maintained for proper operation of the CKE receiver. For proper Self refresh entry and exit, Vref must be maintained to this input.
$\overline{CS}$	Input	$\overline{CS}$ enables the command decoder when low and disabled the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$	Input	Latches row addresses on the positive going edge of the CK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	Input	Latches column addresses on the positive going edge of the CK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	Input	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
LDQS,UDQS	Input/Output	Data input and output are synchronized with both edge of DQS. For the x16, LDQS corresponds to the data on DQ0-DQ7 ; UDQS corresponds to the data on DQ8-DQ15.
LDM,UDM	Input	Data in Mask. Data In is masked by DM Latency=0 when DM is high in burst write. For the x16, LDM corresponds to the data on DQ0-DQ7 ; UDM correspons to the data on DQ8-DQ15.
DQ0 ~ DQ15	Input/Output	Data inputs/Outputs are multiplexed on the same pins.
BA0, BA1	Input	Selects which bank is to be active.
A0 ~ A12	Input	Row/Column addresses are multiplexed on the same pins. Row addresses : RA0 ~ RA12, Column addresses : CA0 ~ CA8.
V_{DD}/V_{SS}	Power Supply	Power and ground for the input buffers and core logic.
V_{DDQ}/V_{SSQ}	Power Supply	Isolated power supply and ground for the output buffers to provide improved noise immunity.
V_{REF}	Power Supply	Reference voltage for inputs, used for SSTL interface.
NC/RFU	No connection/ Reserved for future use	This pin is recommended to be left "No connection" on the device

*1 : The timing reference point for the differential clocking is the cross point of CK and $\overline{CK}$.
For any applications using the single ended clocking, apply V_{REF} to $\overline{CK}$ pin.

6.0 BLOCK DIAGRAM (4Mbit x 16I/O x 4 Bank)



7.0 FUNCTIONAL DESCRIPTION

7.1 Power-Up Sequence

DDR SDRAMs must be powered up and initialized in a predefined manner to prevent undefined operations.

1. Apply power and keep CKE at low state (All other inputs may be undefined)
   - Apply V_{DD} before V_{DDQ} .
   - Apply V_{DDQ} before V_{REF} & V_{TT}
2. Start clock and maintain stable condition for minimum 200us.
3. The minimum of 200us after stable power and clock(CK,$\overline{CK}$), apply NOP and take CKE to be high .
4. Issue precharge command for all banks of the device.
5. Issue a EMRS command to enable DLL

*1 6. Issue a MRS command to reset DLL. The additional 200 clock cycles are required to lock the DLL.

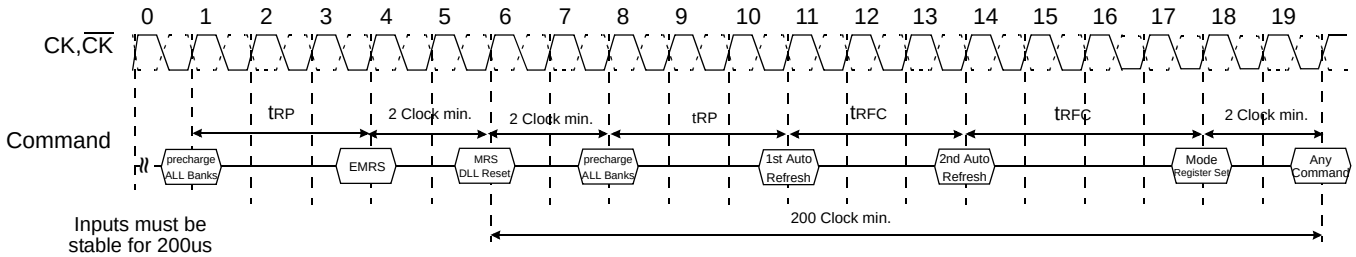
*1,2 7. Issue precharge command for all banks of the device.

8. Issue at least 2 or more auto-refresh commands.
9. Issue a mode register set command with A8 to low to initialize the mode register.

*1 The additional 200cycles of clock input is required to lock the DLL after enabling DLL.

*2 Sequence of 6&7 is regardless of the order.

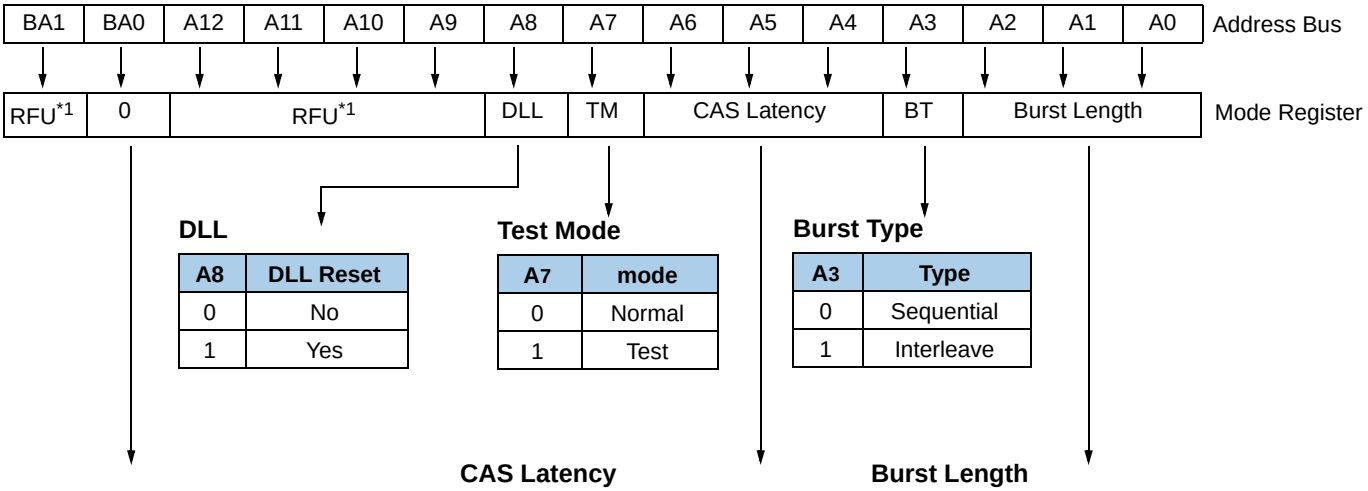
Power up & Initialization Sequence



*** When the operating frequency is changed, DLL reset should be required again.**
After DLL reset again, the minimum 200 cycles of clock input is needed to lock the DLL.

7.2 MODE REGISTER SET(MRS)

The mode register stores the data for controlling the various operating modes of DDR SDRAM. It programs CAS latency, addressing mode, burst length, test mode, DLL reset and various vendor specific options to make DDR SDRAM useful for variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after EMRS setting for proper operation. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$(The DDR SDRAM should be in active mode with CKE already high prior to writing into the mode register). The state of address pins A_0 ~ A_{12} and BA_0, BA_1 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going low is written in the mode register. Minimum two clock cycles are requested to complete the write operation in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields depending on functionality. The burst length uses A_0 ~ A_2, addressing mode uses A_3, CAS latency(read latency from column address) uses A_4 ~ A_6. A_7 is used for test mode. A_8 is used for DLL reset. A_7,A_8, BA_0 and BA_1 must be set to low for normal MRS operation. Refer to the table for specific codes for various burst length, addressing modes and CAS latencies.



DLL

A8	DLL Reset
0	No
1	Yes

Test Mode

A7	mode
0	Normal
1	Test

Burst Type

A3	Type
0	Sequential
1	Interleave

BA0	An ~ A0
0	MRS
1	EMRS

* 1 : RFU(Reserved for future use)
should stay "0" during MRS cycle.

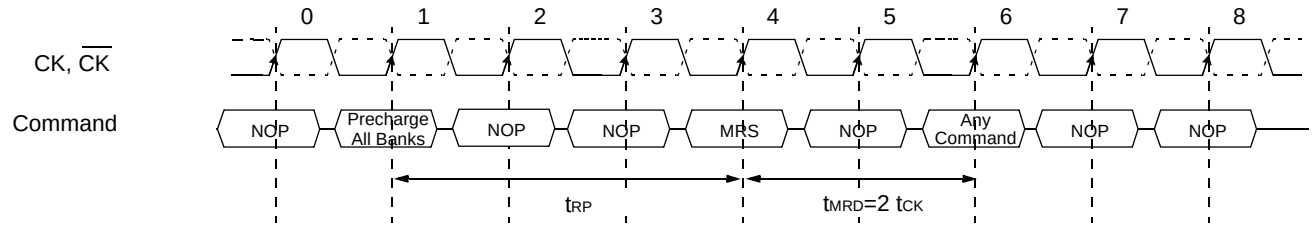
CAS Latency

A6	A5	A4	Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	2.5
1	1	1	Reserved

Burst Length

A2	A1	A0	Burst Type	
			Sequential	Interleave
0	0	0	Reserve	Reserve
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserve	Reserve
1	0	1	Reserve	Reserve
1	1	0	Reserve	Reserve
1	1	1	Reserve	Reserve

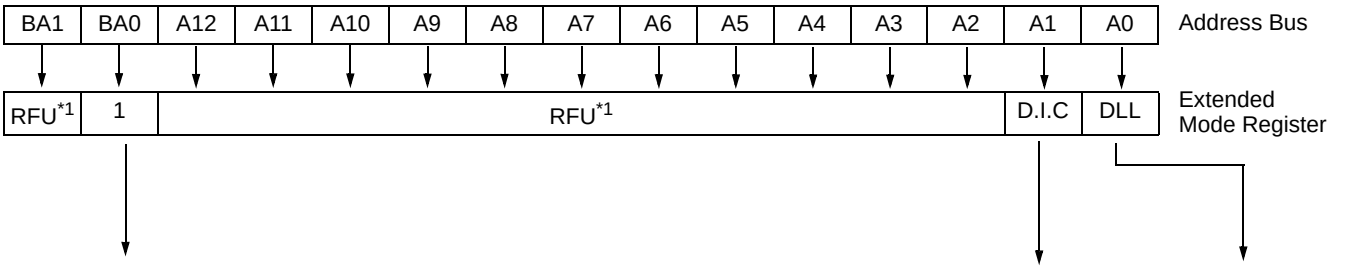
MRS Cycle



*1 : MRS can be issued only at all banks precharge state.
*2 : Minimum tRP is required to issue MRS command.

7.3 EXTENDED MODE REGISTER SET(EMRS)

The extended mode register stores the data for enabling or disabling DLL and selecting output driver strength. The default value of the extended mode register is not defined, therefore the extened mode register must be written after power up for enabling or disabling DLL. The extended mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and high on BA0(The DDR SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register). The state of address pins A0, A2 ~ A5, A7 ~ A12 and BA1 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going low are written in the extended mode register. A1 and A6 are used for setting driver strength to normal, weak or matched impedance. Two clock cycles are required to complete the write operation in the extended mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. A0 is used for DLL enable or disable. "High" on BA0 is used for EMRS. All the other address pins except A0,A1,A6 and BA0 must be set to low for proper EMRS operation. Refer to the table for specific codes.



BA_0	A_n ~ A_0
0	MRS
1	EMRS

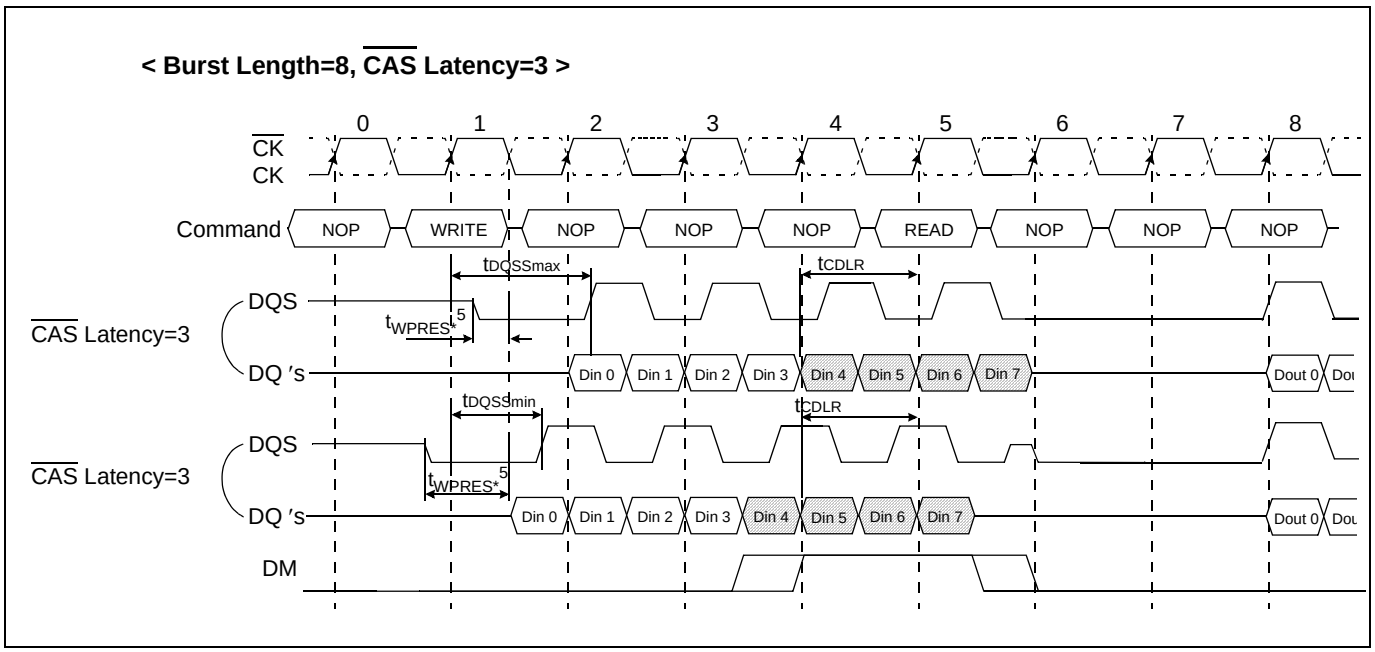
A1	Output Driver Impedence Control	
0	Full	100%
1	Weak	60%

A_0	DLL Enable
0	Enable
1	Disable

*1 : RFU(Reserved for future use) should stay "0" during EMRS cycle.

7.4 WRITE INTERRUPTED BY A READ & DM

A burst write can be interrupted by a read command of any bank. The DQ's must be in the high impedance state at least one clock cycle before the interrupting read data appear on the outputs to avoid data contention. When the read command is registered, any residual data from the burst write cycle must be masked by DM. The delay from the last data to read command (tCDLR) is required to avoid the data contention DRAM inside. Data that are presented on the DQ pins before the read command is initiated will actually be written to the memory. Read command interrupting write can not be issued at the next clock edge of that of write command.



The following function established how a Read command may interrupt a Write burst and which input data is not written into the memory.

1. For Read commands interrupting a Write burst, the minimum Write to Read command delay is 2 clock cycles. The case where the Write to Read delay is 1 clock cycle is disallowed
2. For Read commands interrupting a Write burst, the DM pin must be used to mask the input data words whcich immediately precede the interrupting Read operation and the input data word which immediately follows the interrupting Read operation
3. For all cases of a Read interrupting a Write, the DQ and DQS buses must be released by the driving chip (i.e., the memory controller) in time to allow the buses to turn around before the GDDR drives them during a read operation.
4. If input Write data is masked by the Read command, the DQS input is ignored by the GDDR.

*** This function is only supported in 200/166MHz.**

8.0 ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.5 ~ 3.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}	-1.0 ~ 3.6	V
Voltage on V_{DD} supply relative to Vss	V_{DDQ}	-0.5 ~ 3.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	2.0	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

9.0 AC & DC OPERATING CONDITIONS

9.1 POWER & DC OPERATING CONDITIONS(SSTL_2 In/Out)

Recommended operating conditions(Voltage referenced to V_{SS}=0V, T_A=0 to 65°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Device Supply voltage	V_{DD}	2.35	2.6	2.7	V	1
Output Supply voltage	V_{DDQ}	2.35	2.6	2.7	V	1
Reference voltage	V_{REF}	0.49*V_{DDQ}	-	0.51*V_{DDQ}	V	2
Termination voltage	V_{tt}	V_{REF}-0.04	V_{REF}	V_{REF}+0.04	V	3
Input logic high voltage	V_{IH}(DC)	V_{REF}+0.15	-	V_{DDQ}+0.30	V	4
Input logic low voltage	V_{IL}(DC)	-0.30	-	V_{REF}-0.15	V	5
Output logic high voltage	V_{OH}	V_{tt}+0.76	-	-	V	I_{OH}=-15.2mA
Output logic low voltage	V_{OL}	-	-	V_{tt}-0.76	V	I_{OL}=+15.2mA
Input leakage current	I_{IL}	-5	-	5	uA	6
Output leakage current	I_{OL}	-5	-	5	uA	6

Note :
1. Under all conditions V_{DDQ} must be less than or equal to V_{DD}.
2. V_{REF} is expected to equal 0.50*V_{DDQ} of the transmitting device and to track variations in the DC level of the same. Peak to peak noise on the V_{REF} may not exceed + 2% of the DC value. Thus, from 0.50*V_{DDQ}, V_{REF} is allowed + 25mV for DC error and an additional + 25mV for AC noise.
3. V_{tt} of the transmitting device must track V_{REF} of the receiving device.
4. V_{IH}(max.)= V_{DDQ} +1.5V for a pulse width and it can not be greater than 1/3 of the cycle rate.
5. V_{IL}(mim.)= -1.5V for a pulse width and it can not be greater than 1/3 of the cycle rate.
6. For any pin under test input of 0V ≤ V_{IN} ≤ V_{DD} is acceptable. For all other pins that are not under test V_{IN}=0V.

9.2 DC CHARACTERISTICS

Recommended operating conditions Unless Otherwise Noted, (TA=0 to 65°C)

Parameter	Symbol	Test Condition	Version		Unit	Note
			-40	-50		
Operating Current (One Bank Active)	ICC1	Burst Lenth=2 tRC ≥ tRC(min) IOL=0mA, tCC= tCC(min)	160	140	mA	1, 2
Precharge Standby Current in Power-down mode	ICC2P	CKE ≤ VIL(max), tCC= tCC(min)	5		mA	1, 2
Precharge Standby Current in Non Power-down mode	ICC2N	CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), tCC= tCC(min)	80	70	mA	1, 2
Active Standby Current power-down mode	ICC3P	CKE ≤ VIL(max), tCC= tCC(min)	65	55	mA	1, 2
Active Standby Current in in Non Power-down mode	ICC3N	CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), tCC= tCC(min)	80	70	mA	1, 2
Operating Current (Burst Mode)	ICC4	tRC ≥ tRFC(min)tRC ≥ tRFC(min) Page Burst, All Banks activated.	265	220	mA	1, 2
Refresh Current	ICC5	tRC ≥ tRFC(min)	180	160	mA	1, 2,3
Self Refresh Current	ICC6	CKE ≤ 0.2V	5		mA	1, 2
Operating Current (4Bank Interleaving)	ICC7	Burst Length=4, tRC ≥ tRFC(min) IOL=0mA, tCC = tCC(min)	300	260	mA	1, 2

Note :
1. Measured with output open.
2. Current meassured at V_{DD}(max).
3. Refresh period is 64ms.

9.3 AC INPUT OPERATING CONDITIONS

Recommended operating conditions(Voltage referenced to V_{SS}=0V, V_{DD}/V_{DDQ}=2.35V ~ 2.7V,T_A=0 to 65°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Input High (Logic 1) Voltage; DQ	V_{IH}	V_{REF}+0.35	-	-	V	
Input Low (Logic 0) Voltage; DQ	V_{IL}	-	-	V_{REF}-0.35	V	
Clock Input Differential Voltage; CK and $\overline{CK}$	V_{ID}	0.7	-	V_{DDQ}+0.6	V	1
Clock Input Crossing Point Voltage; CK and $\overline{CK}$	V_{IX}	0.5*$_{VDDQ}$-0.2	-	0.5*V_{DDQ}+0.2	V	2

Note :

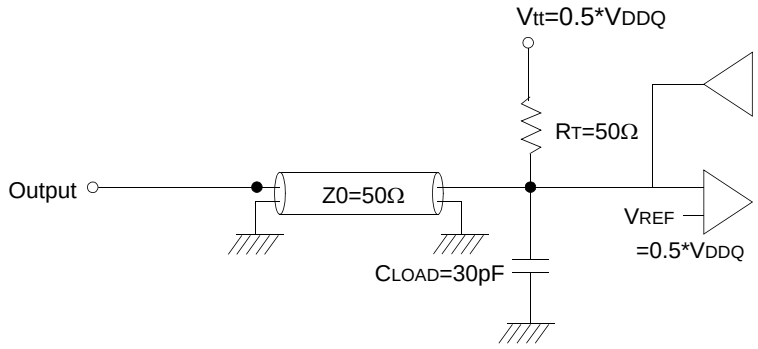
1. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
2. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same.

9.4 AC OPERATING TEST

(V_{DD}=2.35V ~ 2.7V, TA= 0 to 65°C)

Parameter	Value	Unit	Note
Input reference voltage for CK(for single ended)	0.50*V_{DDQ}	V	1
CK and $\overline{CK}$ signal maximum peak swing	1.5	V	
CK signal minimum slew rate	1.0	V/ns	
Input Levels(VIH/VIL)	V_{REF}+0.35/V_{REF}-0.35	V	
Input timing measurement reference level	V_{REF}	V	
Output timing measurement reference level	V_{tt}	V	
Output load condition	See Fig.1		

Note 1 : In case of differential clocks(CK and $\overline{CK}$), input reference voltage for clock is a CK and $\overline{CK}$'s crossing point.



(Fig. 1) Output Load Circuit

9.5 CAPACITANCE

(V_{DD}=2.6V, TA= 25°C, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance(CK, $\overline{CK}$)	C_{IN1}	1.0	5.0	pF
Input capacitance(A_0~A_{12}, BA_0~BA_1)	C_{IN2}	1.0	4.0	pF
Input capacitance(CKE, $\overline{CS}$, $\overline{RAS}$,$\overline{CAS}$, $\overline{WE}$)	C_{IN3}	1.0	4.0	pF
Data & DQS input/output capacitance(DQ_0~DQ_{15})	C_{OUT}	1.0	6.5	pF
Input capacitance(DM0 ~ DM3)	C_{IN4}	1.0	6.5	pF

DECOUPLING CAPACITANCE GUIDE LINE

Recommended decoupling capacitance added to power line at board.

Parameter	Symbol	Value	Unit
Decoupling Capacitance between V_{DD} and V_{SS}	C_{DC1}	0.1 + 0.01	uF
Decoupling Capacitance between V_{DDQ} and V_{SSQ}	C_{DC2}	0.1 + 0.01	uF

Note :

1. V_{DD} and V_{DDQ} pins are separated each other. All V_{DD} pins are connected in chip. All V_{DDQ} pins are connected in chip.
2. V_{SS} and V_{SSQ} pins are separated each other. All V_{SS} pins are connected in chip. All V_{SSQ} pins are connected in chip.

9.6 AC CHARACTERISTICS(I)

Parameter		Symbol	-40		-50		Unit	Note
			Min	Max	Min	Max		
CK cycle time	CL=3	tCK	4.0	10	5.0	10	ns	
	CL=2.5		-	-	6.0	10		
CK high level width		tCH	0.45	0.55	0.45	0.55	tCK	
CK low level width		tCL	0.45	0.55	0.45	0.55	tCK	
DQS out access time from CK		tDQSCK	-0.6	0.6	-0.55	0.55	ns	
Output access time from CK		tAC	-0.6	0.6	-0.65	0.65	ns	
Data strobe edge to Dout edge		tDQSQ	-	0.4	-	0.4	ns	1
Read preamble		tRPRE	0.9	1.1	0.9	1.1	tCK	
Read postamble		tRPST	0.4	0.6	0.4	0.6	tCK	
CK to valid DQS-in		tDQSS	0.85	1.15	0.72	1.28	tCK	
DQS-In setup time		tWPRES	0	-	0	-	ns	
DQS-in hold time		tWPREH	0.35	-	0.25	-	tCK	
DQS write postamble		tWPST	0.4	0.6	0.4	0.6	tCK	
DQS-In high level width		tDQSH	0.4	0.6	0.35	-	tCK	
DQS-In low level width		tDQSL	0.4	0.6	0.35	-	tCK	
Address and Control input setup		tIS	0.9	-	0.6	-	ns	
Address and Control input hold		tIH	0.9	-	0.6	-	ns	
DQ and DM setup time to DQS		tDS	0.4	-	0.4	-	ns	
DQ and DM hold time to DQS		tDH	0.4	-	0.4	-	ns	
Clock half period		tHP	tCLmin or tCHmin	-	tCLmin or tCHmin	-	ns	1
Data output hold time from DQS		tQH	tHP-0.4	-	tHP-0.5	-	ns	1

Note 1 :

- The JEDEC DDR specification currently defines the output data valid window(tDV) as the time period when the data strobe and all data associated with that data strobe are coincidentally valid.
- The previously used definition of tDV(=0.35tCK) artificially penalizes system timing budgets by assuming the worst case output vaild window even then the clock duty cycle applied to the device is better than 45/55%
- A new AC timing term, tQH which stands for data output hold time from DQS is difined to account for clock duty cycle variation and replaces tDV
- tQHmin = tHP-X where
  . tHP=Minimum half clock period for any given cycle and is defined by clock high or clock low time(tCH,tCL)

AC CHARACTERISTICS (I)

Parameter	Symbol	-40		-50		Unit	Note
		Min	Max	Min	Max		
Row cycle time	tRC	13	-	12	-	tCK	
Refresh row cycle time	tRFC	15	-	14	-	tCK	
Row active time	tRAS	9	100K	8	100K	tCK	
$\overline{RAS}$ to $\overline{CAS}$ delay for Read	tRCDRD	4	-	4	-	tCK	
$\overline{RAS}$ to $\overline{CAS}$ delay for Write	tRCDWR	2	-	2	-	tCK	
Row precharge time	tRP	4	-	4	-	tCK	
Row active to Row active	tRRD	3	-	2	-	tCK	
Last data in to Row precharge @Normal Precharge	tWR	3	-	3	-	tCK	1
Last data in to Row precharge @Auto Precharge	tWR_A	3	-	3	-	tCK	1
Last data in to Read command	tCDLR	2	-	2	-	tCK	1
Col. address to Col. address	tCCD	1	-	1	-	tCK	
Mode register set cycle time	tMRD	2	-	2	-	tCK	
Auto precharge write recovery + Precharge	tDAL	7	-	7	-	tCK	
Exit self refresh to read command	tXSR	200	-	200	-	tCK	
Power down exit time	tPDEX	3tCK +tIS	-	1tCK +tIS	-	ns	
Refresh interval time	tREF	-	7.8	-	7.8	us	

Note : 1. For normal write operation, even numbers of Din are to be written inside DRAM

AC CHARACTERISTICS (II)

(Unit : Number of Clock)

K4D551638H-LC40

Frequency	Cas Latency	tRC	tRFC	tRAS	tRCDRD	tRCDWR	tRP	tRRD	tDAL	Unit
250MHz (4.0ns)	3	13	15	9	4	2	4	3	7	tCK
200MHz (5.0ns)	3	12	14	8	4	2	4	3	7	tCK

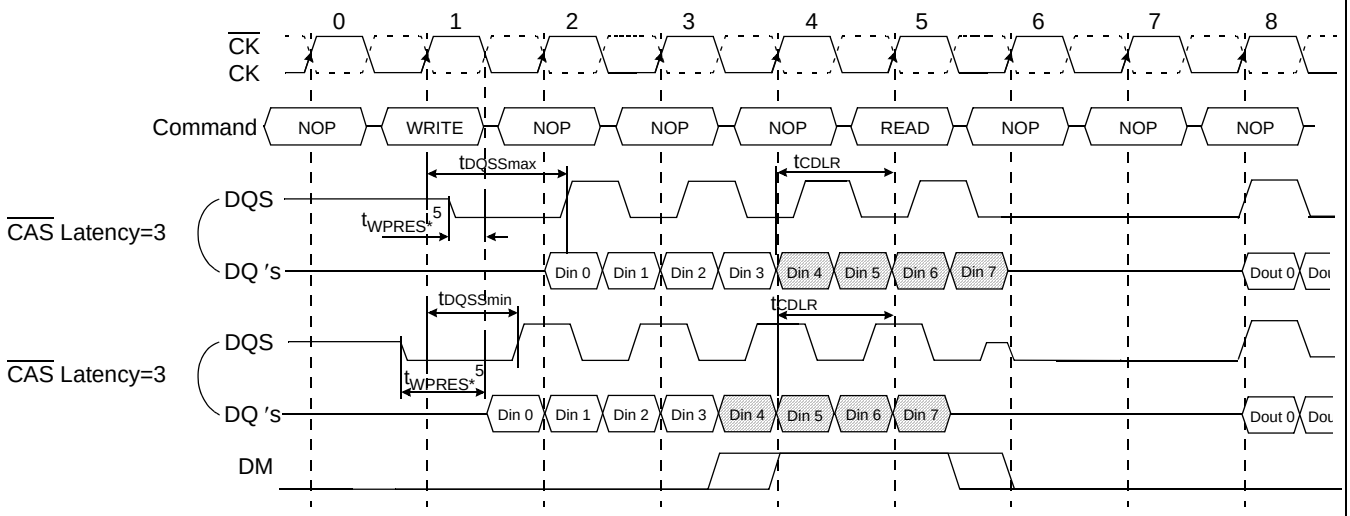
K4D551638H-LC50

Frequency	Cas Latency	tRC	tRFC	tRAS	tRCDRD	tRCDWR	tRP	tRRD	tDAL	Unit
200MHz (5.0ns)	3	12	14	8	4	2	4	2	7	tCK
166MHz (6.0ns)	2.5	10	12	7	3	2	3	2	6	tCK

Write Interrupted by a Read & DM

A burst write can be interrupted by a read command of any bank. The DQ's must be in the high impedance state at least one clock cycle before the interrupting read data appear on the outputs to avoid data contention. When the read command is registered, any residual data from the burst write cycle must be masked by DM. The delay from the last data to read command (tCDLR) is required to avoid the data contention DRAM inside. Data that are presented on the DQ pins before the read command is initiated will actually be written to the memory. Read command interrupting write can not be issued at the next clock edge of that of write command.

< Burst Length=8, $\overline{\text{CAS}}$ Latency=3 >



The following function established how a Read command may interrupt a Write burst and which input data is not written into the memory.

1. For Read commands interrupting a Write burst, the minimum Write to Read command delay is 2 clock cycles. The case where the Write to Read delay is 1 clock cycle is disallowed.
2. For Read commands interrupting a Write burst, the DM pin must be used to mask the input data words whcich immediately precede the interrupting Read operation and the input data word which immediately follows the interrupting Read operation.
3. For all cases of a Read interrupting a Write, the DQ and DQS buses must be released by the driving chip (i.e., the memory controller) in time to allow the buses to turn around before the GDDR drives them during a read operation.
4. If input Write data is masked by the Read command, the DQS input is ignored by the GDDR.

*** This function is only supported in 200/166MHz.**

10.0 IBIS : I/V Characteristics for Input and Output Buffers

(1) Full Strength Driver Characteristics

	Pulldown Current (mA)		Pullup Current (mA)	
Voltage (V)	Minimum	Maximum	Minimum	Maximum
0.0	0	0	0	0
0.1	4.8	10.0	-4.8	-10.4
0.2	9.6	18.9	-9.6	-20.8
0.3	14.4	27.0	-14.4	-31.0
0.4	19.1	35.3	-19.1	-40.4
0.5	23.9	43.5	-23.9	-48.7
0.6	28.8	51.4	-28.8	-56.6
0.7	33.5	59.1	-33.5	-64.3
0.8	38.3	65.7	-37.4	-72.3
0.9	41.2	72.7	-39.7	-80.4
1.0	44.3	79.4	-40.2	-88.6
1.1	46.6	85.8	-40.6	-96.7
1.2	48.0	91.8	-40.6	-104.6
1.3	49.0	97.6	-41.0	-112.4
1.4	49.3	103.1	-41.2	-120.1
1.5	49.6	108.0	-41.5	-127.9
1.6	49.9	112.7	-41.7	-135.6
1.7	50.3	116.6	-41.8	-142.2
1.8	50.9	120.5	-41.9	-150.0
1.9	51.1	124.4	-42.0	-156.5
2.0	51.4	128.2	-42.1	-163.2
2.1	51.6	131.6	-42.2	-169.7
2.2	51.8	134.7	-42.3	-176.4
2.3	51.9	137.7	-42.4	-183.0
2.4	52.0	140.4	-42.5	-188.6
2.5	52.2	142.8	-42.6	-195.1
2.6	52.4	144.8	-42.7	-200.6
2.7	52.5	146.4	-42.8	-206.1

10.0 IBIS : I/V Characteristics for Input and Output Buffers

(2) Weak Strength Driver Characteristics

	Pulldown Current (mA)		Pullup Current (mA)	
Voltage (V)	Minimum	Maximum	Minimum	Maximum
0.0	0	0	0	0
0.1	2.7	5.2	-2.7	-5.2
0.2	5.4	10.3	-5.4	-10.3
0.3	8.1	15.2	-8.1	-15.2
0.4	10.8	20.0	-10.8	-20.0
0.5	13.5	24.5	-13.5	-24.5
0.6	16.3	29.1	-16.3	-29.1
0.7	18.9	33.5	-18.9	-33.5
0.8	21.6	37.2	-21.2	-37.2
0.9	23.3	41.1	-22.5	-41.1
1.0	25.1	44.9	-22.8	-44.9
1.1	26.4	48.6	-23.0	-48.6
1.2	27.2	52.0	-23.1	-52.0
1.3	27.7	55.2	-23.2	-55.2
1.4	27.9	58.3	-23.3	-58.3
1.5	28.1	61.0	-23.5	-61.0
1.6	28.3	63.9	-23.6	-63.9
1.7	28.5	66.0	-23.6	-66.0
1.8	28.8	68.2	-23.7	-68.2
1.9	28.9	70.4	-23.8	-70.4
2.0	29.1	72.6	-23.8	-72.6
2.1	29.2	74.5	-23.9	-74.5
2.2	29.3	76.2	-24.0	-76.2
2.3	29.4	77.9	-24.1	-77.9
2.4	29.4	79.5	-24.1	-79.5
2.5	29.5	80.8	-24.1	-80.8
2.6	29.6	82.0	-24.2	-82.0
2.7	29.7	82.9	-24.2	-82.9

11.0 PACKAGE DIMENSIONS (66pin TSOP-II)