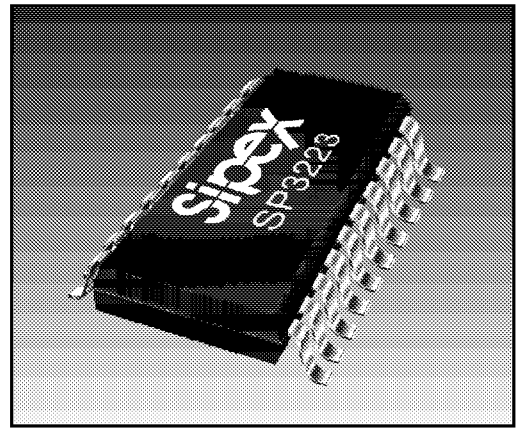
SP3221E/3223E/3243E

True +3.0V to +5.5V RS-232 Transceivers

- Meets true EIA/TIA-232-F Standards from a +3.0V to +5.5V power supply
- Adheres to EIA/TIA-562 specifications down to +2.7V power source
- Auto-Online circuitry allows 1µA supply current when in shutdown
- 120Kbps data rate under load
- 6V/µs minimum slew rate
- The **SP3221E** is the industries smallest single-supply RS-232 transceiver package
- Enhanced ESD Specifications:
  ±15KV Human Body Model
  ±15KV IEC1000-4-2 Air Discharge
  ±8KV IEC1000-4-2 Contact Discharge



DESCRIPTION...

The **SP3221E/3223E/3243E** series is an RS-232 transceiver solution intended for portable or hand-held applications such as notebook or palmtop computers. The **SP3221E/3223E/3243E** series has a high-efficiency, charge-pump power supply that requires only 0.1µF capacitors in 3.3V operation. This charge pump and low-dropout transmitters allow the **SP3221E/3223E/3243E** series to deliver true RS-232 performance from a single power supply ranging from +3.3V to +5.0V. The **SP3221E** is a 1-driver/1-receiver device, the **SP3223E** is a 2-driver/2-receiver device, and the **SP3243E** is a 3-driver/5-receiver device ideal for notebook or subnotebook computer applications. The **SP3243E** include one complementary always-active receiver that can monitor an external device (such as a modem) in shutdown, without forward biasing the protection diodes in a UART that may have V_{CC} completely removed.

The **SP3243E** contains a complementary always-active receiver that can monitor an external device (such as a modem) in the ***Auto-Online*** mode. The ***Auto-Online*** mode allows the device to automatically "wake-up" during a shutdown state when an incoming signal is detected. Conversely, the device automatically shuts itself down when no incoming signal is detected at the inputs of the recievers over a period of time, drawing less than 1µA.

SELECTION TABLE

MODEL	Power Supplies	RS-232 Drivers	RS-232 Receivers	External Components	***Auto-Online*** Circuitry	TTL 3-State	No. of Pins
SP3221E	+3.0V to +5.5V	1	1	4 capacitors	YES	YES	16
SP3223E	+3.0V to +5.5V	2	2	4 capacitors	YES	YES	20
SP3243E	+3.0V to +5.5V	3	5	4 capacitors	YES	YES	28

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

V_{CC}.....-0.3V to +6.0V
V+ (NOTE 1).....-0.3V to +7.0V
V- (NOTE 1).....+0.3V to -7.0V
V+ + |V-| (NOTE 1).....+13V
I_{CC} (DC V_{CC} or GND current).....±100mA

Input Voltages

TxIN, FORCEON, $\overline{\text{FORCEOFF}}$, $\overline{\text{EN}}$ (SP3243).....-0.3V to +6.0V
RxIN.....±15V

Output Voltages

TxOUT.....±15V
RxOUT, $\overline{\text{INVALID}}$.....-0.3V to ($V_{CC}$ + 0.3V)

Short-Circuit Duration

TxOUT.....Continuous
Storage Temperature.....-65°C to +150°C
P_{tot} (Power dissipation perpackage).....1000mW

NOTE 1: V+ and V- can have maximum magnitudes of 7V, but their absolute difference cannot exceed 13V.

SPECIFICATIONS

Unless otherwise noted, the following specifications apply for V_{CC} = +3.0V to +5.0V with T_{AMB} = 0°C to +70°C. Typical values apply at V_{CC} = +3.0V or +5.0V and T_{AMB} = 25°C.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DC CHARACTERISTICS					
Supply Current, Auto-Online		1.0	10	µA	All RxIN open, FORCEON = GND, $\overline{\text{FORCEOFF}}$ = V_{CC}, V_{CC} = +3.3V, T_{AMB} = +25° C
Supply Current, Shutdown		1.0	10	µA	$\overline{\text{FORCEOFF}}$ = GND, V_{CC} = +3.3V, T_{AMB} = +25° C
Supply Current, Auto-Online Disabled		0.3	1.0	mA	FORCEON = $\overline{\text{FORCEOFF}}$ = V_{CC}, no load, V_{CC} = +3.3V, T_{AMB} = +25° C
LOGIC INPUTS AND RECEIVER OUTPUTS					
Input Logic Threshold LOW			0.8	V	TxIN, FORCEON, $\overline{\text{FORCEOFF}}$, $\overline{\text{EN}}$ (SP3223)
Input Logic Threshold HIGH	2.0			V	V_{CC} = +3.3V or +5.0V, TxIN, $\overline{\text{EN}}$, FORCEON, $\overline{\text{FORCEOFF}}$
Input Leakage Current		±0.01	±1.0	µA	TxIN, $\overline{\text{EN}}$, FORCEON, $\overline{\text{FORCEOFF}}$, T_{AMB} = +25° C
Output Leakage Current		±0.05	±10	µA	Receivers disabled
Output Voltage LOW			0.4	V	I_{OUT} = +1.6mA
Output Voltage HIGH	V_{CC} - 0.6	V_{CC} - 0.1		V	I_{OUT} = -1.0mA

SPECIFICATIONS (continued)

Unless otherwise noted, the following specifications apply for V_{CC} = +3.0V to +5.0V with T_{AMB} = 0°C to +70°C. Typical values apply at V_{CC} = +3.0V or +5.0V and T_{AMB} = 25°C.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DRIVER OUTPUTS					
Output Voltage Swing	±5.0	±5.4		V	All driver outputs loaded with 3KΩ to GND, T_{AMB} = +25° C
Output Voltage Swing	±5.0			V	T1IN = T2IN = GND, T3IN = V_{CC}, T3OUT loaded with 3KΩ to GND, T1OUT and T2OUT each loaded by 2.5mA, T_{AMB} = +25° C
Output Resistance	300			Ω	V_{CC} = V+ = V- = 0V or 3.0V to 5.5V, Drivers disabled
Output Short-Circuit Current		±35 ±70	±60 ±100	mA	V_{OUT} = 0V V_{OUT} = ±15V
Output Leakage Current			±25	µA	V_{CC} = 0V or 3.0V to 5.5V, V_{OUT} = ±12V, Drivers disabled
RECEIVER INPUTS					
Input Voltage Range	-15		15	V	
Input Threshold LOW	0.6	1.2		V	V_{CC} = 3.3V, T_{AMB} = +25° C
Input Threshold LOW	0.8	1.5		V	V_{CC} = 5.0V, T_{AMB} = +25° C
Input Threshold HIGH		1.5	2.4	V	V_{CC} = 3.3V, T_{AMB} = +25° C
Input Threshold HIGH		1.8	2.4	V	V_{CC} = 5.0V, T_{AMB} = +25° C
Input Hysteresis		0.3		V	
Input Resistance	3	5	7	KΩ	T_{AMB} = +25° C
***AUTO-ONLINE* CIRCUITRY CHARACTERISTICS (FORCEON = GND, $\overline{\text{FORCEOFF}}$ = V_{CC})**					
Receiver Input Thresholds to Drivers Enabled	-2.7		2.7	V	Positive threshold, Figure 23
Receiver Input Thresholds to Drivers Disabled	-0.3		0.3	V	1µA supply current, Figure 23
$\overline{\text{INVALID}}$ Output Voltage LOW			0.4	V	I_{OUT} = 1.6mA
$\overline{\text{INVALID}}$ Output Voltage HIGH	V_{CC} - 0.6			V	I_{OUT} = -1.0mA
Receiver Threshold to Drivers Enabled (t_{WU})		250		µS	Figure 23
Receiver Positive or Negative Threshold to INVALID HIGH (t_{INVH})		1		µS	Figure 23
Receiver Positive or Negative Threshold to INVALID LOW (t_{INVL})		30		µS	Figure 23; V_{CC} = 3.3V

SPECIFICATIONS (continued)

Unless otherwise noted, the following specifications apply for V_{CC} = +3.0V to +5.0V with T_{AMB} = 0°C to +70°C. Typical values apply at V_{CC} = +3.0V or +5.0V and T_{AMB} = 25°C.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TIMING CHARACTERISTICS					
Maximum Data Rate	120	235		Kbps	R_L = 3KΩ, C_L = 1000pF, one driver active
Receiver Propagation Delay					
t_{PHL}		0.3		µs	Receiver input to Receiver output, C_L = 150pF
t_{PLH}		0.3		µs	Receiver input to Receiver output, C_L = 150pF
Receiver Output Enable Time		200		ns	Normal operation
Receiver Output Disable Time		200		ns	Normal operation
Driver Skew		100	500	ns	$\lvert t_{PHL} - t_{PLH} \rvert$
Receiver Skew		200	1000	ns	$\lvert t_{PHL} - t_{PLH} \rvert$
Transition-Region Slew Rate			30	V/µs	V_{CC}= 3.3V, R_L = 3KΩ, T_{AMB} = +25° C, measurements taken from -3.0V to +3.0V or +3.0V to -3.0V

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, the following performance characteristics apply for V_{CC} = +3.3V, 235Kbps data rate, all drivers loaded with 3KΩ, 0.1µF charge pump capacitors, and T_{AMB} = +25°C.

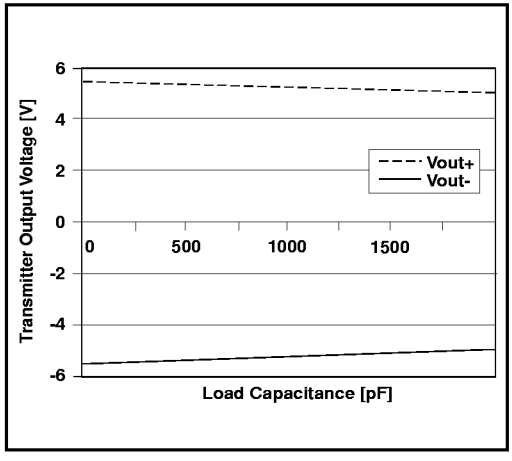


Figure 1. Transmitter Output Voltage VS. Load Capacitance for the SP3221E and the SP3223E

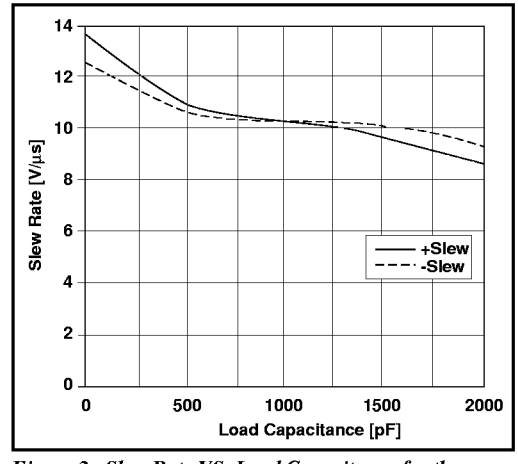


Figure 2. Slew Rate VS. Load Capacitance for the SP3221E and the SP3223E

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise noted, the following performance characteristics apply for V_{CC} = +3.3V, 235Kbps data rate, all drivers loaded with 3KΩ, 0.1µF charge pump capacitors, and T_{AMB} = +25°C.

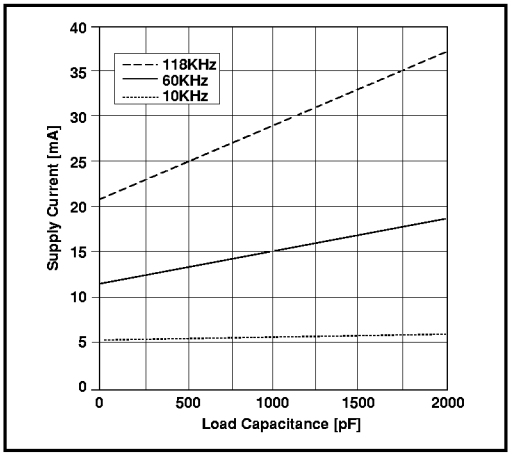


Figure 3. Supply Current VS. Load Capacitance when Transmitting Data for the SP3221E and the SP3223E

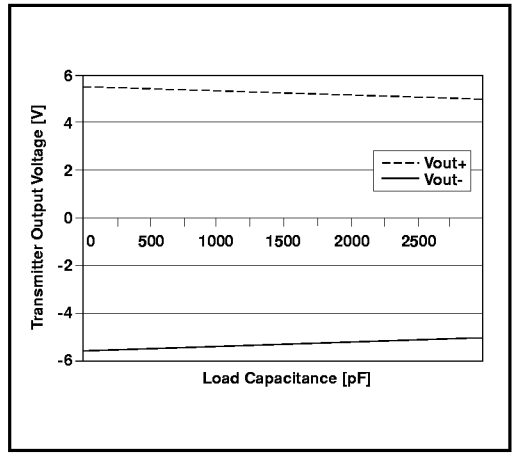


Figure 4. Transmitter Output Voltage VS. Load Capacitance for the SP3243E

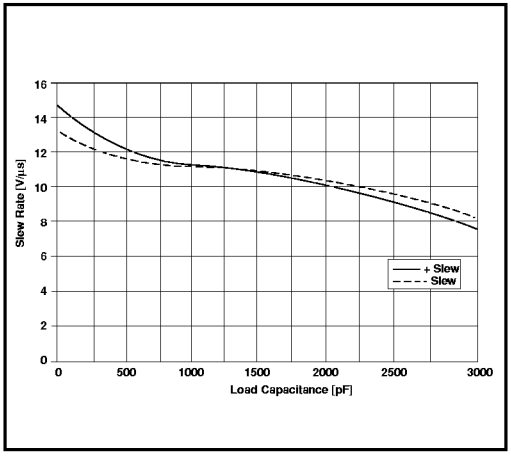


Figure 5. Slew Rate VS. Load Capacitance for the SP3243E

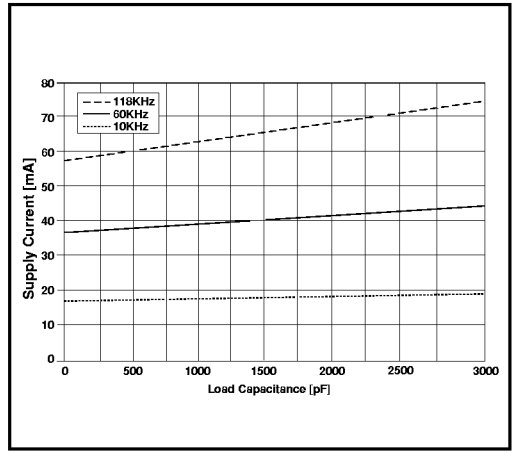


Figure 6. Supply Current VS. Load Capacitance when Transmitting Data for the SP3243E

NAME	FUNCTION	PIN NUMBER		
		SP3221E	SP3223E	SP3243E
$\overline{EN}$	Receiver Enable Control. Drive HIGH for normal operation. Drive LOW to Tri-State the receiver outputs (high-Z state).	1	1	-
C1+	Positive terminal of the voltage doubler charge-pump capacitor.	2	2	28
V+	+5.5V generated by the charge pump.	3	3	27
C1-	Negative terminal of the voltage doubler charge-pump capacitor.	4	4	24
C2+	Positive terminal of the inverting charge-pump capacitor.	5	5	1
C2-	Negative terminal of the inverting charge-pump capacitor.	6	6	2
V-	-5.5V generated by the charge pump.	7	7	3
R1IN	RS-232 receiver input.	8	16	4
R2IN	RS-232 receiver input.	-	9	5
R3IN	RS-232 receiver input.	-	-	6
R4IN	RS-232 receiver input.	-	-	7
R5IN	RS-232 receiver input.	-	-	8
R1OUT	TTL/CMOS receiver output.	9	15	19
R2OUT	TTL/CMOS receiver output.	-	10	18
R2OUTB	Noninverting receiver output, active in shutdown.	-	-	20
R3OUT	TTL/CMOS receiver output.	-	-	17
R4OUT	TTL/CMOS receiver output.	-	-	16
R5OUT	TTL/CMOS receiver output.	-	-	15
$\overline{INVALID}$	Output of the valid signal detector that indicates if a valid RS-232 level singal is present on receiver inputs with a logic "1."	10	11	21
T1IN	TTL/CMOS driver input.	11	13	14
T2IN	TTL/CMOS driver input.	-	12	13
T3IN	TTL/CMOS driver input.	-	-	12
$\overline{SHDN}$	Drive HIGH to override automatic circuitry keeping drivers active (FORCEOFF must also be HIGH, refer to Table xxx).	12	14	23
T1OUT	RS-232 driver output.	13	17	9
T2OUT	RS-232 driver output.	-	8	10
T3OUT	RS-232 driver output.	-	-	11
GND	Ground.	14	18	25
V_{CC}	+3.0V to +5.5V supply voltage.	15	19	26
$\overline{SHDN}$	Drive LOW to shut down drivers and on-board power supply. This overrides all automatic circuitry and FORCEON (refer to Table 2).	16	20	22

Table 1. Device Pin Description

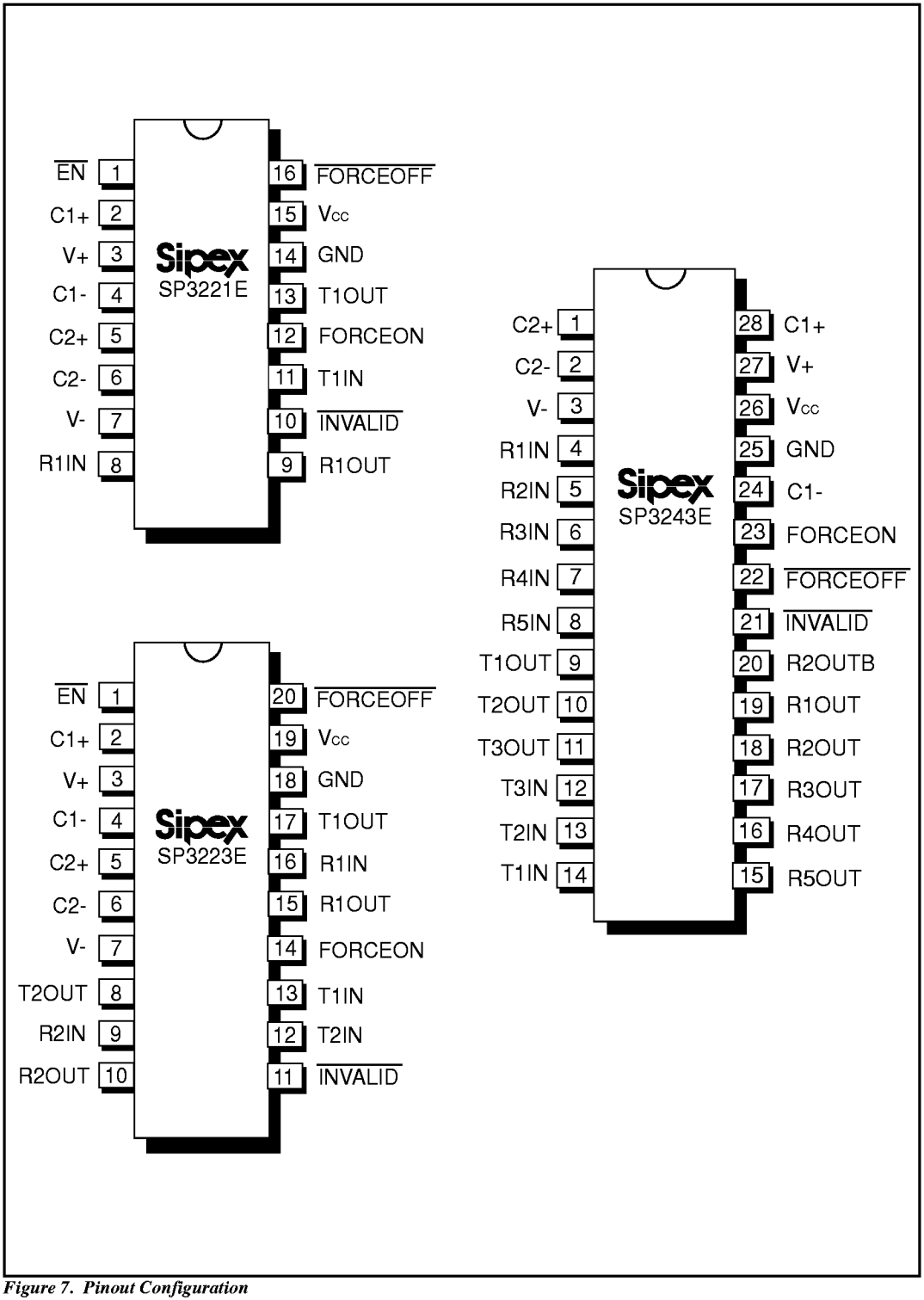


Figure 7. Pinout Configuration

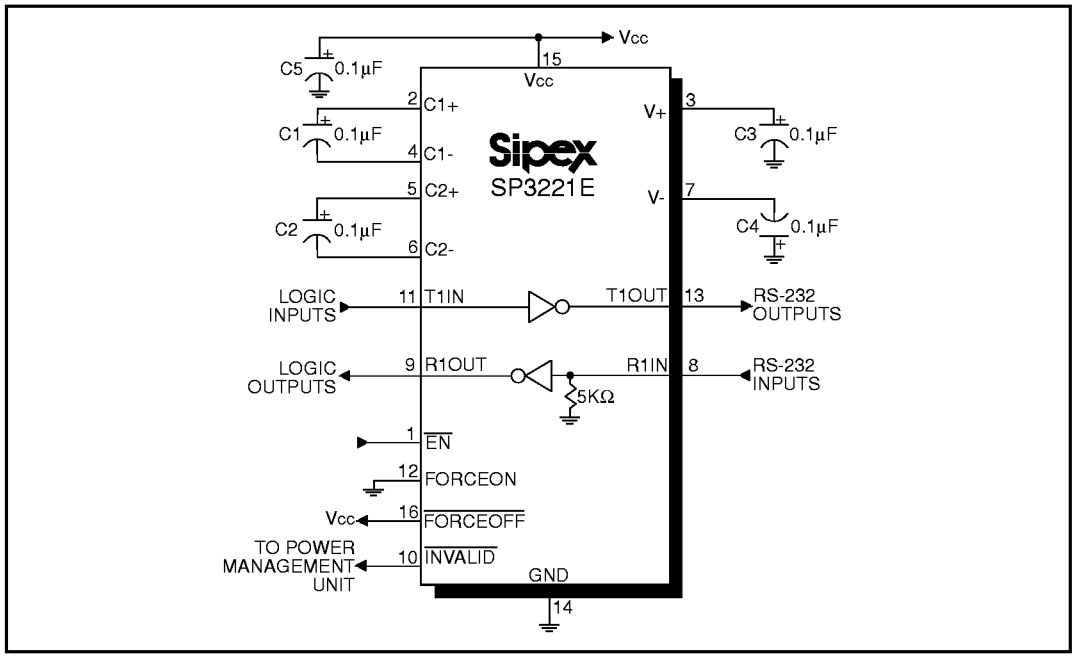


Figure 8. SP3221E Typical Operating Circuit

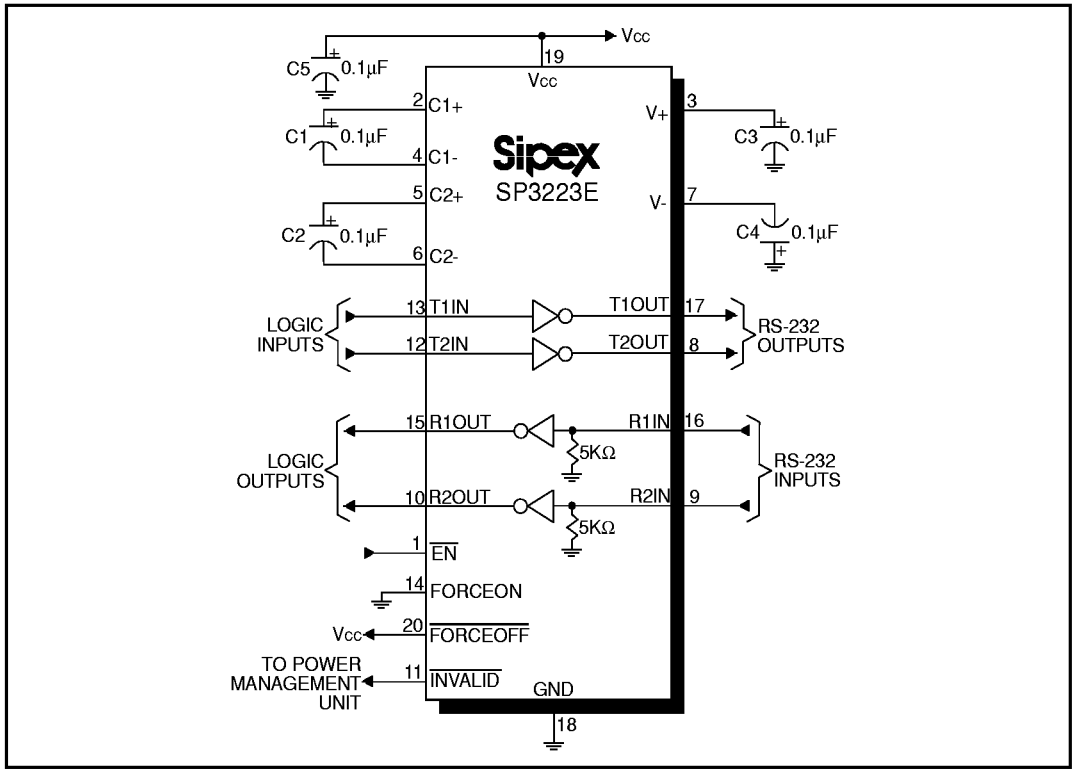


Figure 9. SP3223E Typical Operating Circuit

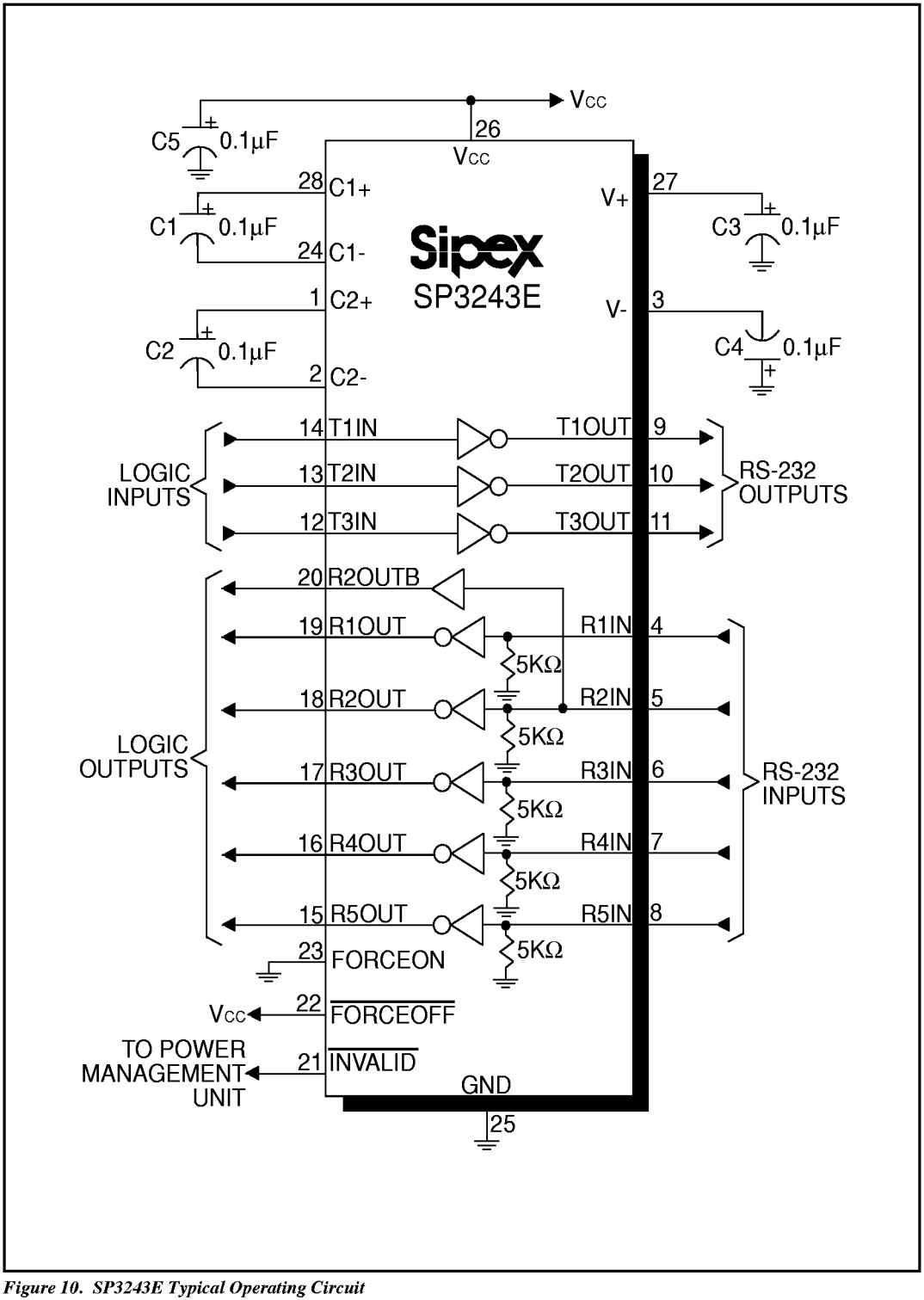


Figure 10. SP3243E Typical Operating Circuit

DESCRIPTION

The **SP3221E/3223E/3243E** transceivers meet the EIA/TIA-232 and V.28/V.24 communication protocols and can be implemented in battery-powered, portable, or hand-held applications such as notebook or palmtop computers. The **SP3221E/3223E/3243E** devices all feature Sipex's proprietary on-board charge pump circuitry that generates ±5.5V RS-232 voltage levels from a single +3.0V to +5.5V power supply. This series is ideal for +3.3V-only systems, mixed +3.3V to +5.5V systems, or +5.0V-only systems that require true RS-232 performance. The **SP3221E/3223E/3243E** series have drivers that operate at a typical data rate of 1.5Mbps, 1Mbps fully loaded.

The **SP3221E** is a 1-driver/1-receiver device, the **SP3223E** is a 2-driver/2-receiver device, and the **SP3243E** is a 3-driver/5-receiver device ideal for portable or hand-held applications. The **SP3243E** includes one complementary always-active receiver that can monitor an external device (such as a modem) in shutdown without forward biasing the protection diodes in a UART where V_{CC} may be disconnected.

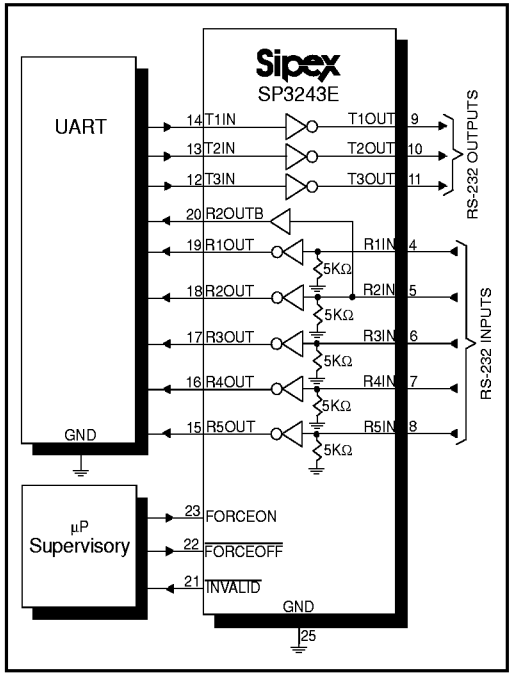


Figure 11. Interface Circuitry Controlled by Microprocessor Supervisory Circuit

The **SP3221E/3223E/3243E** series is a solid match for designs with concerns in power consumption. The **SP3221E/3223E/3243E** series features ***Auto-Online*** circuitry which reduces the power supply drain to a 1µA supply current. In many portable or hand-held applications, an RS-232 cable can be disconnected or a connected peripheral can be turned off. When the receivers of the **SP3221E/3223E/3243E** series do not sense a valid signal level on their inputs for a period of 30µs or more, the on-board charge pump power supply and the drivers shut down. The system automatically comes online when a valid RS-232 level signal is applied to any receiver input. This feature allows design engineers to address power saving concerns without changes to the existing BIOS or operating system.

THEORY OF OPERATION

The **SP3221E/3223E/3243E** series are made up of four basic circuit blocks: 1. Drivers, 2. Receivers, 3. the Sipex proprietary charge pump, and 4. ***Auto-Online*** circuitry.

Drivers

The drivers are inverting level transmitters that convert TTL or CMOS logic levels to 5.0V EIA/TIA-232 levels with an inverted sense relative to the input logic levels. Typically, the RS-232 output voltage swing is ±5.4V with no load and ±5V minimum fully loaded. The driver outputs are protected against infinite short-circuits to ground without degradation in reliability.

The drivers typically can operate at a data rate of 1.5Mbps. The drivers can guarantee a data rate of 1Mbps fully loaded with 3KΩ in parallel with 1000pF, ensuring compatibility with PC-to-PC communication software.

DEVICES: SP3221E and SP3223E			
$\overline{FORCEOFF}$	$\overline{EN}$	TxOUT	RxOUT
0	0	Tri-state	Active
0	1	Tri-state	Tri-state
1	0	Active	Active
1	1	Active	Tri-state
DEVICE: SP3243E			
$\overline{FORCEOFF}$	TxOUT	RxOUT	R2OUTB
0	Tri-state	Tri-state	Active
1	Active	Active	Active

Table 2. $\overline{FORCEOFF}$ and $\overline{ENABLE}$ Truth Tables

Note: In Auto-Online Mode where FORCEON = GND and $\overline{FORCEOFF}$ = V_{CC}, the device will shut down if no valid RS-232 levels are present at the Receiver inputs.

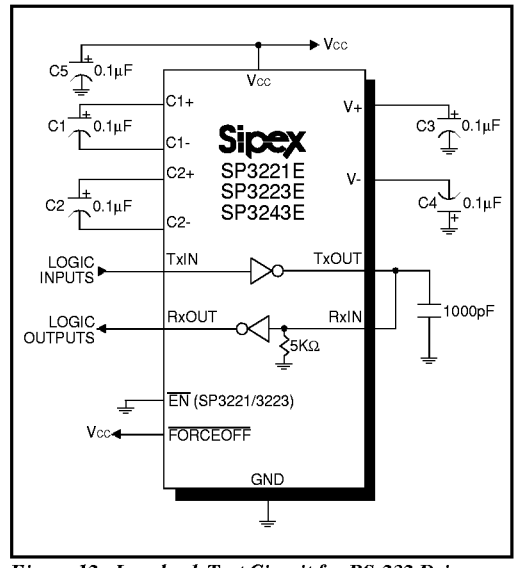


Figure 12. Loopback Test Circuit for RS-232 Driver Data Transmission Rates

When the ***Auto-Online*** circuitry senses invalid voltage levels at all receiver inputs for a period longer than 30µs or when $\overline{FORCEOFF}$ is driven to ground, the drivers are disabled with their outputs forced into high-impedance. The truth table logic of the **SP3221E/3223E/3243E** Driver and Receiver outputs can be found in *Table 2*.

The slew rate of the driver output is internally limited to a maximum of 30V/µs in order to meet the EIA standards (EIA RS-232D 2.1.7, Paragraph 5). The transition of the loaded output from HIGH to LOW also meets the monotonicity requirements of the standard.

The **SP3221E/3223E/3243E** Drivers can maintain high data rates up to 240Kbps fully loaded. *Figure 12* shows a loopback test circuit used to test the RS-232 Drivers. *Figure 13* shows the test results of the loopback circuit with all three drivers active at 120Kbps with RS-232 loads in parallel with 1000pF capacitors. *Figure 14* shows the test results where one driver was active at 240Kbps and all three drivers loaded with an

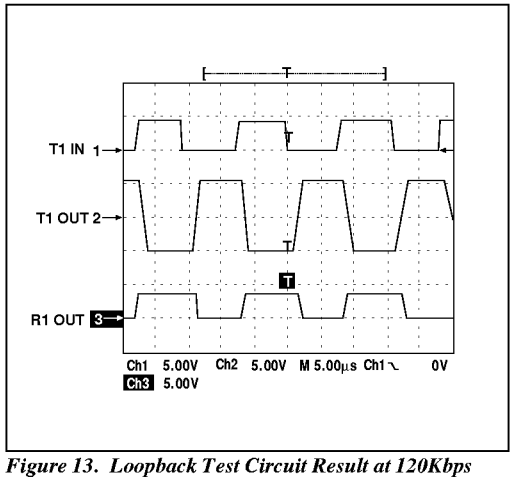


Figure 13. Loopback Test Circuit Result at 120Kbps (All Drivers Fully Loaded)

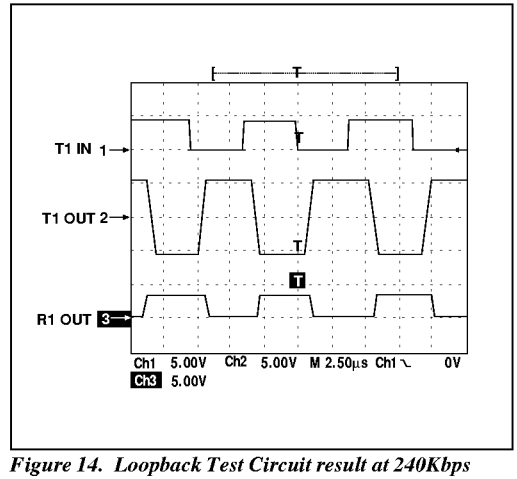


Figure 14. Loopback Test Circuit result at 240Kbps (All Drivers Fully Loaded)

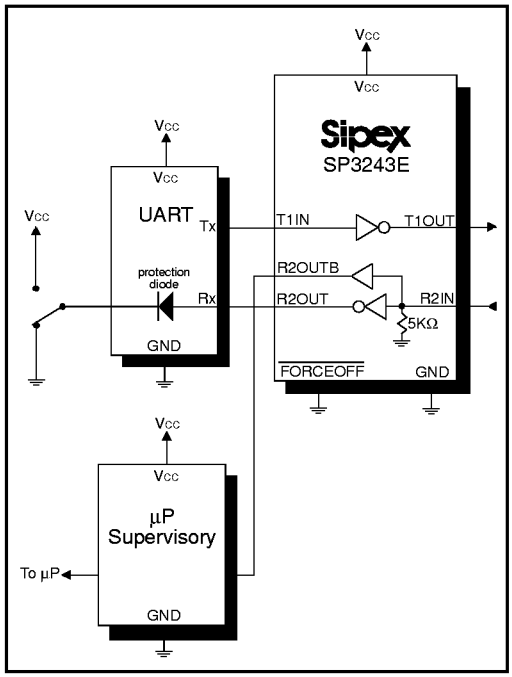


Figure 15. Detection of RS-232 Level Signals with the SP3243E

RS-232 receiver in parallel with a 1000pF capacitor. A solid RS-232 data transmission rate of 120Kbps provides compatibility with many designs in personal computer peripherals and LAN applications.

Receivers

The receivers convert 5.0V EIA/TIA-232 levels to TTL or CMOS logic output levels. All receivers have an inverting tri-state output.

Receivers are active when the Auto-Online circuitry senses invalid voltage levels at all receiver inputs for a period longer than 30µs or when $\overline{\text{FORCEOFF}}$ is driven to ground. Driving $\overline{\text{EN}}$ HIGH forces the outputs of the receivers into high-impedance. The truth table logic of the **SP3221E/3223E/3243E** Driver and Receiver outputs can be found in *Table 2*.

The **SP3243E** receiver outputs are forced into high impedance when the device is shut down. The **SP3243E** has an always-active output, R2OUTB. R2OUTB is an extra output that monitors receiver activity while the other receiver outputs are forced into high impedance. This allows Ring Indicator to be monitored without forward biasing other devices connected to the receiver outputs. This is ideal for systems where V_{CC} is set to 0V in shutdown to accommodate peripherals, such as UARTs *(Figure 15)*.

Since receiver input is usually from a transmission line where long cable lengths and system interference can degrade the signal, the inputs have a typical hysteresis margin of 300mV. This ensures that the receiver is virtually immune to noisy transmission lines. Should an input be left unconnected, a 5KΩ pulldown resistor to ground will commit the output of the receiver to a HIGH state.

Charge Pump

The charge pump is a **Sipex**–patented design (5,306,954) and uses a unique approach compared to older less–efficient designs. The charge pump still requires four external capacitors, but uses a four–phase voltage shifting technique to attain symmetrical 5.5V power supplies. The internal power supply consists of a regulated dual charge pump that provides output voltages 5.5V regardless of the input voltage (V_{CC}) over the +3.0V to +5.5V range.

The charge pumps operate in a discontinuous mode using an internal oscillator. If the output voltages are less than a magnitude of 5.5V, the charge pumps are enabled. If the output voltage exceed a magnitude of 5.5V, the charge pumps are disabled. This oscillator controls the four phases of the voltage shifting. A description of each phase follows.

Phase 1

— V_{SS} charge storage — During this phase of the clock cycle, the positive side of capacitors C_1 and C_2 are initially charged to V_{CC}. C_1^+ is then switched to GND and the charge in C_1^- is transferred to C_2^-. Since C_2^+ is connected to V_{CC}, the voltage potential across capacitor C_2 is now 2 times V_{CC}.

Phase 2

— V_{SS} transfer — Phase two of the clock connects the negative terminal of C_2 to the V_{SS} storage capacitor and the positive terminal of C_2 to GND. This transfers a negative generated voltage to C_3. This generated voltage is regulated to a minimum voltage of -5.5V. Simultaneous with the transfer of the voltage to C_3, the positive side of capacitor C_1 is switched to V_{CC} and the negative side is connected to GND.

Phase 3

— V_{DD} charge storage — The third phase of the clock is identical to the first phase — the charge transferred in C_1 produces $-V_{CC}$ in the negative terminal of C_1, which is applied to the negative side of capacitor C_2. Since C_2^+ is at V_{CC}, the voltage potential across C_2 is 2 times V_{CC}.

Phase 4

— V_{DD} transfer — The fourth phase of the clock connects the negative terminal of C_2 to GND, and transfers this positive generated voltage across C_2 to C_4, the V_{DD} storage capacitor. This voltage is regulated to +5.5V. At this voltage, the internal oscillator is disabled. Simultaneous with the transfer of the voltage to C_4, the positive side of capacitor C_1 is switched to V_{CC} and the negative side is connected to GND, allowing the charge pump cycle to begin again. The charge pump cycle will continue as long as the operational conditions for the internal oscillator are present.

Since both V^+ and V^- are separately generated from V_{CC}; in a no–load condition V^+ and V^- will be symmetrical. Older charge pump approaches that generate V^- from V^+ will show a decrease in the magnitude of V^- compared to V^+ due to the inherent inefficiencies in the design.

The clock rate for the charge pump typically operates at 250kHz. The external capacitors can be as low as 0.1µF with a 16V breakdown voltage rating.

SP3243E Serial Mouse Driveability

The **SP3243E** has been specifically designed to power serial mice while operating from low-voltage power supplies. The **SP3243E** can successfully drive all serial mice and meet their respective current and voltage requirements. *Figure 21* shows the circuit for *Figure 22* which shows the driver outputs under increasing load current. *Figure 23* shows a typical DB9/mouse connection using the **SP3243E**. The **SP3243E's** switching regulator ensures the drivers will supply at least ±5V during fully loaded conditions. The ***Auto-Online*** feature does not work with a mouse, so $\overline{\text{FORCEOFF}}$ and FORCEON should be connected to V_{CC}.

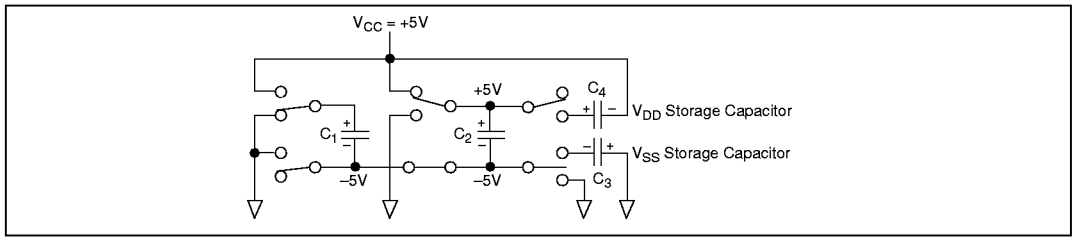


Figure 16. Charge Pump — Phase 1

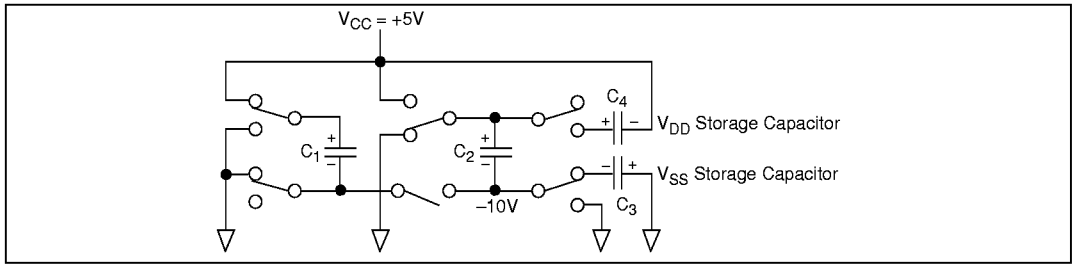


Figure 17. Charge Pump — Phase 2

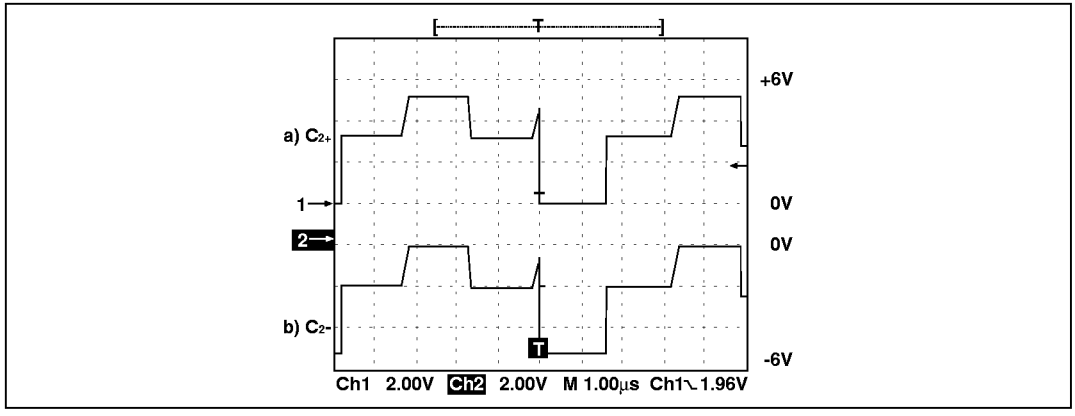


Figure 18. Charge Pump Waveforms

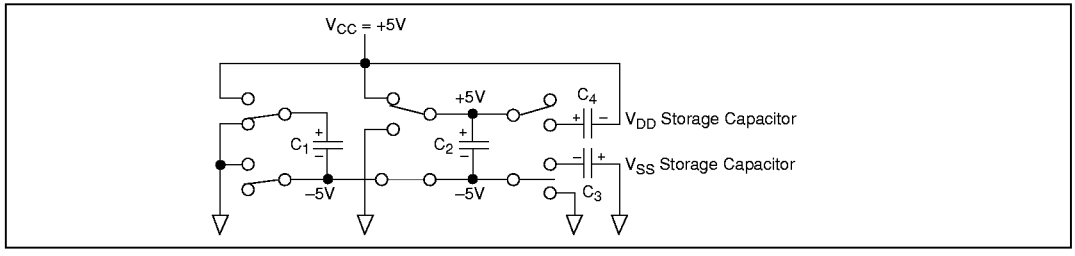


Figure 19. Charge Pump — Phase 3

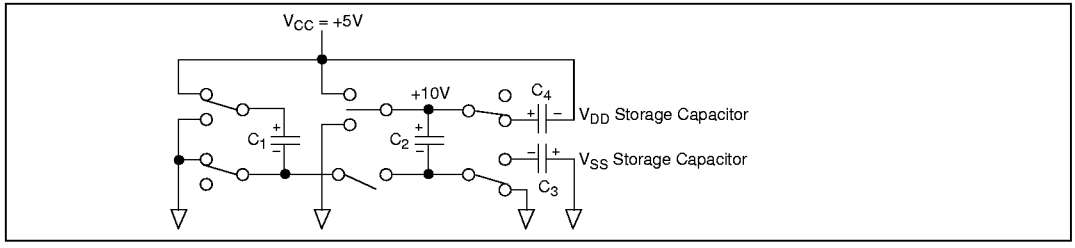


Figure 20. Charge Pump — Phase 4

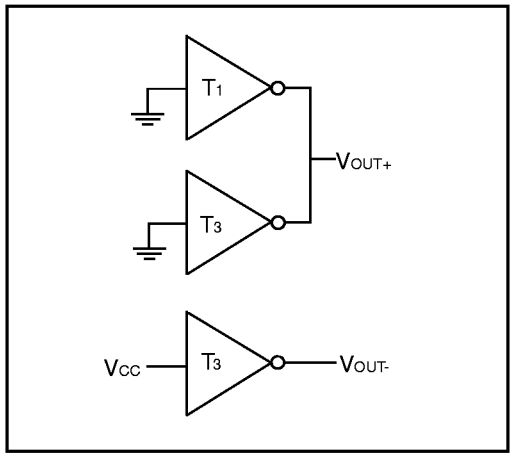


Figure 21. The Circuit for the SP3243E Driver Output Voltages vs. Load Current per Transmitter

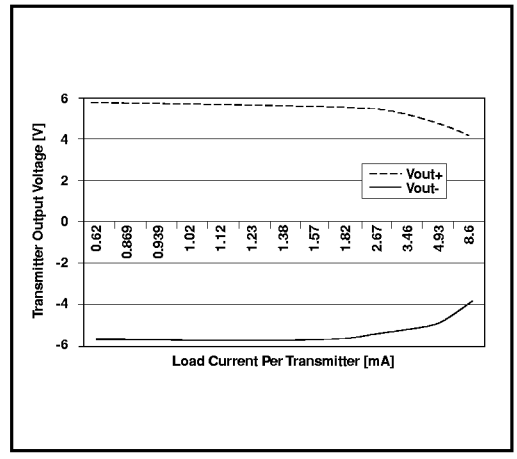


Figure 22. SP3243E Driver Output Voltages vs. Load Current per Transmitter

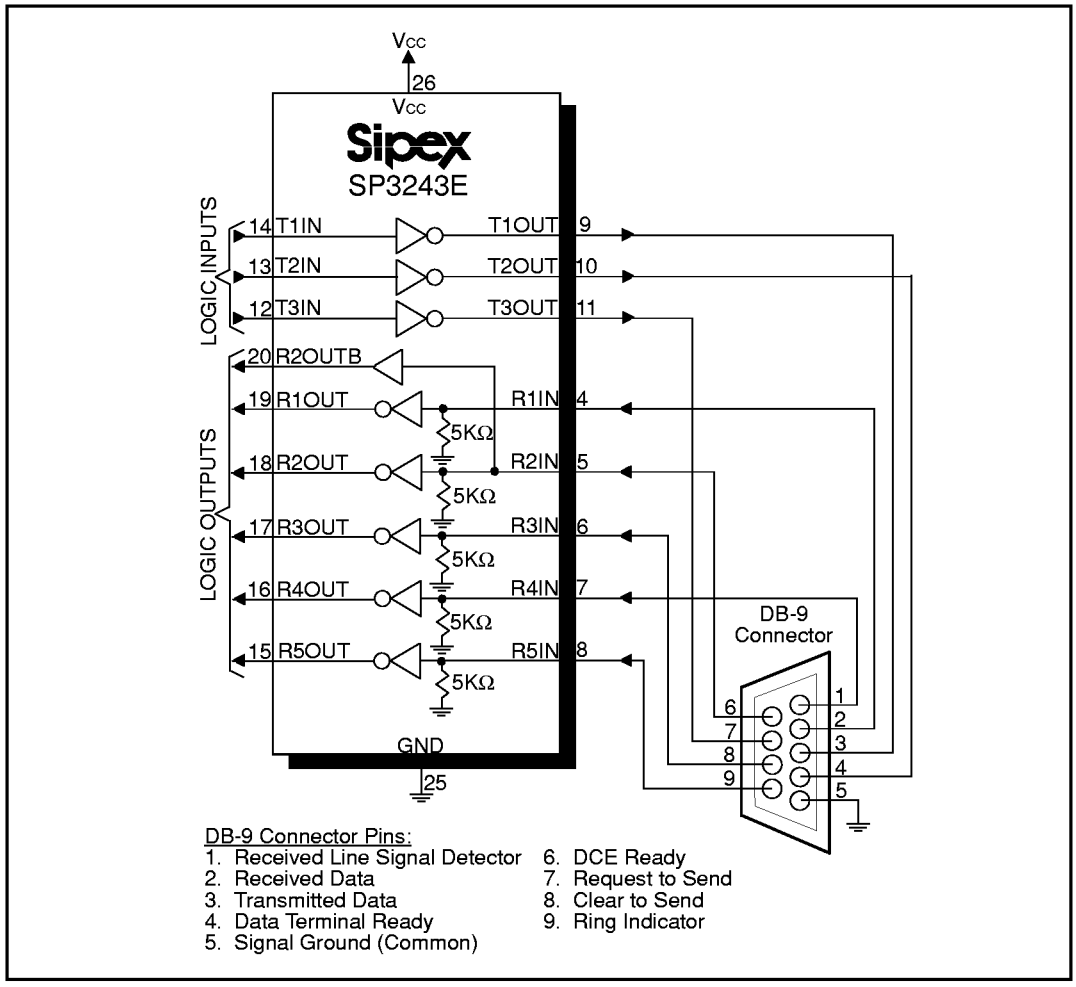


Figure 23. Circuit for the connectivity of the SP3243E with a DB-9 connector

RS-232 SIGNAL AT RECEIVER INPUT	FORCEOFF INPUT	FORCEON INPUT	INVALID OUTPUT	TRANSCEIVER STATUS
YES	HIGH	-	HIGH	Normal Operation
NO	HIGH	HIGH	LOW	Normal Operation (Forced On)
NO	HIGH	LOW	LOW	Shutdown (Autoshutdown)
YES	LOW	-	HIGH	Shutdown (Forced Off)
NO	LOW	-	LOW	Shutdown (Forced Off)

Table 3. Auto-Online Logic

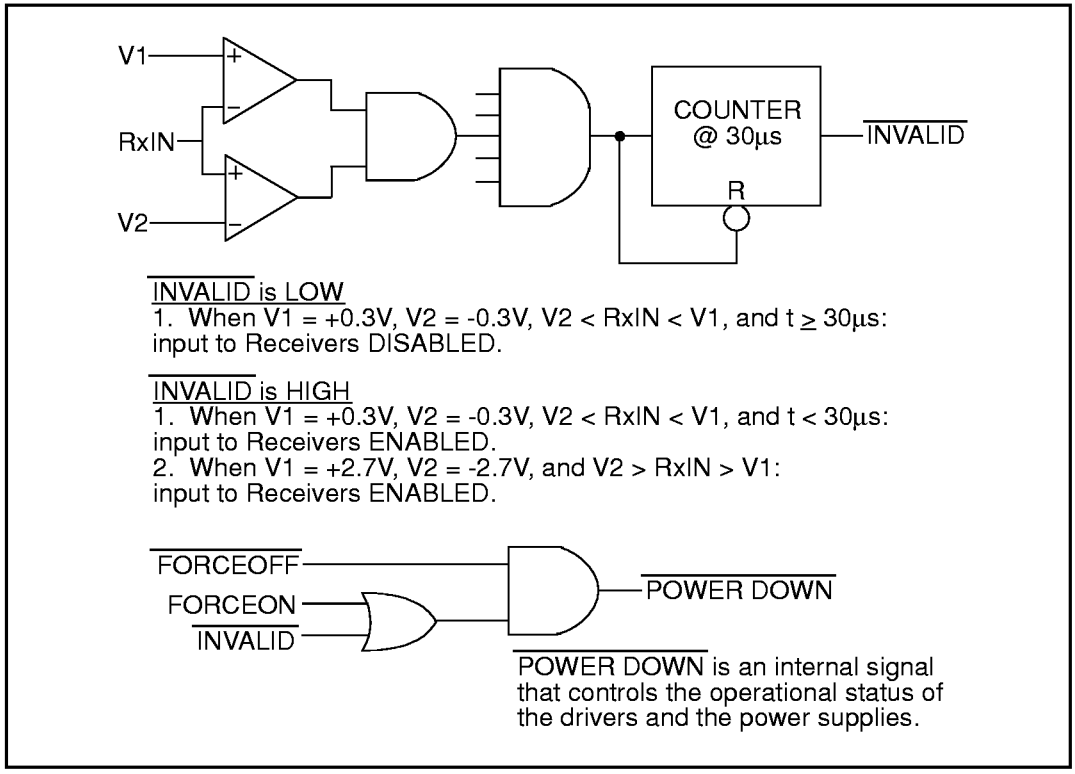


Figure 24. Auto-Online Circuitry Logic

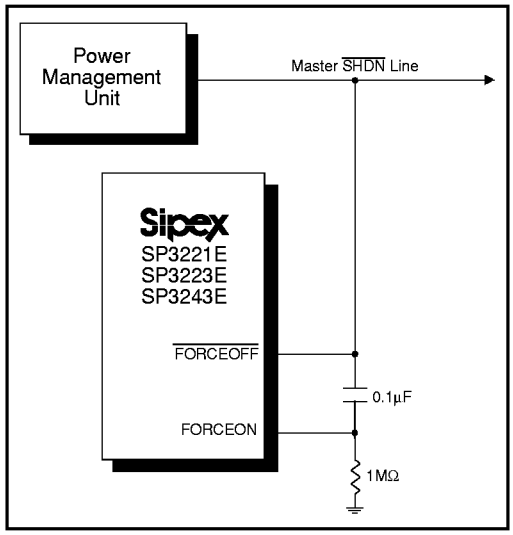


Figure 25. Auto-Online Circuitry to wake up a mouse or another system

Auto-Online Circuitry

The **SP3221E/3223E/3243E** devices have an ***Auto-Online*** Circuitry on board that will save power in the system the devices are designed into without changes to the existing BIOS or operating system.

When FORCEON is LOW and $\overline{\text{FORCEOFF}}$ is HIGH, the **SP3221E/3223E/3243E** devices are in the ***Auto-Online*** mode and a 1µA supply current is achieved. When the **SP3221E/3223E/3243E** devices sense no valid RS-232 signal levels at all receiver inputs for 30µs, the **SP3221E/3223E/3243E** drivers and on-board power supply are shut off, reducing the supply current to 1µA. This can commonly occur in hand-held or portable applications where the RS-232 cable is disconnected or the connected peripheral drivers are turned off. The **SP3221E/3223E/3243E** devices will come online when a valid RS-232 level signal is applied to any receiver input.

In the ***Auto-Online*** mode, the $\overline{\text{INVALID}}$ output is HIGH when the device is on and LOW when the device is shut down. The $\overline{\text{INVALID}}$ pin can be used in any mode as an indicator of all **SP3221E/3223E/3243E** receiver inputs. *Table 3* and *Figure 24* summarize the logic of the ***Auto-Online*** operating modes. The truth table logic of the **SP3221E/3223E/3243E** Driver and Receiver outputs can be found in *Table 2*.

FORCEON and $\overline{\text{FORCEOFF}}$ override the Auto-Online feature and can force the transceivers into its normal operating or low-power standby states. With neither FORCEON or $\overline{\text{FORCEOFF}}$ asserted, the **SP3221E/3223E/3243E** devices will select between these states automatically based on receiver input levels. Valid and invalid RS-232 receiver levels can be referred to in *Figure 24*.

Figure 25 shows a circuit that can be implemented to force the transmitters on for 100ms, allowing enough time for a system with the Auto-Online circuitry to reallize that the **SP3221E/3223E/3243E** devices are awake. If the other system outputs valid RS-232 signals with the 100ms timeframe, the RS-232 ports on both systems remain enabled.

Figure 26 depicts the electrical operation of the charge pump voltage levels during shut down. When the **SP3221E/3223E/3243E** devices are shut down, the charge pumps are turned off.

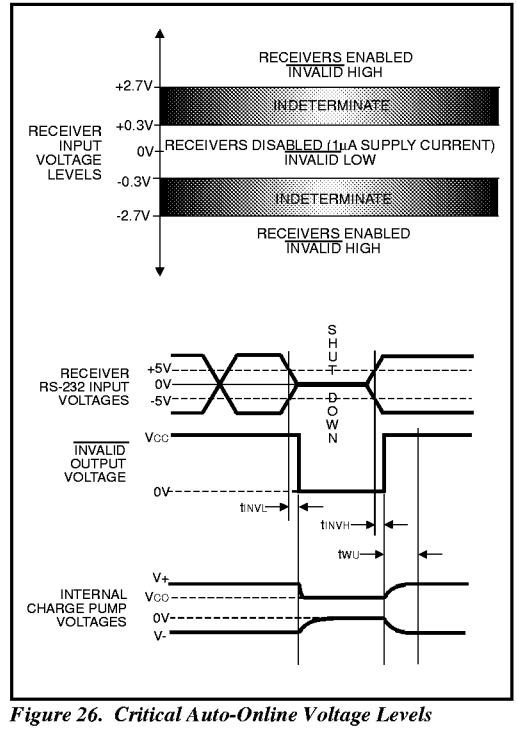


Figure 26. Critical Auto-Online Voltage Levels

V+ decays to V_{CC}, V- decays to GND, and the driver outputs are tri-stated (high impedance). The time required to exit the shut down state is typically 100µs.

If designs using the **SP3221E/3223E/3243E** require software programmability, $\overline{\text{INVALID}}$ can be used to indicate DTR or a Ring Indicator signal. Tying FORCEON and $\overline{\text{FORCEOFF}}$ together will bypass the ***Auto-Online*** circuitry so the line acts like a $\overline{\text{SHDN}}$ input.

ESD TOLERANCE

The **SP3221E/3223E/3243E** series incorporates ruggedized ESD cells on all driver output and receiver input pins. The ESD structure is improved over our previous family for more rugged applications and environments sensitive to electro-static discharges and associated transients. The improved ESD tolerance is at least ±15kV without damage nor latch-up.

There are different methods of ESD testing applied:

a) MIL-STD-883, Method 3015.7
b) IEC1000-4-2 Air-Discharge
c) IEC1000-4-2 Direct Contact

The Human Body Model has been the generally accepted ESD testing method for semiconductors. This method is also specified in MIL-STD-883, Method 3015.7 for ESD testing. The premise of this ESD test is to simulate the human body's potential to store electro-static energy and discharge it to an integrated circuit. The simulation is performed by using a test model as shown in *Figure 27*. This method will test the IC's capability to withstand an ESD transient during normal handling such as in manufacturing areas where the ICs tend to be handled frequently.

The IEC-1000-4-2, formerly IEC801-2, is generally used for testing ESD on equipment and systems. For system manufacturers, they must guarantee a certain amount of ESD protection since the system itself is exposed to the outside environment and human presence. The premise with IEC1000-4-2 is that the system is required to withstand an amount of static electricity when ESD is applied to points and surfaces of the equipment that are accessible to personnel during normal usage. The transceiver IC receives most of the ESD current when the ESD source is applied to the connector pins. The test circuit for IEC1000-4-2 is shown on *Figure 28*. There are two methods within IEC1000-4-2, the Air Discharge method and the Contact Discharge method.

With the Air Discharge Method, an ESD voltage is applied to the equipment under test (EUT) through air. This simulates an electrically charged person ready to connect a cable onto the rear of the system only to find an unpleasant zap just before the person touches the back panel. The high energy potential on the person discharges through an arcing path to the rear panel of the system before he or she even touches the system. This energy, whether discharged directly or through air, is predominantly a function of the discharge current rather than the discharge voltage. Variables with an air discharge such as approach speed of the object carrying the ESD potential to the system and humidity will tend to change the discharge current. For example, the rise time of the discharge current varies with the approach speed.

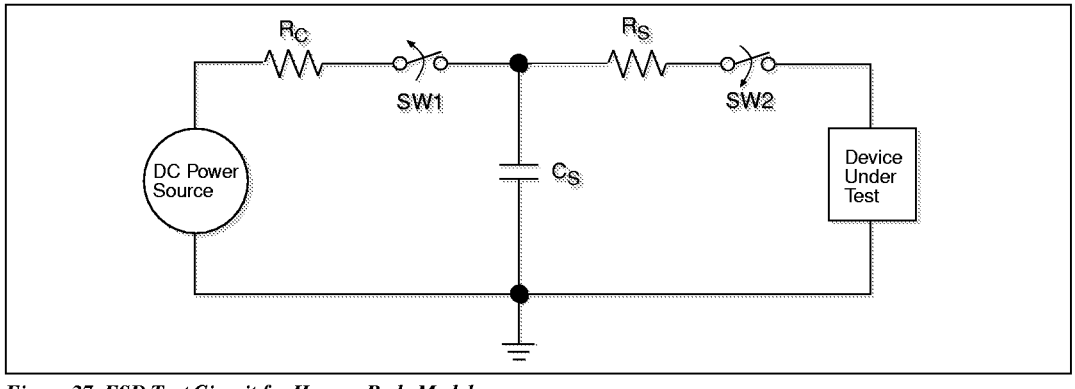


Figure 27. ESD Test Circuit for Human Body Model

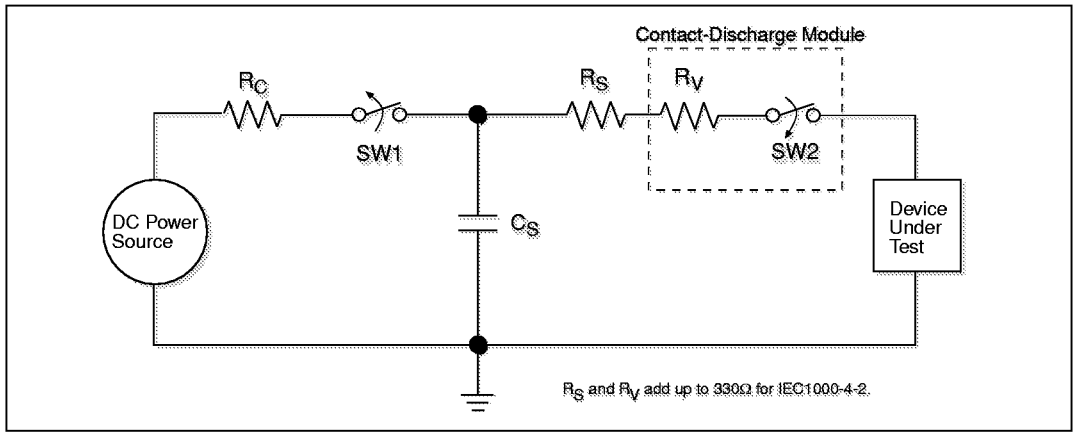


Figure 28. ESD Test Circuit for IEC1000-4-2

The Contact Discharge Method applies the ESD current directly to the EUT. This method was devised to reduce the unpredictability of the ESD arc. The discharge current rise time is constant since the energy is directly transferred without the air-gap arc. In situations such as hand held systems, the ESD charge can be directly discharged to the equipment from a person already holding the equipment. The current is transferred on to the keypad or the serial port of the equipment directly and then travels through the PCB and finally to the IC.

The circuit model in *Figures 27* and *28* represent the typical ESD testing circuit used for all three methods. The C_S is initially charged with the DC power supply when the first switch (SW1) is on. Now that the capacitor is charged, the second switch (SW2) is on while SW1 switches off. The voltage stored in the capacitor is then applied through R_S, the current limiting resistor, onto the device under test (DUT). In ESD tests, the SW2 switch is pulsed so that the device under test receives a duration of voltage.

For the Human Body Model, the current limiting resistor (R_S) and the source capacitor (C_S) are 1.5kΩ an 100pF, respectively. For IEC-1000-4-2, the current limiting resistor (R_S) and the source capacitor (C_S) are 330Ω an 150pF, respectively.

The higher C_S value and lower R_S value in the IEC1000-4-2 model are more stringent than the Human Body Model. The larger storage capacitor injects a higher voltage to the test point when SW2 is switched on. The lower current limiting resistor increases the current charge onto the test point.

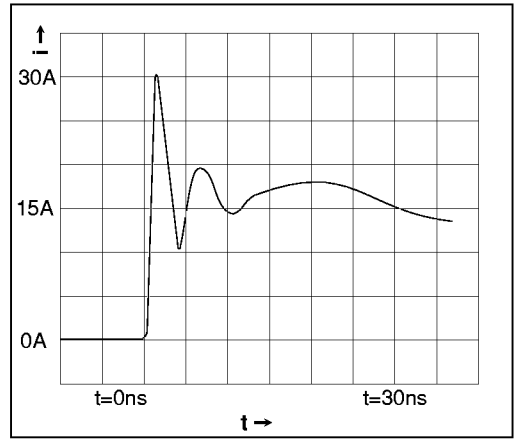
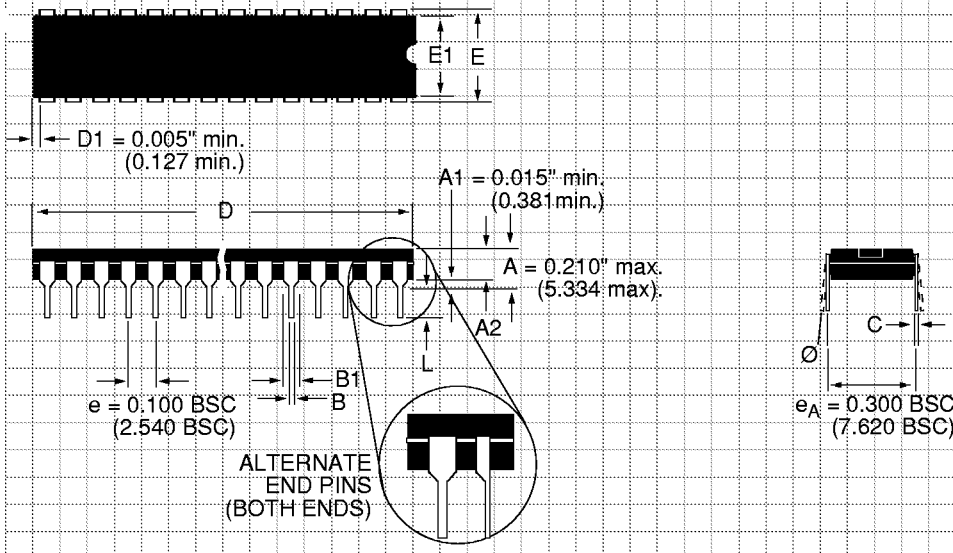


Figure 29. ESD Test Waveform for IEC1000-4-2

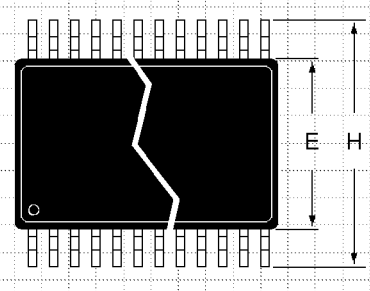
DEVICE PIN TESTED	HUMAN BODY MODEL	IEC1000-4-2		
		Air Discharge	Direct Contact	Level
Driver Outputs	±15kV	±15kV	±8kV	4
Receiver Inputs	±15kV	±15kV	±8kV	4

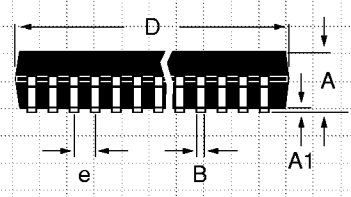
PACKAGE: PLASTIC DUAL–IN–LINE (NARROW)

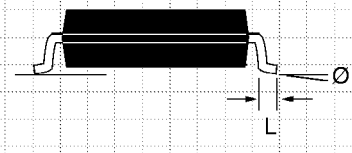


DIMENSIONS (Inches) Minimum/Maximum (mm)	16–PIN	20–PIN	28–PIN
A2	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)	0.068/0.078 (1.73/1.99)
B	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)	0.002/0.008 (0.05/0.21)
B1	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)	0.010/0.015 (0.25/0.38)
C	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)	0.397/0.407 (10.07/10.33)
D	0.780/0.800 (19.812/20.320)	0.980/1.060 (24.892/26.924)	0.205/0.212 (5.20/5.38)
E	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)	0.0256 BSC (0.65 BSC)
E1	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)	0.301/0.311 (7.65/7.90)
L	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)	0.022/0.037 (0.55/0.95)
Ø	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)	0°/8° (0°/8°)

PACKAGE: PLASTIC SHRINK SMALL OUTLINE (SSOP)

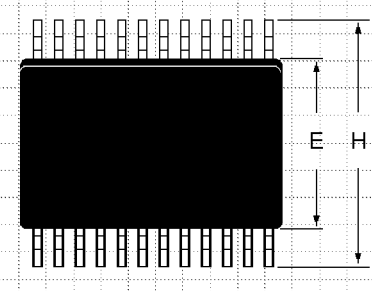


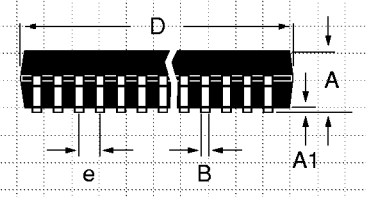


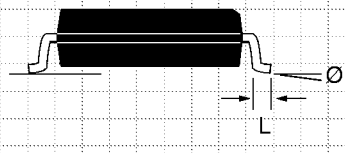


DIMENSIONS (Inches) Minimum/Maximum (mm)	16–PIN	20–PIN	24–PIN	28–PIN
A	0.068/0.078 (1.73/1.99)	0.068/0.078 (1.73/1.99)	0.068/0.078 (1.73/1.99)	0.068/0.078 (1.73/1.99)
A1	0.002/0.008 (0.05/0.21)	0.002/0.008 (0.05/0.21)	0.002/0.008 (0.05/0.21)	0.002/0.008 (0.05/0.21)
B	0.010/0.015 (0.25/0.38)	0.010/0.015 (0.25/0.38)	0.010/0.015 (0.25/0.38)	0.010/0.015 (0.25/0.38)
D	0.239/0.249 (6.07/6.33)	0.278/0.289 (7.07/7.33)	0.317/0.328 (8.07/8.33)	0.397/0.407 (10.07/10.33)
E	0.205/0.212 (5.20/5.38)	0.205/0.212 (5.20/5.38)	0.205/0.212 (5.20/5.38)	0.205/0.212 (5.20/5.38)
e	0.0256 BSC (0.65 BSC)	0.0256 BSC (0.65 BSC)	0.0256 BSC (0.65 BSC)	0.0256 BSC (0.65 BSC)
H	0.301/0.311 (7.65/7.90)	0.301/0.311 (7.65/7.90)	0.301/0.311 (7.65/7.90)	0.301/0.311 (7.65/7.90)
L	0.022/0.037 (0.55/0.95)	0.022/0.037 (0.55/0.95)	0.022/0.037 (0.55/0.95)	0.022/0.037 (0.55/0.95)
Ø	0°/8° (0°/8°)	0°/8° (0°/8°)	0°/8° (0°/8°)	0°/8° (0°/8°)

PACKAGE: PLASTIC SMALL OUTLINE (SOIC) (WIDE)

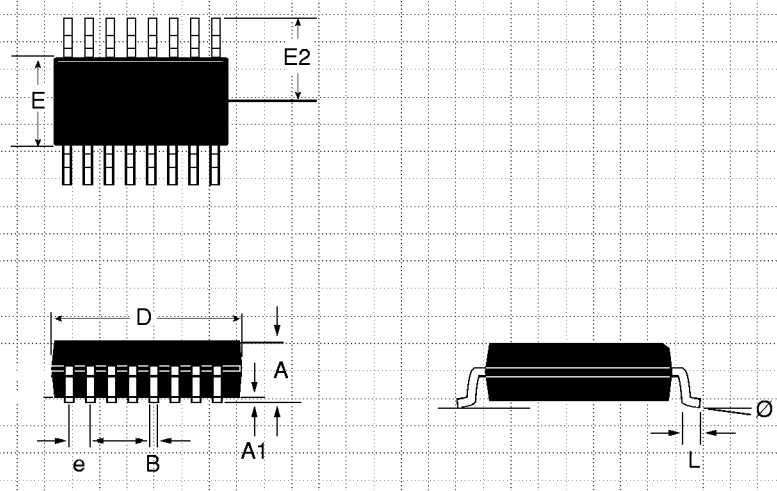






DIMENSIONS (Inches) Minimum/Maximum (mm)	28–PIN
A	0.093/0.104 (2.352/2.649)
A1	0.004/0.012 (0.102/0.300)
B	0.013/0.020 (0.330/0.508)
D	0.697/0.713 (17.70/18.09)
E	0.291/0.299 (7.402/7.600)
e	0.050 BSC (1.270 BSC)
H	0.394/0.419 (10.00/10.64)
L	0.016/0.050 (0.406/1.270)
Ø	0°/8° (0°/8°)

PACKAGE: PLASTIC THIN SMALL OUTLINE (TSSOP)



DIMENSIONS in inches (mm) Minimum/Maximum	16–PIN	20–PIN
A	- /0.043 (- /1.10)	- /0.043 (- /1.10)
A1	0.002/0.006 (0.05/0.15)	0.002/0.006 (0.05/0.15)
B	0.007/0.012 (0.19/0.30)	0.007/0.012 (0.19/0.30)
D	0.193/0.201 (4.90/5.10)	0.252/0.260 (6.40/6.60)
E	0.169/0.177 (4.30/4.50)	0.169/0.177 (4.30/4.50)
e	0.026 BSC (0.65 BSC)	0.026 BSC (0.65 BSC)
E2	0.126 BSC (3.20 BSC)	0.126 BSC (3.20 BSC)
L	0.020/0.030 (0.50/0.75)	0.020/0.030 (0.50/0.75)
Ø	0°/8°	0°/8°

ORDERING INFORMATION

Model	Temperature Range	Package Types
SP3221ECP	0°C to +70°C	16-pin PDIP
SP3221ECA	0°C to +70°C	16-pin SSOP
SP3223ECP	0°C to +70°C	20-pin PDIP
SP3223ECA	0°C to +70°C	20-pin SSOP
SP3223ECY	0ºC to +70ºC	20-pin TSSOP
SP3243ECT	0°C to +70°C	28-pin Wide SOIC
SP3243ECA	0°C to +70°C	28-pin SSOP

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