

# MITSUBISHI HIGH SPEED CMOS M74HC08P/FP/DP

## QUADRUPLE 2-INPUT POSITIVE AND GATE

### DESCRIPTION

The M74HC08 is a semiconductor integrated circuit consisting of four 2-input positive-logic AND gates, usable as negative-logic OR gates.

### FEATURES

- High-speed: 9.5ns typ. ( $C_L=15\text{pF}$ ,  $V_{CC}=5\text{V}$ )
- Low power dissipation:  $5\mu\text{W}/\text{package}$ , max ( $V_{CC}=5\text{V}$ ,  $T_a=25^\circ\text{C}$ , quiescent state)
- High noise margin: 30% of  $V_{CC}$ , min ( $V_{CC}=4.5\text{V}$ ,  $6\text{V}$ )
- Capable of driving 10 74LS TTL loads
- Wide operating voltage range:  $V_{CC}=2\sim 6\text{V}$
- Wide operating temperature range:  $T_a=-40\sim +85^\circ\text{C}$

### APPLICATION

General purpose, for use in industrial and consumer digital equipment.

### FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC08 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS08.

Buffered outputs Y improve input-to-output transfer characteristics and minimizes output impedance variations with respect to input voltage variations.

When both inputs A and B are high, the output Y will become high, and when at least one of the inputs is low, Y will become low.

### FUNCTION TABLE

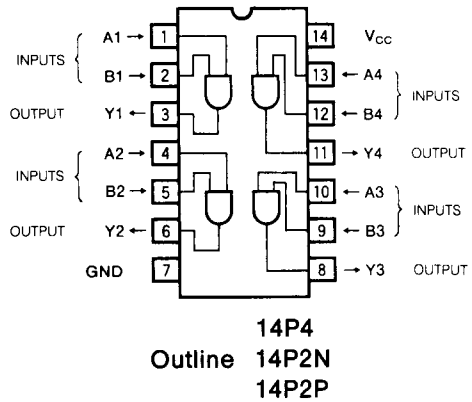
Inputs		Output
A	B	Y
L	L	L
H	L	L
L	H	L
H	H	H

### ABSOLUTE MAXIMUM RATINGS ( $T_a = -40\sim +85^\circ\text{C}$ , unless otherwise noted)

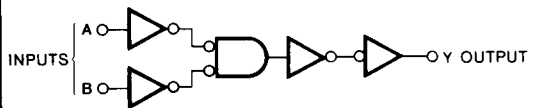
Symbol	Parameter	Conditions	Ratings	Unit
$V_{CC}$	Supply voltage		$-0.5\sim +7.0$	V
$V_i$	Input voltage		$-0.5\sim V_{CC}+0.5$	V
$V_o$	Output voltage		$-0.5\sim V_{CC}+0.5$	V
$I_{IK}$	Input protection diode current	$V_i < 0\text{V}$	-20	mA
		$V_i > V_{CC}$	20	
$I_{OK}$	Output parasitic diode current	$V_o < 0\text{V}$	-20	mA
		$V_o > V_{CC}$	20	
$I_o$	Output current per output pin		$\pm 25$	mA
$I_{CC}$	Supply/GND current	$V_{CC}$ , GND	$\pm 50$	mA
$P_d$	Power dissipation	(Note 1)	500	mW
$T_{stg}$	Storage temperature range		$-65\sim +150$	$^\circ\text{C}$

Note 1 : M74HC08FP,  $T_a = -40\sim +60^\circ\text{C}$  and  $T_a = 60\sim 85^\circ\text{C}$  are derated at  $-6\text{mW}/^\circ\text{C}$ .  
M74HC08DP,  $T_a = -40\sim +50^\circ\text{C}$  and  $T_a = 50\sim 85^\circ\text{C}$  are derated at  $-5\text{mW}/^\circ\text{C}$ .

### PIN CONFIGURATION (TOP VIEW)



### LOGIC DIAGRAM (EACH GATE)



QUADRUPLE 2-INPUT POSITIVE AND GATE

RECOMMENDED OPERATING CONDITIONS ( $T_a = -40 \sim +85^\circ\text{C}$ )

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
$V_{CC}$	Supply voltage	2		6	V
$V_i$	Input voltage	0		$V_{CC}$	V
$V_o$	Output voltage	0		$V_{CC}$	V
$T_{opr}$	Operating temperature range	-40		+85	$^\circ\text{C}$
$t_r, t_f$	Input risetime, falltime	$V_{CC} = 2.0\text{V}$	0	1000	ns
		$V_{CC} = 4.5\text{V}$	0	500	
		$V_{CC} = 6.0\text{V}$	0	400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions	Limits						Unit	
			$V_{CC}(\text{V})$	25 $^\circ\text{C}$			-40 $^\circ\text{C}$ ~ +85 $^\circ\text{C}$			
				Min	Typ	Max	Min	Max		
$V_{IH}$	High-level input voltage	$V_o = 0.1\text{V}, V_{CC} = 0.1\text{V}$ $ I_o  = 20\mu\text{A}$	2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		V	
$V_{IL}$	Low-level input voltage	$V_o = 0.1\text{V}$ $ I_o  = 20\mu\text{A}$	2.0 4.5 6.0			0.5 1.35 1.8	0.5 1.35 1.8		V	
$V_{OH}$	High-level output voltage	$V_i = V_{IH}$	$I_{OH} = -20\mu\text{A}$	2.0	1.9			1.9		V
			$I_{OH} = -20\mu\text{A}$	4.5	4.4			4.4		
			$I_{OH} = -20\mu\text{A}$	6.0	5.9			5.9		
			$I_{OH} = -4.0\text{mA}$	4.5	4.18			4.13		
			$I_{OH} = -5.2\text{mA}$	6.0	5.68			5.63		
$V_{OL}$	Low-level output voltage	$V_i = V_{IH}, V_{IL}$	$I_{OL} = 20\mu\text{A}$	2.0			0.1	0.1	V	
			$I_{OL} = 20\mu\text{A}$	4.5			0.1	0.1		
			$I_{OL} = 20\mu\text{A}$	6.0			0.1	0.1		
			$I_{OL} = 4.0\text{mA}$	4.5			0.26	0.33		
			$I_{OL} = 5.2\text{mA}$	6.0			0.26	0.33		
$I_{IH}$	High-level input current	$V_i = 6\text{V}$	6.0			0.1		1.0	$\mu\text{A}$	
$I_{IL}$	Low-level input current	$V_i = 0\text{V}$	6.0			-0.1		-1.0	$\mu\text{A}$	
$I_{CC}$	Quiescent supply current	$V_i = V_{CC}, \text{GND}, I_o = 0\mu\text{A}$	6.0			1.0		10.0	$\mu\text{A}$	

QUADRUPLE 2-INPUT POSITIVE AND GATE

SWITCHING CHARACTERISTICS ( $V_{CC} = 5V, T_a = 25^\circ C$ )

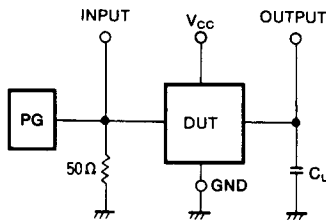
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{TLH}$	Low-level to high-level and high-level to low-level output transition time	$C_L = 15pF$ (Note 3)			10	ns
$t_{THL}$					10	
$t_{PLH}$	Low-level to high-level and high-level to low-level output propagation time				15	ns
$t_{PHL}$					20	

SWITCHING CHARACTERISTICS ( $V_{CC} = 2\sim 6V, T_a = -40\sim +85^\circ C$ )

Symbol	Parameter	Test conditions	Limits						Unit
			25°C			-40~+85°C			
			$V_{CC}(V)$	Min	Typ	Max	Min	Max	
$t_{TLH}$	Low-level to high-level and high-level to low-level output transition time	$C_L = 50pF$ (Note 3)	2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
$t_{THL}$	output transition time		2.0			75		95	ns
			4.5			15		19	
			6.0			13		16	
$t_{PLH}$	Low-level to high-level and high-level to low-level output propagation time	2.0			121		151	ns	
		4.5			24		30		
		6.0			20		25		
$t_{PHL}$	output propagation time	2.0			121		151	ns	
		4.5			24		30		
		6.0			20		25		
$C_I$	Input capacitance				10		10	pF	
$C_{PD}$	Power dissipation capacitance (Note 2)			40				pF	

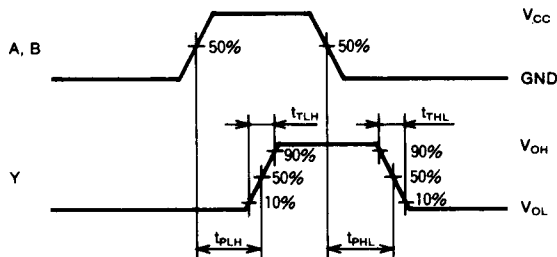
Note 2 :  $C_{PD}$  is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per gate)  
The power dissipation during operation under no-load conditions is calculated using the following formula:  
 $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$

Note 3 : Test Circuit



- (1) The pulse generator (PG) has the following characteristics (10%~90%):  $t_r = 6ns, t_f = 6ns$
- (2) The capacitance  $C_L$  includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



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PACKAGE OUTLINES

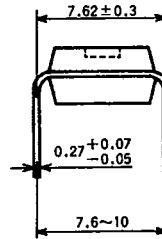
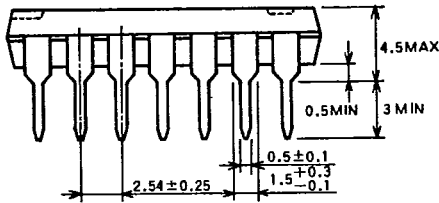
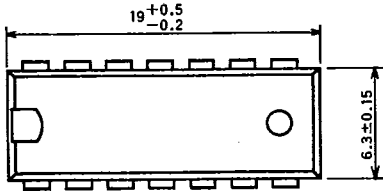
6249827 MITSUBISHI (DGTL LOGIC)

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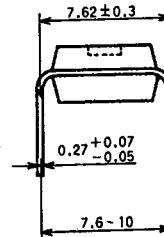
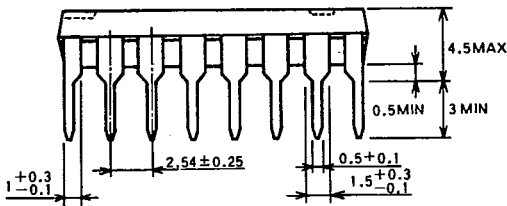
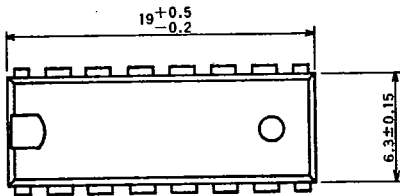
TYPE 14P4 14-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE 16P4 16-PIN MOLDED PLASTIC DIP

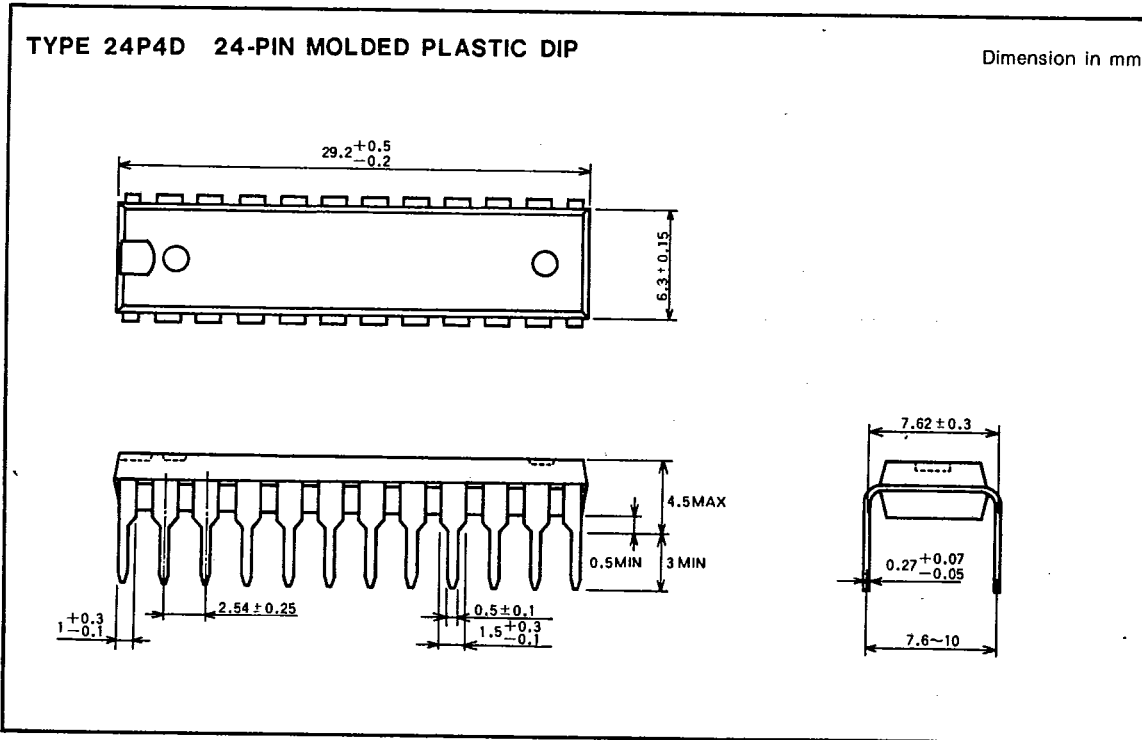
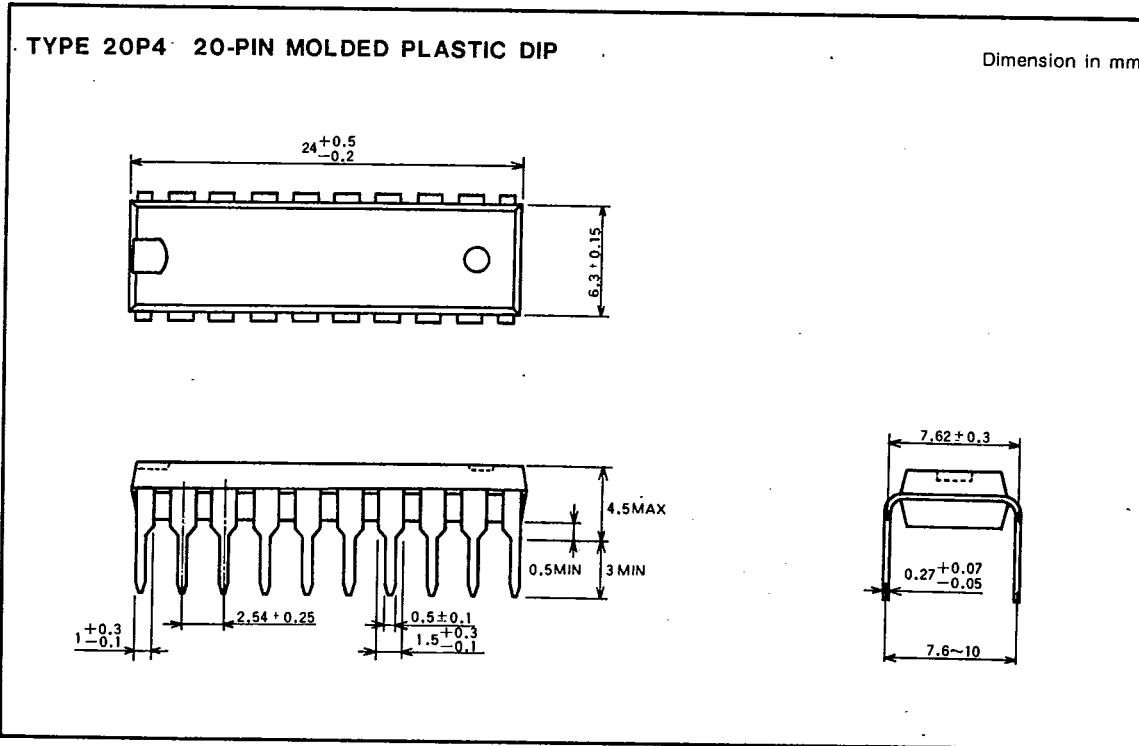
Dimension in mm



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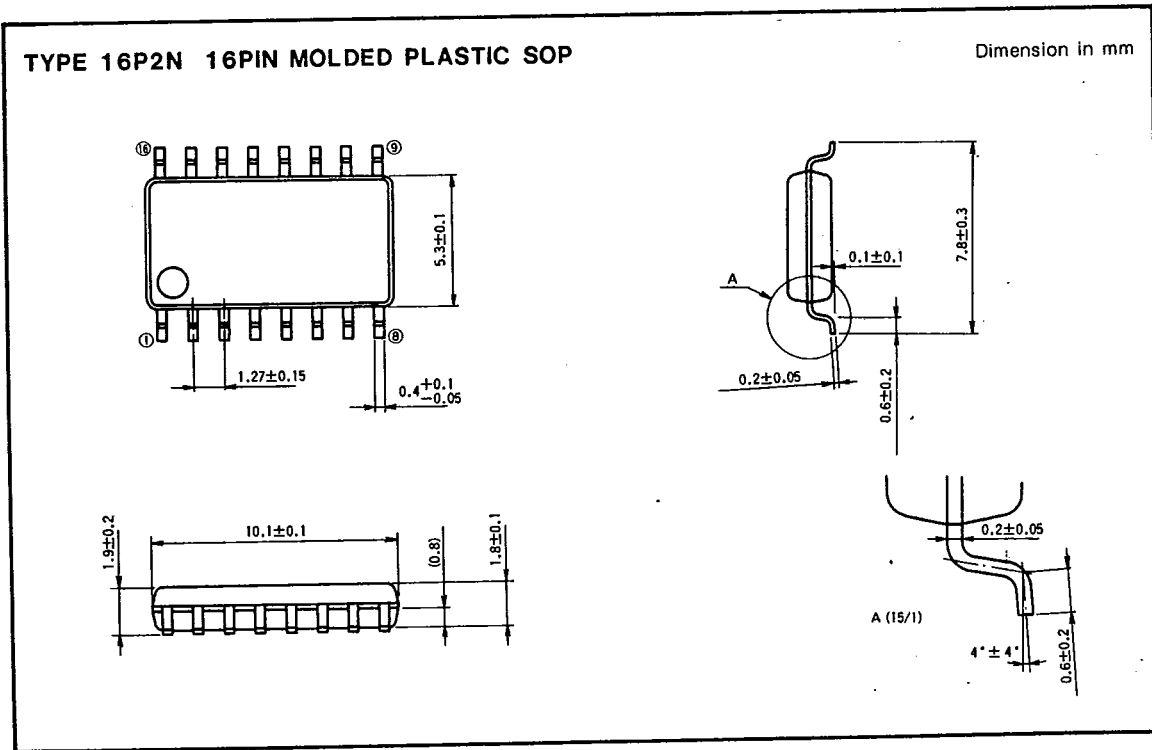
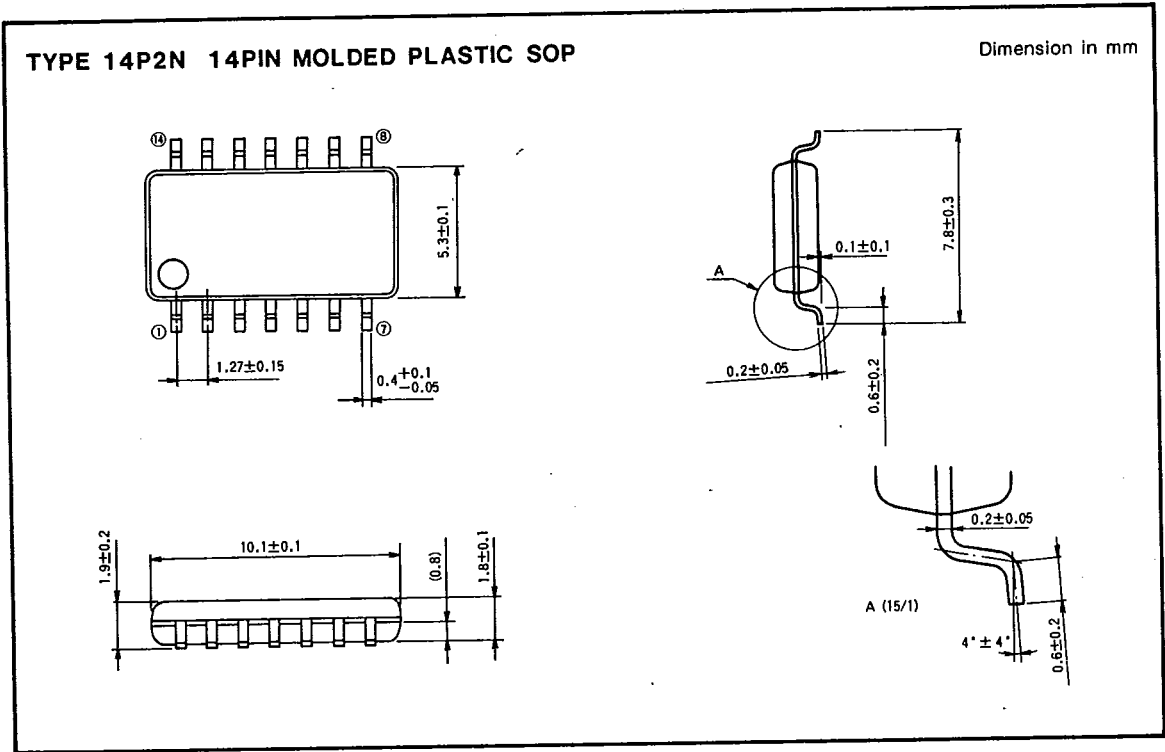
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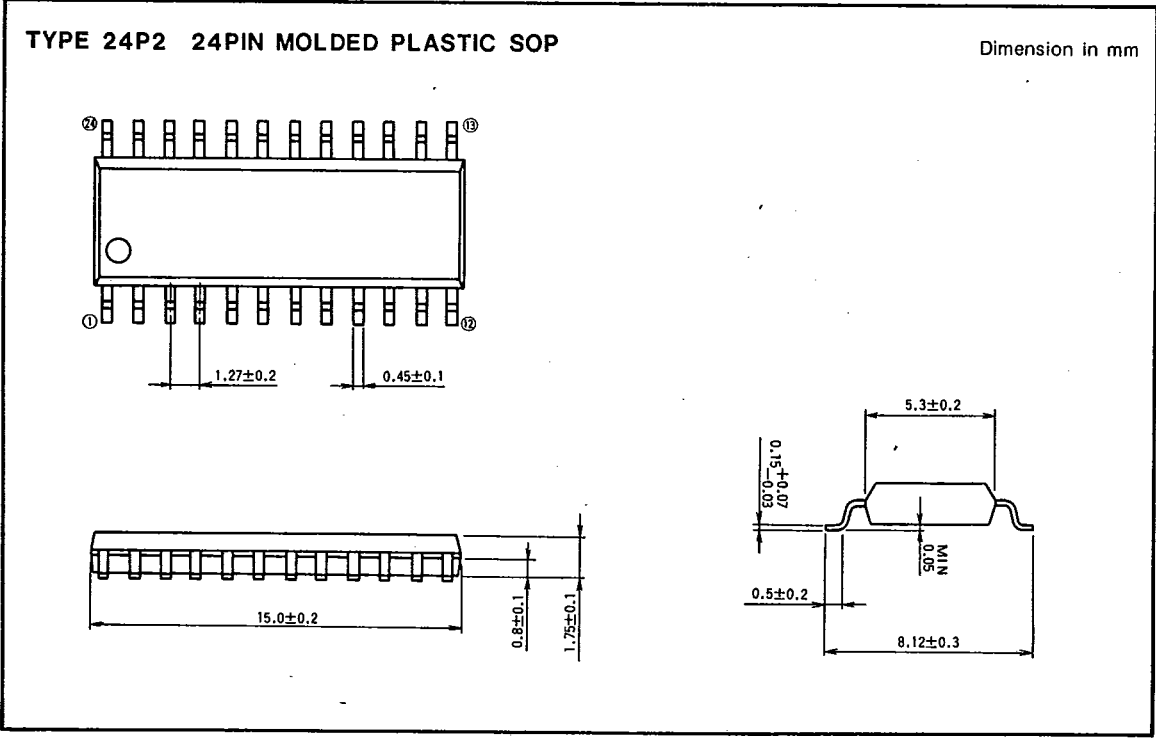
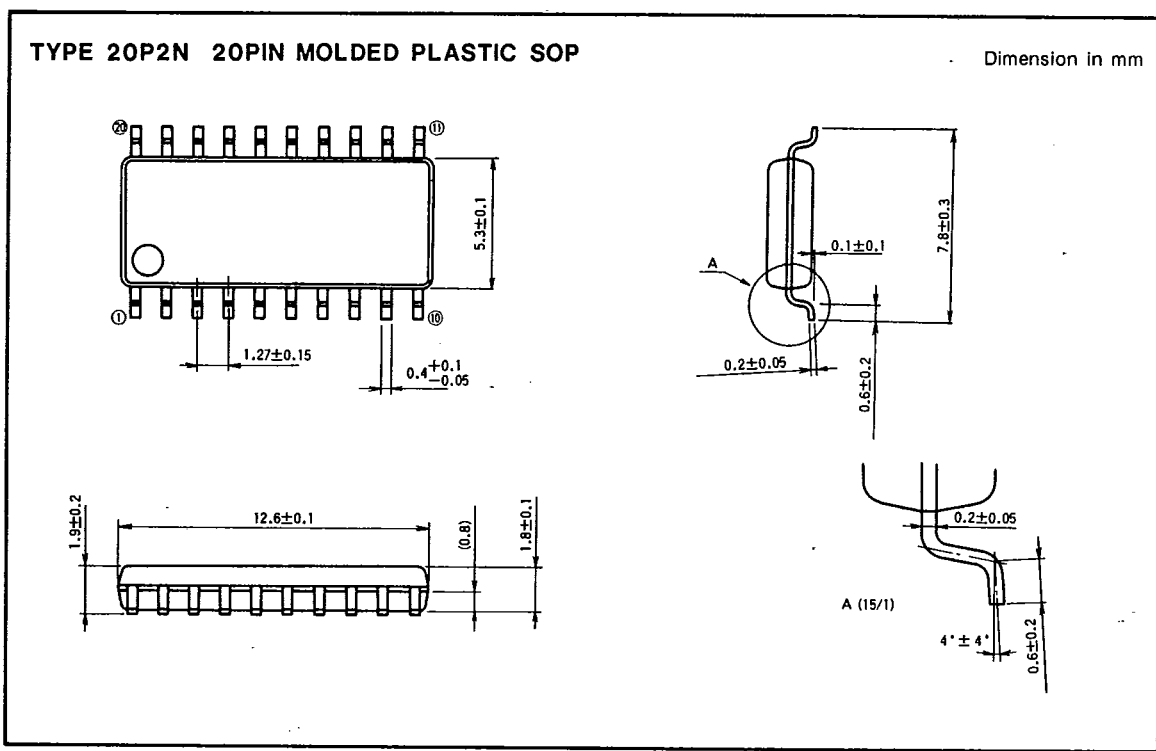
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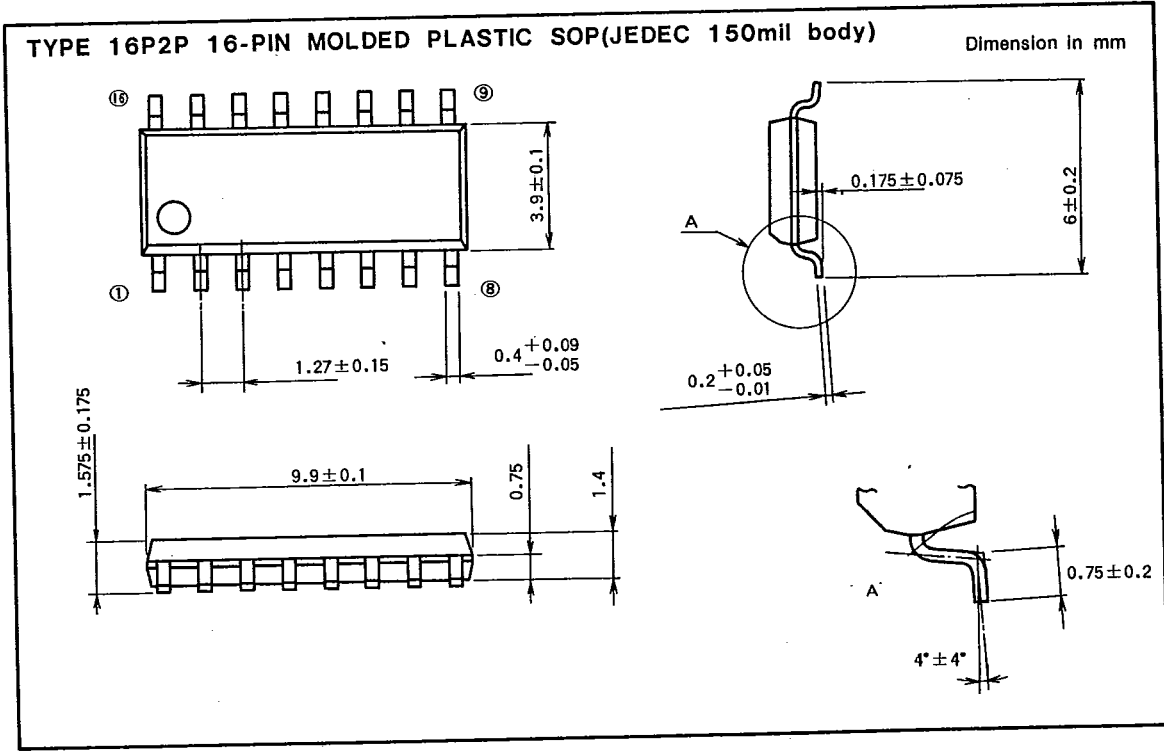
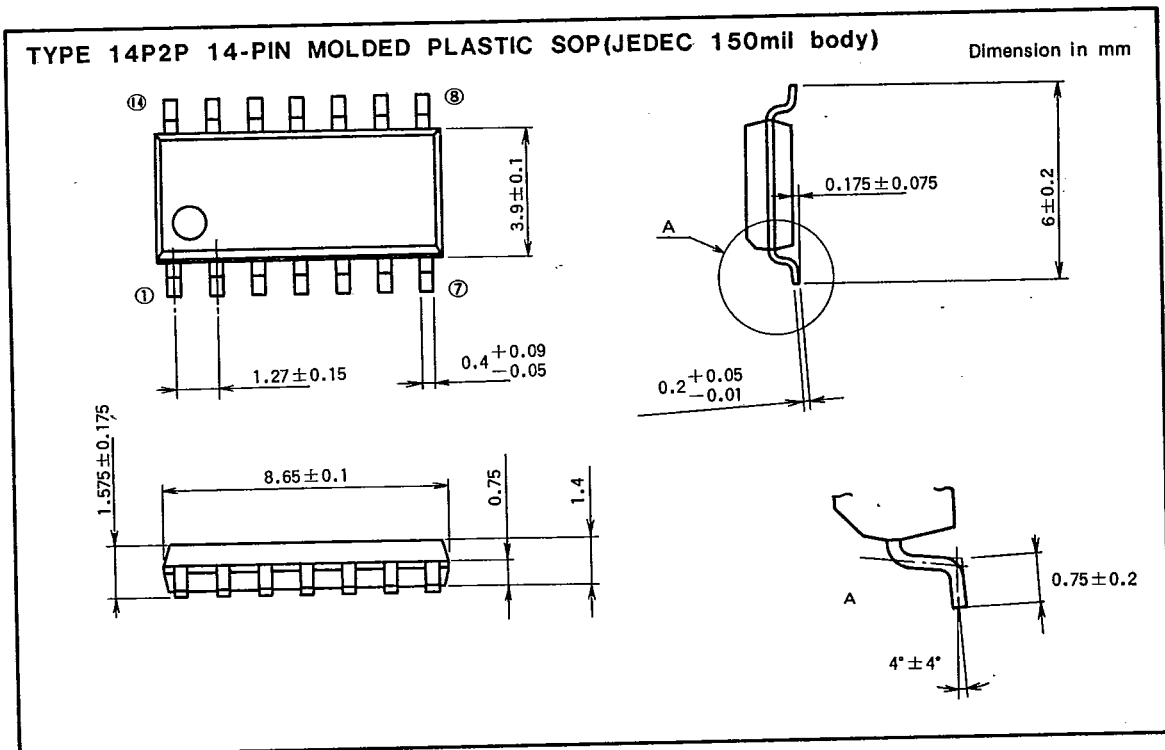
91D 12851 D T-90.20





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91D 12853 D T90-20



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