CMOS Quad Sample-and-Hold Amplifier

SMP-04

FEATURES

- Four Independent Sample-and-Holds
- Internal Hold Capacitors
- High Accuracy – 12-Bit
- Very Low Droop Rate (2mV/s Typ)
- Output Buffers Stable for $C_L \leq 500pF$
- TTL/CMOS Compatible Logic Inputs
- Single or Dual Supply Applications
- Monolithic Low Power CMOS Design

APPLICATIONS

- Signal Processing Systems
- Multichannel Data Acquisition Systems
- Automatic Test Equipment
- Medical and Analytical Instrumentation
- Event Analysis
- DAC Deglitching

ORDERING INFORMATION †

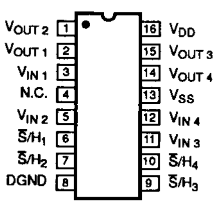
PACKAGE		OPERATING TEMPERATURE RANGE
PLASTIC 16-PIN	CERDIP 16-PIN	
—	SMP04AQ/883*	MIL
SMP04EP	SMP04EQ	XIND
SMP04ES††	—	XIND

* Consult factory for 883 data sheet.

† Burn-in is available on extended industrial temperature range parts in CerDIP and plastic DIP packages.

†† For availability and burn-in information on SO packages, contact your local sales office.

PIN CONNECTIONS



16-PIN CERDIP (Q-Suffix)

16-PIN PLASTIC DIP (P-Suffix)

16-PIN SO (S-Suffix)

GENERAL DESCRIPTION

The SMP-04 is a monolithic quad sample-and-hold; it has four internal precision buffer amplifiers and internal hold capacitors. It is manufactured in PMI's advanced oxide isolated CMOS technology to obtain high accuracy, low droop rate and fast acquisition time required by data acquisition and signal processing systems. The device can acquire an 8-bit input signal to ±1/2 LSB in less than seven microseconds. The SMP-04 can operate from single or dual power supplies with TTL/CMOS logic compatibility. Its output swing includes the negative supply.

The SMP-04 is ideally suited for a wide variety of sample-and-hold applications including amplifier offset or VCA gain adjustments. One or more can be used with a single or multiple DACs to provide multiple set points within a system.

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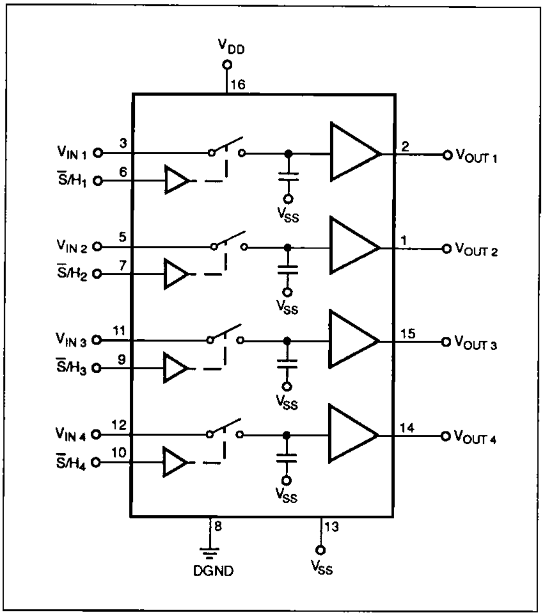
The SMP-04 offers significant cost and size reduction over equivalent module or discrete designs. It is available in a 16-pin hermetic or plastic DIP and surface mount SOIC packages. It is specified over the extended industrial temperature range of –40°C to +85°C. See SMP-04/883 data sheet for –55°C to +125°C specifications.

FUNCTIONAL DIAGRAM



Manufactured under the following U.S. patent: 4,739,281

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

V_{DD} to DGND .... –0.3V, 17V
V_{DD} to V_{SS} .... –0.7V, 17V
V_{LOGIC} to DGND .... –0.3V, V_{DD}
V_{IN} to DGND .... V_{SS}, V_{DD}
V_{OUT} to DGND .... V_{SS}, V_{DD}
Analog Output Current .... ±20mA
(Not short-circuit protected)
Digital Input Voltage to DGND .... –0.3V, V_{DD} +0.3V
Operating Temperature Range
EQ, EP, ES .... –40°C to +85°C
AQ .... –55°C to +125°C
Junction Temperature .... +150°C
Storage Temperature .... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) .... +300°C

PACKAGE TYPE	Θ_{jA} (Note 1)	Θ_{jC}	UNITS
16-Pin CerDIP (Q)	94	12	°C/W
16-Pin Plastic DIP (P)	76	33	°C/W
16-Pin SO (S)	92	27	°C/W

NOTE:
1. Θ_{jA} is specified for worst case mounting conditions, i.e., Θ_{jA} is specified for device in socket for CerDIP and P-DIP packages; Θ_{jA} is specified for device soldered to printed circuit board for SO package.

CAUTION:
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and function operation at or above this specification is not implied. Exposure to the above maximum rating conditions for extended periods may affect device reliability.
2. Digital inputs and outputs are protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam or packaging at all times until ready to use. Use proper anti-static handling procedures.
3. Remove power before inserting or removing units from their sockets.

ELECTRICAL CHARACTERISTICS at V_{DD} = +12.0V, V_{SS} = DGND = 0V, R_L = No Load, T_A = Operating Temperature Range specified in Absolute Maximum Ratings, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	SMP-04 MIN	TYP	MAX	UNITS
Linearity Error			–	0.01	–	%
Buffer Offset Voltage	V_{OS}	V_{IN} = 6V	–10	±2.5	+10	mV
Hold Step	V_{HS}	V_{IN} = 6V	–	1	±4	mV
Droop Rate	ΔV/Δt	V_{IN} = 6V, T_A = +25°C	–	2	25	mV/s
Output Source Current	I_{SOURCE}	V_{IN} = 6V (Note 1)	1.2	–	–	mA
Output Sink Current	I_{SINK}	V_{IN} = 6V (Note 1)	0.5	–	–	mA
Output Voltage Range	OVR	R_L = 20kΩ R_L = 10kΩ	0.06 0.06	– –	10.0 9.5	V
LOGIC CHARACTERISTICS						
Logic Input High Voltage	V_{INH}		2.4	–	–	V
Logic Input Low Voltage	V_{INL}		–	–	0.8	V
Logic Input Current	I_{IN}		–	0.5	1	µA
DYNAMIC PERFORMANCE (Note 2)						
Acquisition Time	t_A	T_A = +25°C, 0 to 10V step to 0.1%	–	7	–	µs
Acquisition Time	t_A	T_A = +25°C, 0 to 10V step to 0.01%	–	9	–	µs
Hold Mode Settling Time	t_H	To 1mV	–	1	–	µs
Slew Rate	SR	R_L = 20kΩ (Note 3)	3	4	–	V/µs
Capacitive Load Stability	C_L	<30% Overshoot	–	500	–	pF
Analog Crosstalk		0 to 10V step	–	–80	–	dB
SUPPLY CHARACTERISTICS						
Power Supply Rejection Ratio	PSRR	10.8 ≤ V_{DD} ≤ 13.2V	60	75	–	dB
Supply Current	I_{DD}		–	4	7	mA
Power Dissipation	P_{DIS}		–	–	84	mW

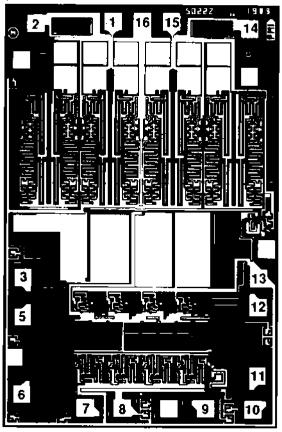
NOTES:
1. Outputs are capable of sinking and sourcing over 20mA but linearity and offset are guaranteed at specified load levels.
2. All input control signals are specified with t_r = t_f = 5ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.
3. Slew rate is measured in the sample mode with a 0 to 10 volt step from 20 to 80%.

ELECTRICAL CHARACTERISTICS at V_{DD} = +5.0V, V_{SS} = –5.0V, DGND = 0.0V, R_L = No Load, T_A = Operating Temperature Range specified in Absolute Maximum Ratings, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	SMP-04 MIN	TYP	MAX	UNITS
Linearity Error			–	.01	–	%
Buffer Offset Voltage	V_{OS}	V_{IN} = 0V	–10	±2.5	+10	mV
Hold Step	V_{HS}	V_{IN} = 0V	–	–1	±4	mV
Droop Rate	ΔV/Δt	V_{IN} = 0V, T_A = +25°C	–	2	25	mV/s
Output Resistance	R_{OUT}		–	1	–	Ω
Output Source Current	I_{SOURCE}	V_{IN} = 0V (Note 1)	1.2	–	–	mA
Output Sink Current	I_{SINK}	V_{IN} = 0V (Note 1)	0.5	–	–	mA
Output Voltage Range	OVR	R_L = 20kΩ	–3.0	–	+3.0	V
LOGIC CHARACTERISTICS						
Logic Input High Voltage	V_{INH}		2.4	–	–	V
Logic Input Low Voltage	V_{INL}		–	–	0.8	V
Logic Input Current	I_{IN}		–	0.5	1	μA
DYNAMIC PERFORMANCE (Note 2)						
Acquisition Time	t_A	–3 to +3V step to 0.1%	–	7	–	μs
Acquisition Time	t_A	–3 to +3V step to 0.01%	–	9	–	μs
Hold Mode Settling Time	t_H	To 1mV	–	1	–	μs
Slew Rate	SR	R_L = 20kΩ (Note 3)	–	3	–	V/μs
Capacitive Load Stability	C_L	<30% Overshoot	500	–	–	pF
SUPPLY CHARACTERISTICS						
Power Supply Rejection Ratio	PSRR	$\pm 5 \leq V_{DD} \leq \pm 6V$	60	75	–	dB
Supply Current	I_{DD}		–	3.5	5.5	mA
Power Dissipation	P_{DIS}		–	–	55	mW

NOTES:
1. Outputs are capable of sinking and sourcing over 20mA but linearity and offset are guaranteed at specified load levels.
2. All input control signals are specified with $t_r = t_f$ = 5ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.
3. Slew rate is measured in the sample mode with a –3 to +3 volt step from 20 to 80%.

DICE CHARACTERISTICS



DIE SIZE 0.080 x 0.120 inch, 9,600 sq. mils (2.032 x 3.048 mm, 6.193 sq. mm)

1. $V_{OUT\,2}$
2. $V_{OUT\,1}$
3. $V_{IN\,1}$
4. N.C.
5. $V_{IN\,2}$
6. S/H_1
7. S/H_2
8. DGND
9. S/H_3
10. S/H_4
11. $V_{IN\,3}$
12. $V_{IN\,4}$
13. V_{SS}
14. $V_{OUT\,4}$
15. $V_{OUT\,3}$
16. V_{DD}

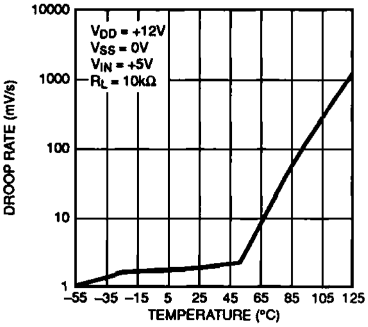
WAFER TEST LIMITS at V_{DD} = +12.0V, V_{SS} = DGND = 0V, R_L = No Load, T_A = +25°C, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	SMP-04G LIMITS	UNITS
Buffer Offset Voltage	V_{OS}	V_{IN} = 6V	±10	mV MAX
Hold Step	V_{HS}	V_{IN} = 6V	±4	mV MAX
Droop Rate	ΔV/Δt	V_{IN} = 6V	25	mV/s MAX
Output Source Current	I_{SOURCE}	V_{IN} = 6V	1.2	mA MIN
Output Sink Current	I_{SINK}	V_{IN} = 6V	0.5	mA MIN
Output Voltage Range	OVR	R_L = 20kΩ R_L = 10kΩ	0.06/10.0 0.06/9.5	V MIN/MAX
LOGIC CHARACTERISTICS				
Logic Input High Voltage	V_{INH}		2.4	V MIN
Logic Input Low Voltage	V_{INL}		0.8	V MAX
Logic Input Current	I_{IN}		1	μA MAX
SUPPLY CHARACTERISTICS				
Power Supply Rejection Ratio	PSRR	$10.8 \le V_{DD} \le 13.2V$	60	dB MIN
Supply Current	I_{DD}		7	mA MAX
Power Dissipation	P_{DIS}		84	mW MAX

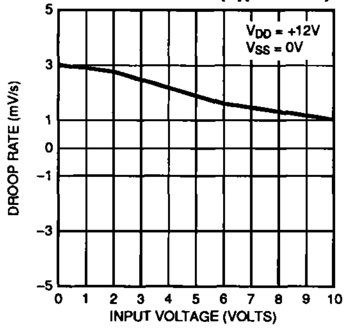
NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS Continued

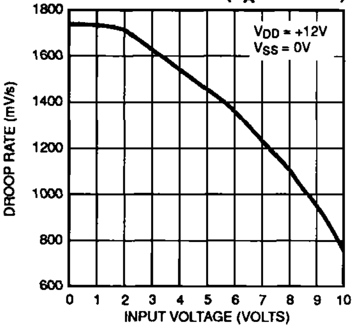
DROOP RATE vs TEMPERATURE



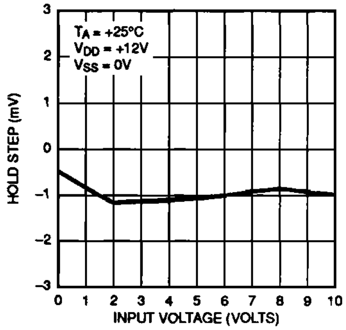
DROOP RATE vs INPUT VOLTAGE (T_A = +25°C)



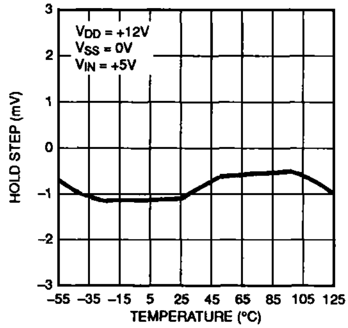
DROOP RATE vs INPUT VOLTAGE (T_A = +125°C)



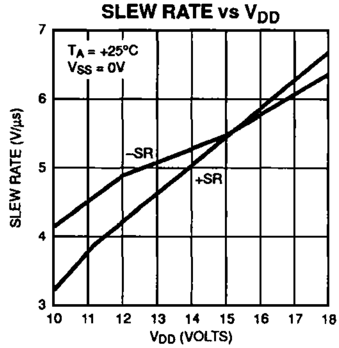
HOLD STEP vs INPUT VOLTAGE



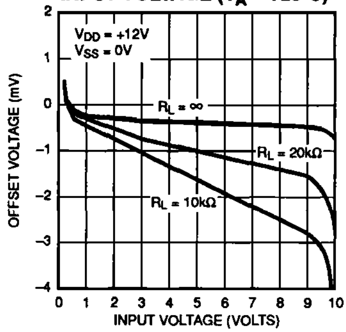
HOLD STEP vs TEMPERATURE



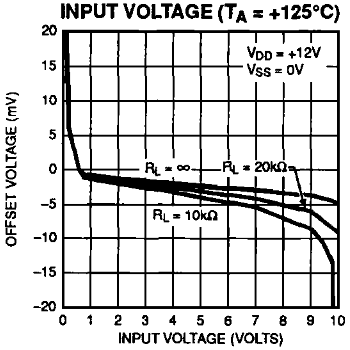
SLEW RATE vs V_{DD}



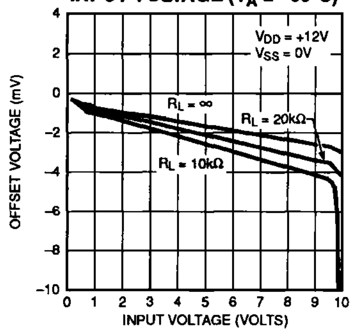
OFFSET VOLTAGE VS INPUT VOLTAGE (T_A = +25°C)



OFFSET VOLTAGE vs INPUT VOLTAGE (T_A = +125°C)



OFFSET VOLTAGE vs INPUT VOLTAGE (T_A = –55°C)



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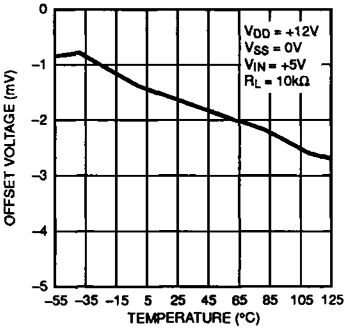
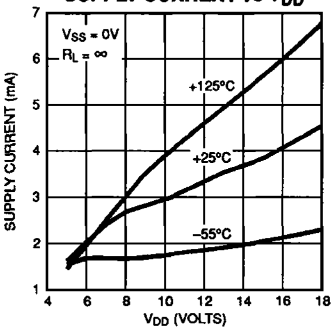
TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

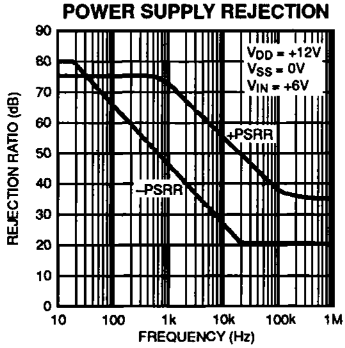
OFFSET VOLTAGE vs TEMPERATURE



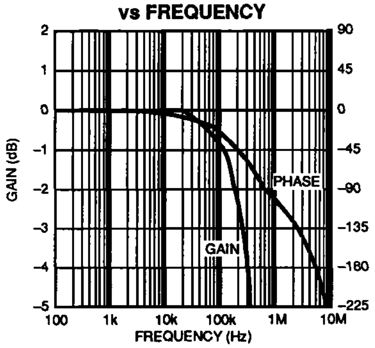
SUPPLY CURRENT vs V_{DD}



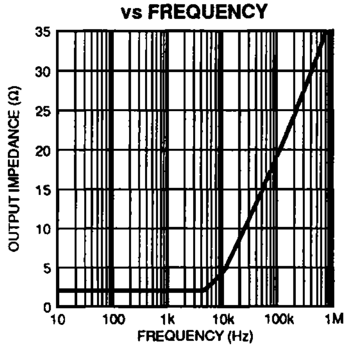
SAMPLE MODE POWER SUPPLY REJECTION



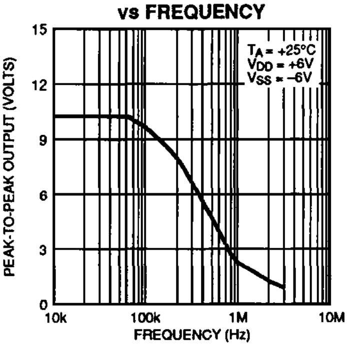
GAIN, PHASE SHIFT vs FREQUENCY



OUTPUT IMPEDANCE vs FREQUENCY



MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



GENERAL INFORMATION

The SMP-04 is a quad sample-and-hold with each track-and-hold having its own input, output, control, and on-chip hold capacitor. The combination of four high-performance track-and-hold capacitors on a single chip greatly reduces board space and design time while increasing reliability.

After the device selection, the primary considerations in using track-and-holds are the hold capacitor and layout. The SMP-04 eliminates most of these problems by having the hold capacitors internal, eliminating the problems of leakage, feed-through, guard-ring layout and dielectric absorption.

POWER SUPPLIES

The SMP-04 is capable of operating with either single or dual supplies over a voltage range of 7 to 15 volts. Based on the supply voltages chosen, V_{DD} and V_{SS} establish the output voltage range, which is:

$$V_{SS} + .05V \le V_{OUT} \le V_{DD} - 2V$$

Note that several specifications, including acquisition time, offset and output voltage compliance will degrade for a total supply voltage of less than 7V. Positive supply current is typically 4mA with the outputs unloaded. The SMP-04 has an internally regulated TTL supply so that TTL/CMOS compatibility will be maintained over the full supply range.

Single Supply Operation Grounding Considerations – In single supply applications, it is extremely important that the V_{SS} (negative supply) pin be connected to a clean ground. This is because the hold capacitor is internally tied to V_{SS}. Any noise or disturbance in the ground will directly couple to the output of the sample-and-hold, degrading the signal-to-noise performance. It is advisable that the analog and digital ground traces on the circuit board be physically separated to reduce digital switching noise from entering the analog circuitry.

Power Supply Bypassing – For optimum performance, the V_{DD} supply pin must also be bypassed with a good quality, high-frequency ceramic capacitor. The recommended value is 0.1µF. In the case where dual supplies are used, V_{SS} (negative supply) bypassing is particularly important. Again this is because the internal hold capacitor is tied to V_{SS}. Good bypassing prevents high frequency noise from entering the sample-and-hold amplifier. A 0.1µF ceramic bypass capacitor is generally sufficient. For high noise environments, adding a 10µF tantalum capacitor in parallel with the 0.1µF provides additional protection.

Power Supply Sequencing – It may be advisable to have the V_{DD} turn on prior to having logic levels on the inputs. The SMP-04 has been designed to be resistant to latch-up, but standard precautions should still be taken.

OUTPUT BUFFERS (Pins 1, 2, 14, and 15)

The buffer offset specification is ±10mV; this is less than 1/2 LSB of an 8-bit DAC with 10V full scale. Change in offset over the output range is typically 3mV. The hold step is the magnitude of the voltage step caused when switching from sample-to-hold mode. This error is sometimes referred to as the pedestal error or sample-to-hold offset, and is about 1mV with little variation. The droop rate of a held channel is 2µV/ms typical and ±25µV/ms maximum.

The buffers are designed primarily to drive loads connected to ground. The outputs can source more than 1.2mA each, over the full voltage range and maintain specified accuracy. In split supply operation, symmetrical output swings can be obtained by restricting the output range to 2V from either supply.

On-chip SMP-04 buffers eliminate potential stability problems associated with external buffers; outputs are stable with capacitive loads up to 500pF. However, since the SMP-04's buffer outputs are not short-circuit protected, care should be taken to avoid shorting any output to the supplies or ground.

SIGNAL INPUT (Pins 3, 5, 11, and 12)

The signal inputs should be driven from a low impedance voltage source such as the output of an op amp. The op amp should have a high slew rate and fast settling time if the SMP-04's fast acquisition time characteristics are to be maintained. As with all CMOS devices, all input voltages should be kept within range of the supply rails ($V_{SS} \leq V_{IN} \leq V_{DD}$) to avoid the possibility of setting up a latch-up condition.

The internal hold capacitance is typically 60pF and the internal switch ON resistance is 4kΩ.

If single supply operation is desired, op amps such as the OP-21, OP-80, or OP-90 that have input and output voltage compliances including ground, can be used to drive the inputs. Split supplies, such as ±7.5V, can be used with the SMP-04 and the above mentioned op amps.

APPLICATION TIPS

All unused digital inputs should be connected to logic LOW and the analog inputs connected to analog ground. For connector-driven analog inputs that may become temporarily disconnected, a resistor to V_{SS} or analog ground should be used with a value ranging from 0.2 to 1MΩ.

Do not apply signals to the SMP-04 with power off unless the input current's value is limited to less than 10mA.

Track-and-holds are sensitive to layout and physical connections. For the best performance, the SMP-04 should not be socketed.

FREQUENCY DOMAIN PERFORMANCE

The SMP-04 has been characterized in the frequency domain for those applications that require capture of dynamic signals. See Figure 1a for typical 86.1kHz sample rate and an 8kHz input signal. Typically, the SMP-04 can sample at rates up to 85kHz. In addition to the maximum sample rate, a minimum sample pulse width will also be acceptable for a given design. Our testing shows a drop in performance as the sample pulse width becomes less than 4µs.

a)

b)

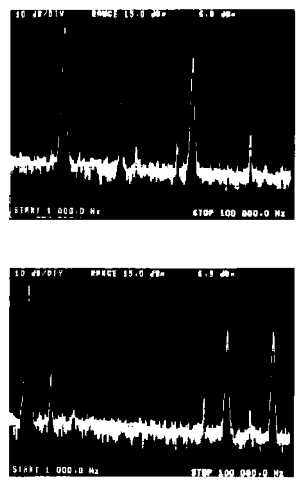


FIGURE 1: *Spectral response at a sampling frequency of 86kHz. Photo (a) shows a 20kHz carrier frequency, and photo (b) shows an 8kHz frequency.*

Optimizing Dynamic Performance of the SMP-04 – Various operating parameters such as input voltage amplitude, sampling pulse width and, as mentioned before, supply bypassing and grounding all have an effect on the signal-to-noise ratio. Table 1 shows the SNR versus input level for the SMP-04.
Distortion of the SMP-04 is reduced by increasing the supply voltage. This has the effect of increasing the positive slew rate. Table 2 shows data taken at 12.3kHz sample rate and 2kHz input frequency. Total harmonic distortion is dominated by the second and third harmonics.

Table 3 shows the effect of sampling pulse width on the SNR of the SMP-04. The recommended operating pulse width should be a minimum of 5 µs to achieve a good balance between acquisition time and SNR for the 1.4Vp-p signal shown. For larger swings the pulse width will need to be larger to account for the time required for the signal to slew the additional voltage. This could be used as a method of measuring acquisition time indirectly.

TABLE 1: SNR vs. V_{IN}

INPUT VOLTAGE (Vp-p)	SNR (dB)
1	–61
2	–53
3	–50
4	–47
5	–45
6	–44

Conditions: $V_S = \pm 6V$, $f_S = 14.4kHz$, $f_{IN} = 1.8kHz$, $t_{PW} = 10\ \mu s$.

TABLE 2: SNR vs. Supply Voltage

SUPPLY VOLTAGE	2nd (dB)	3rd (dB)
10V	–49	–62
12V	–55	–71
14V	–60	–80
15V	–62	<–80
16V	–63	<–83
17V	–65	<–85

TABLE 3: SNR vs. Sample Pulse Width

SAMPLE PULSE WIDTH (µs)	SNR (dB)
1	–37
2	–44
3	–50
4	–54
5	–54.9
6	–55
7	–55.3

Conditions: $V_S = \pm 6V$, $V_{IN} = 1.4Vp\text{-}p$, $f_S = 14.4kHz$, $f_{IN} = 1.8kHz$

Sample-Mode Distortion Characteristics – Although designed as a sample-and-hold, the SMP-04 may be used as a straight buffer amplifier by configuring it in a continuous sample mode. This is done by connecting the $\overline{S}$/H control pin to a logic LOW. Its buffer bandwidth is primarily limited by the distortion content as the signal frequency increases. Figure 2 shows the distortion characteristics of the SMP-04 versus frequency. It maintains less than 1% total harmonic distortion over a voice-band of 8kHz.

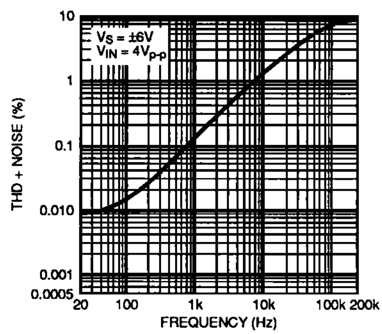


FIGURE 2: *THD+N vs. Frequency*

Sampled Data Dynamic Performance – In continuous sampled data applications such as voice digitization or communication circuits, it is important to analyze the spectral response of a sample-and-hold. Figures 1a and b show the SMP-04 sampling at a frequency of 86kHz with a 1.4Vp-p pure sine wave input of 20kHz and 8kHz respectively. The photos include the sampling carrier frequency as well as its multiplying frequencies. In the case of the 20kHz carrier frequency, the second harmonic measures 41dB down from the fundamental, because the second is dominant, the signal-to-noise ratio is –40.9dB. The 8kHz case produces an improved S/N performance of –48 dB.

In the V.32 and V.33 modem environment, where a 1.8kHz carrier signal frequency is applied to the SMP-04, Figure 3 compares the spectral responses of the SMP-04 under three different sampling frequencies of 14.4kHz, 9.6kHz and 7.2kHz. The signal-to-noise ratios measure to be 58.2dB, 59.3dB and 60dB respectively.

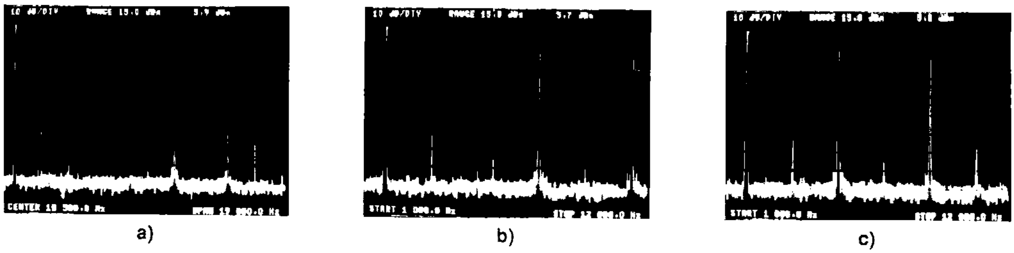


FIGURE 3: *SMP-04 spectral response with a 1.8kHz carrier frequency. (a) shows the sampling frequency at 14.4kHz; it exhibits a S/N ratio of 58.2dB. (b) shows a 59.3dB S/N at a sampling frequency of 8.6kHz. (c) shows a 60dB S/N at 7.2kHz.*

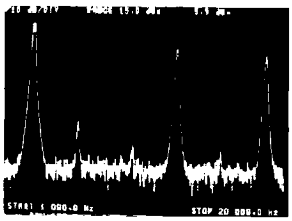


FIGURE 4: *SMP-04 spectral response with an input carrier frequency of 3kHz and the sampling frequency of 15.7kHz.*

Figure 4 depicts SMP-04's spectral response operating with voice frequency of 3kHz sampling at a 15.7kHz rate. Under this condition, the signal-to-noise measures 53dB.

APPLICATIONS

MULTIPLEXED QUAD DAC (Figure 5)

The SMP-04 can be used to demultiplex a single DAC converter's output into four separate analog outputs. The circuit is greatly simplified by using a voltage output DAC such as the DAC-8228. To minimize output voltage perturbation, 5μs should be allowed to settle to its final voltage before a sample signal is asserted. Each sample-and-hold amplifier must be refreshed every second or less in order to assure the droop does not exceed 10mV or 1/2 LSB.

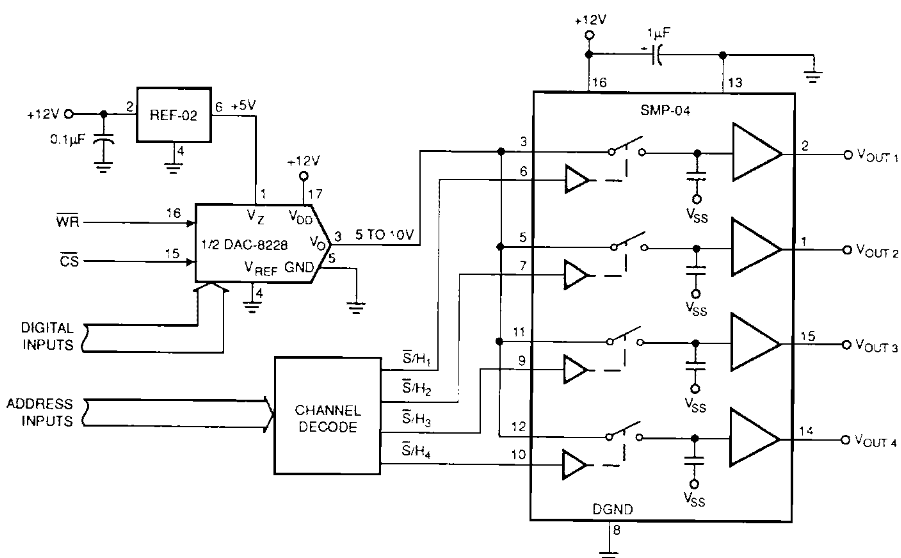


FIGURE 5: *Multiplexed Quad DAC*

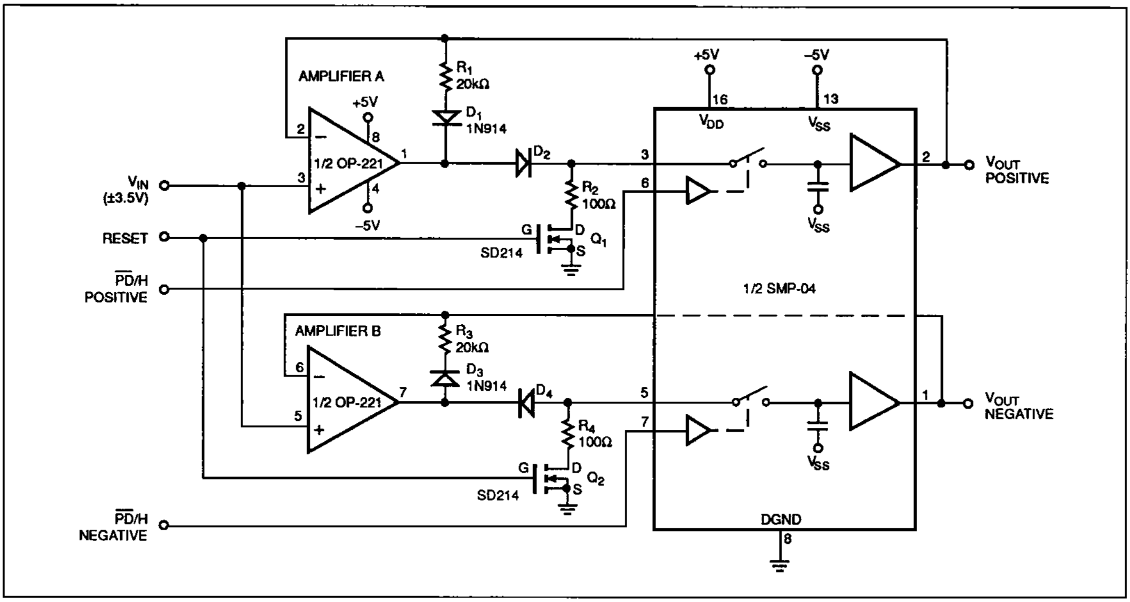


FIGURE 6: *Positive and Negative Peak Detector with Hold Control*

POSITIVE AND NEGATIVE PEAK DETECTOR WITH HOLD CONTROL (Figure 6)

In this application the top amplifier (amplifier A) is the positive peak detector and the bottom amplifier (amplifier B) is the negative peak detector. Operation can be analyzed as follows: Assume that the $\overline{S}$/H switch is closed. As a positive increasing voltage is applied to A_{IN}, D_2 turns on, and D_1 turns off, closing the feedback loop around amplifier A and the SMP-04, causing the output to track the input. Conversely, in the negative peak detector circuit at the bottom, D_4 turns off and D_3 turns on, holding the last most negative input voltage on the SMP-04. This voltage is buffered to the $V_{O(NEG)}$ output.

As V_{IN} falls in voltage the above conditions reverse, causing the most positive peak voltage to be held at $V_{O(POS)}$ output. This voltage will be held until the input has a more positive voltage than the previously held peak voltage, or a reset condition is applied.

An optional HOLD control can be used by applying a logic HIGH to the $\overline{PD}$/H inputs. This HOLD mode further reduces leakage current through the reverse-biased diodes (D_2 and D_4) during peak hold.

GAIN OF 10 SAMPLE-AND-HOLD (Figure 7)

This application places the SMP-04 in a feedback loop of an amplifier. Because the SMP-04 has no sign inversion and the amplifier has very high open-loop gain, the gain of the circuit is set by the ratio of the sum of the source and feedback resistances to the source resistance. When a logic LOW is applied to the $\overline{S}$/H control input, the loop is closed around the OP-490, yielding a gain of 10 (in the example shown) amplifier. When the $\overline{S}$/H control goes HIGH, the loop opens and the SMP-04 holds the last sampled voltage. The loop remains open and the output is unaffected by the input until a logic LOW is reapplied to the $\overline{S}$/H control. The pair of back-to-back diodes from the output of the op amp to the output of the track-and-hold prevents the op amp from saturating when the track-and-hold is in the hold mode and the loop is open.

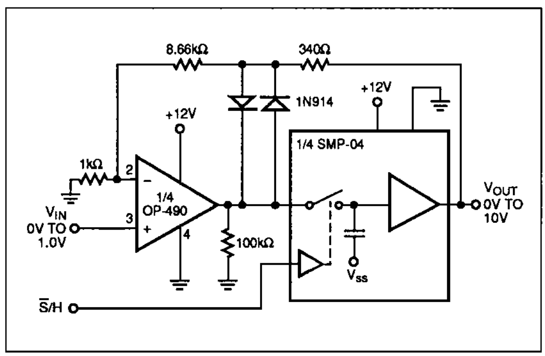


FIGURE 7: *Gain of 10 Sample-and-Hold Amplifier*

SAMPLE AND DIFFERENCE AMPLIFIER (Figure 8)

This circuit uses two sample-and-holds to measure the voltage difference of a signal between two time points, t_1 and t_2. The sampled voltages are fed into the differential inputs of the AMP-02 instrumentation amplifier. A single resistor R_G sets the gain of this instrumentation amplifier. Using two of the SMP-04s in this application has the advantage of matched sample-and-hold performance, since they are both on the same chip.

SINGLE SUPPLY, SAMPLING, INSTRUMENTATION AMPLIFIER (Figure 9)

This application again uses two channels of the SMP-04 and an instrumentation amplifier to provide a sampled difference signal. The sample-and-hold signals in this circuit are tied together to sample at the same point in time. The other two parts of the SMP-04 are used as amplifiers by grounding their control lines so that they are always sampling. One section is used to drive a guard to the common-mode voltage and the other to generate a +6V reference to serve as an offset for single supply operation.

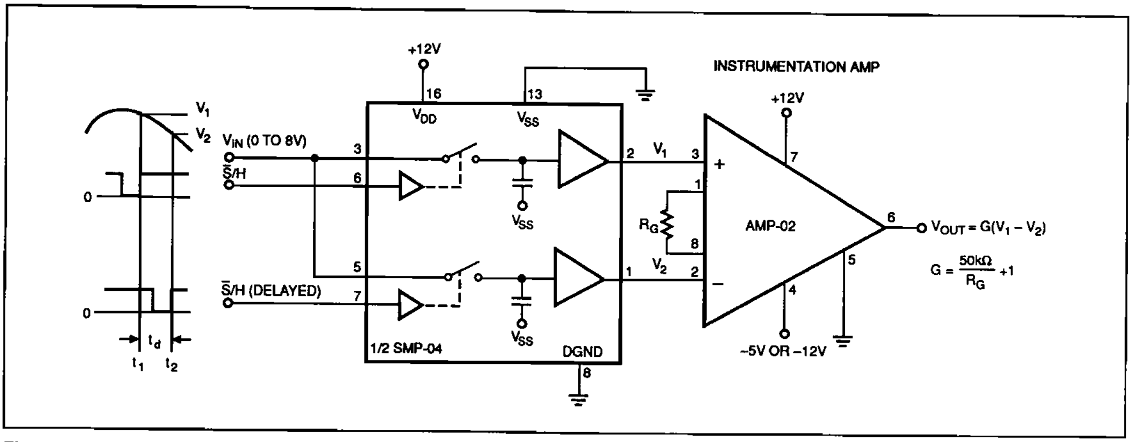


FIGURE 8: *Time Delta Sample-and-Difference Measurement*

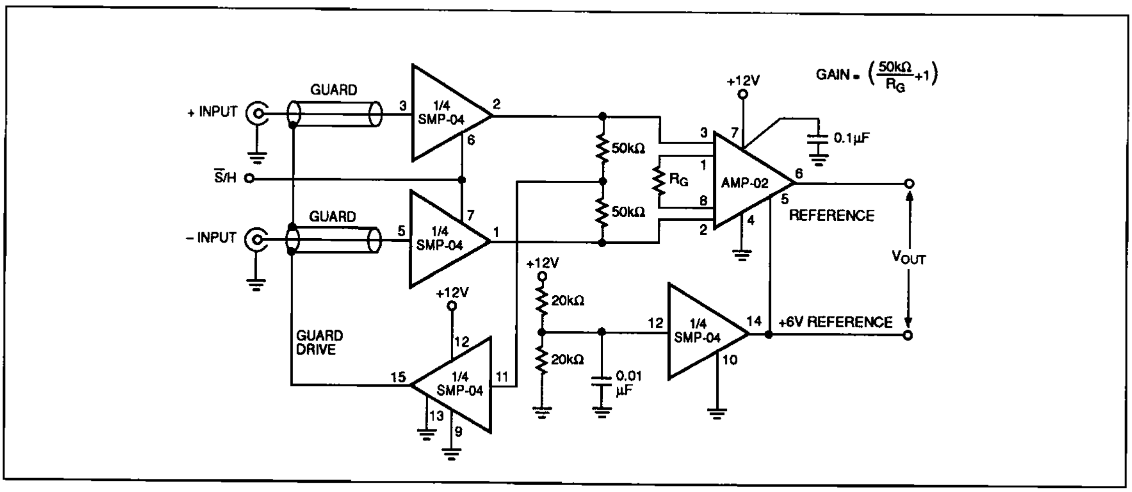


FIGURE 9: *+12V Single Supply Sampling Instrumentation Amplifier with Guard Drive*

D/A CONVERTER DEGLITCHER

Most D/A converters output an appreciable amount of glitch energy during a transition from one code to another. The glitch amplitude can range from several millivolts to hundreds of millivolts. This may become unacceptable in many applications. By selectively delaying the DAC's output transition, the SMP-04 can be used to smooth the output waveform. Figure 10 shows the schematic diagram of such a deglitcher circuit. Two simple logic gates (an OR and a NAND gate) provide the proper timing sequence for the DAC $\overline{WR}$ strobe and the $\overline{S}$/H control signal to the SMP-04. In this example a linear ramp signal is generated by feeding the most significant 8-bits of the 10-bit binary counter to the DAC. The two least significant bits are used to produce the delayed $\overline{WR}$ strobe and the $\overline{S}$/H control signals. Referring to Figure 11a, new data to the DAC input is set up at the $\overline{S}$/H's falling edge, but the DAC output does not change yet until a $\overline{WR}$ strobe goes active. During this period, the SMP-04 is in a sample mode whose output tracks the DAC output. When $\overline{S}$/H goes HIGH, the current DAC output voltage is held by the SMP-04. After 1.2μs settling, the $\overline{WR}$ strobe goes LOW to allow the DAC output to change. Any glitch that occurs at the DAC output is effectively blocked by the SMP-04. As soon as the $\overline{WR}$ strobe goes HIGH, the digital data is latched; at the same time the $\overline{S}$/H goes LOW, allowing the SMP-04 to track to the new DAC output voltage.

Figure 11b shows the deglitching operation. The top trace shows the DAC output during a transition, while the bottom trace shows the deglitched output of the SMP-04.

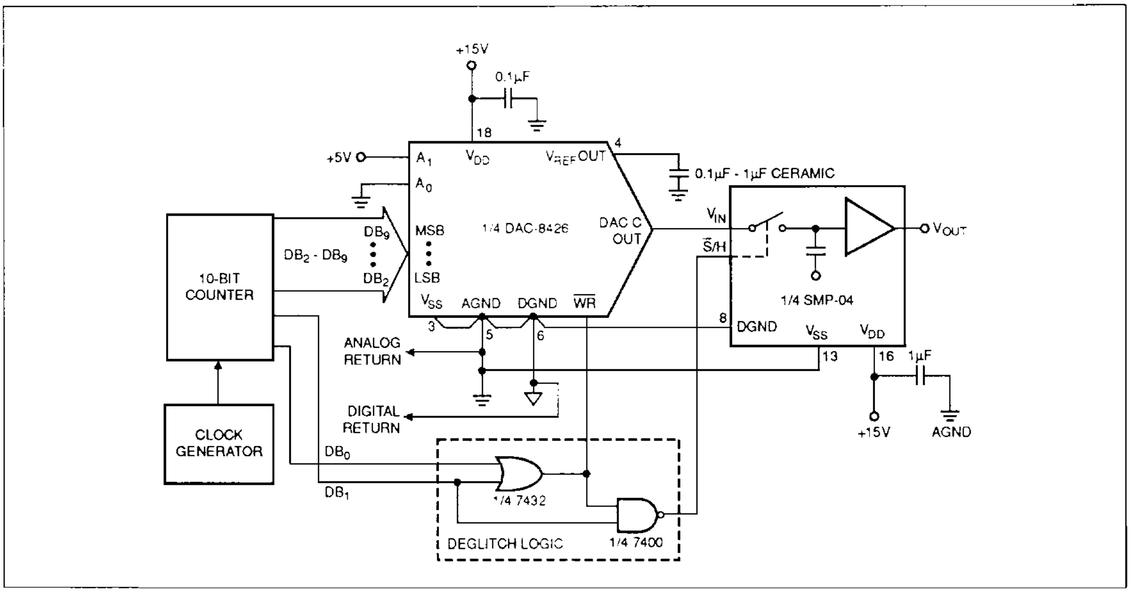


FIGURE 10: *DAC Deglitcher*

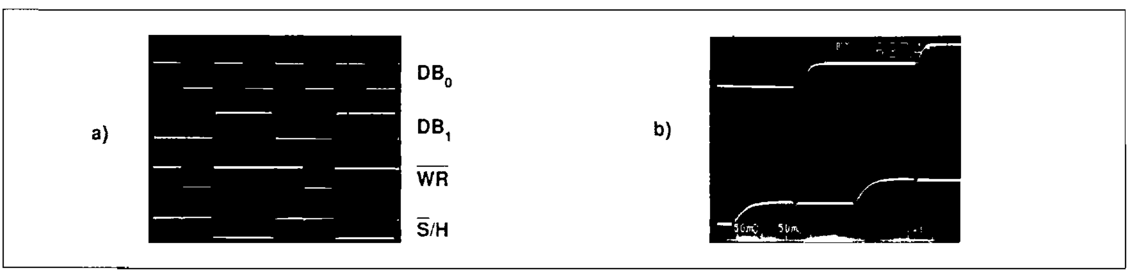
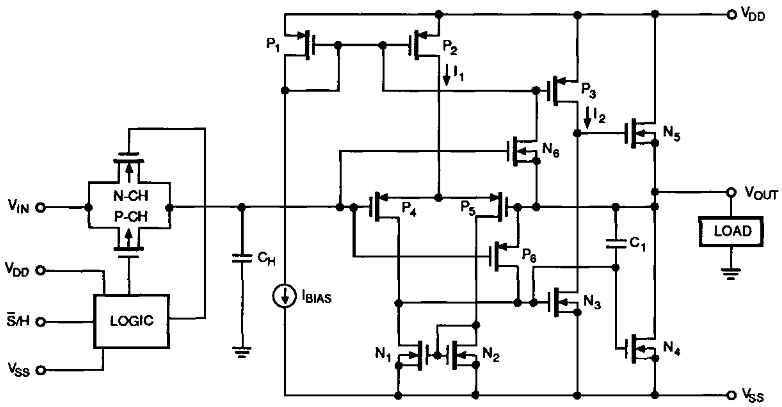


FIGURE 11: *(a) shows the logic timing of the deglitcher. The top two traces are the two least significant bits, DB_0 and DB_1, respectively. These are used to generate the $\overline{WR}$ and $\overline{S}$/H signals which are shown in the bottom two traces. (b) shows the typical glitch amplitude of a DAC (top trace) and the deglitched output of the AMP-04 (bottom trace).*

SIMPLIFIED SCHEMATIC



BURN-IN CIRCUIT