VTC Inc.
Value the Customer™

VM65010

ANALOG PRML CHANNEL DETECTOR

950801

PRELIMINARY

August,1995

FEATURES

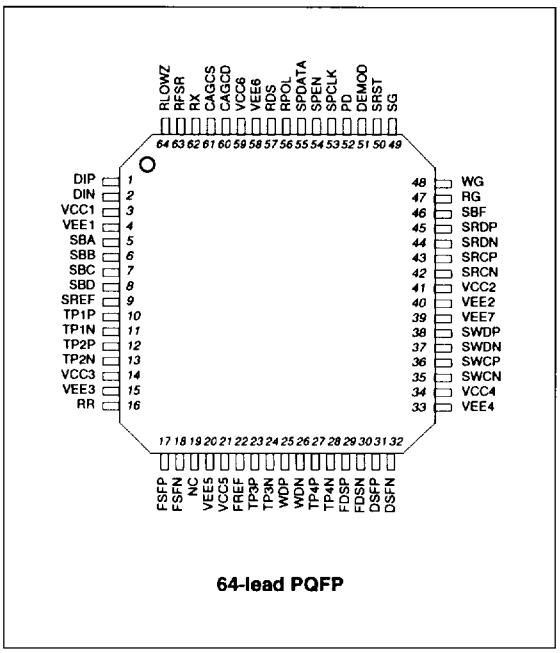
- Register programmable user data rates from 46 to 140 Mbps
- Sampled data read channel with maximum likelihood Viterbi detection
- Programmable continuous-time filter with two independently variable real zeros
- Programmable seven tap transversal filter for PR4 equalization
- Programmable two level write precompensation
- Direct Write/Read feature for equalizer optimization
- Analog/sampled AGC
- Zero phase restart for fast timing acquisition
- Servo area detectors for burst demodulation
- Equalization tool aids in equalizer optimization
- Fast timing control during acquisition by bypassing FIR filter
- Register programmable power management (<5 mW Power Down mode)
- Serial interface port for access to internal program storage registers to load and verify
- Single power supply (5V ±10%)
- Small footprint 64-pin PQFP package

DESCRIPTION

The VM65010 is a high performance BiCMOS read channel IC that provides all of the data processing needed to implement the front end of a Partial Response Maximum Likelihood (PRML) read channel for zoned recording hard disk drive systems with user data rates from 46 to 140 Mbps. BiCMOS process technology along with advanced circuit design techniques result in high performance devices with low power consumption. The part requires a single +5V power supply and is available in a 64-Lead PQFP package. This chip along with its companion, the VM65020, provides a complete channel solution.

Functional blocks include AGC, programmable filter, sampling FIR filter, maximum likelihood Viterbi detector, synchronizer, frequency synthesizer, 2-level nonlinear write precomp, area detectors for servo bursts and an equalization tool to aid in equalizer adjustment. Programmable functions such as data rate, filter cutoff/boost, FIR tap weights, write precomp values, etc. are controlled by writing to the serial port registers. No external component changes are required to change zones.

CONNECTION DIAGRAM



64-lead PQFP

READ CHANNEL CIRCUITS

BLOCK DIAGRAM DESCRIPTION

AUTOMATIC GAIN CONTROL:
- Dual mode AGC, analog during acquisition, sampled during read data
- Separate AGC level storage pins for data and servo
- Dual rate attack and decay charge pump for rapid AGC recovery
- Programmable, symmetric, charge pump currents during read data
- Charge pump currents track programmable data rate
- Low drift AGC hold circuitry
- Internal Low Z for write mode.
- Externally adjustable one-shot pulse width for LOWZ control
- AGC hold, fast recovery, and AGC input impedance control signals
- Wide bandwidth, precision full-wave rectifier

LOW PASS FILTER/EQUALIZER:
Programmable, 7-pole, continuous time filter provides:
- Programmable cutoff frequency from 7 to 48 MHz
- Programmable boost/equalization of 0 to 13 dB
- Programmable group delay of ±30%
- Equalization to PR4
- Differentiator outputs match normal output phase
- Minimizes size and power

FIR FILTER/EQUALIZER:
- Seven tap filter
- Individual tap adjustment for fine equalization to PR4 target
- No external components required

LEVEL QUALIFICATION:
- Level pulse qualifier for servo reads
- Independent positive and negative thresholds for asymmetrical signals (e.g. from MR heads)
- Independent thresholds for servo

MAXIMUM LIKELIHOOD DETECTOR:
- Sampled Viterbi detection of signal equalized to PR4
- Programmable threshold window.
- Survival register length of five.

FREQUENCY SYNTHESIZER:
- Better than 1% frequency resolution
- Up to 160 MHz frequency output
- Independent M and N divide-by registers
- No active external components required

TIMING RECOVERY
- Single external capacitor required
- Register programmable channel rate of 160 Mbps operation
- Fast Acquisition, sampled data phase lock loop
- Decision directed clock recovery from data samples
- Programmable damping ratio which is constant over all data rates

WRITE PRECOMPENSATION:
- Independently programmable write precompensation for three data patterns.
- Step resolution of 1.25% up to 40% of bit period.
- Precompensation tracks Frequency Synthesizer period
- Differential PECL write data output
- Precoding function suited for PR4 channel

SERVO:
- Wide bandwidth, precision full-wave rectifier
- Separate, automatically selected, registers for servo f_c, boost, and threshold
- Four individual area detectors for servo bursts A, B, C and D.
- Programmable servo gain of ± 4 dB.

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BLOCK DIAGRAM