LITEON
OPTOELECTRONICS

Optical Sensor

Product Data Sheet

LTR-530RGB-01

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RELEASE

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Optical Sensor
LTR-530RGB-01

Description

The LTR-530RGB-01 is an integrated low voltage I^2C ambient light sensor (ALS), a color sensor (CS), and a proximity sensor (PS), as well as an LED driver in a single miniature chipled lead-free surface mount package.

With the advanced RGB color sensor, this sensor converts light (Red, Green, Blue, and White) intensity to a digital output signal capable of direct I^2C interface. The ALS provides a linear response over a wide dynamic range of 1:3000000, which is well suited to applications under very low or bright ambient brightness. Besides, with built-in proximity sensor, this sensor offers the feature to detect object at a user configurable distance.

The sensor has a programmable interrupt with hysteresis to response to events and that removes the need to poll the sensor for a reading which improves system efficiency. This CMOS design and factory-set one time trimming capability ensure minimal sensor-to-sensor variations for ease of manufacturability to the end customers.

Application

To control brightness and color of the display panel, and/or object detection in mobile, computing, and consumer devices.

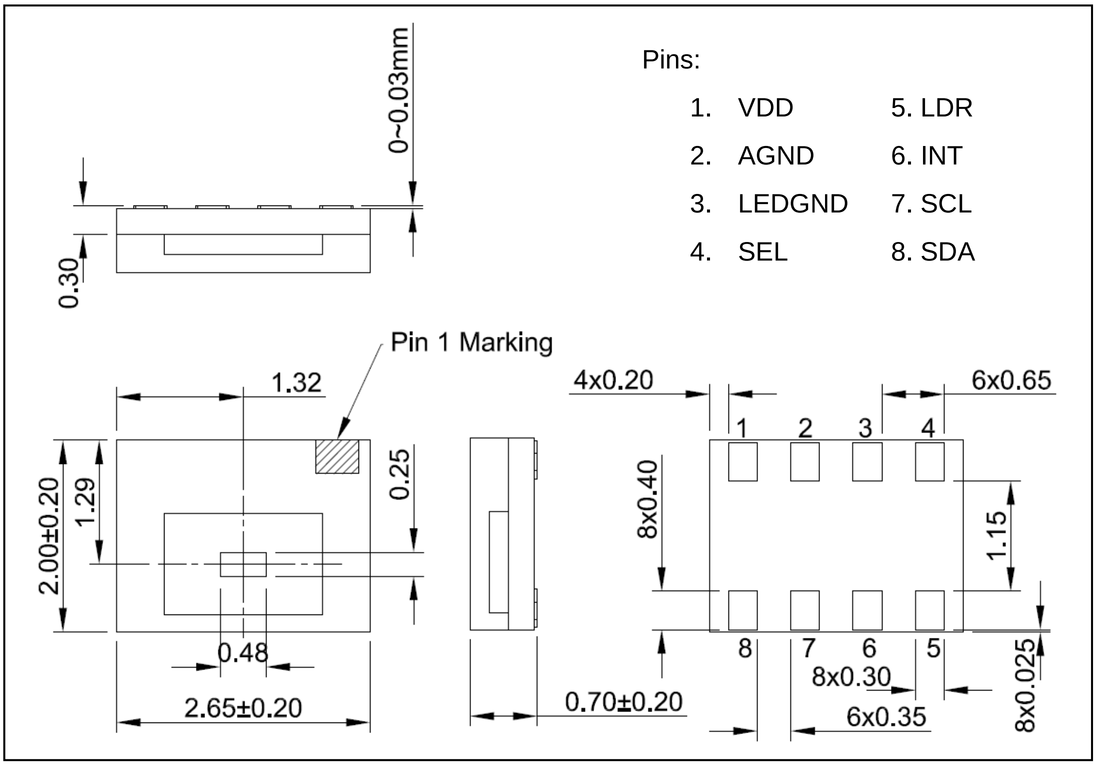
Features

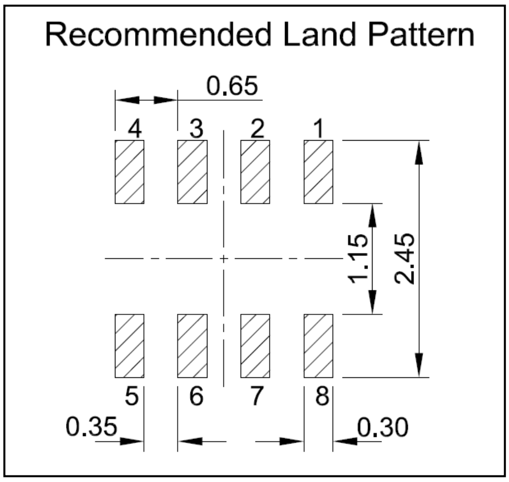
- I^2C interface (Standard mode @100kHz or Fast mode @400kHz)
- Ambient Light / Advanced RGB Technology and Proximity Sensing in one ultra-small ChipLED package
- Very low power consumption with sleep mode capability
- Operating voltage ranges: 2.4V to 3.6V
- Operating temperature ranges: -40 to +85 ºC
- Built-in temperature compensation circuit
- Programmable interrupt function for ALS and PS with upper and lower thresholds
- RoHS and Halogen free compliant
- **CS/ALS Features**
  - 14 to 18 bits effective resolution
  - Wide dynamic range of 1:3000000 with linear response
  - Close to human eye spectral response
  - Automatic rejection for 50Hz/60Hz lighting flicker
- **PS Features**
  - Built-in LED driver and detector
  - High ambient light suppression
  - 11-bit effective resolution
  - Cancellation of crosstalk
  - Programmable LED drive settings

Ordering Information

Part Number	Packaging Type	Package	Quantity
LTR-530RGB-01	Tape and Reel	8-pin chipled package	2500

1. Outline Dimensions



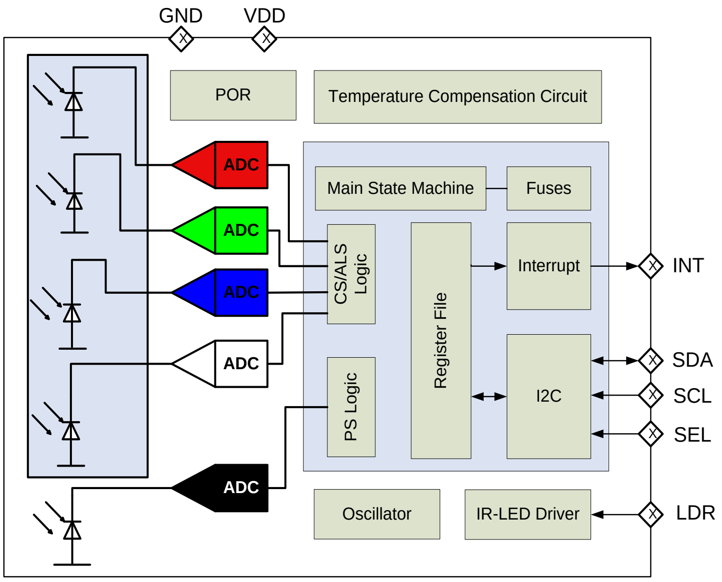


Note:

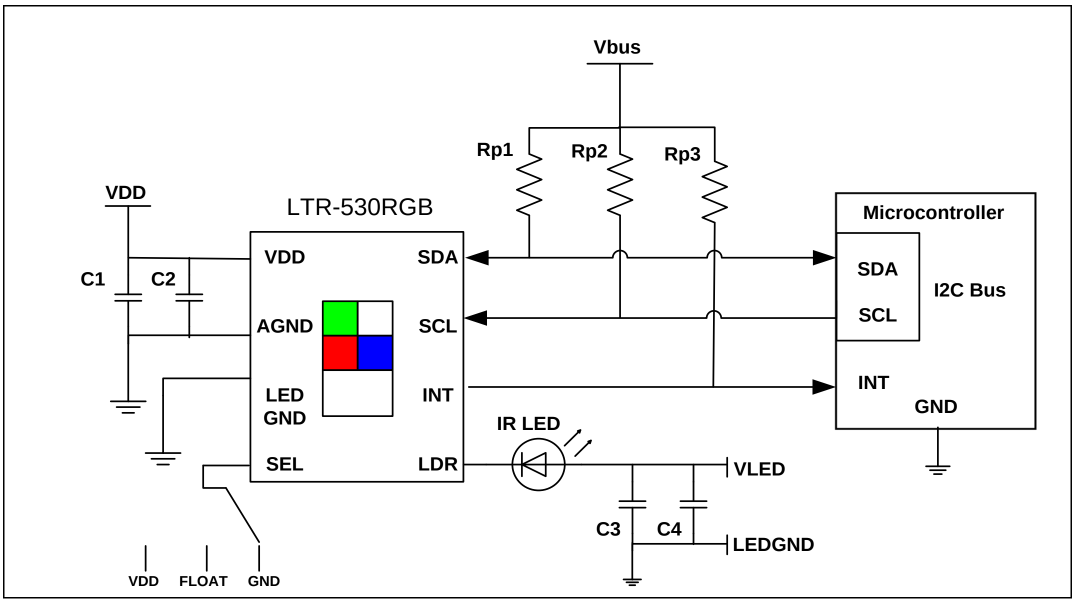
1. All dimensions are in millimeters

2. Functional Block Diagram

LTR-530RGB-01 contains 5 integrated photodiodes (1 for proximity diode, 4 diodes for red, green, blue, and white channel) for respective photocurrent measurement. The photodiode currents are converted to digital values by ADCs. The sensor also included a driver circuit for an external proximity LED, as well as some peripheral circuits such as an internal oscillator, a current course, voltage reference, and internal fuses to store trimming information.



3. Application Circuit



I/O Pins Configuration Table

Pin	I/O Type	Symbol	Description
1	Supply	VDD	Power Supply Voltage
2	Ground	AGND	Analog Ground
3	Ground	LED GND	LED Driver Ground
4	IN	SEL	I^2C slave address selector
5	OUT	LDR	To connect to LED Cathode
6	OUT	INT	Interrupt
7	IN	SCL	I^2C serial data
8	IN/OUT	SDA	I^2C serial clock

Recommended Application Circuit Components

Component	Recommended Value
Rp1, Rp2, Rp3 [1]	1 kΩ to 10 kΩ
C1, C3	0.1uF
C2, C4	4.7uF

Notes:

[1] Selection of pull-up resistors value is dependent on bus capacitance values. For more details, please refer to I2C Specifications: http://www.nxp.com/documents/user_manual/UM10204.pdf

[2] IR LED = LTE-C249 (850nm)

4. Rating and Specification

4.1. Absolute Maximum Rating at Ta=25°C

Parameter	Symbol	Rating	Unit
Supply Voltage	VDD	4.0	V
Digital Voltage Range	SCL, SDA, INT	4.0	V
Digital Output Current	SCL, SDA, INT	10	mA
Storage Temperature	T_{stg}	-45 to 95	°C
Electrostatic Discharge Protection (Human Body Model JESD22-A114)	V_{HBM}	2000	V

Note: Exceeding these ratings could cause damage to the sensor. All voltages are with respect to ground. Currents are positive into, negative out of the specified terminal.

4.2. Recommended Operating Conditions

Description	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	VDD	2.4		3.6	V
LED Supply Voltage	V_{LED}	2.3		4.5	V
Interface signal input high	$V_{I2Chigh}$	1.3		VDD	V
Interface signal input low	V_{I2Clow}	0		0.4	V
Operating Temperature	T_{ope}	-40		85	°C

4.3. Electrical Specifications (VDD = 3.0V, Ta=25°C, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Unit	Condition
ALS Active Supply Current		175		uA	14-bit resolution 50ms measurement rate
CS Active Supply Current		250		uA	
PS Active Supply Current		120		uA	IRLED with 32pulses 6.25ms measurement rate
Standby Current			5	uA	Standby / Sleep Mode
Initial Startup Time	100			ms	From VDD power up to Standby
Wakeup Time from Standby		5	10	ms	From Standby to Active mode where measurement can start

4.4. Characteristics Ambient Light / Color Sensor

Parameter	Min.	Typ.	Max.	Unit	Condition
ALS/CS Resolution	14		18	Bit	
Dark Level Count		0	5	count	0 Lux, T_{ope}=25°C, 14-bit resolution
Calibrated Lux Error In Gain Range 1			10	%	White LED, T_{ope}=25°C
Light Source Matching			10	%	Incandescent/Fluorescent light
Color Temperature Accuracy			10	%	
ALS Accuracy			10	%	
50/60 Hz flicker noise error			±5	%	
Temperature Dependency	-0.25		+0.25	%/ºC	At 1000 Lux
Voltage Dependency	-5		+5	%	At 1000 Lux, At operating voltage ranges

4.4.1. Irradiance Responsivity at Characteristic Wavelengths

Table below describes the specifications for irradiance responsivity in units of counts (µW/cm^2).
Test conditions are VDD = 3.0V, T_{ope} = 25°C, Gain Mode = X1, Output Resolution =14-bit

Test Conditions	Red Channel Note1			Green Channel Note1			Blue Channel Note1			White Channel Note1		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
λ_D = 470nm Note2	0%		16%	18%		54%	71%		107%	1.91	2.39	2.87
λ_D = 530nm Note3	15%		46%	83%		86%	0%		14%	2.92	3.64	3.64
λ_D = 625nm Note4	84%		114%	0%		17%	0%		14%	3.46	4.32	4.32

Notes:

1. The percentage shown represents the ratio of the respective red, green, or blue channel value to the white channel value.
2. The 470nm input irradiance is supplied by a blue LED with spectral bandwidth (50% irradiance) of 25nm.
3. The 530nm input irradiance is supplied by a green LED with spectral bandwidth (50% irradiance) of 33nm.
4. The 615nm input irradiance is supplied by a red LED with spectral bandwidth (50% irradiance) of 18nm.

4.5. Characteristics Proximity Sensor

Parameter	Min.	Typ.	Max.	Unit	Condition
PS Output Resolution			11	Bit	
Sensitivity Range		850		nm	
Detection Distance		30		mm	850nm IR LED, 8 pulses, 60kHz, 100mA, 18% Gray Card
LED Pulse Current	25		125	mA	
LED Current Accuracy	-10		+10	%	
LED Pulse Frequency	60		100	kHz	
LED Pulse Count	1		32	Pulses	
LED Duty Cycle		50		%	Fixed at 50% Duty Cycle
VDD Dependency	-10		+10	%	
VLED Dependency	-10		+10	%	

4.6. Typical Device Parameter (VDD = 3.0V, Ta=25°C, default power-up settings, unless otherwise noted)

Photodiodes Spectral Response

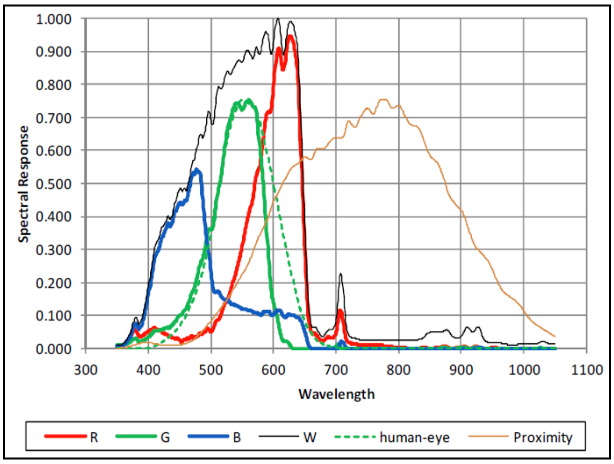


Figure 4.1 : Spectral response for R,G, B, W and Proximity photodiodes.

ALS Angular Response

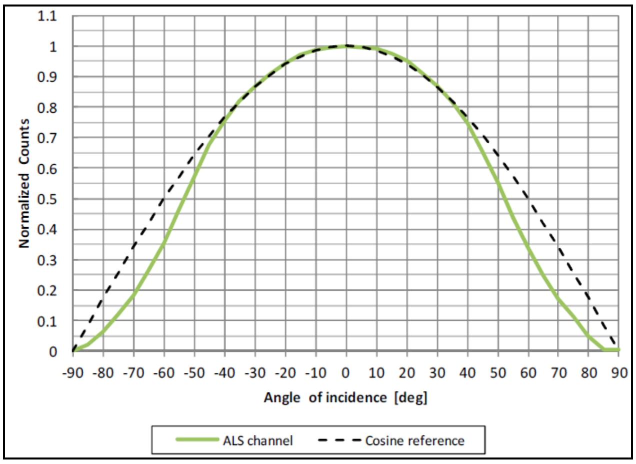


Figure 4.2 : ALS Sensitivity versus Angle of Incidence.

PS Count Versus Distance
(Different No. of Pulses)

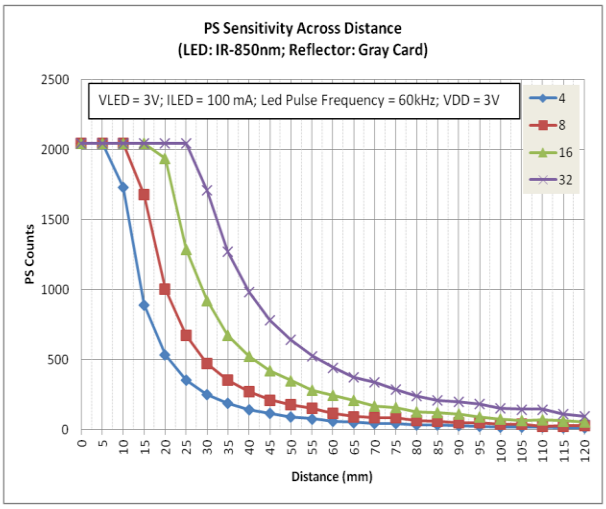


Figure 4.3: PS count versus distance for different number of pulses.

PS Count Versus Distance
(Different Reflector)

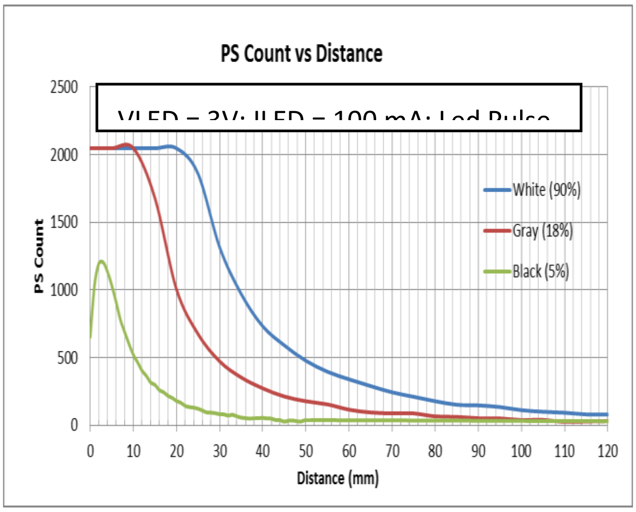
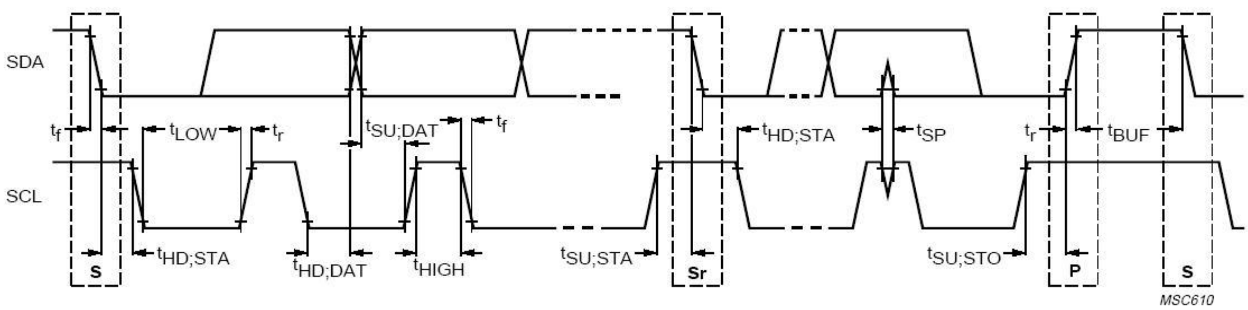


Figure 4.4 : PS count versus distance for different reflector.

4.7. AC Electrical Characteristics

All specifications are at VBus = 1.7V, T_{ope} = 25°C, unless otherwise noted.

Parameter	Symbol	Standard (Min)	Fast (Min)	Unit
SCL clock frequency	f_{SCL}	100	400	KHz
Bus free time between a STOP and START condition	t_{BUF}	4.7		us
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	4		us
LOW period of the SCL clock	t_{LOW}	4.7		us
HIGH period of the SCL clock	t_{HIGH}	4		us
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7		us
Set-up time for STOP condition	$t_{SU;STO}$	4		us
Rise time of both SDA and SCL signals	t_r	30	300	ns
Fall time of both SDA and SCL signals	t_f	30	300	ns
Data hold time	$t_{HD;DAT}$	0		us
Data setup time	$t_{SU;DAT}$	100	100	ns
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	0	50	ns

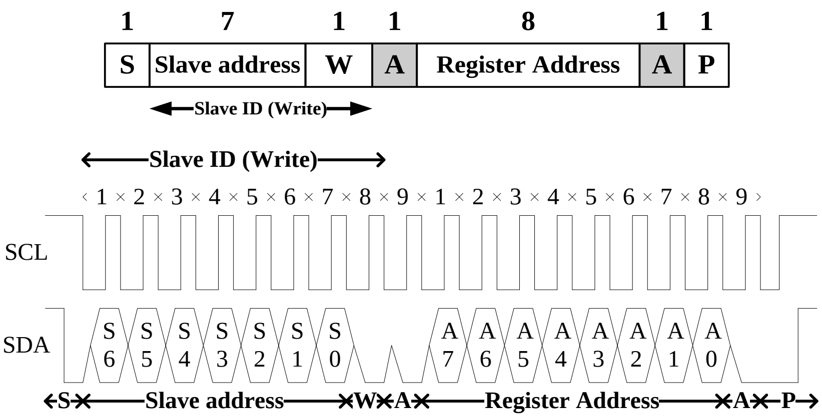


Definition of timing for I²C bus

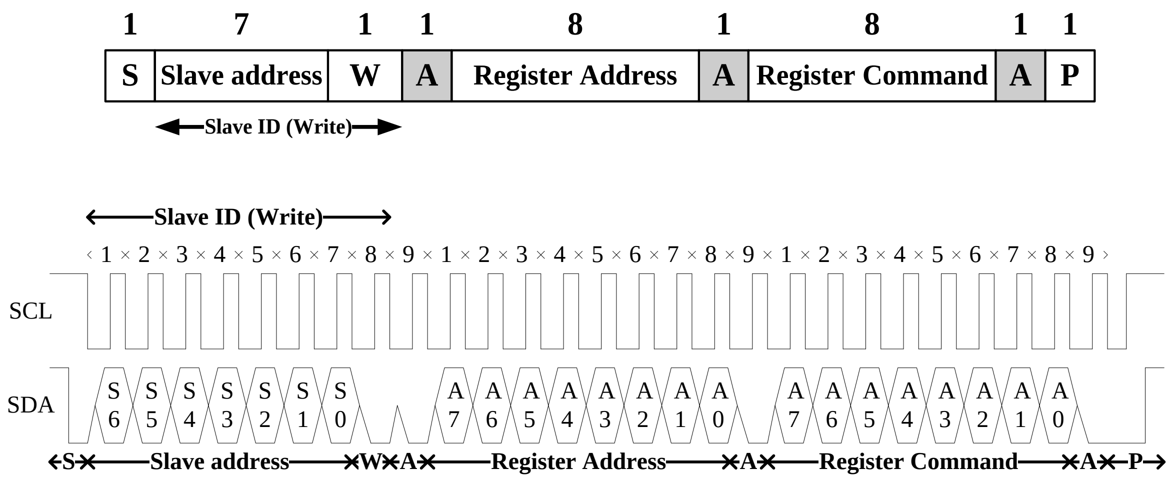
5. Principle of Operation

5.1. I2C Protocol

5.1.1. I2C Write Protocol (type 1)



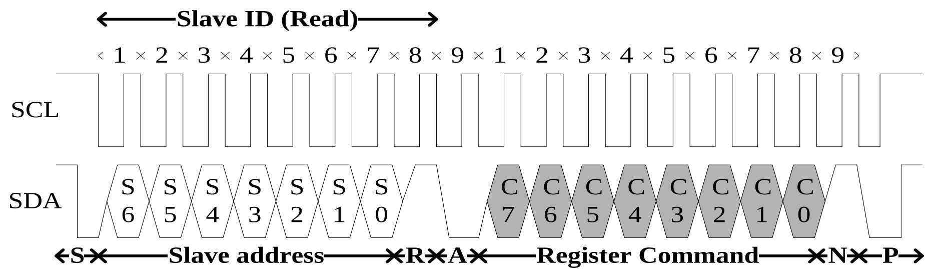
5.1.2. I2C Write Protocol (type 2)



5.1.3. I2C Read Protocol

1	7	1	1	8	1	1
S	Slave address	R	A	Register Command	N	P

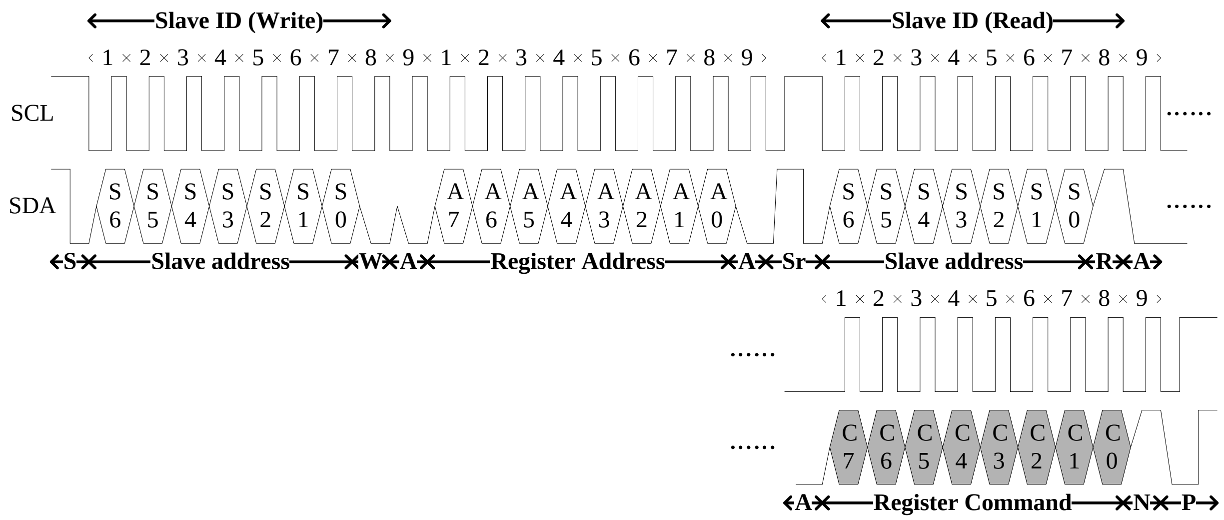
←Slave ID (Read)→



5.1.4. I2C Read (Combined format) Protocol

1	7	1	1	8	1	1	7	1	1	8	1	1
S	Slave address	W	A	Register Address	A	Sr	Slave address	R	A	Register Command	N	P

←Slave ID (Write)→ ←Slave ID (Read)→



A	Acknowledge (0 for an ACK)	**N**	Non-Acknowledge(1 for an NACK)
S	Start condition	**Sr**	Repeated Start condition
P	Stop condition		
W	Write (0 for writing)	**R**	Read (1 for read)
(grey box)	Slave-to-master	(white box)	Master-to-Slave

5.2. I2C Slave Address

The device offers three slave addresses that are selectable via pin 4 (SEL). The slave addresses are 7 bits. A read/write bit should be appended to the slave address by the master device to properly communicate with the device.

(1) SEL Pin is “VDD” :

I²C Slave Address (SEL = VDD)									
Command Type	(0x53)							W/R	value
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Write	1	0	1	0	0	1	1	0	0xA6
Read	1	0	1	0	0	1	1	1	0xA7

(1) SEL Pin is Float :

I²C Slave Address (SEL = Float)									
Command Type	(0x52)							W/R	value
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Write	1	0	1	0	0	1	0	0	0xA4
Read	1	0	1	0	0	1	0	1	0xA5

(1) SEL Pin is “GND” :

I²C Slave Address (SEL = GND)									
Command Type	(0x51)							W/R	value
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Write	1	0	1	0	0	0	1	0	0xA2
Read	1	0	1	0	0	0	1	1	0xA3

The SEL pin read cycle is only executed once after power-on-reset or software reset.

6. Register Set

Address	R / W	Register Name	Description	Reset Value
0x80	R/W	CS_ALS_CONTR	CS/ALS operation mode control SW reset	0x00
0x81	R/W	PS_ CONTR	PS operation mode control	0x00
0x82	R/W	PS_LED	PS LED settings	0x63
0x83	R/W	PS_N_PULSES	PS number of LED pulses	0x08
0x84	R/W	PS_MEAS_RATE	PS measurement rate in active mode	0x05
0x85	R/W	CS_ALS_MEAS_RATE	CS/ALS measurement rate in active mode, CS/ALS resolution, and ALS gain	0x83
0x86	R	PART_ID	Part number ID and revision ID	0xA0
0x87	--	Reserved	--	--
0x88	R	CS_ALS_PS_STATUS	Interrupt status, data status, and PS logic signal status	0x00
0x89	R	PS_DATA_0	PS measurement data, Lower Byte	0x00
0x8A	R	PS_DATA_1	PS measurement data, Upper Byte, and overflow	0x00
0x8B	R	CS_DATA_RED_0	CS Red measurement data, Lower Byte	0x00
0x8C	R	CS_DATA_RED_1	CS Red measurement data, Middle Byte	0x00
0x8D	R	CS_DATA_RED_2	CS Red measurement data, Upper Byte	0x00
0x8E	R	CS_DATA_GREEN_0	CS Green measurement data, Lower Byte	0x00
0x8F	R	CS_DATA_GREEN_1	CS Green measurement data, Middle Byte	0x00
0x90	R	CS_DATA_GREEN_2	CS Green measurement data, Upper Byte	0x00
0x91	R	CS_DATA_BLUE_0	CS Blue measurement data, Lower Byte	0x00
0x92	R	CS_DATA_BLUE_1	CS Blue measurement data, Middle Byte	0x00
0x93	R	CS_DATA_BLUE_2	CS Blue measurement data, Upper Byte	0x00
0x94	R	CS_DATA_WHITE_0	CS White measurement data, Lower Byte	0x00
0x95	R	CS_DATA_WHITE_1	CS White measurement data, Middle Byte	0x00
0x96	R	CS_DATA_WHITE_2	CS White measurement data, Upper Byte	0x00
0x97	--	Reserved	--	--
0x98	R/W	INTERRUPT	Interrupt configuration and PS logic mode	0x00
0x99	R/W	PS_THRES_UP_0	PS interrupt upper threshold, Lower Byte	0xFF
0x9A	R/W	PS_THRES_UP_1	PS interrupt upper threshold, Upper Byte	0x07
0x9B	R/W	PS_THRES_LOW_0	PS interrupt lower threshold, Lower Byte	0x00
0x9C	R/W	PS_THRES_LOW_1	PS interrupt lower threshold, Upper Byte	0x00
0x9D	--	Reserved	--	--
0x9E	R/W	PS_CAN_0	PS intelligent cancellation level setting, Lower Byte	0x00
0x9F	R/W	PS_CAN_1	PS intelligent cancellation level setting, Upper Byte	0x00
0xA0	R/W	CS_ALS_THRES_UP_0	CS/ALS interrupt upper threshold, Lower Byte	0xFF
0xA1	R/W	CS_ALS_THRES_UP_1	CS/ALS interrupt upper threshold, Middle Byte	0xFF
0xA2	R/W	CS_ALS_THRES_UP_2	CS/ALS interrupt upper threshold, Upper Byte	0x03
0xA3	R/W	CS_ALS_THRES_LOW_0	CS/ALS interrupt lower threshold, Lower Byte	0x00
0xA4	R/W	CS_ALS_THRES_LOW_1	CS/ALS interrupt lower threshold, Middle Byte	0x00
0xA5	R/W	CS_ALS_THRES_LOW_2	CS/ALS interrupt lower threshold, Upper Byte	0x00
0xA6	--	Reserved	--	--
0xA7	R/W	INTERRUPT_PERSIST	CS/ALS and PS interrupt persist setting	0x00

6.1. CS_ALS_CONTR Register (Address: 0x80) (Read/Write)

This register controls the operation modes of CS/ALS, which can be set to either standby or active mode. When writing to this register, it will cause a stop to any ongoing measurements (both ALS/CS and PS) and start new measurement.

0x80	CS_ALS_CONTR (default = 0x00)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Reserved					***SW Reset***	***CS_ALS Enable***	

Field	Bits	Default	Description	
Reserved	7:3	0000 00	--	--
SW Reset	2	0	0	Software reset is NOT triggered (default)
			1	Software reset is triggered
CS_ALS Enable	1:0	00	00	CS/ALS on standby
			11	CS/ALS active
			10/01	Reserved

6.2. PS_CONTR Register (Address: 0x81) (Read/Write)

This register controls the Proximity Sensor (PS) operation mode. The PS can be set to either standby or active mode. When writing to this register, it will cause a stop to any ongoing measurements (both ALS/CS and PS) and start new measurement.

0x81	PS_CTRL (default = 0x00)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Reserved						***PS Enable***	***Reserved***

Field	Bits	Default	Description	
Reserved	7:2	000000	--	--
PS Enable	1	0	0	PS on standby
			1	PS active
Reserved	0	0	--	--

6.3. PS_LED Register (Address: 0x82) (Read/Write)

This register controls the LED driving current and the LED pulse modulation frequency.

0x82	PS_LED (default = 0x63)							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
	LED Pulse Modulation Frequency			***Reserved***		***LED Current***		

Field	Bits	Default	Description	
LED Pulse Modulation Frequency	7:5	011	000/001/010	Reserved
			011	60kHz (default)
			100	70kHz
			101	80kHz
			110	90kHz
			111	100kHz
Reserved	4:3	00	00	--
LED Current	2:0	011	000	25mA
			001	50mA
			010	75mA
			011	100mA (default)
			1XX	125mA

6.4. PS_N_PULSES Register (Address: 0x83) (Read/Write)

This register controls the number of PS LED pulses emitted (up to 32 pulses)

0x83	PS_N_PULSES (default = 0x08)							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
	Reserved		***Number of LED Pulses***					

Field	Bits	Default	Description	
Reserved	7:6	00	00	Reserved
Number of LED pulses	5:0	00 1000	00 0000	0 pulse (no light emission)
			00 0001	1 pulse
			00 0010	2 pulses
			…	…
			00 1000	8 pulses (default)
			…	…
			10 0000	32 pulses
			1X XXXX	Reserved

6.5. PS_MEAS_RATE Register (Address: 0x84) (Read/Write)

This register controls the timing of the periodic measurements of the PS during active mode. When the measurement rate is programmed to be faster than possible for the programmed ADC measurement, the rate will be lowered than programmed (maximum speed).

0x84	PS_MEAS_RATE (default = 0x05)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Reserved					***PS Measurement Rate***		

Field	Bits	Default	Description	
Reserved	7:3	00000	--	--
PS Measurement Rate	2:0	101	000	6.25ms
			001	12.5ms
			010	25ms
			011	50ms
			100	75ms
			101	100ms (default)
			110	200ms
			111	400ms

6.6. CS_ALS_MEAS_RATE Register (Address: 0x85) (Read/Write)

This register controls CS/ALS measurement resolution, Gain setting and measurement rate. When the measurement rate is programmed to be faster than possible for the programmed ADC measurement, the rate will be lowered than programmed (maximum speed).

0x85	CS_ALS_MEAS_RATE (default = 0x83)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	CS/ALS Resolution / Bit Width			***CS/ALS Gain Range***		***CS/ALS Measurement Rate***		

Field	Bits	Default	Description	
CS/ALS Resolution / Bit Width	7:5	100	000	18 Bit, Conversion time = 800ms
			001	17 Bit, Conversion time = 400ms
			010	16 Bit, Conversion time = 200ms
			011	15 Bit, Conversion time = 100ms
			100	14 Bit, Conversion time = 50ms (default)
			101/110/111	Reserved
CS/ALS Gain Range	4:3	00	00	Gain X1 (2 to 32768 Lux) (default)
			01	Gain X5 (0.4 to 6554 Lux)
			10	Gain X10 (0.2 to 3277 Lux)
			11	Gain X20 (0.1 to 1638 Lux)
CS/ALS Measurement Rate	2:0	011	000	50ms
			001	100ms
			010	200ms
			011	500ms (default)
			100	1000ms
			101/110/111	2000ms

6.7. PART_ID Register (Address: 0x86) (Read Only)

This register defines the part number and revision identification of the sensor.

0x86	PART_ID (default = 0xA0)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Part Number ID				***Reserved***			

Field	Bits	Default	Description
Part Number ID	7:4	1010	Part Number ID
Reserved	3:0	0000	--

6.8. CS_ALS_PS_STATUS Register (Address: 0x88) (Read Only)

This register stores the information about the CS/ ALS and PS interrupts and data status. The interrupt status in Bit 1 and Bit 5 determines if the CS/ALS and PS interrupt criteria are met in Normal Interrupt Mode : its triggers when the CS/ALS and/or PS data is above the upper or below the lower threshold for a specified number of consecutive measurements in respective interrupt persist settings. This register also provides PS logic signal status, which is used for indicating whether the detected object is near (PS data larger than PS upper threshold settings) or far (PS data smaller than PS lower threshold settings). For details interrupt behavior, refer to Section 6 (page 33).

0x88	CS_ALS_PS_STATUS (default = 0x00)							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
	Reserved		***CS/ALS interrupt status***	***CS/ALS data status***	***Reserved***	***PS logic signal status***	***PS interrupt status***	***PS data status***

Field	Bits	Default	Description	
Reserved	7:6	00	--	--
CS/ALS Interrupt Status	5	0	0	Interrupt is NOT triggered (default)
			1	Interrupt is triggered and will be cleared after read
CS/ALS Data Status	4	0	0	CS/ALS data is old data (Data has been read)
			1	CS/ALS data is new data (Data has not been read and will be cleared after read)
Reserved	3	0	--	--
PS Logic Signal Status	2	0	0	Object is far (default)
			1	Object is near
PS Interrupt Status	1	0	0	Interrupt is NOT triggered (default)
			1	Interrupt is triggered and will be cleared after read
PS Data Status	0	0	0	PS data is old data (Data has been read)
			1	PS data is new data (Data has not been read and will be cleared after read)

6.9. PS_DATA Registers (Address: 0x89 / 0x8A) (Read Only)

The PS ADC channel data are expressed as an 11-bit data spread over 2 registers. The PS_DATA_0 and PS_DATA_1 registers provide the lower and upper byte respectively. An overflow bit is available to check if the PS data overflows.

When I^2C read operation is active and points to any of the register address between 0x88 and 0x96, both registers PS_DATA_0 and PS_DATA_1 will be locked until the I^2C read operation has been completed or the specified address range is left. New measurement data is stored into temporary registers and the PS_DATA registers will be updated as soon as there is no on-going I^2C read operation to the address range 0x88 to 0x96.

0x89	PS_DATA_0 (default = 0x00)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	PS Data Low							
0x8A	**PS_DATA_1 (default = 0x00)**							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Reserved			*Overflow*	*Reserved*	*PS Data High*		

Field	Address	Bits	Default	Description	
PS Data, Low	0x89	7:0	00000000	--	PS ADC lower byte data
Reserved	0x8A	7:5	000	--	--
Overflow	0x8A	4	0	0	Valid PS data (default)
				1	Overflow of PS data
Reserved	0x8A	3	0	--	--
PS Data, High	0x8A	2:0	000	--	PS ADC upper byte data

6.10. CS_DATA_RED Registers (Address: 0x8B / 0x8C / 0x8D) (Read Only)

The Color Sensor Red Channel digital output data are expressed as a 14 to 18 bit unsigned integer data. When I^2C read operation is active and points to any of the register address between 0x88 and 0x96, all 3 registers will be locked until the I^2C read operation has been completed or the specified address range is left. This is to ensure that the data in the registers is from the same measurement even if an additional measurement cycle ends during the read operation. New measurement data is stored into temporary registers and the CS_DATA_RED registers will be updated as soon as there is no on-going I^2C read operation to the address range 0x88 to 0x96.

0x8B	CS_DATA_RED_0 (default = 0x00)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	CS DATA RED, Low							
0x8C	**CS_DATA_RED_1 (default = 0x00)**							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	CS DATA RED, Middle							
0x8D	**CS_DATA_RED_2 (default = 0x00)**							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Reserved						*CS DATA RED, High*	

Field	Address	Bits	Default	Description
CS Data Red, Low	0x8B	7:0	00000000	CS Data (Red) lower byte data
CS Data Red, Middle	0x8C	7:0	00000000	CS Data (Red) Middle byte data
CS Data Red, High	0x8D	7:2	000000	Reserved
		1:0	00	CS Data (Red) Higher byte data

6.11. CS_DATA_GREEN Registers (Address: 0x8E / 0x8F / 0x90) (Read Only)

The Color Sensor Green Channel digital output data are expressed as a 14 to 18 bit unsigned integer data. When I^2C read operation is active and points to any of the register address between 0x88 and 0x96, all 3 registers will be locked until the I^2C read operation has been completed or the specified address range is left. This is to ensure that the data in the registers is from the same measurement even if an additional measurement cycle ends during the read operation. New measurement data is stored into temporary registers and the CS_DATA_GREEN registers will be updated as soon as there is no on-going I^2C read operation to the address range 0x88 to 0x96.

0x8E	CS_DATA_GREEN_0 (default = 0x00)							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
	CS DATA GREEN, Low							
0x8F	**CS_DATA_GREEN_1 (default = 0x00)**							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
	CS DATA GREEN, Middle							
0x90	**CS_DATA_GREEN_2 (default = 0x00)**							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
	Reserved						***CS DATA GREEN, High***	

Field	Address	Bits	Default	Description
CS Data Green, Low	0x8B	7:0	00000000	CS Data (Green) lower byte data
CS Data Green, Middle	0x8C	7:0	00000000	CS Data (Green) Middle byte data
CS Data Green, High	0x8D	7:2	000000	Reserved
		1:0	00	CS Data (Green) Higher byte data

6.12. CS_DATA_BLUE Registers (Address: 0x91 / 0x92 / 0x93) (Read Only)

The Color Sensor Blue Channel digital output data are expressed as a 14 to 18 bit unsigned integer data.

When I^2C read operation is active and points to any of the register address between 0x88 and 0x96, all 3 registers will be locked until the I^2C read operation has been completed or the specified address range is left. This is to ensure that the data in the registers is from the same measurement even if an additional measurement cycle ends during the read operation. New measurement data is stored into temporary registers and the CS_DATA_BLUE registers will be updated as soon as there is no on-going I^2C read operation to the address range 0x88 to 0x96.

0x91	CS_DATA_BLUE_0 (default = 0x00)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	CS DATA BLUE, Low							
0x92	CS_DATA_BLUE_1 (default = 0x00)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	CS DATA BLUE, Middle							
0x93	CS_DATA_BLUE_2 (default = 0x00)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Reserved						*CS DATA BLUE, High*	

Field	Address	Bits	Default	Description
CS Data Blue, Low	0x91	7:0	00000000	CS Data (Blue) Lower byte data
CS Data Blue, Middle	0x92	7:0	00000000	CS Data (Blue) Middle byte data
CS Data Blue, High	0x93	7:2	000000	Reserved
		1:0	00	CS Data (Blue) Higher byte data

6.13. CS_DATA_WHITE Registers (Address: 0x94 / 0x95 / 0x96) (Read Only)

The Color Sensor White Channel digital output data are expressed as a 14 to 18 bit unsigned integer data. When I^2C read operation is active and points to any of the register address between 0x88 and 0x96, all 3 registers will be locked until the I^2C read operation has been completed or the specified address range is left. This is to ensure that the data in the registers is from the same measurement even if an additional measurement cycle ends during the read operation. New measurement data is stored into temporary registers and the CS_DATA_WHITE registers will be updated as soon as there is no on-going I^2C read operation to the address range 0x88 to 0x96.

0x94	CS_DATA_WHITE_0 (default = 0x00)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	CS DATA WHITE, Low							

0x95	CS_DATA_WHITE_1 (default = 0x00)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	CS DATA WHITE, Middle							

0x96	CS_DATA_WHITE_2 (default = 0x00)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Reserved				*CS DATA WHITE, High*			

Field	Address	Bits	Default	Description
CS Data White, Low	0x94	7:0	00000000	CS Data (White) lower byte data
CS Data White, Middle	0x95	7:0	00000000	CS Data (White) Middle byte data
CS Data White, High	0x96	7:4	0000	Reserved
		3:0	0000	CS Data (White) Higher byte data

6.14. INTERRUPT Register (Address: 0x98) (Read/Write)

This register controls the operation of the interrupt pin and functions. CS/ALS and PS have independent interrupt signal and both CS/ALS and PS interrupts are active low.

CS/ALS interrupt is enabled by Bit 0, and it is threshold triggered based. Besides, PS interrupt is enabled by Bit 2, and its output pin can be selected as either Normal Interrupt Mode or PS Logic Output Mode through Bit 3.

Under Normal Interrupt Mode, the edge-triggered interrupt signal output will be maintains at active level until CS_ALS_PS_STATUS register is read. While for PS Logic Output Mode, the interrupt pin output is updated after every measurement and output state is maintained between measurements. The PS Logic Output Mode has priority over any other interrupt signal, and hence no CS/ALS interrupt can be signaled at the interrupt pin under this mode.

0x98	INTERRUPT (default = 0x00)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Reserved				*INT PIN OUTPUT MODE*	*PS INT PIN ENABLE*	*Reserved*	*CS/ALS INT PIN ENABLE*

Field	Bits	Default	Description	
Reserved	7:4	0000	--	--
Interrupt Pin Output Mode	3	0	0	Normal Interrupt Mode: After interrupt event, INT output pin maintains active level until CS_ALS_PS_STATUS register is read (default)
			1	PS Logic Output Mode: INT output pin is updated after every measurement and maintains output state between measurements.
PS Interrupt Pin Enable	2	0	0	PS interrupt disabled (default)
			1	PS interrupt enabled
Reserved	1	0	0	Must be 0
CS/ALS Interrupt Pin Enable	0	0	0	CS/ALS interrupt disabled (default)
			1	CS/ALS interrupt enabled

6.15. PS_THRES Registers (Address: 0x99 / 0x9A / 0x9B / 0x9C) (Read/Write)

The PS_THRES_UP (16-bits) and PS_THRES_LOW (16-bits) registers determines the upper and lower limit of the interrupt threshold value respectively. Interrupt will be triggered if measurement data in PS_DATA registers is exceeding the upper and lower limits.

0x99	PS_THRES_UP_0 (default = 0xFF)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	PS Upper Threshold, Low							
0x9A	PS_THRES_UP_1 (default = 0x07)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Reserved					***PS Upper Threshold, High***		

0x9B	PS_THRES_LOW_0 (default = 0x00)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	PS Lower Threshold, Low							
0x9C	PS_THRES_LOW_1 (default = 0x00)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Reserved					***PS Lower Threshold, High***		

Field	Address	Bits	Default	Description
PS Upper Threshold, Low	0x99	7:0	00000000	PS Upper Interrupt Threshold, Low byte
Reserved	0x9A	7:3	00000	--
PS Upper Threshold, High	0x9A	2:0	000	PS Upper Interrupt Threshold, High byte
PS Lower Threshold, Low	0x9B	7:0	00000000	PS Lower Interrupt Threshold, Low byte
Reserved	0x9C	7:3	00000	--
PS Lower Threshold, High	0x9C	2:0	000	PS Lower Interrupt Threshold, High byte

6.16. PS_CAN Registers (Address: 0x9E / 0x9F) (Read/Write)

This register defines the offset compensation value for proximity offsets caused by device variations, optical crosstalk and other environment factors. This register sets the PS cancellation value to be subtracted from the measured PS data before the data is transferred to the PS_DATA registers.

0x9E	PS_CAN_0 (default = 0x00)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	PS Cancellation Level, Low							
0x9F	PS_CAN_1 (default = 0x00)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Reserved					*PS Cancellation Level, High*		

Field	Address	Bits	Default	Description
PS Cancellation Level, Low	0x9E	7:0	00000000	PS Cancellation Level, Low byte
Reserved	0x9F	7:3	00000	--
PS Cancellation Level, High	0x9F	2:0	000	PS Cancellation Level, High byte

6.17. CS_ALS_THRES Registers (Address: 0xA0-0xA2 / 0xA3-0xA5) (Read/Write)

The CS_ALS_THRES_UP (up to 18-bits) and CS_ALS_THRES_LOW (up to 18-bits) registers determines the upper and lower limit of the interrupt threshold value respectively. Interrupt will be triggered if measurement data in CS_ALS_DATA_GREEN registers is exceeding the upper and lower limits.

0xA0	CS_ALS_THRES_UP_0 (default = 0xFF)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	CS/ALS Upper Threshold, Low							
0xA1	CS_ALS_THRES_UP_1 (default = 0xFF)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	CS/ALS Upper Threshold, Mid							
0xA2	CS_ALS_THRES_UP_2 (default = 0xFF)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Reserved						*CS/ALS Upper Threshold, High*	

0xA3	CS_ALS_THRES_LOW_0 (default = 0x00)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	CS/ALS Lower Threshold, Low							

0xA4	CS_ALS_THRES_LOW_1 (default = 0x00)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	CS/ALS Lower Threshold, Mid							

0xA5	CS_ALS_THRES_LOW_2 (default = 0x00)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Reserved						*CS/ALS Lower Threshold, High*	

Field	Address	Bits	Default	Description
CS/ALS Upper Threshold, Low	0xA0	7:0	11111111	CS/ALS upper interrupt threshold, Low byte
CS/ALS Upper Threshold, Mid	0xA1	7:0	11111111	CS/ALS upper interrupt threshold, Mid byte
CS/ALS Upper Threshold, High	0xA2	7:2	111111	Reserved
		1:0	11	CS/ALS upper interrupt threshold, High byte
CS/ALS Lower Threshold, Low	0xA3	7:0	00000000	CS/ALS lower interrupt threshold, Low byte
CS/ALS Lower Threshold, Mid	0xA4	7:0	00000000	CS/ALS lower interrupt threshold, Mid byte
CS/ALS Lower Threshold, High	0xA5	7:2	000000	Reserved
		1:0	00	CS/ALS lower interrupt threshold, High byte

6.18. INTERRUPT_PERSIST Register (Address: 0xA7) (Read/Write)

This register sets the PS and CS/ALS persist level. Persist is the *N* number of times the measurement data is outside the range defined by the upper and lower threshold limits before asserting the interrupt.

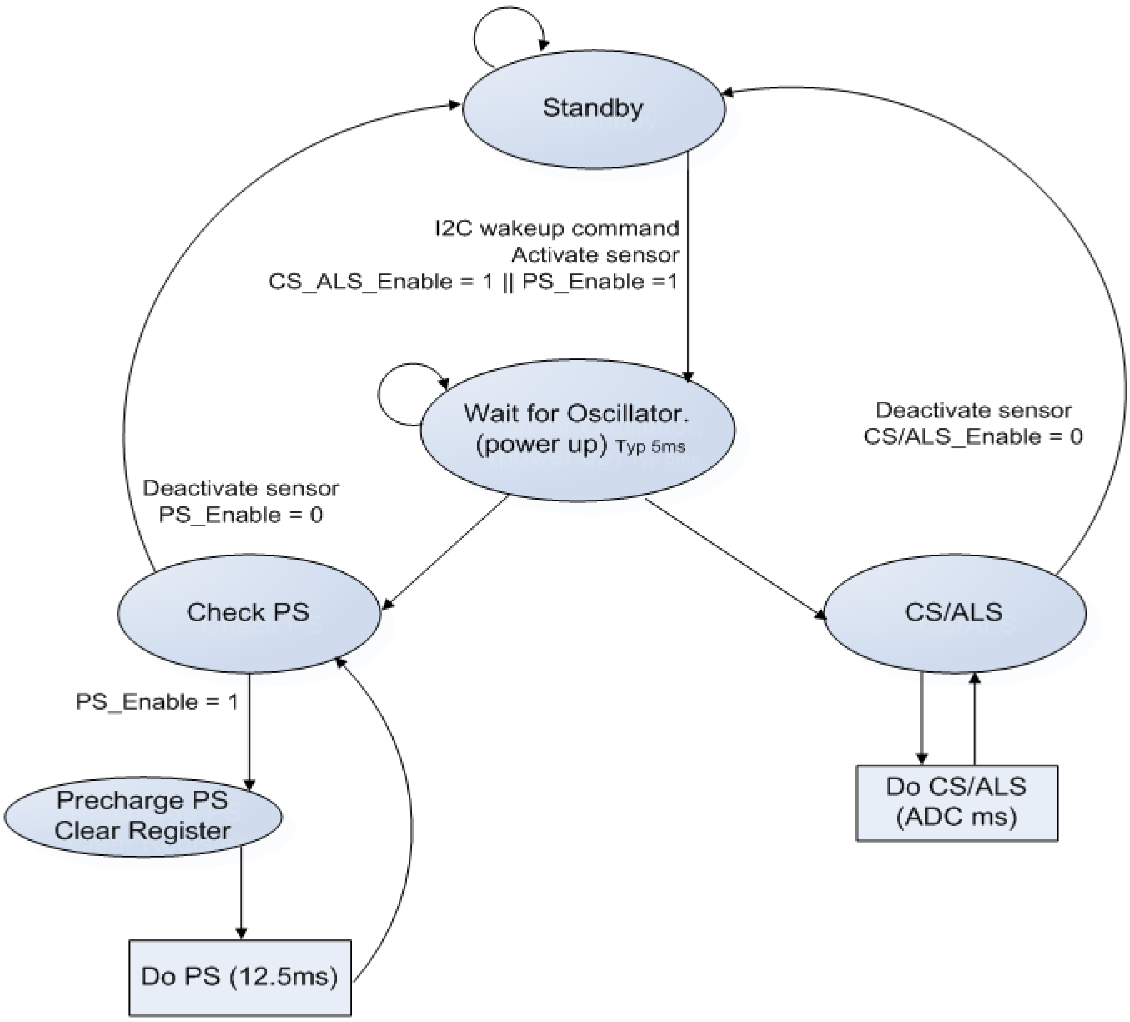
0xA7	INTERRUPT_PERSIST (default = 0x00)							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
	PS Persist				***CS/ALS Persist***			

Field	Bits	Default	Description	
PS Persist	7:4	00000	0000	Every PS value out of threshold range asserts an interrupt (default)
			0001	2 consecutive PS values out of threshold range assert an interrupt
			…	…
			1111	16 consecutive PS values out of threshold range assert an interrupt
CS/ALS Persist	3:0	0000	0000	Every CS/ALS value out of threshold range asserts an interrupt (default)
			0001	2 consecutive CS/ALS values out of threshold range assert an interrupt
			…	…
			1111	16 consecutive CS/ALS values out of threshold range assert an interrupt

7. Device Operation (State Machine and Interrupt Features)

7.1. State Machine

Below diagram is the main state machine of LTR-530RGB.



During the CS/ALS and PS Operation, CS/ALS measurements can be activated by setting the CS_ALS_Enable bit to 1, and PS measurement can be activated by setting the PS_Enable bit to 1. As soon as the PS and/or the CS/ALS sensors become activated through an I2C command, the internal support blocks are powered on. Once the voltages and currents are settled (typically after 5ms), the state machine checks for trigger events from a measurement scheduler to start CS/ALS or PS conversions according to the selected measurement repeat rates. Once PS_Enable or CS_ALS_Enable is changed back to 0, a running conversion on the respective channel will be completed and the relevant ADCs and support blocks will move to power-down state.

7.2. Interrupt Features

This device generates independent CS/ALS and PS interrupt signals that can be multiplexed and output to the INT output pin. Both CS/ALS and PS interrupts are active low. The interrupt conditions are always evaluated after completion of a new conversion on the CS/ALS and PS channels. Figure 7.1 below illustrates the interrupt status (In register 0x88) as well as interrupt pin signal (configure through register 0x98).

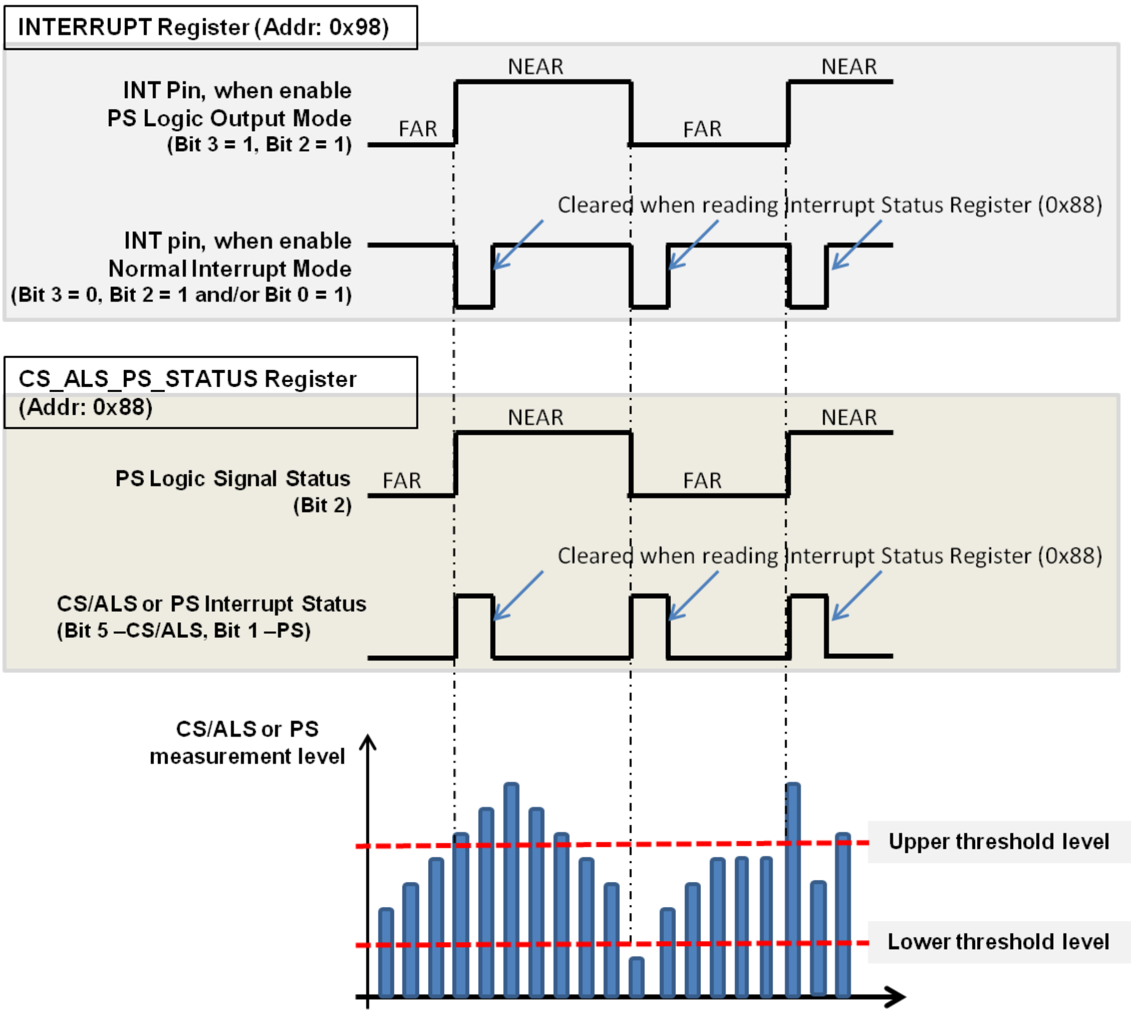


Figure 7.1 : Interrupt behavior for different interrupt configuration in register 0x98 and 0x88.

8. Pseudo Codes Examples

Slave address

// The I2C slave address of LTR-530 is a function of digital logic at SEL PIN. Please choose appropriate to hardware.

```
Slave_Addr = 0xA4                               // Slave address with SEL PIN = FLOAT
```

CS_ALS_CONTR Register

// This defines the operating modes of the CS/ALS
// Default settings is 0x00 in Standby mode.

```
Register_Addr = 0x80                            // CS_ALS_CONTR register
Command = 0x03                                  // CS/ALS in Active Mode
WriteByte(Slave_Addr, Register_Addr, Command);
```

PS_CONTR Register

// This defines the operating modes of the PS
// Default settings is 0x00 in Standby mode.

```
Register_Addr = 0x81                            // PS_CONTR register
Command = 0x02                                  // PS in Active Mode
WriteByte(Slave_Addr, Register_Addr, Command);
```

PS_LED Register

// This defines the LED pulse modulation frequency and Peak current.
// Default setting is 0x63 (Pulse Freq = 60kHz, peak current = 100mA).

```
Register_Addr = 0x82                            // PS_LED register
Command = 0x63                                  // For Pulse Freq = 60kHz, Peak Current =100mA
                                                // For Pulse Freq = 70kHz, Peak Current =100mA, Command =0x83
                                                // For Pulse Freq = 70kHz, Peak Current = 50mA, Command = 0x81
                                                // For Pulse Freq = 100kHz, Peak Current = 100mA, Command = 0xE3
                                                // For Pulse Freq = 100kHz, Peak Current = 125mA, Command = 0xE4
WriteByte(Slave_Addr, Register_Addr, Command)
```

PS_N_PULSES

// This controls the number of PS LED pulses emitted (Up to 32 pulses)
// Default setting of the register is 0x08 (8 pulses)

```
Register_Addr = 0x83                            // PS_N_PULSES register
Command = 0x08                                  // 8 pulses
                                                // 0 (no light), Command = 0x00
                                                // 4 pulses, Command = 0x04
                                                // 32 pulses, Command = 0x20
WriteByte(Slave_Addr, Register_Addr, Command)
```

PS_MEAS_RATE

//This controls the PS measurement rate.
// Default setting of the register is 0x05 (Measurement rate 100ms)

```
Register_Addr = 0x84                            // PS_MEAS_RATE register
Command = 0x05                                  // Meas rate = 100ms
                                                // For Meas rate = 400ms, Command = 0x07
                                                // For Meas rate = 6.25ms, Command = 0x00
WriteByte(Slave_Addr, Register_Addr, Command)
```

CS_ALS_MEAS_RATE

// This controls the CS/ALS measurement resolution, gain setting and measurement rate.
// Default setting of the register is 0x83 (Integration time 50ms or 14 bit resolution, Gain=x1, Measurement rate of 500ms)

```
Register_Addr = 0x85                         // CS_ALS_MEAS_RATE register
Command = 0x83                               // Resolution 14 bit, Gain =1, Meas rate =500ms
                                             // For Resolution 18 bit, Gain =1, Meas rate =500ms, Command =0x03
                                             // For Resolution 18 bit, Gain =20, Meas rate =500ms, Command =0x1B
                                             // For Resolution 18 bit, Gain =5, Meas rate =1000ms, Command =0x0C
                                             // For Resolution 16 bit, Gain =10, Meas rate =2000ms, Command =0x55
WriteByte(Slave_Addr, Register_Addr, Command)
```

CS_ALS_PS_STATUS Register (Read Only)

// This Register contains the information on Interrupt, CS/ALS and PS data availability status.

```
Register_Addr = 0x88                         // CS_ALS_PS_STATUS register address
Data = ReadByte(Slave_Addr, Register_Addr)

CS/ALS_Interrupt_Status = Data & 0x20        // If 0x20 Interrupt condition fulfilled,
                                             // If 0x00 Interrupt condition not fulfilled
CS/ALS_Data_Status = Data & 0x10             // If 0x10 New Data
                                             // If 0x00 Old (previously read) Data
PS_Logic_Signal_Status = Data & 0x04         // If 0x04 Object is close
                                             // If 0x00 Object is far
PS_Interrupt_Status = Data & 0x02            // If 0x02 Interrupt condition fulfilled,
                                             // If 0x00 Interrupt condition not fulfilled
PS_Data_Status = Data & 0x01                 // If 0x01 New Data
                                             // If 0x00 Old (previously read) Data
```

PS_DATA Registers (Read Only)

//The register 0x89 contains PS ADC lower byte data.
//The register 0x8A contains PS ADC 3 bits of upper byte data and PS Overflow flag
//These registers should be read as a group, with the lower address being read first.

```
Register_Addr = 0x89                         // PS_DATA0 low byte address
Data0=ReadByte(Slave_Addr, Register_Addr)    // Data= PS ADC lower byte data

Register_Addr = 0x8A                         // PS_DATA1 high byte address
Data=ReadByte(Slave_Addr, Register_Addr)     // Data= PS ADC lower byte data
Data1=Data&0x03                              // Mask with 0x03 to extract data
PS_ADC_Data = (Data1 << 8) | Data0           // Shift and combine lower and upper bytes to give 11-bit PS data

PS_Overflow_status = Data & 0x10             // If 0x10 PS Data is overflow
                                             // If 0x00 PS Data is valid
```

CS_DATA_RED Registers (Read Only)

// The register 0x8B contains CS_RED ADC lower byte data.
//The register 0x8C contains CS_RED ADC 1 upper byte data.
//The register 0x8D contains CS_RED ADC 2 (top) upper byte data.
//These registers should be read as a group, with the lower address being read first.

```
Register_Addr = 0x8B                         // CS_DATA_RED0 low byte address
Data0=ReadByte(Slave_Addr, Register_Addr)
Register_Addr = 0x8C                         // CS_DATA_RED1 middle byte address
Data1=ReadByte(Slave_Addr, Register_Addr)
Register_Addr = 0x8D                         // CS_DATA_RED2 upper byte address
Data2=ReadByte(Slave_Addr, Register_Addr)
CS_RED_ADC_Data =(Data2<<16)| (Data1 << 8) | Data0
                                             // Shift and combine all register data to get CS_RED ADC Data
```

CS_DATA_GREEN Registers (Read Only)

// The register 0x8E contains CS_GREEN ADC lower byte data.
// The register 0x8F contains CS_GREEN ADC 1 upper byte data.
// The register 0x90 contains CS_GREEN ADC 2 (top) upper byte data.
// These registers should be read as a group, with the lower address being read first.

```
Register_Addr = 0x8E                            // CS_DATA_GREEN0 low byte address
Data0=ReadByte(Slave_Addr, Register_Addr)
Register_Addr = 0x8F                            // CS_DATA_GREEN1 middle byte address
Data1=ReadByte(Slave_Addr, Register_Addr)
Register_Addr = 0x90                            // CS_DATA_GREEN2 upper byte address
Data2=ReadByte(Slave_Addr, Register_Addr)
CS_GREEN_ADC_Data =(Data2<<16)| (Data1 << 8) | Data0
        // Shift and combine all register data to get CS_GREEN ADC Data
```

CS_DATA_BLUE Registers (Read Only)

// The register 0x91 contains CS_BLUE ADC lower byte data.
// The register 0x92 contains CS_BLUE ADC 1 upper byte data.
// The register 0x93 contains CS_BLUE ADC 2 (top) upper byte data.
// These registers should be read as a group, with the lower address being read first.

```
Register_Addr = 0x91                            // CS_DATA_BLUE0 low byte address
Data0=ReadByte(Slave_Addr, Register_Addr)
Register_Addr = 0x92                            // CS_DATA_BLUE1 middle byte address
Data1=ReadByte(Slave_Addr, Register_Addr)
Register_Addr = 0x93                            // CS_DATA_BLUE2 upper byte address
Data2=ReadByte(Slave_Addr, Register_Addr)
CS_BLUE_ADC_Data =(Data2<<16)| (Data1 << 8) | Data0
        // Shift and combine all register data to get CS_BLUE ADC Data
```

CS_DATA_WHITE Registers (Read Only)

//The register 0x94 contains CS_WHITE ADC lower byte data.
//The register 0x95 contains CS_WHITE ADC 1 upper byte data.
//The register 0x96 contains CS_WHITE ADC 2 (top) upper byte data.
//These registers should be read as a group, with the lower address being read first.

```
Register_Addr = 0x94                            // CS_DATA_WHITE0 low byte address
Data0=ReadByte(Slave_Addr, Register_Addr)
Register_Addr = 0x95                            // CS_DATA_WHITE1 middle byte address
Data1=ReadByte(Slave_Addr, Register_Addr)
Register_Addr = 0x96                            // CS_DATA_WHITE2 upper byte address
Data2=ReadByte(Slave_Addr, Register_Addr)
CS_WHITE_ADC_Data =(Data2<<16)| (Data1 << 8) | Data0
        // Shift and combine all register data to get CS_WHITE ADC Data
```

INTERRUPT Register

//This register controls the operation of the interrupt pins and options to trigger interrupt for CS/ALS and PS.
//The default value for this INTERRUPT register is 0x00 (Interrupts inactive for both CS/ALS and PS)

```
Register_Addr = 0x98                            // INTERRUPT Register address
// Normal Interrupt Mode: After interrupt event, INT output pin maintains active level until CS_ALS_PS_STATUS register is read
Command = 0x00                                  // CS/ALS Interrupt Disable, Threshold trigger mode; PS Interrupt Disable
Command = 0x01                                  // CS/ALS Interrupt Enable, Threshold trigger mode; PS Interrupt Disable
Command = 0x04                                  // CS/ALS Interrupt Disable, Threshold trigger mode; PS Interrupt
```

```
Enable
Command = 0x05          // CS/ALS Interrupt Enable, Threshold trigger mode; PS Interrupt Enable

// PS Logic Output Mode: INT output pin is updated after every measurement and maintains output state between measurements.
Command = 0x08          // PS Interrupt Disable, CS/ALS in Threshold trigger mode
Command = 0x09          // CS/ALS Interrupt Enable, Threshold trigger mode; PS Interrupt Disable
Command = 0x0C          // CS/ALS Interrupt Disable, Threshold trigger mode; PS Interrupt Enable
Command = 0x0D          // CS/ALS Interrupt Enable, Threshold trigger mode; PS Interrupt Enable
WriteByte(Slave_Addr, Register_Addr, Command)
```

PS_THRES Registers

```
// The register 0x99 contains PS Interrupt upper threshold lower byte data (PS_THRES_UP_0)
// The register 0x9A contains PS Interrupt upper threshold upper byte data (PS_THRES_UP_1)
// The register 0x9B contains PS Interrupt lower threshold lower byte data (PS_THRES_LOW_0)
// The register 0x9C contains PS Interrupt lower threshold upper byte data (PS_THREH_LOW_1)

// To set PS Upper threshold for Interrupt
Upper_Threshold_Value=1000                  // Example 1000
Data1 = Upper_Threshold_Value >> 8          // Shift right to extract the upper byte
Data0 = Upper_Threshold_Value & 0xFF        // Mask to extract lower byte.
Register_Addr = 0x99                        // PS_THRES_UP_0 Register address
WriteByte(Slave_Addr, Register_Addr, Data0)
Register_Addr = 0x9A                        // PS_THRES_UP_1 Register address
WriteByte(Slave_Addr, Register_Addr, Data1)

// To set PS Lower threshold for Interrupt

Lower_Threshold_Value=100                   // Example 100
Data1 = Lower_Threshold_Value >> 8          // Shift right to extract the upper byte
Data0 =Lower_Threshold_Value & 0xFF         // Mask to extract lower byte.
Register_Addr = 0x9B                        // PS_THRES_LOW_0 Register address
WriteByte(Slave_Addr, Register_Addr, Data0)
Register_Addr = 0x9C                        // PS_THRES_LOW_1 Register address
WriteByte(Slave_Addr, Register_Addr, Data1)
```

PS_CAN Registers

```
//The register 0x9E contains PS cancellation lower byte data (PS_CAN_0)
//The register 0x9F contains 3 bits of PS cancellation upper byte data (PS_CAN_1)

//To set PS Cancellation Value (0 to 2047)
PS_Cancel_Value=100                         // Example 100
Data1 = PS_Cancel_Value >> 8                // Shift right to extract the upper byte
Data0 = PS_Cancel_Value & 0xFF              // Mask to extract lower byte.
Register_Addr = 0x9E                        // PS_CAN_0 Register address
WriteByte(Slave_Addr, Register_Addr, Data0)
Register_Addr = 0x9F                        // PS_CAN_1 Register address
WriteByte(Slave_Addr, Register_Addr, Data1)
```

ALS_THRES Registers

```
//The register 0xA0 contains CS/ALS Interrupt upper threshold lower byte data (ALS_THRES_UP_0)
//The register 0xA1 contains CS/ALS Interrupt upper threshold 1 upper byte data (ALS_THRES_UP_1)
//The register 0xA2 contains CS/ALS Interrupt upper threshold 2 upper byte data (ALS_THRES_UP_2)

//The register 0xA3 contains CS/ALS Interrupt lower threshold lower byte data (ALS_THRES_LOW_0)
//The register 0xA4 contains CS/ALS Interrupt lower threshold 1 upper byte data (ALS_THRES_LOW_1)
```

//The register 0xA5 contains CS/ALS Interrupt lower threshold 2 upper byte data (ALS_THRES_LOW_2)

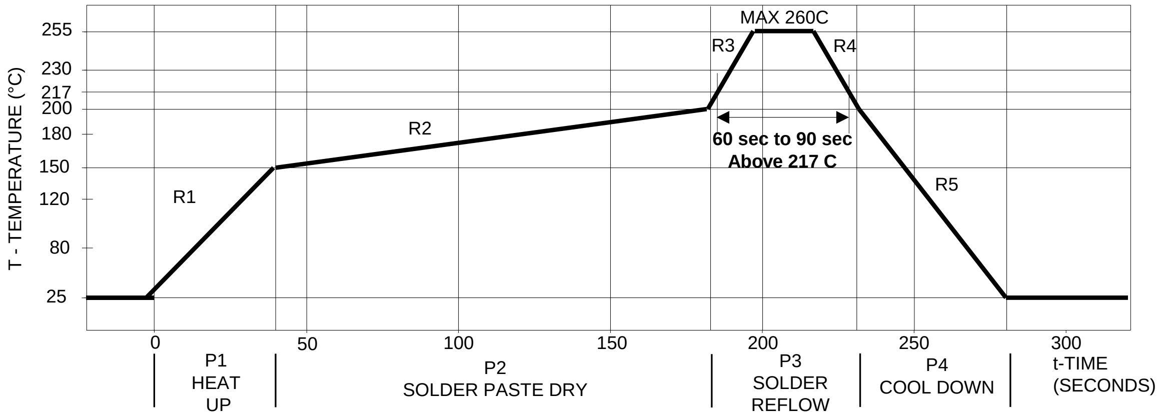
```
// To set ALS Upper threshold for Interrupt
Upper_Threshold_Value=1000                  // Example 1000
Data2 = Upper_Threshold_Value >> 16         // Shift right to extract the 2 upper byte
Data1 = Upper_Threshold_Value >> 8          // Shift right to extract the 1 upper byte
Data0 = Upper_Threshold_Value & 0xFF        // Mask to extract lower byte.

Register_Addr = 0xA0                        // CS/ALS_THRES_UP_0 Register address
WriteByte(Slave_Addr, Register_Addr, Data0)
Register_Addr = 0xA1                        // CS/ALS_THRES_UP_1 Register address
WriteByte(Slave_Addr, Register_Addr, Data1)
Register_Addr = 0xA2                        // CS/ALS_THRES_UP_2 Register address
WriteByte(Slave_Addr, Register_Addr, Data2)

// To set ALS Lower threshold for Interrupt
Lower_Threshold_Value=100                   // Example 100
Data2 = Lower_Threshold_Value >> 16         // Shift right to extract the 2 upper byte
Data1 = Lower_Threshold_Value >> 8          // Shift right to extract the 1 upper byte
Data0 = Lower_Threshold_Value & 0xFF        // Mask to extract lower byte.

Register_Addr = 0xA3                        // CS/ALS_THRES_LOW_0 Register address
WriteByte(Slave_Addr, Register_Addr, Data0)
Register_Addr = 0xA4                        // CS/ALS_THRES_LOW_1 Register address
WriteByte(Slave_Addr, Register_Addr, Data1)
Register_Addr = 0xA5                        // CS/ALS_THRES_LOW_2 Register address
WriteByte(Slave_Addr, Register_Addr, Data2)
```

INTERRUPT_PERSIST Register

// This register sets the CS/ALS and PS persist level.
// The default setting is 0x00. Interrupt at every CS/ALS and PS reading outside set thresholds.

```
Register_Addr = 0xA7     // INTERRUPT_PERSIST register
Command = 0x00           // Interrupt for every CS/ALS and PS value outside threshold
                         // Subsequent 2 ALS and every PS value, outside threshold range, Command =0x01
                         // Subsequent 2 ALS and PS values, outside threshold range, Command =0x11
                         // Subsequent 8 ALS and subsequent 11 PS values, outside threshold range, Command =0xA7
                         // Subsequent 11 ALS and subsequent 8 PS values, outside threshold range, Command =0x7A
WriteByte(Slave_Addr, Register_Addr, Command)
```

9. Recommended Leadfree Reflow Profile



Process Zone	Symbol	ΔT	Maximum ΔT/Δtime or Duration
Heat Up	P1, R1	25°C to 150°C	3°C/s
Solder Paste Dry	P2, R2	150°C to 200°C	100s to 180s
Solder Reflow	P3, R3	200°C to 260°C	3°C/s
	P3, R4	260°C to 200°C	-6°C/s
Cool Down	P4, R5	200°C to 25°C	-6°C/s
Time maintained above liquidus point , 217°C		> 217°C	60s to 90s
Peak Temperature		260°C	-
Time within 5°C of actual Peak Temperature		> 255°C	20s
Time 25°C to Peak Temperature		25°C to 260°C	8mins

It is recommended to perform reflow soldering no more than twice.

10. Moisture Proof Packaging

All LTR-530RGB-01 are shipped in moisture proof package. Once opened, moisture absorption begins. This part is compliant to JEDEC J-STD-033A Level 3.

10.1. Time from Unsealing to Soldering

After removal from the moisture barrier bag, the parts should be stored at the recommended storage conditions and soldered within seven days. When the moisture barrier bag is opened and the parts are exposed to the recommended storage conditions for more than seven days, the parts must be baked before reflow to prevent damage to the parts.

10.1.1. Recommended Storage Conditions

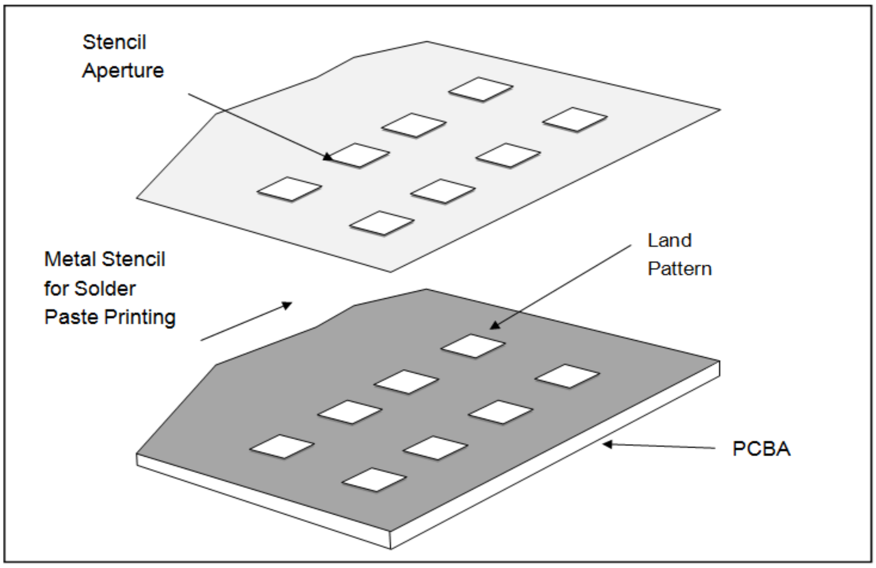
Storage Temperature	10°C to 30°C
Relative Humidity	Below 60% RH

10.1.2. Baking Conditions

Package	Temperature	Time
In Reels	60°C	48 hours
In Bulk	100°C	4 hours

Baking should only be done once.

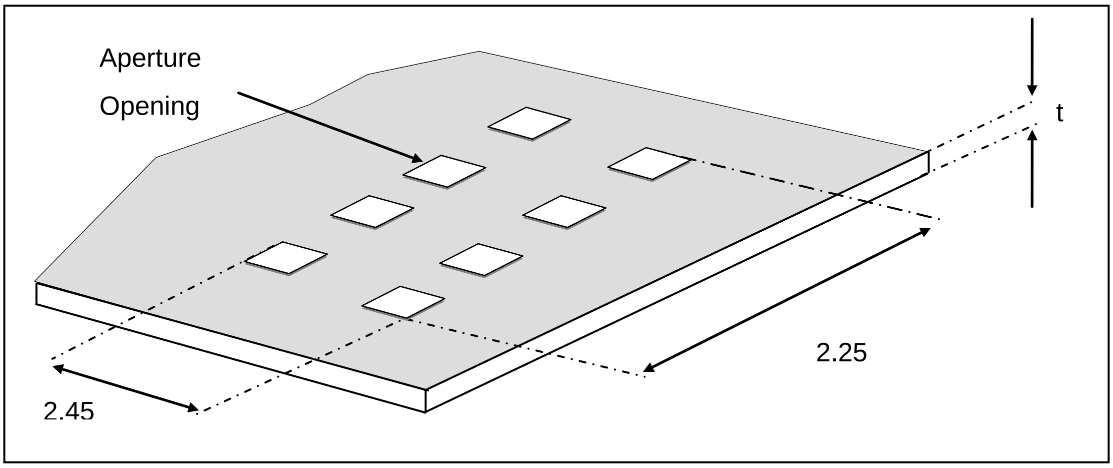
11. Recommended Land Pattern and Metal Stencil Aperture



11.1. Recommended Metal Stencil Aperture

It is recommended that the metal stencil used for solder paste printing has a thickness (t) of 0.11mm (0.004 inches / 4 mils) or 0.127mm (0.005 inches / 5 mils).

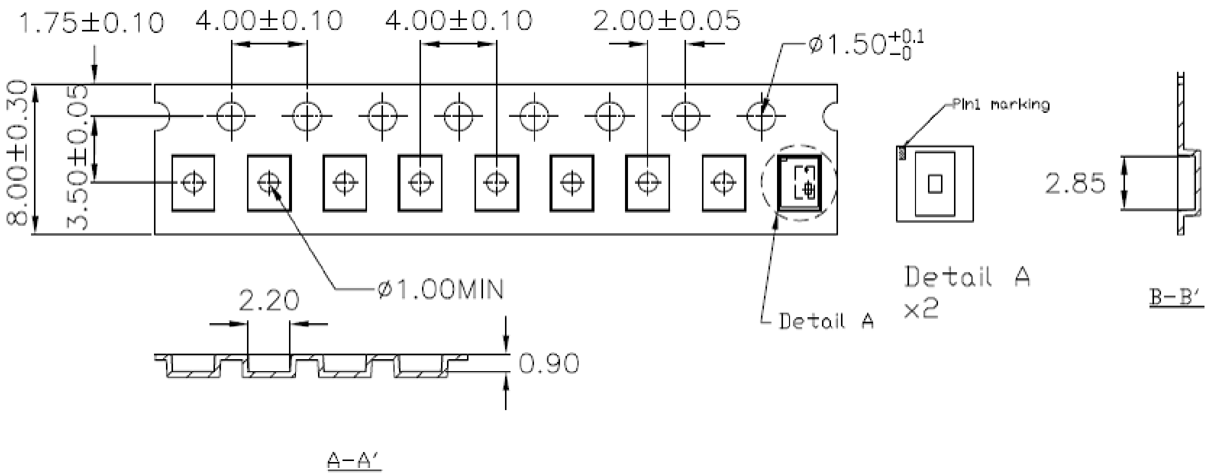
The stencil aperture opening is recommended to be 0.3mm x 0.65mm which has the same dimension as the land pattern. This is to ensure adequate printed solder paste volume and yet no shorting.



Note:

1. All dimensions are in millimeters

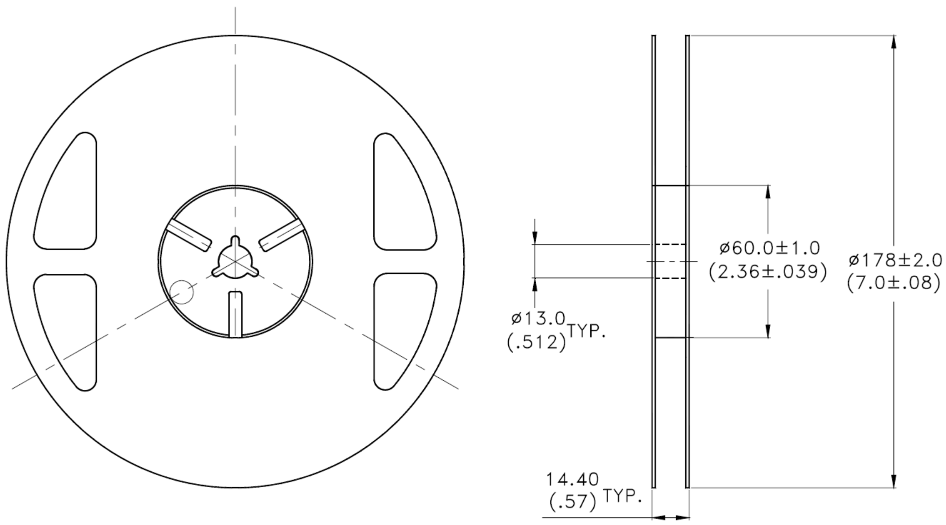
12. Package Dimension for Tape and Reel



Note:

1. All dimensions are in millimeters

12.1. Package Dimension of Reel



Notes:

1. All dimensions are in millimeters (inches)
2. Empty component pockets sealed with top cover tape
3. 7 inch reel - 2500 pieces per reel