

February 1985

OBJECTIVE
SPECIFICATIONS

Quad 2-Line to 1-Line Data Selector/Multiplexers

Features

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs:**
 $I_{OL} = 8 \text{ mA} @ V_{OL} = 0.5\text{V}$
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
74HCTLS: -40°C to $+85^{\circ}\text{C}$
54HCTLS: -55°C to $+125^{\circ}\text{C}$

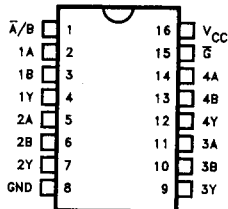
Description

These are data selector/multiplexers which select a 4-bit word from one of two sources via the control of a common select input (\bar{A}/B). A separate strobe input (\bar{G}) is provided. The '157 presents true data whereas the '158 presents inverted data at the outputs.

Fabricated using Zytrex's proprietary ICE-MOS process, these devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Pin Configuration

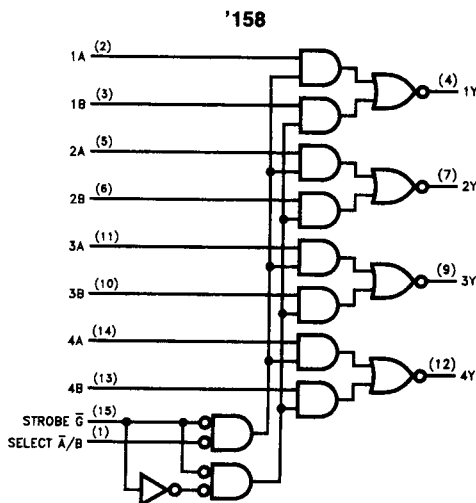


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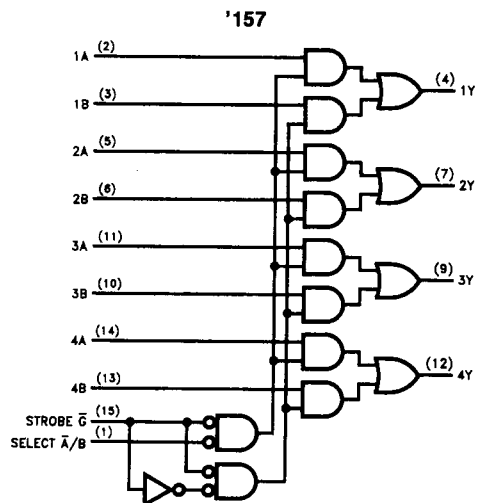
Function Table

Inputs				Output Y	
Strobe \bar{G}	Select \bar{A}/B	Data		'157	'158
		A	B		
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

Logic Diagrams



0086-2



0086-3

Absolute Maximum Ratings*

Supply Voltage Range, V_{CC} -0.5V to 7V
 DC Input Diode Current, I_{IK}
 ($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) ± 20 mA
 DC Output Diode Current, I_{OK}
 ($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) ± 20 mA
 Continuous Output Current Per Pin, I_O
 ($-0.5V < V_O < V_{CC} + 0.5V$) ± 35 mA
 Continuous Current Through
 V_{CC} or GND pins ± 125 mA
 Storage Temperature Range, T_{STG} .. -65°C to +150°C
 Power Dissipation Per Package, P_D † 500 mW

† Power Dissipation temperature derating:
 Plastic Package (N): -12 mW/°C from 65°C to 85°C
 Ceramic Package (J): -12 mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} 4.5V to 5.5V
 DC Input & Output Voltages*, V_{IN} , V_{OUT} 0V to V_{CC}
 Operating Temperature
 Range ZX74HCTL5: -40°C to +85°C
 ZX54HCTL5: -55°C to +125°C
 Input Rise & Fall Times, t_r , t_f Max 500 ns

*Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

*Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC Electrical Characteristics ($V_{CC} = 5V \pm 10\%$ Unless Otherwise Specified)

Symbol	Parameter	Test Conditions	$T_A = 25^\circ C$			Unit	
			Typ	Guaranteed Limits			
V_{IH}	Minimum High-Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low-Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High-Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $I_O = -20 \mu A$ $I_O = -4 mA$	V_{CC} 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
V_{OL}	Maximum Low-Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $I_O = 20 \mu A$ $I_O = 4 mA$ $I_O = 8 mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
I_{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND		± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$		8.0	80.0	160.0	μA

AC Electrical Characteristics (Input $t_r, t_f \leq 6$ ns), HCTL5157, HCTL5158

Symbol	Parameter	Conditions†	$T_A = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		74HCTL5	54HCTL5	Unit
					$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	
			Typ	Guaranteed Limits			
t_{PLH}	Maximum Propagation Delay, A or B to Y	$C_L = 50$ pF	11	14	18	21	ns
t_{PHL}			11	14	18	21	
t_{PLH}	Maximum Propagation Delay, \bar{A}/B to Y		17	23	29	34	ns
t_{PHL}			17	23	29	34	
t_{PLH}	Maximum Propagation Delay, \bar{G} to Y		15	20	25	30	ns
t_{PHL}			15	20	25	30	
C_{IN}	Maximum Input Capacitance		5				pF
C_{PD}	Power Dissipation Capacitance*						pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
 †For AC switching test circuits and timing waveforms see section 2.