Am9360 • Am54/74192
Am9366 • Am54/74193
Decimal and Hexadecimal Up/Down Counters

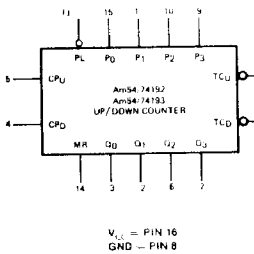
tinctive Characteristics

- eparate up and down clocks
- synchronous parallel load
- 2 MHz typical count rate
- 100% reliability assurance testing in compliance with MIL STD 883

FUNCTIONAL DESCRIPTION

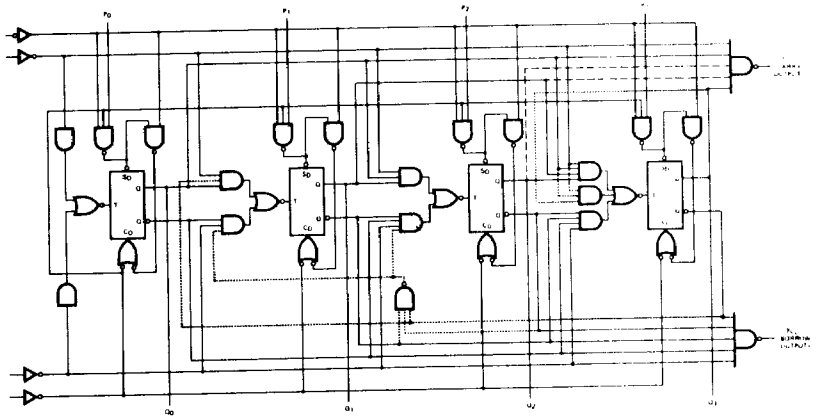
The Am54/74192 (Am9360) and Am54/74193 (Am9366) are 4-bit up-down counters. The 54/74192 counts in BCD code, and the 54/74193 in binary. The counters have separate count-up and count-down clock inputs (CP_U and CP_D). The outputs ($Q_{n...}$) change synchronously following a LOW to HIGH transition on either clock input. Only one clock input can be LOW at a time or erroneous counting will result. Each of the four flip-flops can be preset to HIGH or LOW by means of the four parallel inputs, $P_{n...}$. When the parallel load input ($\overline{PL}$) goes LOW, all four flip-flops set to the state of their P inputs irrespective of the clock inputs. An active HIGH master reset (MR) is provided that overrides both the clock and parallel load inputs, forcing all Q outputs LOW. Two terminal count outputs are gated with the clock inputs to provide clock signals to other counters. The $\overline{TC}_D$ output goes LOW when the counter is in state 0000 and the count-down clock goes LOW. The $\overline{TC}_U$ output goes LOW when the count-up clock goes LOW and the counter is in state 1001 (74192) or state 1111 (74193). The signals can drive directly the count-up and count-down clocks on the next counter in a series.

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

LOGIC DIAGRAM



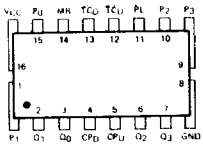
Am54/74192 or Am9360 Decade Counter only .....
Am54/74193 or Am9366 Hexadecimal Counter only — — — — —

Am54/74192, 3 ORDERING INFORMATION

Package Type	Temperature Range	Am54/74192 Order Number	Am54/74193 Order Number	Am9360 Order Number	Am9366 Order Number
Molded DIP	0°C to +75°C	SN74192N	SN74193N	U6M936059X	U6M936659X
Hermetic DIP	0°C to +75°C	SN74192J	SN74193J	U7B936059X	U7B936659X
Hermetic DIP	−55°C to +125°C	SN54192J	SN54193J	U7B936051X	U7B936651X
Hermetic Flat Pak	−55°C to +125°C	SN54192W	SN54193W	U4L936051X	U4L936651X
Dice	Note	SN74192	SN74193	UXX9360XXD	UXX9366XXD

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.
Low-power versions of these circuits are available

CONNECTION DIAGRAM
Top View



NOTE: PIN 1 is marked for orientation.

MAXIMUM RATI (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

SWITCHING CHARACTERISTICS V_{CC} = 5 V, T_A = 25°C,

Parameter	From (Input)	To (Output)	Test Conditions	Min	Typ	Max	Units
t_{pd+}	C_n	C_{n+4}		12	36	54	ns
t_{pd-}				12	23	35	
t_{pd+}	C_n	any $\overline{F}$ (Note 3)	M = 0 V (SUM or DIFF mode)	12	31	47	
t_{pd-}				12	34	36	ns
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{G}$	M = 0 V, S_0 = S_3 = 4.5 V, S_1 = S_2 = 0 V (SUM mode)	12	31	47	
t_{pd-}				12	23	50	ns
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{G}$	M = 0 V, S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V (DIFF mode)	12	35	53	
t_{pd-}				12	26	54	ns
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{P}$	M = 0 V, S_0 = S_3 = 4.5 V, S_1 = S_2 = 0 V (SUM mode)	12	35	53	
t_{pd-}				12	26	39	ns
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{P}$	M = 0 V, S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V (DIFF mode)	12	37	56	
t_{pd-}				12	34	51	ns
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}$ (Note 3)	M = 0 V, S_0 = S_3 = 4.5 V, S_1 = S_2 = 0 V (SUM mode)	12	48	72	
t_{pd-}				12	47	71	ns
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}$ (Note 3)	M = 0 V, S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V (DIFF mode)	12	53	80	
t_{pd-}				12	52	79	ns
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_i$	M = 4.5 V (LOGIC mode)	12	38	57	
t_{pd-}				12	46	69	ns
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	C_{n+4}	M = 0 V, S_0 = S_3 = 4.5 V, S_1 = S_2 = 0 V (SUM mode)	20	40	60	
t_{pd-}				20	44	66	ns
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	C_{n+4}	M = 0 V, S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V (DIFF mode)	20	44	70	
t_{pd-}				20	49	74	ns
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	A = B	M = 0 V, S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V (DIFF mode)	20	53	80	
t_{pd-}				20	50	75	ns

Note 3: F_i output is worst case.

Switching Characteristics (T_A = 25°C)

Parameters	Definition	Test Conditions	Min	Typ	Max	Units
t_{pd+} (Q)	Delay from clock to Q output HIGH	C_L = 15 pF See Fig. 1	12	25	38	ns
t_{pd-} (Q)	Delay from clock to Q output LOW		15	31	47	ns
t_{pd+} ($\overline{TC}$)	Delay from up or down clock to corresponding TC output HIGH	C_L = 15 pF See Fig. 1	8	16	26	ns
t_{pd-} ($\overline{TC}$)	Delay from up or down clock to corresponding TC output LOW		8	16	24	ns
t_{pw} (CP)	Minimum clock LOW or HIGH time (Note 1)				20	ns
t_{pw} ($\overline{PL}$)	Minimum LOW time on $\overline{PL}$ input	See Fig. 2			25	ns
t_s (P)	Set up time, P inputs		0		20	ns
t_{pw} (MR)	Minimum HIGH time on master reset input	See Fig. 3			20	ns
t_{rec} (MR)	Master reset recovery time				20	ns
f_{max}	Maximum count frequency		25	32		MHz
t_{pd-} (MR)	Delay, master reset to outputs LOW	See Fig. 3		25	38	ns
t_{rec} ($\overline{PL}$)	Recovery time, parallel load input	See Fig. 2			20	ns

Notes 1) Either input must be LOW for t_{pw} (CP) and both inputs must be HIGH for t_{pw} (CP) between clocks.

ITION OF TERMS

RIPT TERMS

IONAL TERMS

:ount-up clock input. A LOW-to-HIGH edge on this input the contents of the counter to increment by one.

:ount-down input. A LOW-to-HIGH edge on this input causes itents of the counter to decrement by one.

he outputs of the four internal flip-flops. Q_0 is the least sig- bit of the counter.

ie parallel load control. When this input is LOW, the four flip- re forced into the states defined by the P inputs. The $\overline{PL}$ verrides the clock, and causes a direct set or clear of the os.

he parallel data inputs. When $\overline{PL}$ is LOW, each flip-flop is iately SET if its P input is HIGH and RESET if its P input is

laster Reset. If this input is HIGH, all four flip-flops are forced 0 state irrespective of any other input.

Terminal Count Down. This output is the CP_D input gated by 0's state in the counter. If the Q outputs are all LOW, the llows CP_D.

Terminal Count Up. This output is the CP_U input gated by the um count state of the counter. For the 54/74192, the TC_U follows CP_U input if the Q outputs are H L L H (= 9). For the 193 the $\overline{TC}_U$ output follows the CP_U input if the Q outputs are 3H (= 15).

t The driving capability of the outputs, in terms of TTL unit

Unit Load The loading represented by a TTL gate input, as d in the "electrical characteristics."

OPERATIONAL TERMS

SWITCHING TERMS

t_{pd+} **(Q)** The delay from a LOW-to-HIGH transition on either clock input to a LOW-to-HIGH transition on a Q output.

t_{pd-} **(Q)** The delay from a LOW-to-HIGH transition on either clock input to a HIGH-to-LOW transition on a Q output.

t_{pd+} **($\overline{TC}$)** The delay from a LOW-to-HIGH transition on either clock input to a LOW-to-HIGH transition on the corresponding $\overline{TC}$ output.

t_{pd-} **($\overline{TC}$)** The delay from a HIGH-to-LOW transition on either clock input to a HIGH-to-LOW transition on the corresponding $\overline{TC}$ output.

t_w **(CP)** The minimum time that a clock signal can reside in either logic level for reliable operation.

t_w **($\overline{PL}$)** The shortest LOW time on the $\overline{PL}$ input that will cause all four flip-flops to be set to the proper state.

t_s **(P)** The time before the $\overline{PL}$ input goes HIGH at which the flip-flop samples the P input. Data on the P inputs must not change between t_s (P) max and t_s (P) min.

t_w **(MR)** The shortest HIGH time on the MR input that will reset all four flip-flops.

t_{rec} **(MR)** Master Reset recovery time. The time that must lapse between the end of a reset signal and a clock LOW-to-HIGH transition for the counter to accept the clock.

t_{rec} **($\overline{PL}$)** The parallel load recovery time. The time that must lapse between the end of a parallel load command and a clock LOW-to-HIGH transition for the counter to accept the clock.

t_{pd-} **(MR)** The delay from a LOW-to-HIGH transition on the MR input to a HIGH-to-LOW transition on a Q output.

f_{max} The maximum frequency at which the counter can be operated.

SWITCHING WAVEFORMS

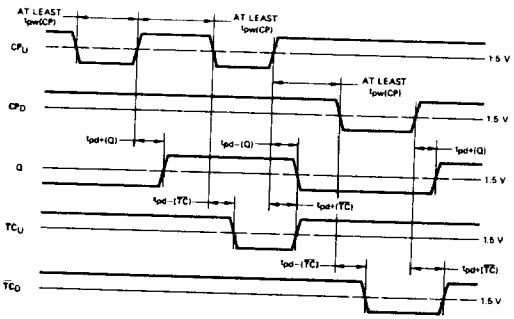


Fig. 1

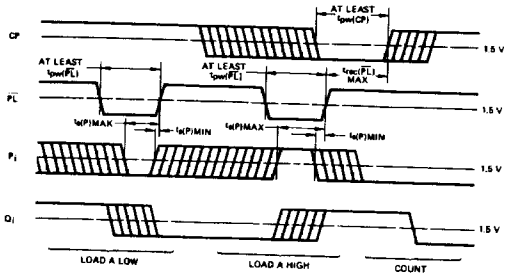


Fig. 2 Input Timing Requirements for Parallel Load

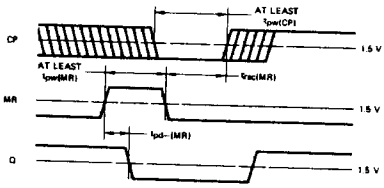


Fig. 3 Master Reset Timing

KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN

MSI INTERFACING RULES

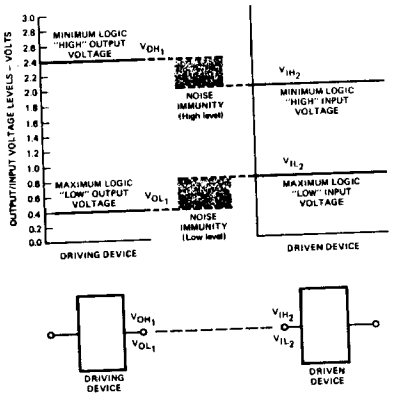
Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
Advanced Micro Devices 54/7400	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

LOADING RULES

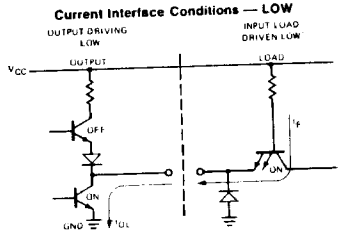
Input/Output	Pin No.'s	Input Unit Load	Fanout Output HIGH	Fanout Output Low
P_1	1	1	—	—
Q_1	2	—	20	10
Q_0	3	—	20	10
CP_D	4	1	—	—
CP_U	5	1	—	—
Q_2	6	—	20	10
Q_3	7	—	20	10
GND	8	—	—	—
P_3	9	1	—	—
P_2	10	1	—	—
$\overline{PL}$	11	1	—	—
$\overline{TC}_U$	12	—	20	10
$\overline{TC}_D$	13	—	20	10
MR	14	1	—	—
P_0	15	1	—	—
V_{CC}	16	—	—	—

INPUT/OUTPUT INTERFACE CONDITIONS

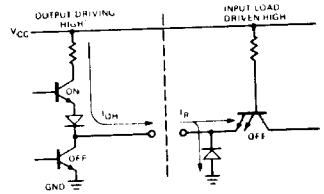
Voltage Interface Conditions — LOW & HIGH



Current Interface Conditions — LOW

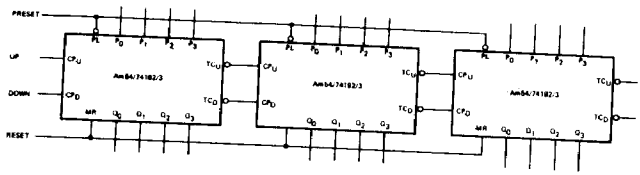


Current Interface Conditions — HIGH

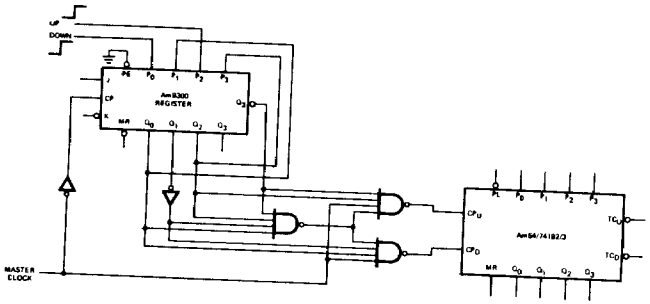


2-189

APPLICATIONS



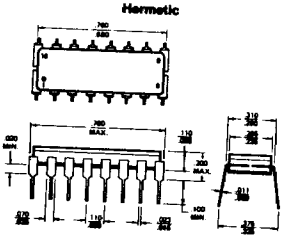
CASCADING UP-DOWN COUNTERS



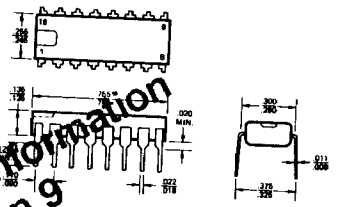
Asynchronous up and down clocks can be synchronized by the circuit shown. The master clock rate must be at least twice the rate of the up and down clocks. The circuit shown detects changes in the up and down inputs and supplies the appropriate clock to the counter. If both signals occur simultaneously, no clocks are produced.

PHYSICAL DIMENSIONS

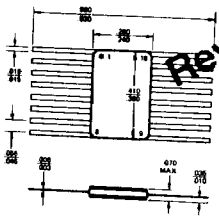
Hermetic
Dual-In-Line



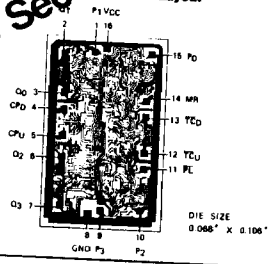
Molded



Flat Package



Metallization and Pad Layout



ADVANCED
MICRO
DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

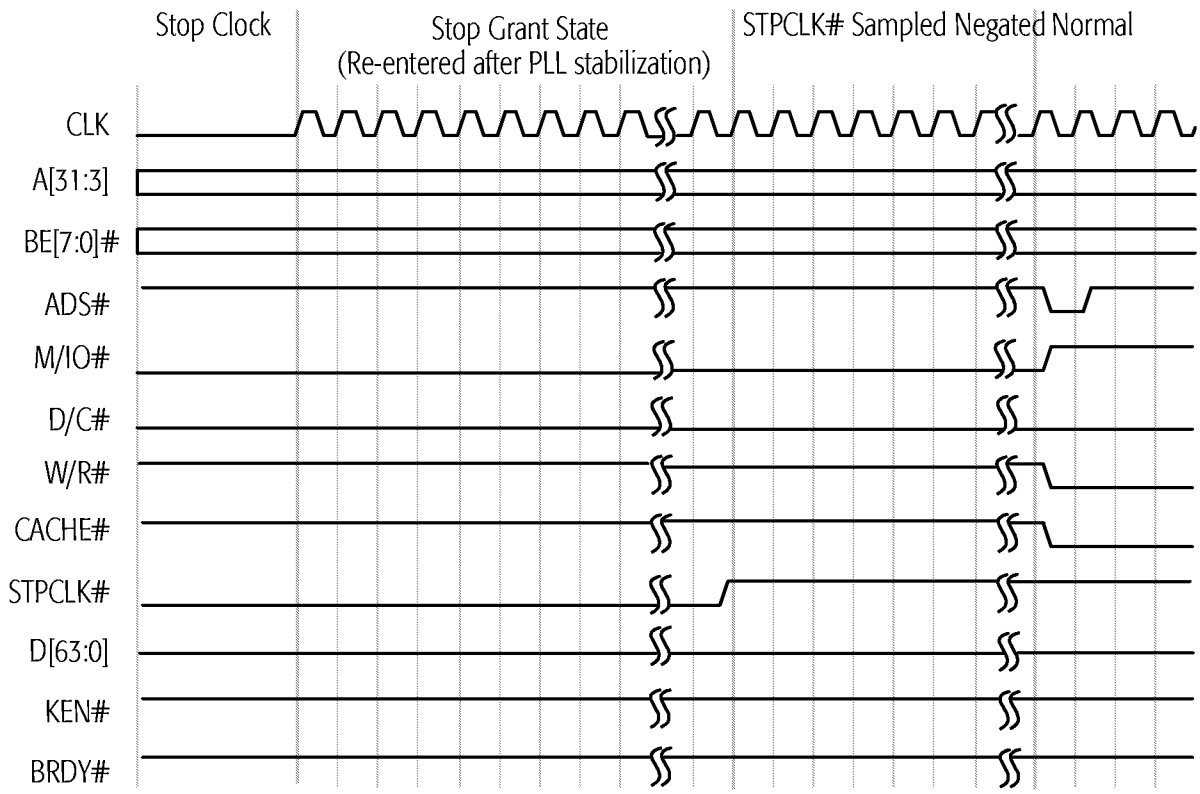


Figure 75. Stop Grant and Stop Clock Modes, Part 2

INIT-Initiated Transition from Protected Mode to Real Mode

INIT is typically asserted in response to a BIOS interrupt that writes to an I/O port. This interrupt is often in response to a Ctrl-Alt-Del keyboard input. The BIOS writes to a port (similar to port 64h in the keyboard controller) that asserts INIT. INIT is also used to support 80286 software that must return to Real mode after accessing extended memory in Protected mode.

The assertion of INIT causes the processor to empty its pipelines, initialize most of its internal state, and branch to address FFFF_FFF0h—the same instruction execution starting point used after RESET. Unlike RESET, the processor preserves the contents of its caches, the floating-point state, the MMX state, Model-Specific Registers (MSRs), the CD and NW bits of the CR0 register, the time stamp counter, and other specific internal resources.

Figure 76 shows an example in which the operating system writes to an I/O port, causing the system logic to assert INIT. The sampling of INIT asserted starts an extended microcode sequence that terminates with a code fetch from FFFF_FFF0h, the reset location. INIT is sampled on every clock edge but is not recognized until the next instruction boundary. During an I/O write cycle, it must be sampled asserted a minimum of three clock edges before BRDY# is sampled asserted if it is to be recognized on the boundary between the I/O write instruction and the following instruction. If INIT is asserted synchronously, it can be asserted for a minimum of one clock. If it is asserted asynchronously, it must have been negated for a minimum of two clocks, followed by an assertion of a minimum of two clocks.

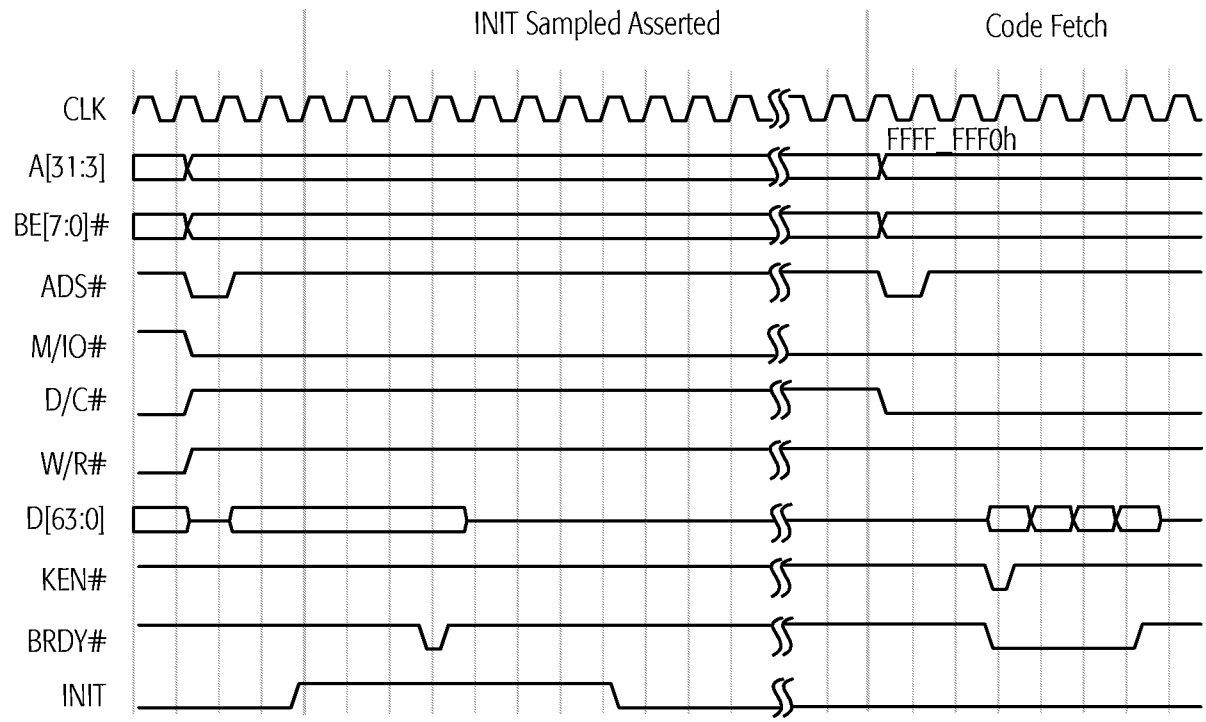


Figure 76. INIT-Initiated Transition from Protected Mode to Real Mode

6 Power-on Configuration and Initialization

On power-on the system logic must reset the AMD-K6-2 processor by asserting the RESET signal. When the processor samples RESET asserted, it immediately flushes and initializes all internal resources and its internal state, including its pipelines and caches, the floating-point state, the MMX and 3DNow! states, and all registers. Then the processor jumps to address FFFF_FFF0h to start instruction execution.

6.1 Signals Sampled During the Falling Transition of RESET

FLUSH# FLUSH# is sampled on the falling transition of RESET to determine if the processor begins normal instruction execution or enters Tri-State Test mode. If FLUSH# is High during the falling transition of RESET, the processor unconditionally runs its Built-In Self Test (BIST), performs the normal reset functions, then jumps to address FFFF_FFF0h to start instruction execution. (See "Built-In Self-Test (BIST)" on page 217 for more details.) If FLUSH# is Low during the falling transition of RESET, the processor enters Tri-State Test mode. (See "Tri-State Test Mode" on page 218 and "FLUSH# (Cache Flush)" on page 103 for more details.)

BF[2:0] The internal operating frequency of the processor is determined by the state of the bus frequency signals BF[2:0] when they are sampled during the falling transition of RESET. The frequency of the CLK input signal is multiplied internally by a ratio defined by BF[2:0]. (See "BF[2:0] (Bus Frequency)" on page 92 for the processor-clock to bus-clock ratios.)

BRDYC# BRDYC# is sampled on the falling transition of RESET to configure the drive strength of A[20:3], ADS#, HITM#, and W/R#. If BRDYC# is Low during the fall of RESET, these outputs are configured using higher drive strengths than the standard strength. If BRDYC# is High during the fall of RESET, the standard strength is selected. (See "BRDYC# (Burst Ready Copy)" on page 95 for more details.)

6.2 RESET Requirements

During the initial power-on reset of the processor, RESET must remain asserted for a minimum of 1.0 ms after CLK and V_{CC} reach specification. (See "CLK Switching Characteristics" on page 255 for clock specifications. See "Electrical Data" on page 247 for V_{CC} specifications.)

During a warm reset while CLK and V_{CC} are within specification, RESET must remain asserted for a minimum of 15 clocks prior to its negation.

6.3 State of Processor After RESET

Output Signals

Table 31 shows the state of all processor outputs and bidirectional signals immediately after RESET is sampled asserted.

Table 31. Output Signal State After RESET

Signal	State	Signal	State
A[31:3], AP	Floating	LOCK#	High
ADS#, ADSC#	High	M/IO#	Low
APCHK#	High	PCD	Low
BE[7:0]#	Floating	PCHK#	High
BREQ	Low	PWT	Low
CACHE#	High	SCYC	Low
D/C#	Low	SMIACT#	High
D[63:0], DP[7:0]	Floating	TDO	Floating
FERR#	High	VCC2DET	Low
HIT#	High	VCC2H/L#	Low
HITM#	High	W/R#	Low
HLDA	Low	–	–

Registers

Table 32 on page 175 shows the state of all architecture registers and Model-Specific Registers (MSRs) after the processor has completed its initialization due to the recognition of the assertion of RESET.