SPC8282F1A

DESCRIPTION

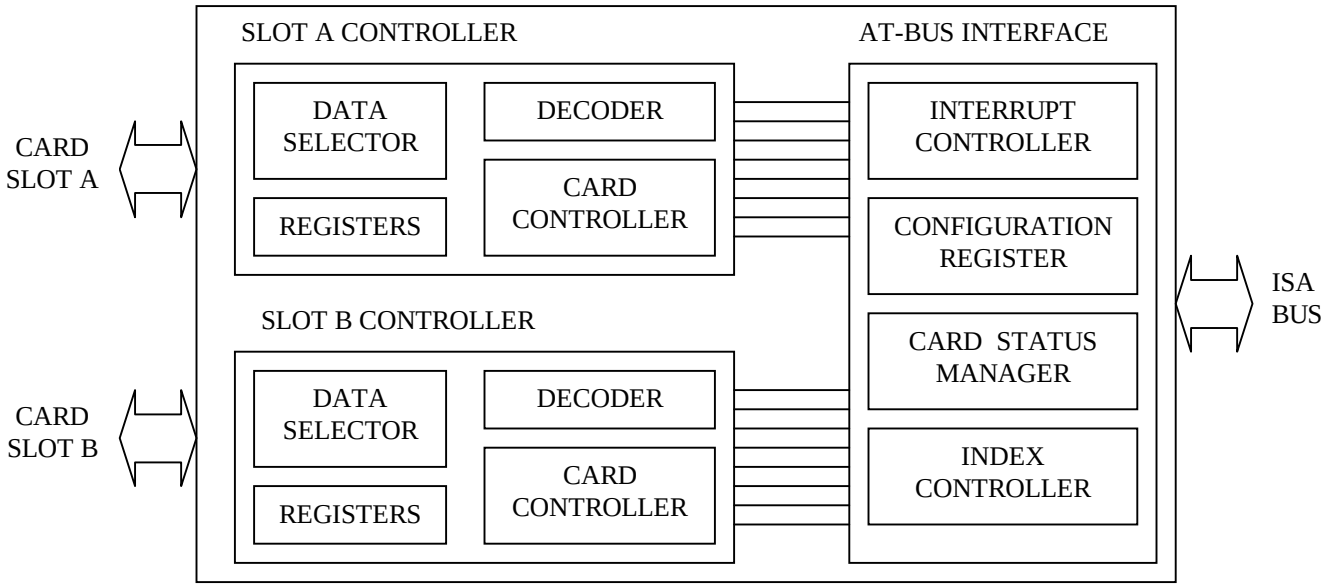
The SPC8282F1A is a PCMCIA to ISA bus host adapter chip capable of controlling two PCMCIA sockets in accordance with PCMCIA-2.1 and JEIDA-4.1 standards. It's internal registers are 82365SL compatible. It supports 8-bit and 16-bit CPU's and PCMCIA devices. It provides programmable memory and I/O windowing as well as support for ATA (IDE) PCMCIA devices. It also incorporates programmable multi-mode power management and supports interrupt steering.

Complete Specification and a reference design (SDU8282#01) are also available.

FEATURES

- All host adapter functions in single chip.
- Direct connection to ISA (PC AT) bus.
- Direct connection to dual PCMCIA sockets.
- Dual socket interface using 208-pin PQFP.
- Five programmable memory windows per socket.
- Two programmable I/O windows per socket.
- 8 or 16 bit CPU interface.
- 8 or 16 bit PCMCIA support.
- Sockets configure-able for ATA disk interface.
- Programmable Interrupt steering.
- 3.3 V or 5.0 V operation.
- Fully compliant with PCMCIA-2.1 and JEIDA-4.1 plus DMA functions.
- Registers compatible with CL-PD7722.

TYPICAL SYSTEM DIAGRAM



SPC8282F1A

PIN CONFIGURATION

Pin #	Signal Name	Power
1	AVPPPGM	S
2	AVPPVCC	S
3	VPPVALID#	S
4	AVCC3#	S
5	AVCC5#	S
6	A5VDET	S
7	B5VDET	S
8	AREG#	A
9	AD3	A
10	ACD1#	A
11	AD4	A
12	AD11	A
13	AD5	A
14	AD12	A
15	AD6	A
16	AD13	A
17	AD7	A
18	AD14	A
19	ACE1#	A
20	AD15	A
21	AA10	A
22	ACE2#	A
23	AOE#	A
24	ASLOTVCC2	A
25	AA11	A
26	AIORD#	A
27	VDD (5V)	A
28	AA9	A
29	AIOWR#	A
30	AA8	A
31	GND	A
32	AA17	A
33	AA13	A
34	AA18	A
35	AA14	A
36	AA19	A
37	AWE#	A
38	AA20	A
39	ARDY_IREQ#	A
40	AA21	A
41	AA16	A
42	AA22	A
43	AA15	A
44	AA23	A
45	AA12	A
46	AA24	A
47	AA7	A
48	AA25	A
49	AA6	A
50	AA5	A
51	ARESET	A
52	ASLOTVCC1	A

Pin #	Signal Name	Power
53	AA4	A
54	AWAIT#	A
55	AA3	A
56	AINPACK#	A
57	AA2	A
58	AA1	A
59	ABVD2_SPKR#	A
60	AA0	A
61	ABVD1_STSCG#	A
62	AD0	A
63	AD8	A
64	AD1	A
65	AD9	A
66	AD2	A
67	AD10	A
68	AWP_IOCS16#	A
69	ACD2#	A
70	GND	A
71	BREG#	B
72	BD3	B
73	BCD1#	B
74	BD4	B
75	BD11	B
76	BD5	B
77	BD12	B
78	BD6	B
79	GND	B
80	BD13	B
81	BD7	B
82	BD14	B
83	BCE1#	B
84	BD15	B
85	BA10	B
86	BCE2#	B
87	BOE#	B
88	BSLOTVCC1	B
89	BA11	B
90	BIORD#	B
91	BA9	B
92	BIOWR#	B
93	BA8	B
94	BA17	B
95	BA13	B
96	BA18	B
97	BA14	B
98	BA19	B
99	BWE#	B
100	BA20	B
101	BRDY/IREQ#	B
102	BA21	B
103	BA16	B
104	BA22	B

Pin #	Signal Name	Power
105	BA15	B
106	BA23	B
107	BA12	B
108	BA24	B
109	BA7	B
110	BA25	B
111	GND	B
112	BA6	B
113	BA5	B
114	BRESET	B
115	BA4	B
116	BWAIT#	B
117	BSLOTVCC2	B
118	BA3	B
119	BINPACK#	B
120	BA2	B
121	BA1	B
122	BBVD2_SPKR#	B
123	BA0	B
124	BBVD1_STCHG#	B
125	BD0	B
126	BD8	B
127	BD1	B
128	BD9	B
129	BD2	B
130	BD10	B
131	BWP_IOCS16#	B
132	BCD2#	B
133	VDD (5V)	I
134	SD15	I
135	SD14	I
136	SD13	I
137	SD12	I
138	ISAVCC	I
139	SD11	I
140	GND	I
141	SD10	I
142	SD9	I
143	SD8	I
144	MEMW#	I
145	MEMR#	I
146	LA17	I
147	LA18	I
148	IRQ14	I
149	LA19	I
150	IRQ15	I
151	LA20	I
152	IRQ12	I
153	LA21	I
154	IRQ11	I
155	LA22	I
156	IRQ10	I

Pin #	Signal Name	Power
157	LA23	V
158	IOCS16#	V
159	SBHE#	V
160	MEMCS16#	V
161	SA0	V
162	SA1	V
163	CLK (8MHz)	V
164	SA2	V
165	SA3	V
166	ALE	V
167	SA4	V
168	SA5	V
169	SA6	V
170	IRQ3	V
171	SA7	V
172	IRQ4	V
173	SA8	V
174	IRQ5	V
175	SA9	V
176	SA10	V
177	IRQ7	V
178	SA11	V
179	SA12	V
180	REFRESH#	V
181	SA13	V
182	SA14	V
183	SA15	V
184	SA16	V
185	IOR#	V
186	IOW#	V
187	AE#	V
188	IOCHRDY	V
189	SD0	V
190	SD1	V
191	0WS#	V
192	GND	V
193	SD2	V
194	SD3	V
195	ISAVCC	V
196	SD4	V
197	SD5	V
198	IRQ9	V
199	SD6	V
200	SD7	V
201	PWRGOOD	V
202	SPKOUT#_CSEL	V
203	INTR#	V
204	BVPPPGM	S
205	BVPPVCC	S
206	BVCC3#	S
207	BVCC5#	S
208	SYSTEM VCC(5V)	S

LEGEND S SYSTEM VCC A A SLOT VCC B B SLOT VCC I

RECOMMENDED OPERATING CONDITIONS

The SPC8282F1A has five power supply systems as follows:

System Control:	SYSTEM VCC (+5VDC recommended)
ISA Bus Interface:	ISAVCC (+5VDC recommended for most case)
SLOT A Interface	A_SLOTVCC
SLOT B Interface:	B_SLOTVCC
Chip Core	VDD (+5VDC only)

SLOT A Interface and SLOT B Interface power supply may operate at LV_{DD} (3.3 V TYP) or HV_{DD} (5.0 V TYP). Recommended operating parameters are shown in the following tables:

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Supply Voltage - high	HV_{DD}	VSS = 0 V	4.5	5.0	5.5	V
Supply Voltage - low	LV_{DD}	VSS = 0 V	3.0	3.3	3.6	V
Input Voltage	V_{IN}	VSS = VSS	VSS		VDD	V
Operating Temperature	T_{OPR}		-40	25	85	° C

7.3 INPUT DC SPECIFICATIONS

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Input High Voltage 1 [a]	V_{IH1}	VDD = HV_{DD} MAX	2.0			V
		VDD = LV_{DD} MAX	1.8			V
Input Low Voltage 1 [a]	V_{IL1}	VDD = HV_{DD} MIN			0.8	
		VDD = LV_{DD} MIN			0.5	V
Input High Voltage 2 [b]	V_{IH2}	VDD = HV_{DD} MAX	3.5			V
		VDD = LV_{DD} MAX	2.2			V
Input Low Voltage 2 [b]	V_{IL2}	VDD = HV_{DD} MIN			1.0	V
		VDD = LV_{DD} MIN			0.8	

[a] Specification applies to all input pins and input sections of all I/O pins except for CD2# and CD1#.

[b] Specification applies to pins CD2# and CD1# only.

7.4 OUTPUT DC SPECIFICATIONS

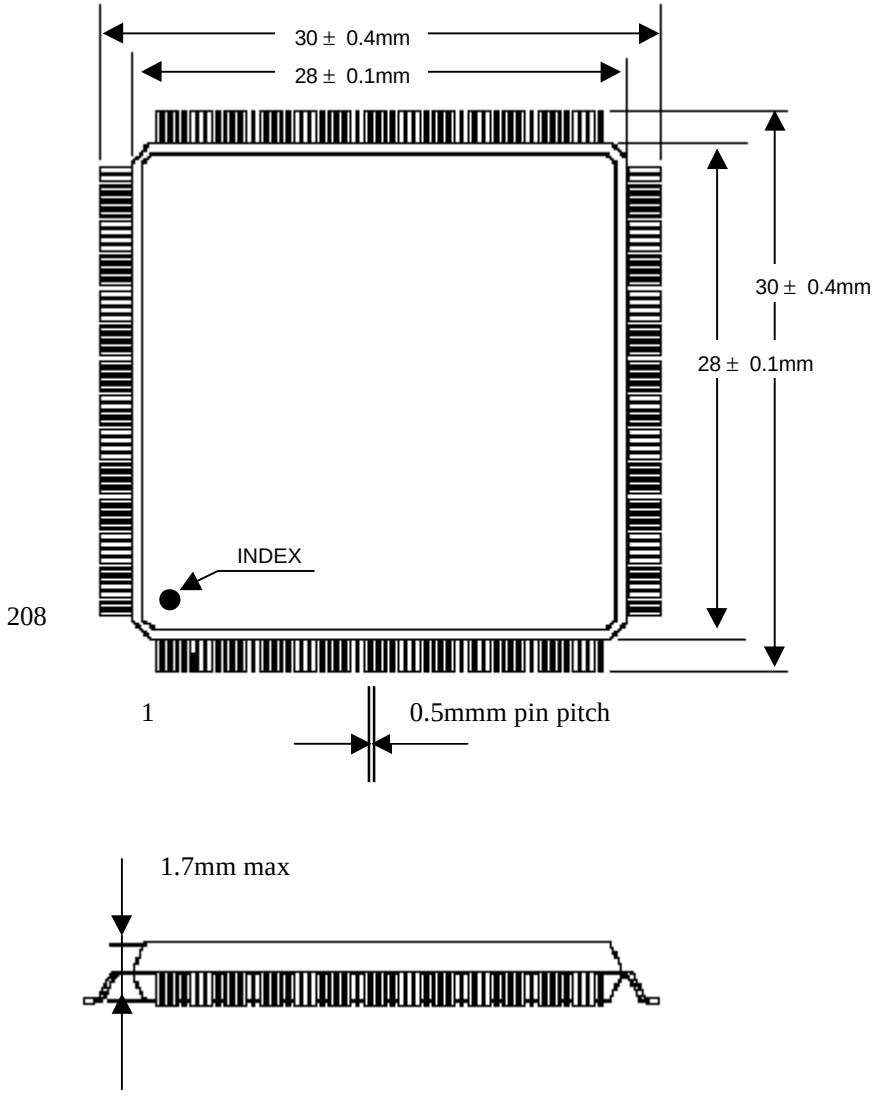
Parameter	Symbol	Conditions	MIN	MAX	Unit
Output High Voltage 1 [a]	V_{OH1}	VDD = HV_{DD} MIN, I_{OH1} = - 4 mA	HV_{DD} - 0.4		V
		VDD = LV_{DD} MIN, I_{OH1} = - 2 mA	LV_{DD} - 0.3		V
Output Low Voltage 1 [a]	V_{OL1}	VDD = HV_{DD} MIN, I_{OL1} = 4 mA		V_{SS} + 0.4	V
		VDD = LV_{DD} MIN, I_{OL1} = 2 mA		V_{SS} + 0.3	V
Output High Voltage 2 [b]	V_{OH2}	VDD = HV_{DD} MIN, I_{OH1} = - 12 mA	HV_{DD} - 0.4		V
		VDD = LV_{DD} MIN, I_{OH1} = - 6 mA	LV_{DD} - 0.3		V
Output Low Voltage 2 [b]	V_{OL2}	VDD = HV_{DD} MIN, I_{OL1} = 12 mA		V_{SS} + 0.4	V
		VDD = LV_{DD} MIN, I_{OL1} = 6 mA		V_{SS} + 0.3	V

[a] Specification applies to all 2/ 4 mA drive output pins and output section of the16 bit card data bus I/O pins, D[15:0]

[b] Specification applies to all 6/12 mA drive output pins and the output section of ISA data bus (SD[15:0]) and SPKROUT# I/O pins.

■ MECHANICAL DATA (Package Dimension)

Plastic LQFP 208pin body size 28 x 28 x 1.4mm (LQFP22)



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