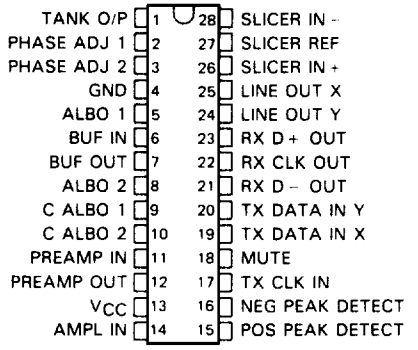
D2861, AUGUST 1985—REVISED DECEMBER 1987

- **Transmits and Receives Serial Bipolar Data at Up to 3 Mbit/s Using Two Twisted-Wire Pairs.**
- **Low-Q Clock Extraction**
- **Two ALBO (Automatic Line Build Out) Taps with a Range of 42 dB**
- **On-Chip Amplifier with 50-dB Open-Loop Voltage Amplification**
- **Phase Adjustment for Recovered Clock**
- **Direct Interface with the TCM2222 AMI/HDB3 (Alternate Mark Inversion/High-Density Bipolar, Third Order) Encoder/Decoder**
- **Receive Line Signal Loss Detection with Mute Output**
- **Bipolar Technology**

TCM2203
J
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The TCM2203 is designed to perform the interface function between the bipolar data encoder/decoder (e.g., TCM2222) and the line. The TCM2203 consists of a receiver that extracts clock information and reshapes the data waveforms, and a transmitter that interfaces bipolar data to the line. Detection of receive signal loss is performed and a mute output is available. Auto-adaptive slicing level ensures excellent jitter and error performance.

The TCM2203 is characterized for operation from 0°C to 70°C.

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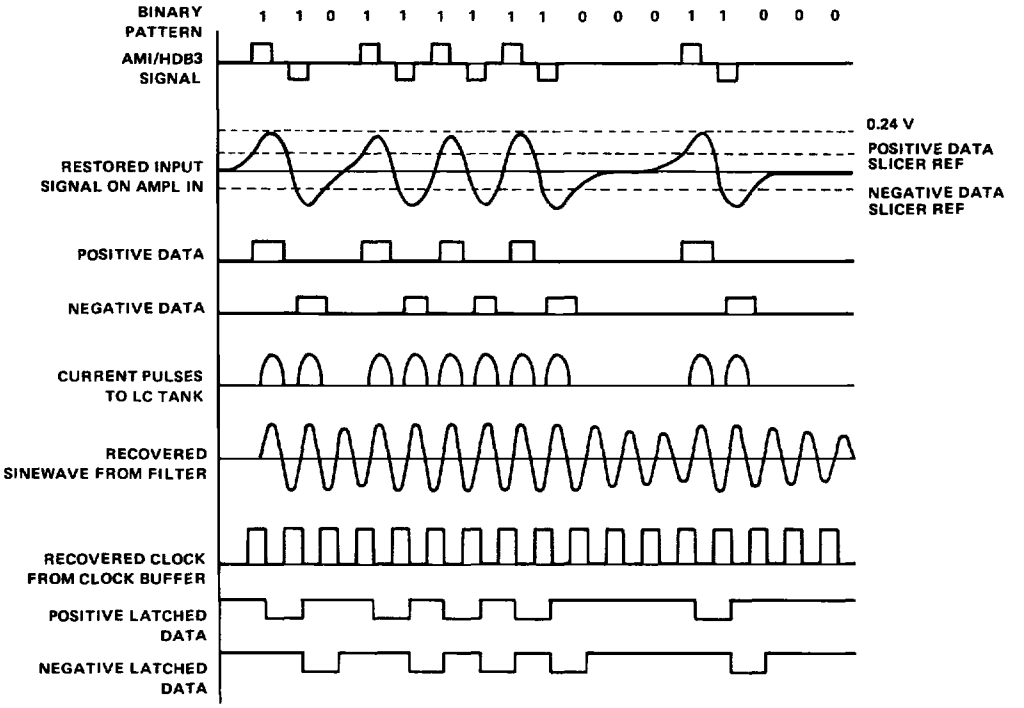
typical timing diagram



NOTE: A low logic level on RX DATA OUT represents a received pulse, or a "mark." RX DATA OUT is latched on the falling edge of RX CK OUT, and tracks the input signal when RX CK OUT is high.

absolute maximum ratings over free-air operating temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 15 V
Continuous total dissipation at 25°C free-air temperature . . . . . 1 W
Operating free-air temperature range . . . . . −10°C to 85°C

NOTE 1: Voltage is with respect to network ground.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5.0	5.5	V
Operating free-air temperature, T_A		0		70	°C
V_{IL}	TX Data in Y			0.80	V
V_{IL}	TX Data in X			0.80	V
V_{IH}	TX CLK in	3.0			V

electrical characteristics over recommended ranges of operating free-air temperature and supply voltage *(unless otherwise noted)*

PARAMETER	SECTION	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	RX D+ out RX D− out RX CLK out	V_{CC} = 5 V, I_{OH} = 40 μA	4.5	4.8		V
I_{IL} I_{IH}	TX Data in Y TX Data in X TX CLK in	V_{IL} = 0 V, V_{IH} = 5 V			±50 ±50	μA
On-state impedance	ALBO			25	50	Ω
Off-state impedance		V_{P-P} = 480 mV	9	11		kΩ
Dynamic resistance matching error				2%		
Transconductance‡ (referenced to pin 14)			0.11	0.15		s
Input impedance	Buffer	f_Q = 1 MHz	10	20		kΩ
Output impedance				40		Ω
Voltage amplification			4.5	5.3	6.0	dB
Input impedance	*Pre-Amp*	*f* = 1 MHz	*40*	*60*		kΩ
Output impedance	Preamplifier	f_Q = 1 MHz		50		Ω
Open-loop voltage amplification		V_{CC} = 5 V, V_F = 1 MHz	42	46		dB
Unity-gain frequency				40		MHz
Input impedance	Phase slicer amplifier	f_Q = 1 MHz	7	11		kΩ
Voltage amplification (each output)			4.5	5.3	6.0	dB
Capacitance-driving capability, peak detect pins					0.1	μF
Input impedance	Clock Slicer	f_Q = 2 MHz	100	150		kΩ
Voltage amplification		f_Q = 2 MHz		60		dB
Input-to-output delay		f_Q = 2 MHz, PHASE ADJ CAP = 75 pF		60		ns
Peak-to-peak eye amplitude	Data Slicer	V_{CC} = 5 V		480		mV
Data slicing level				50%		
Clock slicing level§				66%		
Negative-going threshold voltage	Mute	V_{CC} = 5 V		3.3		V
Positive-going threshold voltage				3.5		
Leakage	RX D+ OUT,	V_{OH} = 5 V			50	μA
Low-level output voltage, V_{OL}	RX D− OUT	I_{OL} = 2 mA		0.85	1	V
Leakage	LINE OUT X,	V_{OH} = 5 V			50	μA
Low-level output voltage, V_{OL}	LINE OUT Y	I_{OL} = 20 mA		0.9	1.1	V
Leakage	Mute	V_{OH} = 5 V			50	μA
Low-level output voltage, V_{OL}	Mute	I_{OL} = 1 mA		250	400	mV
Output rise time, t_r	LINE OUT X,	R_L = 220 Ω		50	100	ns
Output fall time, t_f	LINE OUT Y	R_L = 220 Ω		50	100	ns
Supply current, I_{CC}		V_{CC} = 5 V		25	40	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Transconductance is defined as the change in current for each diode string divided by the change in peak-to-peak voltage at pin 14.
§ Clock slicing level is the data level at which the TANK O/P puts out a current pulse.

TYPICAL CHARACTERISTICS

EYE DIAGRAM REGULATION
(AT INPUT OF 6- dB AMPLIFIER)

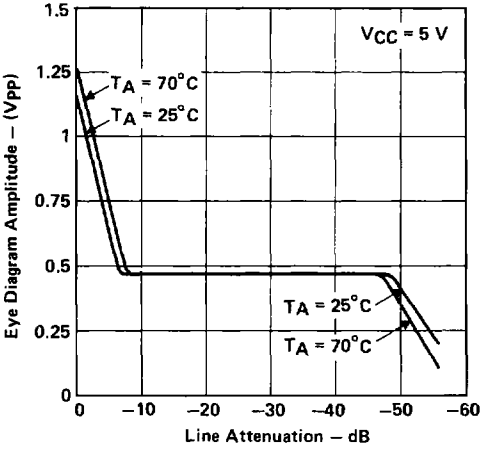


FIGURE 1

TYPICAL PREAMPLIFIER VOLTAGE
AMPLIFICATION CHARACTERISTICS

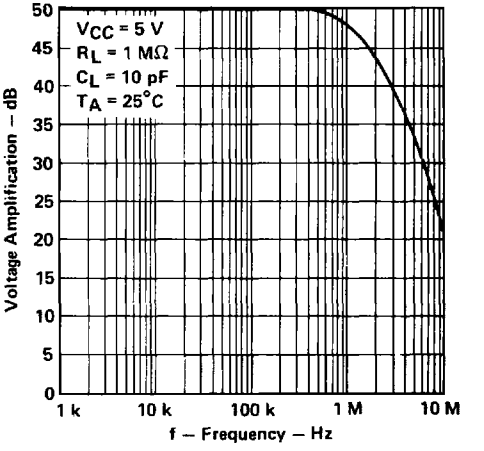


FIGURE 2

TYPICAL PREAMPLIFIER PHASE CHARACTERISTICS

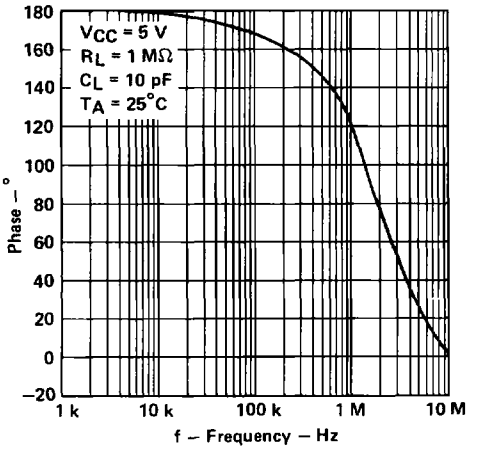


FIGURE 3

PREAMPLIFIER OPEN-LOOP VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

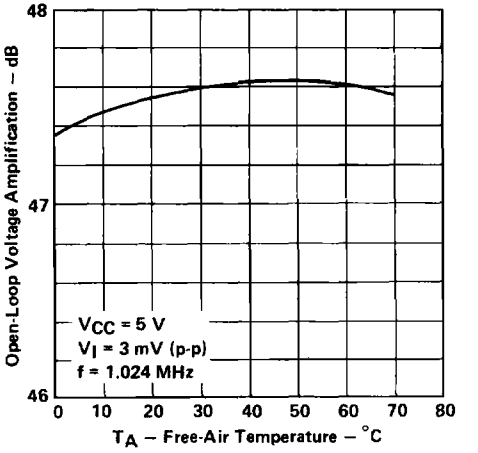


FIGURE 4

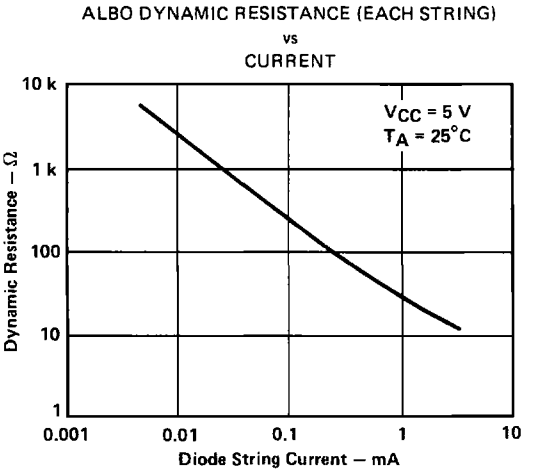


FIGURE 5

PRINCIPLES OF OPERATION

general

The TCM2203 is designed to form the interface between a bipolar decoder/encoder and the transmission line. It is optimized for 1.536 MHz, 1.544 MHz, and 2.048 MHz operation, but is capable of operating at 3.152 MHz and low frequency for special applications. The TCM2203 can be considered in two separate parts, a transmitting section and a receiving section.

receiving section

This section performs three functions: signal restoration, clock recovery, and data slicing. It also detects loss of incoming signal and flags this condition by taking the mute output high.

signal restoration

The incoming signal is typically very distorted and exhibits considerable intersymbol interference. The input section must restore the signal to provide a clear eye diagram to the data and clock slicer. An amplifier with open-loop voltage amplification of 50 dB with externally adjusted gain, together with the bode networks and associated ALBO taps, give a dynamic range of up to 36 dB (6 dB to 42 dB). This allows positioning of the terminal at any line length (within the limits of ALBO dynamic range) from repeater or like transmitter.

Equalization of the line characteristics is performed by a simple external series LC network buffered by the 6-dB amplifier. The restored signal from the 6-dB phase splitter (controlled to 0.48 V peak-to-peak) is sent to two peak detectors that store the peak values on external capacitors. The average peak values are then summed to provide a signal level, which is compared to a V_{CC}-derived reference to form an error signal level. This error signal level controls the current in the ALBO strings. As ALBO string current increases, the dynamic resistance of the string decreases and more signal is shunted to ground. In this way, automatic gain control and automatic line build out are acheived. Typically, there is frequency response contouring associated with the automatic gain control to compensate for the responses of different lengths of line.

clock extraction

The received signal contains its own clock information, which must be extracted in the receive section. An averaged peak input signal is derived from the sum of the positive and negative peak detectors. The negative peak detector is actually the positive peak of AMPL IN inverted. Alternately, the peak average sum is equal to the sum of the averaged absolute values of the negative and positive peaks. When the negative or positive pulse at AMPL IN exceeds 66% of the averaged peak value, a current pulse occurs at the TANK O/P output. These current pulses are filtered by a tuned-primary transformer-coupled circuit to extract the clock and drive the slicer inputs. The slicer converts the sinewave into a binary square-wave clock signal. The transformer-coupled tuned-primary circuit sets the clock extraction Q. The slicer is a high-gain 60-dB comparator that minimizes conversion of amplitude modulation in the sine wave to phase modulation in the recovered square wave clock.

data slicing

The data comparators trigger whenever the signal goes above 50% of the average peak values from the peak detectors. This data is then presented to the data latches and latched into the output buffers by the falling edge of the recovered clock. When the RX CLK OUT is high, RX D− OUT and RX D+ OUT track the comparators. The clock buffer trigger circuit can be externally phase adjusted with a 5-pF to 75-pF trim capacitor across PHASE ADJ 1 and PHASE ADJ 2 to set the falling edge exactly to the center of the data pulses. This maximizes jitter acceptance and noise immunity.

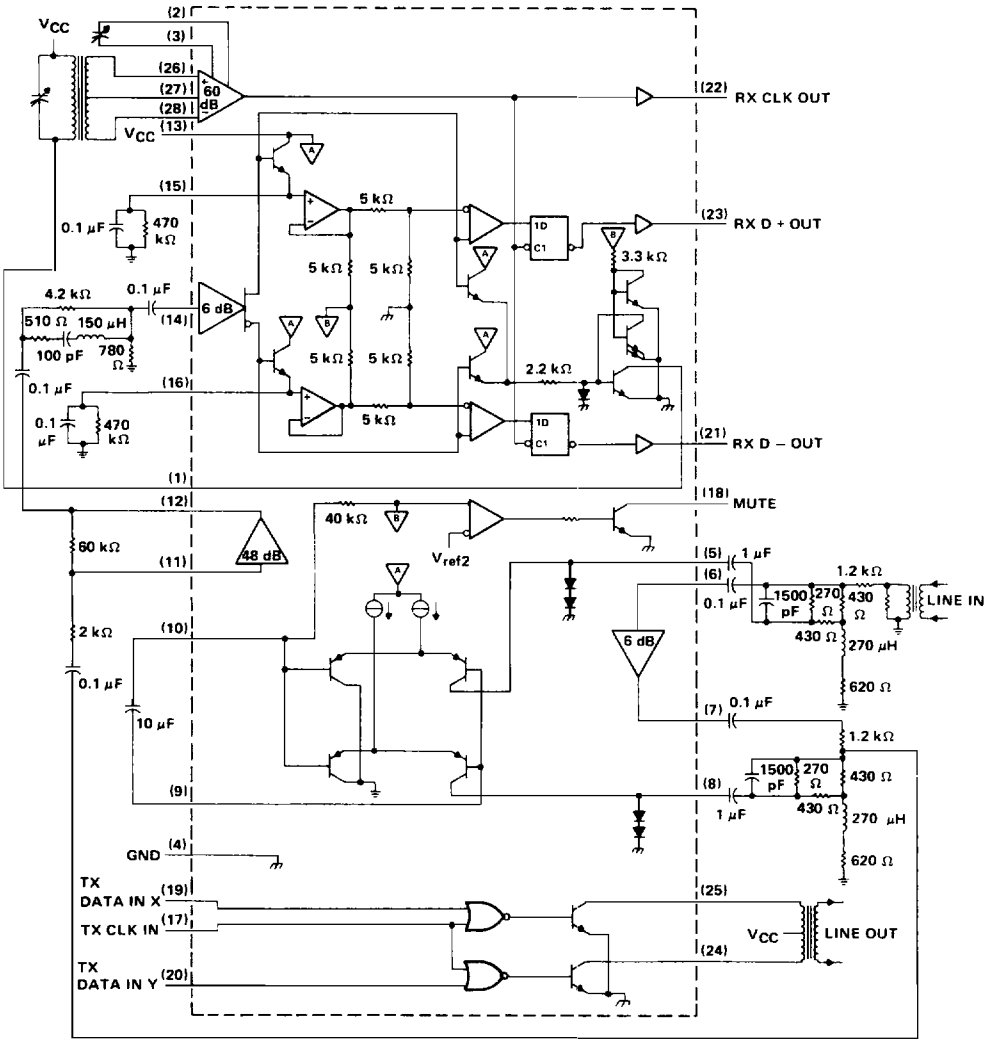
receive signal loss detection

The average peak data values are half-summed to give a dc value that is compared to an internal reference relative to V_{CC}. When the value falls below 33% of the nominal value after ALBO gain control, the MUTE output goes high.

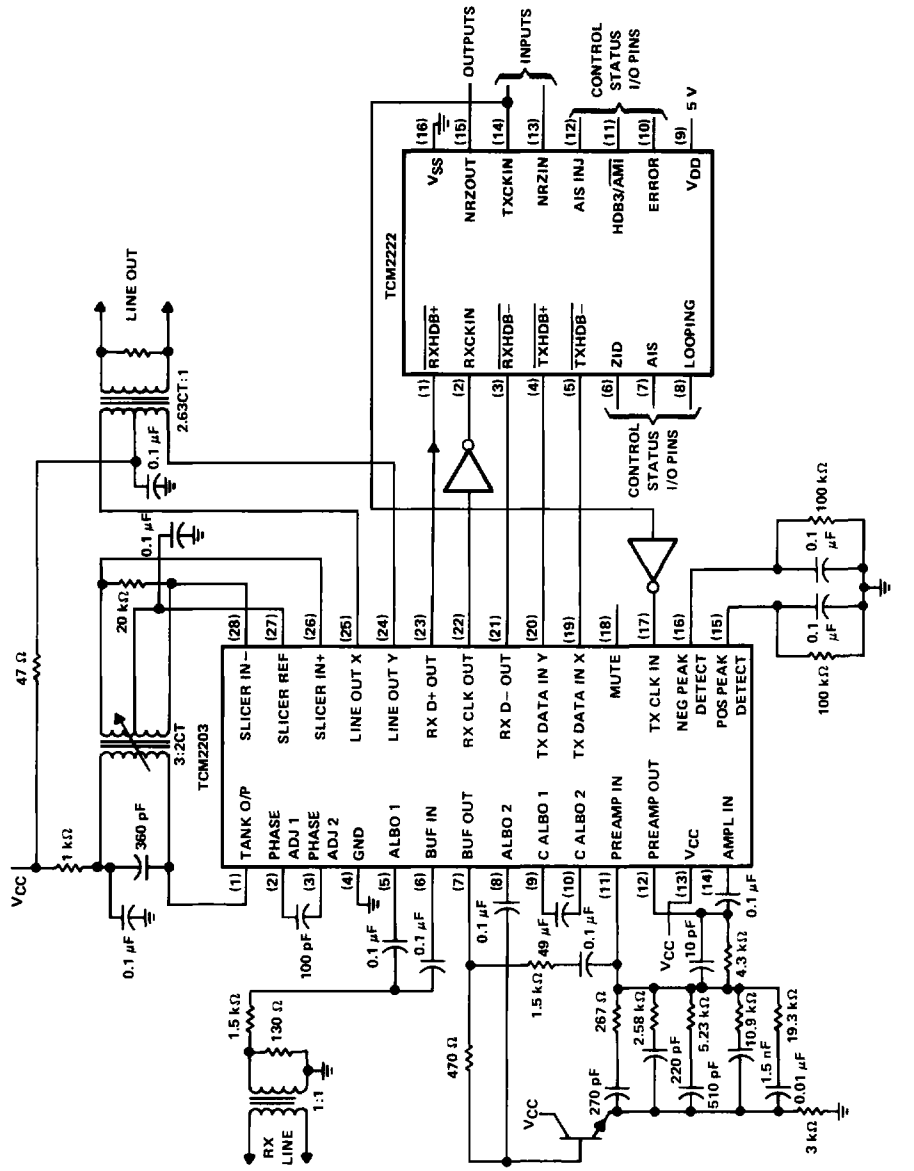
transmitting section

The transmitting section gates the signals applied to TX DATA IN X and TX DATA IN Y with the signal applied to TX CLK IN. The gated signals are then applied to the line outputs. The line output pulse duration is one-half of the bit period. The LINE OUT X and LINE OUT Y outputs are open-collector n-p-n transistors. Each collector will sink 20 milliamperes when the appropriate TX DATA IN input and TX CLK IN are at low levels.

TYPICAL APPLICATION DATA



TYPICAL APPLICATION DATA



NOTE: Filter resistors are 1%.
Filter capacitors are 5%.