



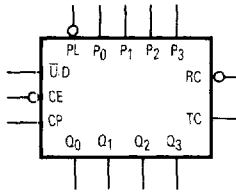
Product Preview

Up/Down Counters with Preset and Ripple Clock

The MC74AC190 is a reversible BCD (8421) decade counter. The MC74AC191 is a reversible modulo 16 binary counter. Both feature synchronous counting and asynchronous presetting. The preset feature allows the MC74AC190 and MC74AC191 to be used in programmable dividers. The Count Enable input, the Terminal Count output and the Ripple Clock output make possible a variety of methods of implementing multistage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

- High-Speed — 120 MHz Typical Count Frequency
- Synchronous Counting
- Asynchronous Parallel Load
- Cascadable
- Outputs Source/Sink 24 mA

LOGIC SYMBOL



PIN NAMES

- CE Count Enable Input
- CP Clock Pulse Input
- P₀-P₃ Parallel Data Inputs
- PL Asynchronous Parallel Load Input
- U/D Up/Down Count Control Input
- Q₀-Q₃ Flip-Flop Outputs
- RC Ripple Clock Output
- TC Terminal Count Output

**MC74AC190
MC74AC191**

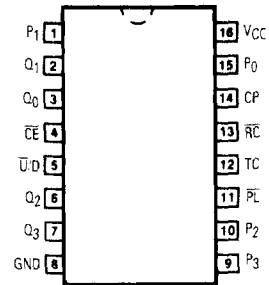
**UP/DOWN COUNTERS
WITH PRESET
AND RIPPLE CLOCK**



**N SUFFIX
CASE 648-08
PLASTIC**



**D SUFFIX
CASE 751B-03
PLASTIC**



MC74AC190 • MC74AC191

FUNCTIONAL DESCRIPTION

The MC74AC190/74C191 are synchronous up/down counters. The MC74AC190 is a BCD decade counter while the MC74AC191 is organized as a 4-bit binary counter. Both contain four edge-triggered flip-flops with internal gating and steering logic to provide individual preset, count-up and count-down operations.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset to any desired number. When the Parallel Load (\overline{PL}) input is LOW, information present on the Parallel Load inputs (P_0 - P_3) is loaded into the counter and appears on the Q outputs. This operation overrides the counting functions, as indicated in the Mode Select Table.

A HIGH signal on the \overline{CE} input inhibits counting. When \overline{CE} is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The direction of counting is determined by the $\overline{U/D}$ input signal, as indicated in the Mode Select Table. \overline{CE} and $\overline{U/D}$ can be changed with the clock in either state, provided only that the recommended setup and hold times are observed.

Two types of outputs are provided as overflow/underflow indicators. The terminal count (TC) output is normally LOW. It goes HIGH when the circuits reach zero in the count down mode or 9 (MC74AC190) or 15 (MC74AC191) in the count up mode. The TC output will then remain HIGH until a state change occurs, whether by counting or presetting or until $\overline{U/D}$ is changed. The TC output should not be used as a clock signal because it is subject to decoding spikes.

The TC signal is also used internally to enable the Ripple Clock (\overline{RC}) output. The \overline{RC} output is normally HIGH. When \overline{CE} is LOW and TC is HIGH, \overline{RC} output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again. This feature simplifies the design of multistage counters, as indicated in Figures a and b. In Figure a, each \overline{RC} output is used as the clock input for the next higher stage. This configuration is particularly advantageous, since it drives only the first stage. To prevent counting in all stages it is only necessary to inhibit the first stage, since a HIGH signal on \overline{CE} inhibits the \overline{RC} output pulse, as indicated in the \overline{RC} Truth Table. A disadvantage of this configuration, in some applications, is the timing skew between state changes in the first and last stages. This represents the cumulative delay of the clock as it ripples through the preceding stages.

A method of causing state changes to occur simultaneously in all stages is shown in Figure c. All clock inputs are driven in parallel and the \overline{RC} outputs propagate the carry/borrow signals in ripple fashion. In this configuration the LOW state duration of the clock must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. There is no such restriction on the HIGH state duration of the clock, since the \overline{RC} output of any device goes HIGH shortly after its CP input goes HIGH.

The configuration shown in Figure c avoids ripple delays and their associated restrictions. The \overline{CE} input for a given stage is formed by combining the TC signals from all the preceding stages. Note that in order to inhibit counting an enable signal must be included in each carry gate. The simple inhibit scheme of Figures a and b doesn't apply, because the TC output of a given stage is not affected by its own \overline{CE} .

MODE SELECT TABLE

Inputs				Mode
\overline{PL}	\overline{CE}	$\overline{U/D}$	CP	
H	L	L	\uparrow	Count Up
H	L	H	\uparrow	Count Down
L	X	X	X	Preset (Asyn.)
H	H	X	X	No Change (Hold)

\overline{RC} TRUTH TABLE

Inputs			Outputs
\overline{CE}	TC*	CP	\overline{RC}
L	H	\uparrow	\uparrow
H	X	X	H
X	L	X	H

*TC is generated internally
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
 \uparrow = LOW-to-HIGH Transition

STATE DIAGRAM

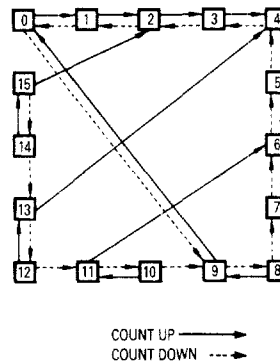


Figure a: N-Stage Counter Using Ripple Clock

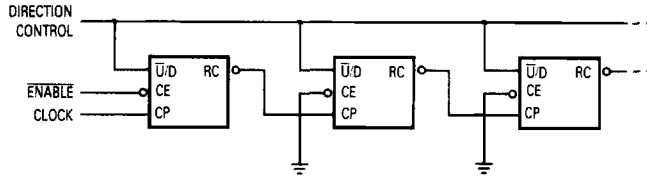


Figure b: Synchronous N-Stage Counter Using Ripple Carry/Borrow

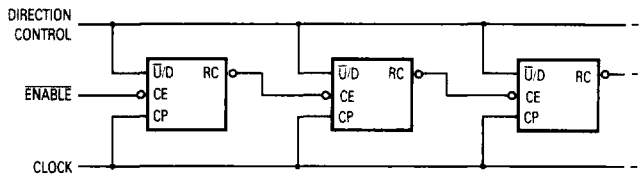
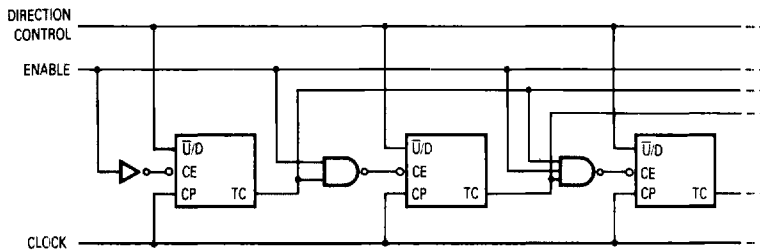


Figure c: Synchronous N-Stage Counter With Parallel Gated Carry/Borrow



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AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC190			74AC190		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Count Frequency	3.3 5.0		88 120				MHz	3-3
t _{PLH}	Propagation Delay CP to Q _n	3.3 5.0		9.5 7.0				ns	3-6
t _{PHL}	Propagation Delay CP to Q _n	3.3 5.0		10.5 7.5				ns	3-6
t _{PLH}	Propagation Delay CP to TC	3.3 5.0		15 11				ns	3-6
t _{PHL}	Propagation Delay CP to TC	3.3 5.0		13 9.5				ns	3-6
t _{PLH}	Propagation Delay CP to RC	3.3 5.0		9.0 6.5				ns	3-6
t _{PHL}	Propagation Delay CP to RC	3.3 5.0		9.5 7.0				ns	3-6
t _{PLH}	Propagation Delay CE to RC	3.3 5.0		9.5 7.0				ns	3-6
t _{PHL}	Propagation Delay CE to RC	3.3 5.0		8.5 6.0				ns	3-6
t _{PLH}	Propagation Delay Ü·D to RC	3.3 5.0		11 8.0				ns	3-6
t _{PHL}	Propagation Delay Ü·D to RC	3.3 5.0		10.5 7.5				ns	3-6
t _{PLH}	Propagation Delay Ü·D to TC	3.3 5.0		9.5 7.0				ns	3-6
t _{PHL}	Propagation Delay Ü·D to TC	3.3 5.0		9.5 7.0				ns	3-6
t _{PLH}	Propagation Delay P _n to Q _n	3.3 5.5		10.5 7.5				ns	3-6
t _{PHL}	Propagation Delay P _n to Q _n	3.3 5.0		9.5 7.0				ns	3-6
t _{PLH}	Propagation Delay PL to Q _n	3.3 5.0		11.5 8.5				ns	3-6
t _{PHL}	Propagation Delay PL to Q _n	3.3 5.0		11.5 8.5				ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74AC190		74AC190		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW P _n to \overline{PL}	3.3 5.0	4.5 3.0			ns	3-9	
t _h	Hold Time, HIGH or LOW P _n to \overline{PL}	3.3 5.0	-0.5 -0.5			ns	3-9	
t _s	Setup Time, LOW CE to CP	3.3 5.0	7.0 5.0			ns	3-9	
t _h	Hold Time, LOW CE to CP	3.3 5.0	-1.5 -1.0			ns	3-9	
t _s	Setup Time, HIGH or LOW $\overline{U/D}$ to CP	3.3 5.0	7.0 5.0			ns	3-9	
t _h	Hold Time, HIGH or LOW $\overline{U/D}$ to CP	3.3 5.0	-1.5 -1.0			ns	3-9	
t _w	\overline{PL} Pulse Width, LOW	3.3 5.0	5.5 6.0			ns	3-6	
t _w	CP Pulse Width, LOW	3.3 5.0	5.5 6.0			ns	3-6	
t _{rec}	Recovery Time \overline{PL} to CP	3.3 5.0	4.5 3.0			ns	3-9	

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74AC191			74AC191		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Count Frequency	3.3 5.0	70 90	105 133		65 85		MHz	3-3
t _{PLH}	Propagation Delay CP to Q _n	3.3 5.0	3.0 2.0	8.5 6.0	15 11	1.0 1.0	16 12	ns	3-6
t _{PHL}	Propagation Delay CP to Q _n	3.3 5.0	3.0 2.0	8.5 6.0	14.5 10.5	1.0 1.0	16 11.5	ns	3-6
t _{PLH}	Propagation Delay CP to TC	3.3 5.0	4.0 3.0	10.5 7.5	18 12	1.0 1.0	20 14	ns	3-6
t _{PHL}	Propagation Delay CP to TC	3.3 5.0	4.5 3.0	10.5 7.5	17.5 12.5	1.0 1.0	19 13.5	ns	3-6
t _{PLH}	Propagation Delay CP to RC	3.3 5.0	3.0 2.5	7.5 5.5	12 9.5	1.0 1.0	13.5 10.5	ns	3-6
t _{PHL}	Propagation Delay CP to RC	3.3 5.0	2.5 2.0	7.0 5.0	11.5 8.5	1.0 1.0	12.5 9.5	ns	3-6
t _{PLH}	Propagation Delay CE to RC	3.3 5.0	2.5 1.5	7.0 5.0	12 8.5	1.0 1.0	13.5 9.5	ns	3-6
t _{PHL}	Propagation Delay CE to RC	3.3 5.0	2.5 1.5	6.5 5.0	11 8.0	1.0 1.0	12.5 9.0	ns	3-6
t _{PLH}	Propagation Delay UD to RC	3.3 5.0	2.5 1.5	6.5 5.0	12.5 9.0	1.0 1.0	14.5 10	ns	3-6
t _{PHL}	Propagation Delay UD to RC	3.3 5.0	2.5 1.5	7.0 5.0	12 8.5	1.0 1.0	13.5 10	ns	3-6
t _{PLH}	Propagation Delay UD to TC	3.3 5.0	2.5 2.0	7.0 5.0	11.5 8.5	1.0 1.0	13.5 9.5	ns	3-6
t _{PHL}	Propagation Delay UD to TC	3.3 5.0	2.5 1.5	6.5 5.0	11 8.5	1.0 1.0	12.5 9.5	ns	3-6
t _{PLH}	Propagation Delay P _n to Q _n	3.3 5.0	3.0 2.0	8.0 5.5	13.5 9.5	1.0 1.0	15.5 10.5	ns	3-6
t _{PHL}	Propagation Delay P _n to Q _n	3.3 5.0	3.0 2.0	7.5 5.5	13 9.5	1.0 1.0	14.5 10.5	ns	3-6
t _{PLH}	Propagation Delay PL to Q _n	3.3 5.0	3.5 2.0	9.5 5.5	14.5 9.5	1.0 1.0	17.5 10.5	ns	3-6
t _{PHL}	Propagation Delay PL to Q _n	3.3 5.0	3.0 2.0	8.0 6.0	13.5 10	1.0 1.0	15.5 11	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
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AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74AC191		74AC191		Units	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW P _n to \overline{PL}	3.3 5.0	1.0 0.5	3.0 2.0	3.0 2.5	ns	3-9	
t _h	Hold Time, HIGH or LOW P _n to \overline{PL}	3.3 5.0	-1.5 -0.5	0.5 1.0	1.0 1.0	ns	3-9	
t _s	Setup Time, LOW \overline{CE} to CP	3.3 5.0	3.0 1.5	6.0 4.0	7.0 4.5	ns	3-9	
t _h	Hold Time, LOW \overline{CE} to CP	3.3 5.0	-4.0 -2.5	-0.5 0	-0.5 0	ns	3-9	
t _s	Setup Time, HIGH or LOW $\overline{U/D}$ to CP	3.3 5.0	4.0 2.5	8.0 5.5	9.0 6.5	ns	3-9	
t _h	Hold Time, HIGH or LOW $\overline{U/D}$ to CP	3.3 5.0	-5.0 -3.0	0 0.5	0 0.5	ns	3-9	
t _w	\overline{PL} Pulse Width, LOW	3.3 5.0	2.0 1.0	3.5 1.0	4.0 1.0	ns	3-6	
t _w	CP Pulse Width, LOW	3.3 5.0	2.0 2.0	3.5 3.0	4.0 4.0	ns	3-6	
t _{rec}	Recovery Time \overline{PL} to CP	3.3 5.0	-0.5 -1.0	0 0	0 0	ns	3-9	

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	75	pF	V _{CC} = 5.0 V