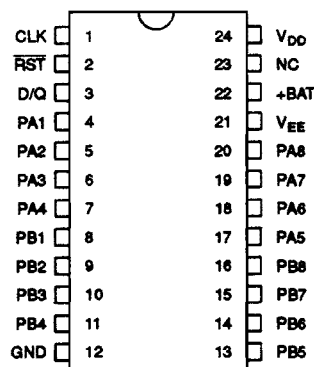


FEATURES

- Any port A input/output can be programmed for connection to any port B input/output
- Registers which define port connections are programmable via a 3-wire serial port
- All port input/output pins will accept both analog and digital signals
- Optional +5 volts and ± 5 volts operation
- Switch registers can be made nonvolatile with external connection of a 3-volt lithium battery
- Applications include:
 - digital/analog switching and multiplexing
 - data scrambling for secure transmission

PIN ASSIGNMENT



24-Pin DIP (600 mil)
See Mech. Drawing
Sect. 16, Pg 4

PIN DESCRIPTION

+BAT	- Battery Input
NC	- No Connection
VEE	- Optional -5 Volts Supply Input
PA1 - PA8	- Port A Input/Output
GND	- Ground
PB1 - PB8	- Port B Input/Output
D/Q	- Serial Port Data Input/Output
CLK	- Serial Port Clock
RST	- Serial Port Reset
V _{DD}	- 5 Volts Power Supply

DESCRIPTION

The DS1277 8-Channel Crosspoint Switch Chip is a programmable, low-power CMOS switching device which has the capacity to interconnect eight digital or analog signals in any combination. Interconnection is controlled by eight data registers of eight bits each which are read and written via a 3-wire serial port. The

eight registers define the 64 possible combinations of the internal crosspoint switch. The DS1277 can be operated from a single +5 volts supply or optional ± 5 volts operation can be selected to allow inputs and outputs to swing above and below ground.

OPERATION – GENERAL

With the -5 volts input grounded and +5 volts applied to pin 24, input/output pins of ports A and B will accept voltage levels between 0 and 5 volts. When V_{EE} is connected to -5 volts with +5 volts applied to pin 24, the input/output pins of ports A and B will accept voltage levels between -5 and +5 volts. Regardless of the voltage selections, applied voltages on port pins will be reproduced on pins which are interconnected by the internal crosspoint switch as defined by the data register settings.

The data registers are shown in Figure 1. As defined, each register specifies one port B I/O pin. Each of the eight bits of the register specifies connection or no connection to each of the port A I/O pins. A logic 1 causes a connection and a logic 0 is a no connection. When the DS1277 is powered up, all register bits are forced to a zero unless a battery voltage of greater than 2 volts is present on pin 22. With proper battery voltage, all registers are retained in the programmable state. If the non-volatile feature is not used then pin 22 must be grounded.

OPERATION – SERIAL PORT

The eight data registers of the DS1277 are written and read via a 3-wire serial port consisting of \overline{RST} , CLK, and D/Q. To initiate data transfer with the DS1277, \overline{RST} is driven high and 24 bits are loaded into the command register on each low-to-high transition of the CLK input. The command register must match the exact bit pattern which defines either a read or a write. If a match does not exist communication will be ignored. If the command register is properly loaded then communication is allowed to continue and the next 64 cycles to the DS1277 will either update the data registers or read the data register content when the data registers are being updated.

Switch settings are not affected until \overline{RST} is driven low at the end of the 64-bit data transfer.

COMMAND WORD

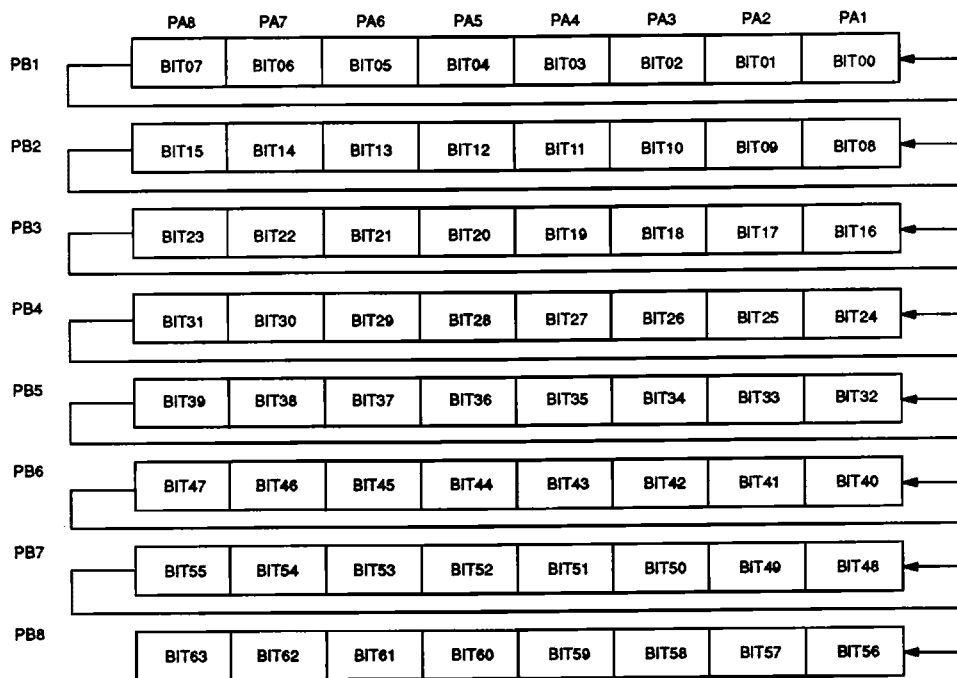
Each data transfer begins with a 3-byte command word as shown in Figure 3. The first byte of the command word specifies whether the 64-bit data registers will be written or read. If any one of the bits of the first byte of the command word fails to meet the exact pattern of read or write, the data transfer will be aborted. The 8-bit pattern for read is 01000110. The pattern for write is 10111001. The second and third bytes of the command word must match the exact pattern 00000000, 11110000 or data transfer is aborted.

RESET AND CLOCK CONTROLS

All data transfers are initiated by driving the \overline{RST} input high. \overline{RST} must remain high for the entire 24-bit command word and the 64-bit data stream. The \overline{RST} input terminates communication and updates the switch settings only after all 64 bits of the data registers have been written when reset is driven low. Reading of registers can be terminated at any time by driving \overline{RST} low.

A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of clock cycles. Command bits and data bits are input on the rising edge of the clock and data bits are output on the falling edge of the clock. All data transfers terminate and D/Q goes to a high impedance state if the \overline{RST} input is low. Transfer of register data to switches occurs as \overline{RST} is driven low only if 64 bits of data have been written. \overline{RST} has no other effect on the register content. Data transfer is illustrated in Figures 4, 5 and 6.

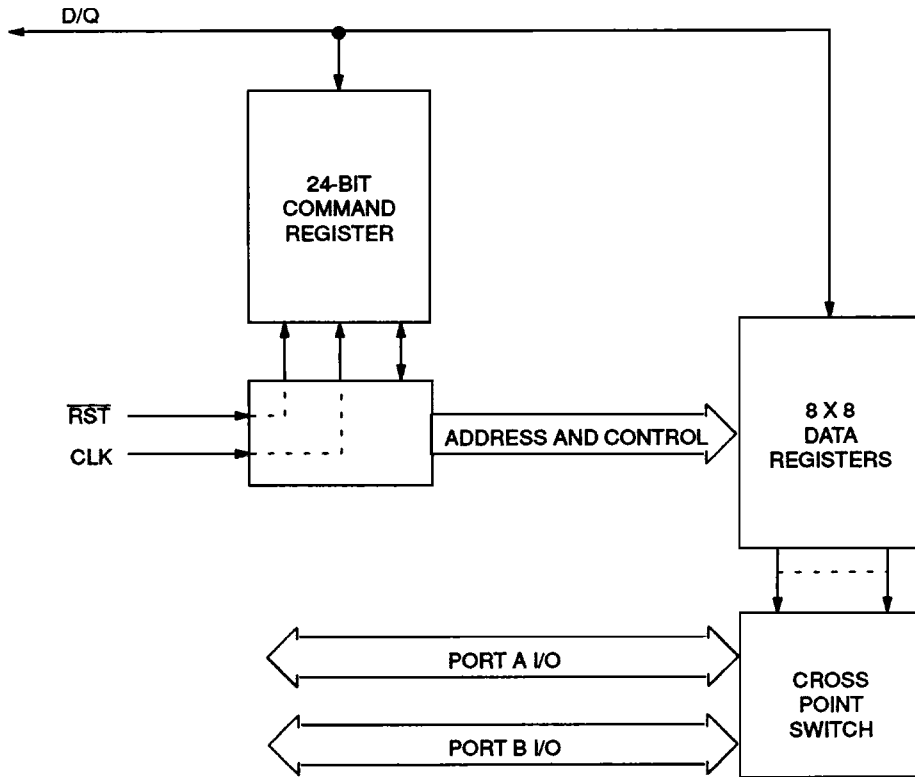
DATA REGISTERS Figure 1



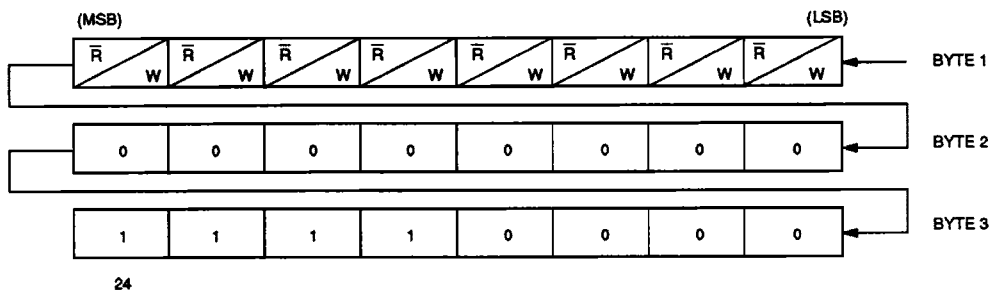
NOTE: Logic 1 closes switch
Logic 0 opens switch

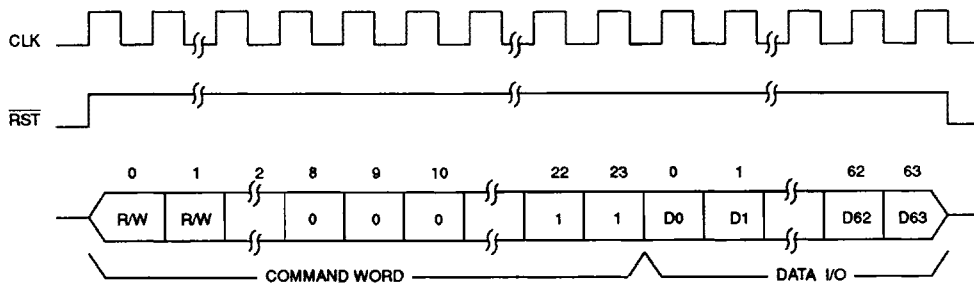
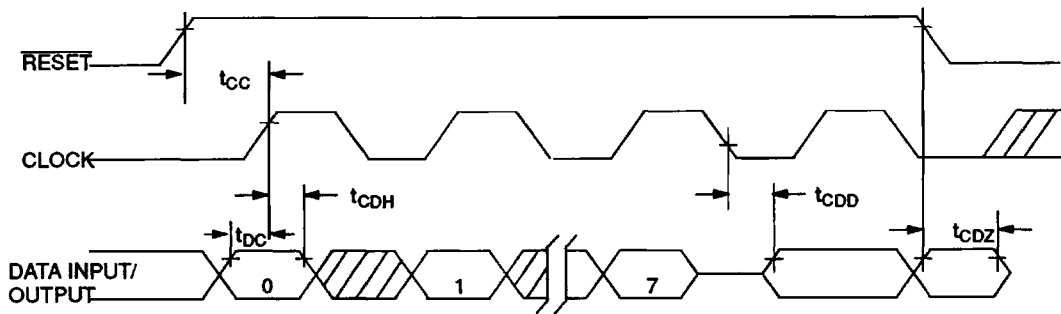
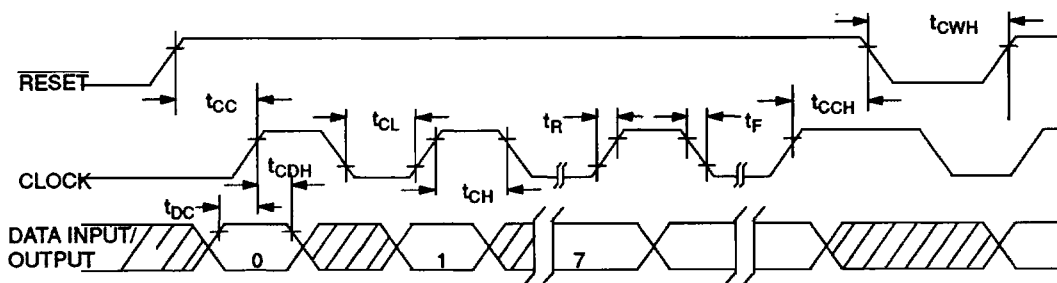
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BLOCK DIAGRAM Figure 2



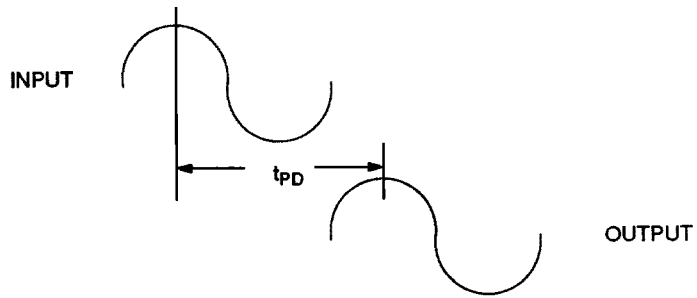
COMMAND REGISTER Figure 3



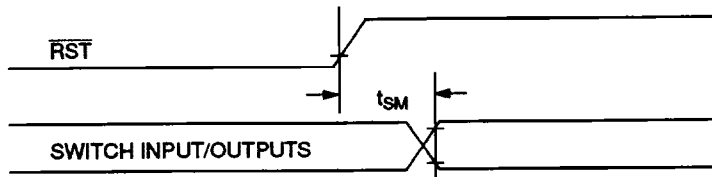
COMMAND WORD/DATA TRANSFER Figure 4**READ DATA TRANSFER** Figure 5**WRITE DATA TRANSFER** Figure 6

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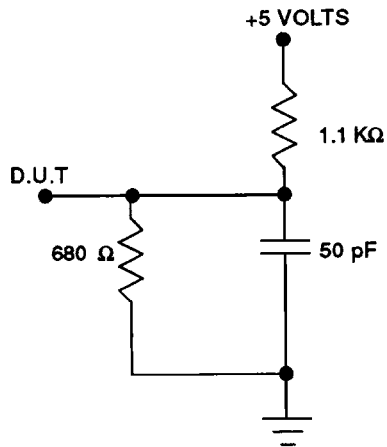
TIMING DIAGRAM: SWITCH PROPAGATION DELAY Figure 7



TIMING DIAGRAM: SWITCH CONNECT t_{SD} Figure 8



OUTPUT LOAD Figure 9



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-5.5V to +7.0V
Operating Temperature	0°C to +70°C
Storage Temperature	-55°C to 125°C
Soldering Temperature	260°C for 10 seconds

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
+ Supply Voltage	V _{DD}	4.5	5.0	5.5	V	1
- Supply Voltage	V _{EE}	0	-5.0	-5.5	V	1
Serial Port Logic 0	V _{IL}	-0.3		0.8	V	1
Serial Port Logic 1	V _{IH}	2.0		V _{DD} +0.3	V	1
A @ B Port Input	V _{IN}	0		V _{DD}	V	-Supply=GND
A @ B Port Input	V _{IN}	-V _{EE}		V _{DD}	V	-Supply=-5.0V
+Battery Input	V _{BAT}	2.5		3.7	V	1

DC ELECTRICAL CHARACTERISTICS(0°C to 70°C; V_{EE} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
D/Q Output Current @ 2.4V	I _{OH}	-1			mA	2
D/Q Output Current @ 0.4V	I _{OL}			+4	mA	2
Input Leakage	I _{IL}	-1		+1	μA	3
Output Leakage	I _{OH}	-1		+1	μA	3
X Switch On Impedance	X _{ON}		250	500	ohms	4
+ Supply Current Active	I _{DD1}			10	mA	
+ Supply Current Quiescent	I _{DD2}		7		mA	5
- Supply Current	I _{EE}			1	mA	
X Switch Off Impedance	X _{OFF}	1 Meg			ohms	
Battery Current @ 3V	I _{BAT}			100	nA	

CAPACITANCE(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C _{IN}			5	pF	
Output Capacitance	C _{OUT}			7	pF	
Feedthrough Capacitance	C _{IN-COUT}			10	pF	

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AC ELECTRICAL CHARACTERISTICS(0°C to 70°C, $V_{CC} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	50			ns	6
CLK to Data Hold	t_{CDH}	50			ns	6
CLK to Data Delay	t_{CDD}			200	ns	2, 6, 7
CLK Low Time	t_{CL}	250			ns	6
CLK High Time	t_{CH}	250			ns	6
CLK Frequency	s_{CLK}	DC		2.0	MHz	6
CLK Rise and Fall	t_{RTF}			500	ns	6
\overline{RST} to CLK Setup	t_{CC}	1			μs	6
CLK to \overline{RST} Hold	t_{CCH}	50			ns	6
RST to I/O High Z	t_{CDZ}			75	ns	6
Input to Output Delay	t_{PD}			50	ns	
\overline{RST} Low to Switch Transition	t_{SM}			50	ns	
\overline{RST} Inactive Time	t_{CWH}	1			μs	

NOTES

1. All voltages are referenced to ground (V_{SS}).
2. Measured with a load as shown in Figure 9.
3. $V_{DD} = +5$ volts, $V_{EE} = -5$ volts, $V_{SS} = GND$: all other pins open.
4. X switch impedance is the terminal resistance of connected switch inputs to outputs.
5. $V_{DD} = +5$ volts, $V_{EE} = -5$ volts, $V_{SS} = GND$, $\overline{RST} = V_{IL}$: all other pins open.
6. Measured at $V_{IH} = 2.0$ or $V_{IL} = 0.8V$ and 10 ns maximum rise (t_R) and fall times (t_F).
7. Measured at $V_{OH} = 2.4$ volts and $V_{OL} = 0.4$ volts.