National Semiconductor

MM58106 Digital Clock and TV Display Circuit

General Description

The MM58106 is a monolithic CMOS integrated circuit which generates a display of channel number and time on the television screen. The circuit can either display United States channel number (2–83) or European program number (1–16). Time display can be 4 or 6-digit, in either 12 or 24-hour mode. Timekeeping is controlled from a 50 Hz or 60 Hz input. The position of the display on the TV screen is controlled by adjusting the external RC time constants.

The circuit is packaged in a 28-lead dual-in-line epoxy package.

Features

- Single chip clock and channel/program number display
- 12 or 24-hour operation
- 4 or 6-digit time display
- Channel or program number display
- 50/60 Hz operation
- Channel and time display on channel change
- Continuous time display
- Continuous time and channel display

Block and Connection Diagrams

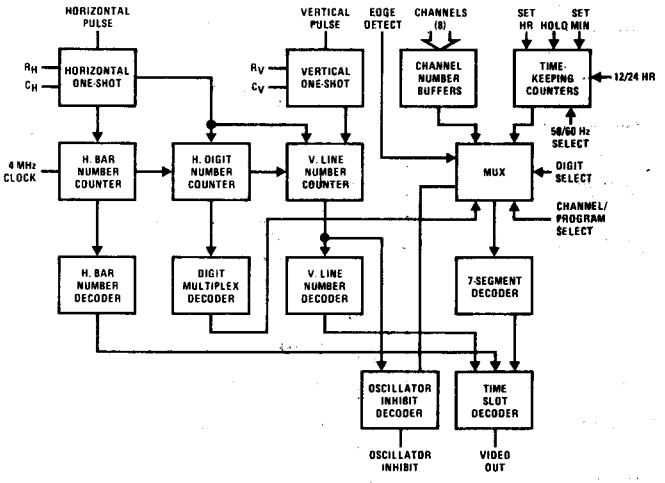
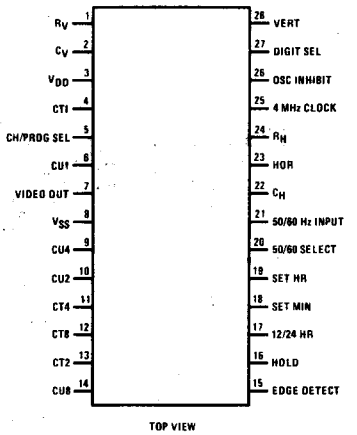


FIGURE 1

Dual-In-Line Package



Order Number MM58106N
See Package 23

FIGURE 2

Absolute Maximum Ratings

Supply Voltage ($V_{DD} - V_{SS}$)	5.5V
Voltage at Any Pin	V_{SS} − 0.3V to +5.5V
Operating Temperature	0°C to +70°C
Storage Temperature	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics V_{DD} = 5V, V_{SS} = 0V, unless otherwise specified

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage, V_{DD}	V_{SS} = 0	4.75	5	5.25	V
Power Supply Current				800	μA
Input Voltage Levels					
Channel Inputs					
Logical Low		V_{SS}−0.3	V_{DD}−5	V_{DD}−4.5	V
Logical High		V_{DD}−0.3	V_{DD}	V_{DD}+0.3	V
Horizontal and Vertical Inputs					
Logical Low		V_{SS}−0.3	V_{DD}−5	V_{DD}−4.5	V
Logical High		V_{DD}−0.3	V_{DD}	V_{DD}+0.3	V
Set Mins, Set Hours, Hold, 12/24-Hour Select, 50/60 Hz Select, Channel/Program Select	Internal Pull-Up Resistor to V_{DD} (600k Min)				
Logical Low		V_{SS}−0.3	V_{SS}	V_{SS}+0.3	V
Logical High			Open		
All Others					
Logical Low		V_{SS}−0.3	V_{SS}	V_{SS}+0.3	V
Logical High		V_{DD}−0.3	V_{DD}	V_{DD}+0.3	V
Input Frequency					
4 MHz Clock		1	4	4.5	MHz
Horizontal	Pulse Width = 14 μs		15.75		kHz
Vertical	Pulse Width = 1 ms		60		Hz
Output Voltage Levels					
Oscillator Inhibit and Video Output					
Logical Low		V_{SS}−0.3	V_{SS}	V_{SS}+0.9	V
Logical High		V_{DD}−0.5	V_{DD}	V_{DD}+0.3	V
One-Shot Output Pulse Duration					
Horizontal			50		μs
Vertical			13		ms
Output Drive					
Video Output					
Logical Low	V_{SS} + 1V	(−1)			mA
Logical High	V_{DD} − 1V	1			mA
Oscillator Inhibit Output					
Logical Low	Output Forced Up to V_{DD} − 4.5V	(−2)			mA
Logical High	V_{DD} − 1V	0.2			mA
External RC					
$C_{VERTICAL}$			0.1		μF
$C_{HORIZONTAL}$			0.001		μF
$R_{VERTICAL}$			100		kΩ pot
$R_{HORIZONTAL}$			100		kΩ pot
Propagation Delay Oscillator Inhibit Output	From Input Clock to Oscillator Inhibit Output			2	clock pulses
Input Leakage				1	μA
Input Capacitance				5	pF
Edge Detect Pulse Duration	C = 2 μF, R = 1 MΩ		2		sec

Functional Description

A block diagram of the MM58106 TV timer is shown in *Figure 1*. A connection diagram is shown in *Figure 2*. Unless otherwise indicated, the following discussions are based on *Figure 1*.

50 or 60 Hz Input: This input has a shaping circuit which allows using a filtered sinewave input. A simple RC filter such as shown in *Figure 3* should be used to remove possible line voltage transients that could either cause the clock to gain time or damage the device. The input should swing between V_{SS} and V_{DD}. The shaper output drives a counter chain which performs the timekeeping function.

Alternatively, in a crystal controlled battery operated system, an oscillator and prescaler circuit such as the MM5369 or MM5368 could be used as a timebase. With a backup battery, the clock will keep time even if the TV power is OFF.

50 or 60 Hz Select Input: This input programs the prescale counter to divide by either 50 or 60 to obtain an internal 1 pps timebase. The counter is programmed for 60 Hz operation by connecting this input to V_{SS}. This input has an internal pull-up resistor. Therefore, leaving this input unconnected programs the clock for 50 Hz operation.

Time Setting Inputs: Inputs to set hours and set minutes as well as a hold input, are provided. Internal pull-up resistors provide the normal timekeeping function. Switching any one of these inputs (one at a time) to V_{SS} results in the desired time setting function. Set Hours advances hours information at one hour per second, and Set Minutes advances minutes information at one minute per second, without roll over into the hours counter. The hold input stops the clock to the minutes counter and resets the seconds counter to 00.

Display Control: The channel number and time display circuits operate from the 4 MHz input clock frequency. This display character size is inversely proportional to the input clock frequency.

The horizontal and vertical position of the display is controlled by adjusting the external RC time constants (R_H, C_H, R_V, C_V).

These monostables are triggered by the horizontal and vertical retrace signals as shown in the timing diagram in *Figure 4 and Figure 5*.

A 7-segment decoder is used to decode either channel inputs or time. Also a time slot decoder is employed to decode the appropriate time slot and the digit to be displayed. It generates a video output signal that can modulate the sweep of the television tube for the on-screen display.

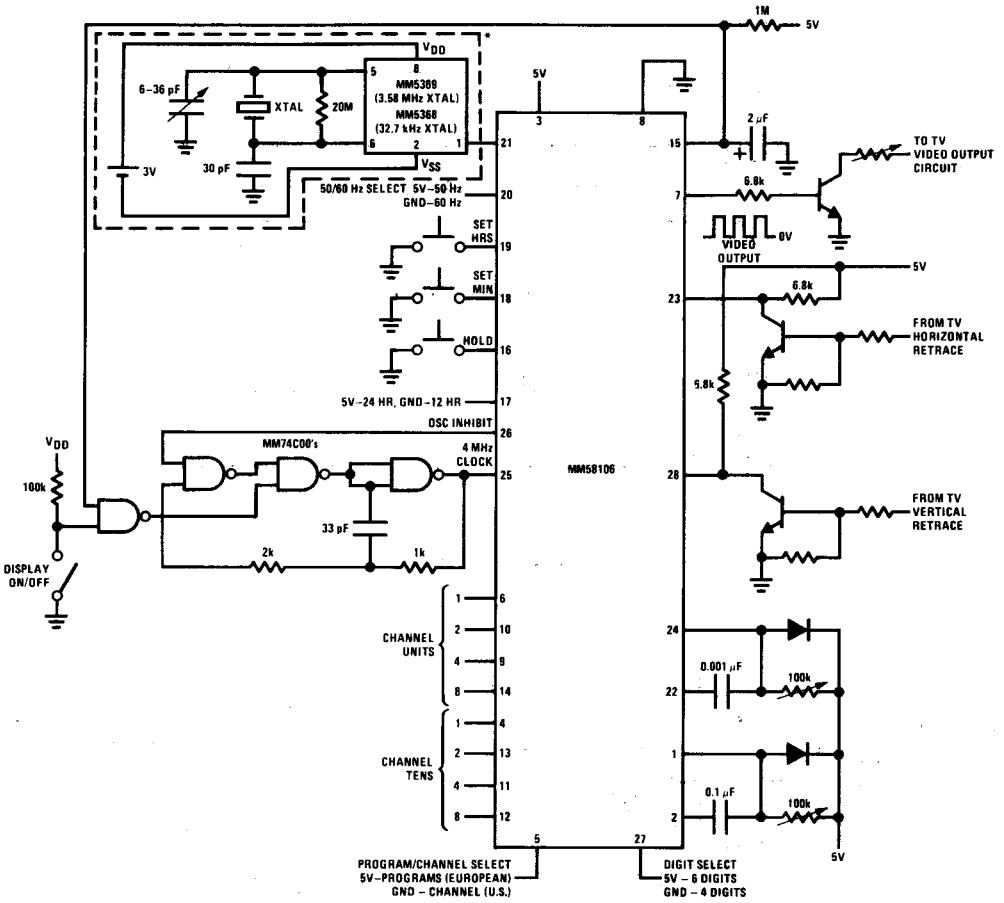
Channel/Program Number Select: This control pin has a pull-up resistor to V_{DD}. With the input open, the chip will accept a binary plus 1 code on the CU1 to CU8 inputs and display the program number from 1 to 16 (European application). With this input at V_{SS}, inputs CU1 to CU8 and CT1 to CT8 will accept BCD inputs for channel units and channel tens, respectively, and display channels 2–83, (U.S. applications), as shown in Table I. Actually, the circuit can display channel number from 0 to 99. Inputs CU1 to CU8 and CT1 to CT8 are negative logic inputs: "1" being V_{SS} level and "0" being V_{DD} level.

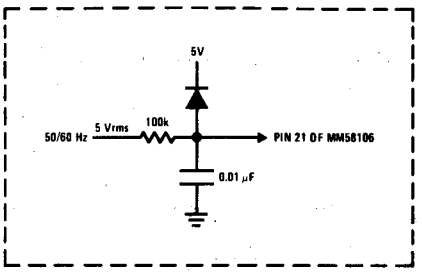
Edge Detect: It is an open-drain output and is a voltage sense input. The output will be ON and sink current to V_{SS} when there is a channel or program change. When the device senses the voltage across the external capacitor *(Figure 3)* less than the lower trip point, the output will be turned OFF (channel display is ON) and the capacitor is then charged towards V_{DD} until the voltage reaches the higher trip point (channel display is OFF). The external RC on this pin will control the ON time of the channel or program number display. When this output is tied to V_{SS}, the channel or program number will display continuously with time display. With Edge Detect tied to V_{DD}, CU1 to CU8 and CT1 to CT8 tied to either V_{DD} or V_{SS}, the device can be used to display time information without channel/program number displayed.

TABLE I. CHANNEL/PROGRAM FUNCTIONAL TRUTH TABLE

CU1/CT1	CU2/CT2	CU4/CT4	CU8/CT8	CHANNEL/PROGRAM SELECT		
				V_{DD} OR OPEN	V_{SS}	
					TEN	UNIT
0	0	0	0	1	BLANK	0
1	0	0	0	2	1	1
0	1	0	0	3	2	2
1	1	0	0	4	3	3
0	0	1	0	5	4	4
1	0	1	0	6	5	5
0	1	1	0	7	6	6
1	1	1	0	8	7	7
0	0	0	1	9	8	8
1	0	0	1	10	9	9
0	1	0	1	11	BLANK	BLANK
1	1	0	1	12	BLANK	BLANK
0	0	1	1	13	BLANK	BLANK
1	0	1	1	14	BLANK	BLANK
0	1	1	1	15	BLANK	BLANK
1	1	1	1	16	BLANK	BLANK

Functional Description (Continued)

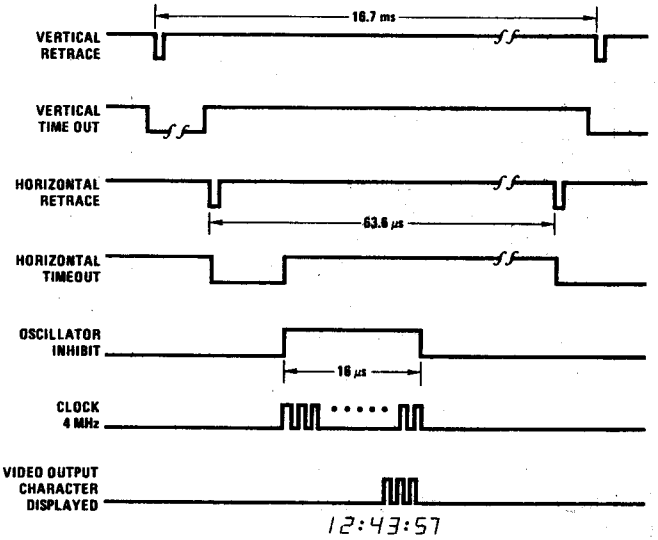




* Optional Input Circuit Utilizing 50/60 Hz AC

FIGURE 3

Functional Description (Continued)



NOTE: Slanted Display of Time

FIGURE 4. Timing Diagram

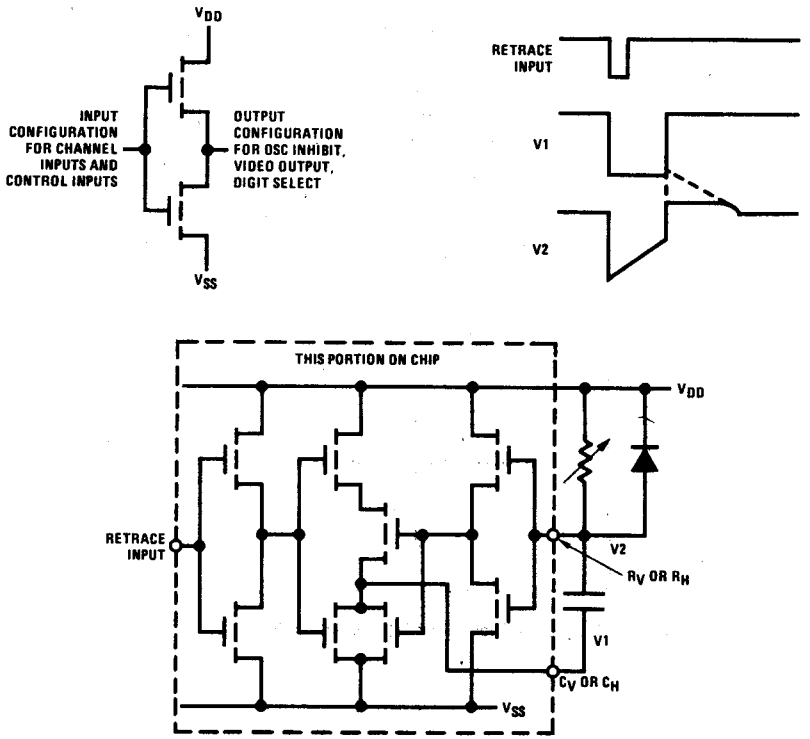


FIGURE 5. Horizontal and Vertical One-Shot Circuit