DATA SHEET

MAY 1999
Revision 2.1

LXP710

HDSL Framer/Mapper for 1168 kbps Applications

General Description

The LXP710 is a complete HDSL framer/mapper that multiplexes and demultiplexes a framed or unframed 2.048 Mbps E1 data stream onto two 1168 kbps HDSL lines. The LXP710 also supports point-to-point and point-to-multipoint fractional E1 applications with 1, 2 or 3 HDSL lines.

The LXP710 interfaces directly with the Level One SK70704/ SK70707 1168 kbps HDSL data pump and industry standard E1 Framers or Line Interface ICs. The framer/mapper is controlled and monitored by an external microprocessor using an 8-bit Intel or Motorola compatible parallel interface. The framer/mapper provides both programmable and 6ms interrupts synchronized to the HDSL frame rate.

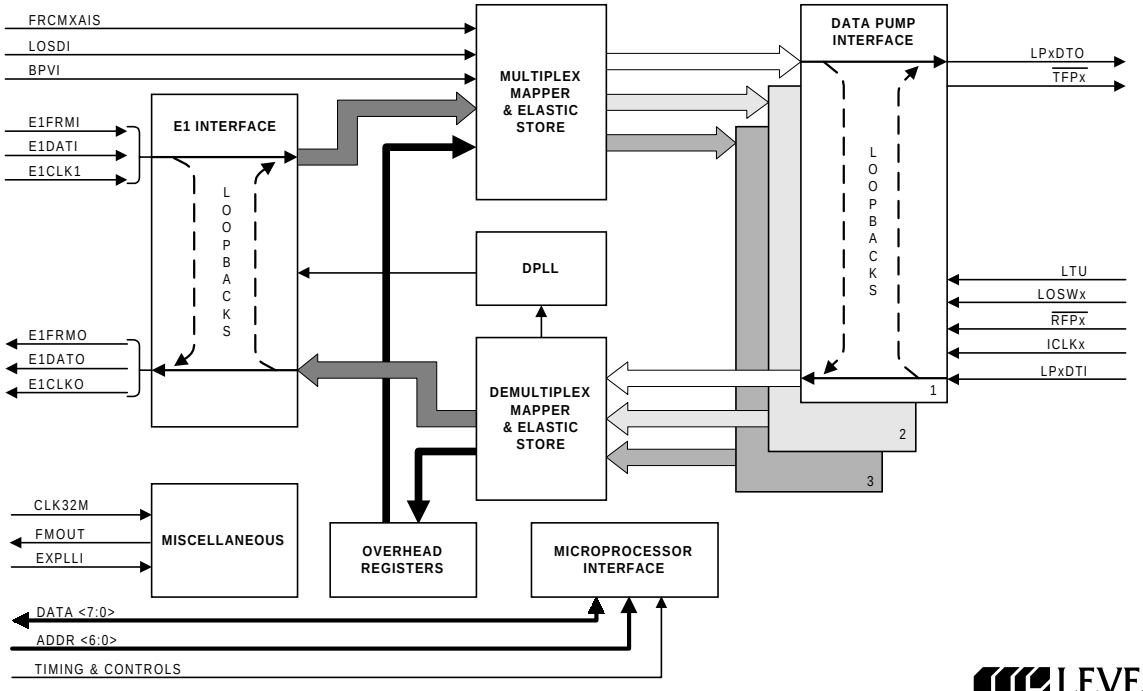
The LXP710 provides fully programmable mapping between the E1 and HDSL interfaces on one or more loops. The LXP710 provides support for system performance monitoring with internal CRC, FEBE and BPV error counters and the capability to inject these errors.

The framer/mapper automatically controls the synchronization between the HDSL loop timing and the E1 payload timing using a digital PLL for E1 timing recovery and a transmitter stuffing control circuit.

Features

- Compliant with ETSI ETR-152 requirements
- Interfaces with 1, 2 or 3 Level One HDSL Data Pumps and industry standard E1 Framers or Line Interface ICs
- 8-bit, Intel or Motorola compatible parallel processor interface with programmable and 6ms interrupts
- E1 to HDSL Loop Multiplexing/Demultiplexing
  - Programmable time slot mapping
  - Accepts framed or unframed E1 data
  - IDLE Code Insertion provides channel blocking in mux and demux directions
  - DS0 Channel Grouping
  - Loopbacks toward E1 and HDSL interfaces
- Diagnostics/Performance Monitoring
  - QRSS Pattern Generation and Detection
  - CRC, BPV and FEBE counters and error generators
- User definable 10 kbps overhead channel
- HDSL Overhead Management
- DPLL for E1 Timing Recovery
- HDSL Transmit Stuffing Control

LXP710 Block Diagram



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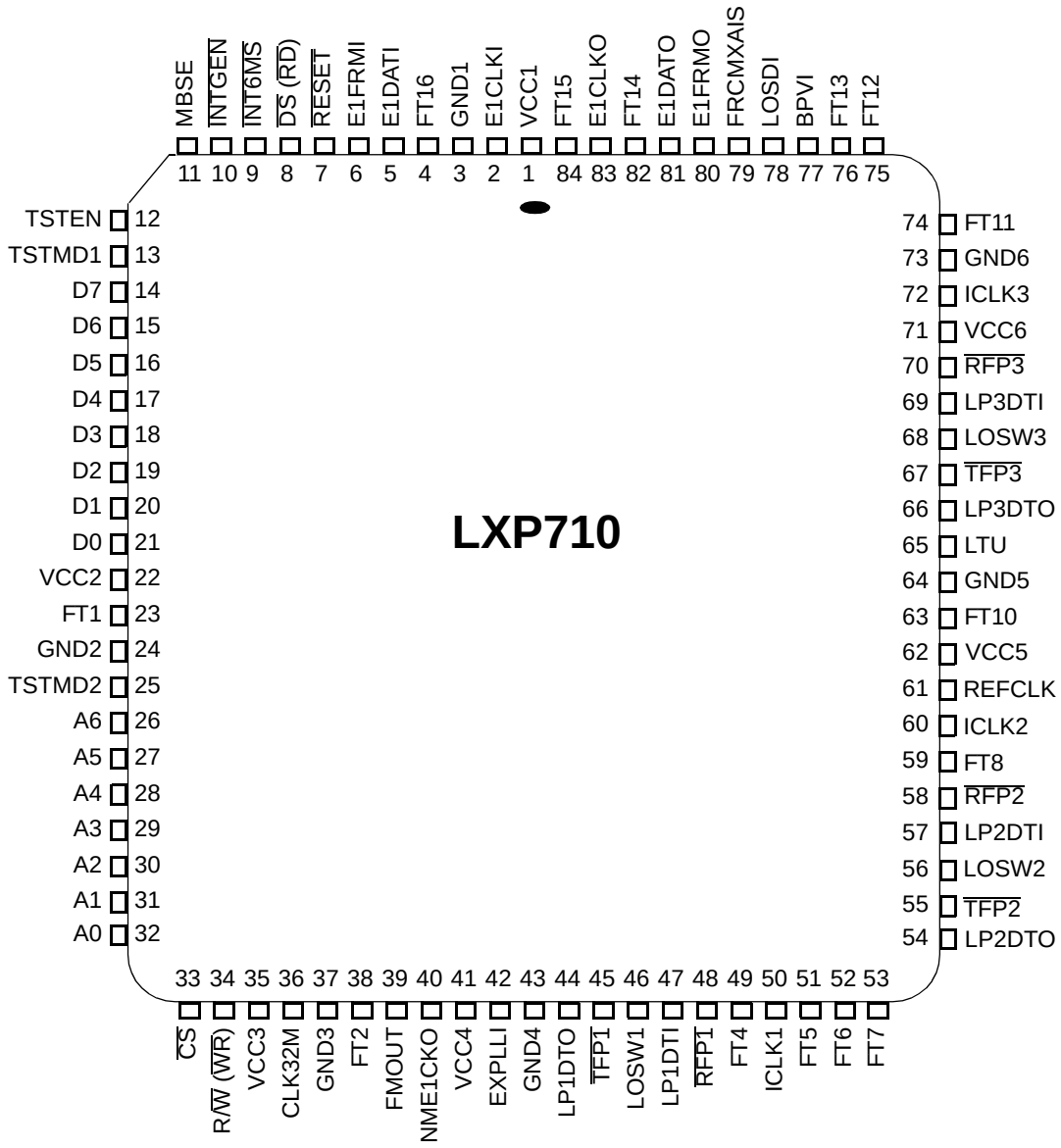
PIN ASSIGNMENTS AND SIGNAL DESCRIPTIONS

Figure 1: LXP710 Pinout Diagram



NOTE:
1. Intel compatible parallel interface signal names are shown in ( ).

Table 1: Pin Descriptions

Pin	Symbol	I/O[1]	Description
1	VCC1	-	**+5 Volt Supply**.
2	E1CLKI	DI	**E1 Clock Input**. This input clock samples mux E1 data and frame mark inputs. The sampling edge of this clock can be inverted by the INVMCK control bit. The nominal frequency of this clock is 2.048 MHz.
3	GND1	-	**Ground**.
4	FT16	-	**Factory Test**. This pin should not be connected and is reserved for factory test.
5	E1DATI	DI	**E1 Data Input**. This input accepts mux E1 data in serial NRZ format.
6	E1FRMI	DI	**E1 Frame Sync Input**. This input identifies the first frame bit position of the mux E1 data. The signal must be High for one E1CLKI period.
7	$\overline{\text{RESET}}$	DI	**Reset** (Active Low). Resets the internal circuits and control registers to their default state when driven Low.
8	$\overline{\text{DS}}$ ($\overline{\text{RD}}$)	DI	**Data Strobe or Read Enable**. In Intel mode, enables a read cycle when Low. In Motorola mode, this signal functions as the data strobe. The LXP710 drives the D<7:0> bus with the contents of the addressed register when $\overline{\text{RD}}$ and $\overline{\text{CS}}$ are Low.
9	$\overline{\text{INT6MS}}$	DO	**6ms Interrupt**. Can be enabled to go Low for a Mux EOC/Overhead bits Ready, a Demux EOC/Overhead bits Ready, or a Triple-Echo Message Compare.
10	$\overline{\text{INTGEN}}$	DO	**General Purpose Interrupt** (Active Low). This output can be enabled to go Low when one or more of the internal general purpose interrupt conditions have been met.
11	MBSE	DI	**Motorola Bus Enable**. When MBSE is High, the LXP710 is configured for Motorola bus mode. When MBSE is Low, the LXP710 is configured for Intel mode. This enable signal configures the $\overline{\text{WR}}$ input to function as R/$\overline{\text{W}}$ and the $\overline{\text{RD}}$ signal to function as $\overline{\text{DS}}$.
12	TSTEN	DI	**Test Mode Enable**. This input should be tied Low to disable factory test modes.
13	TSTMD1	DI	**Test Mode 1**. This input should be tied Low and is reserved for factory test modes.
14	D7	DI/O	**Microprocessor Data Bus**. This 8-bit, bidirectional, tri-state bus is the general purpose data path that can transfer data between the LXP710 and the microprocessor.
15	D6	DI/O	
16	D5	DI/O	
17	D4	DI/O	
18	D3	DI/O	
19	D2	DI/O	
20	D1	DI/O	
21	D0	DI/O	

1. DI = digital input; DO = digital output, DI/O = digital input and output; AI = analog input, AO = analog output.

Table 1: Pin Descriptions – continued

Pin	Symbol	I/O[1]	Description
22	VCC2	-	**+5 Volt Supply**.
23	FT1	-	**Factory Test**. This pin should not be connected and is reserved for factory test.
24	GND2	-	**Ground**.
25	TSTMD2	DI	**Test Mode 2**. This Input should be tied Low and is reserved for factory test modes.
26	A6	DI	**Microprocessor Address Bus**. This 7-bit input bus is used by the microprocessor to select LXP710 registers for read/write data transfer.
27	A5	DI	
28	A4	DI	
29	A3	DI	
30	A2	DI	
31	A1	DI	
32	A0	DI	
33	$\overline{CS}$	DI	**Chip Select** (Active Low). This input must be Low to enable read or write access to the LXP710.
34	R/$\overline{W}$ ($\overline{WR}$)	DI	**Read/Write or Write Enable**. In Intel mode, enables a write cycle when Low. In Motorola mode, this signal functions as the Read/Write control. The D<7:0> bus contents are latched into the addressed register when $\overline{WR}$ and $\overline{CS}$ are Low.
35	VCC3	-	**+5 Volt Supply**.
36	CLK32M	DI	**External Reference Clock**. Requires a 32.768 MHz ±50 ppm input for internal PLL.
37	GND3	-	**Ground**.
38	FT2	-	**Factory Test**. This pin should not be connected and is reserved for factory test.
39	FMOUT	DO	**Frame Pulse Output**. This output pin provides an 6 ms, active High, frame pulse selected from one of $\overline{RFP1}$, $\overline{RFP2}$, or $\overline{RFP3}$ for an external PLL circuit.
40	NME1CKO	DO	**External Reference Clock.** 2.048 Mhz reference for E1 framer and LIU when E1 input has no clock.
41	VCC4	-	**+5 Volt Supply**.
42	EXPLLI	DI	**External PLL Input**. This input clock pin accepts a 2.048 MHz phase locked clock from an external PLL circuit.
43	GND4	-	**Ground**.
44	LP1DTO	DO	**Loop 1 Data Output**. This pin outputs mux data, which is updated on falling edge of ICLK1, to the Loop 1 transceiver. The nominal bit rate of this signal is 1168 kbps.

1. DI = digital input; DO = digital output, DI/O = digital input and output; AI = analog input, AO = analog output.

Table 1: Pin Descriptions – continued

Pin	Symbol	I/O[1]	Description
45	$\overline{\text{TFP1}}$	DO	**Loop 1 Transmit Frame Pulse** (Active Low). A Low level on this signal indicates the last bit position of each mux HDSL frame for Loop 1. The position of this pulse is at bit 7006 when no stuffing is added, or bit 7010 when stuffing is added. This pulse nominally occurs every 6 milliseconds ± 1/584 milliseconds.
46	LOSW1	DI	**Loop 1 Loss of Sync Word Status**. This pin inputs the LOSW status from the Loop 1 transceiver. This pin provides hardware override for the demux TMGSRC control bits, disables Loop 1 error counters, and can force demux E1 Partial-AIS. (If EXTDXAIS bit enabled). It has an internal pull up resistor, and is active High.
47	LP1DTI	DI	**Loop 1 Data In**. This signal inputs demux data, which is sampled on rising edge of ICLK1, from the Loop 1 transceiver. The nominal bit rate of this signal is 1168 kbps.
48	$\overline{\text{RFP1}}$	DI	**Loop 1 Receive Frame Pulse** (Active Low). A Low level on this signal indicates the last bit position of each demux HDSL frame for Loop 1. The position of this pulse is at bit 7006 when no stuffing is added, or bit 7010 when stuffing is added. This pulse nominally occurs every 6 milliseconds ± 1/584 milliseconds.
49	FT4	-	**Factory Test**. This pin should not be connected and is reserved for factory test.
50	ICLK1	DI	**Loop 1 Transceiver Interface Clock**. This clock input synchronizes the transfer of HDSL data and frame mark to/from the Loop 1 transceiver. This clock samples the LP1DTI and $\overline{\text{RFP1}}$ inputs on rising edge, and outputs the LP1DTO and $\overline{\text{TFP1}}$ outputs on the falling edge. The nominal frequency of this clock signal is 1168 kHz.
51	FT5	-	**Factory Test**. This pin should not be connected and is reserved for factory test.
52	FT6	-	**Factory Test**. This pin should not be connected and is reserved for factory test.
53	FT7	-	**Factory Test**. This pin should not be connected and is reserved for factory test.
54	LP2DTO	DO	**Loop 2 Data Output**. This pin outputs mux data, which is updated on falling edge of ICLK2, to the Loop 2 transceiver. The nominal bit rate of this signal is 1168 kbps.
55	$\overline{\text{TFP2}}$	DO	**Loop 2 Transmit Frame Pulse** (Active Low). A Low level on this signal indicates the last bit position of each mux HDSL frame for Loop 2. This position of this pulse is at bit 7006 when no stuffing is added, or bit 7010 when stuffing is added. This pulse nominally occurs every 6 milliseconds ± 1/584 milliseconds.
56	LOSW2	DI	**Loop 2 Loss of Sync Word Status**. This pin inputs the LOSW status from the Loop 2 transceiver. This pin provides hardware override for the demux TMGSRC control bits, disables Loop 2 error counters, and can demux E1 Partial-AIS. It has an internal pull up resistor.

1. DI = digital input; DO = digital output, DI/O = digital input and output; AI = analog input, AO = analog output.

Table 1: Pin Descriptions – continued

Pin	Symbol	I/O[1]	Description
57	LP2DTI	DI	**Loop 2 Data In**. This signal inputs demux data, which is sampled on rising edge of ICLK1, from the Loop 2 transceiver. The nominal bit rate of this signal is 1168 kbps.
58	$\overline{\text{RFP2}}$	DI	**Loop 2 Receive Frame Pulse** (Active Low). A Low level on this signal indicates the last bit position of each demux HDSL frame for Loop 2. The position of this pulse is at bit 7006 when no stuffing is added, or bit 7010 when stuffing is added. This pulse nominally occurs every 6 milliseconds ± 1/584 milliseconds.
59	FT8	-	**Factory Test**. This pin should not be connected and is reserved for factory test.
60	ICLK2	DI	**Loop 2 Transceiver Interface Clock**. This clock input synchronizes the transfer of HDSL data and frame mark to/from the Loop 2 transceiver. This clock samples the LP2DTI and $\overline{\text{RFP2}}$ inputs on rising edge, and outputs the LP2DTO and $\overline{\text{TFP2}}$ outputs on the falling edge. The nominal frequency of this clock signal is 1168 kHz.
61	REFCLK	DI	**Reference Clock.** Provides 18.688 MHz reference clock for HDSL Loopback test.
62	VCC5	-	**+5 Volt Supply**.
63	FT10	-	**Factory Test**. This pin should not be connected and is reserved for factory test.
64	GND5	-	**Ground**.
65	LTU	DI	**LTU Mode Enable**. When this input is High, the LTU mode is selected otherwise, the NTU mode is selected.
66	LP3DTO	DO	**Loop 3 Data Output**. This pin outputs mux data, which is updated on falling edge of ICLK3, to the Loop 3 transceiver. The nominal bit rate of this signal is 1168 kbps.
67	$\overline{\text{TFP3}}$	DO	**Loop 3 Transmit Frame Pulse** (Active Low). A Low level on this signal indicates the last bit position of each mux HDSL frame for Loop 3. This position of this pulse is at bit 7006 when no stuffing is added, or bit 7010 when stuffing is added. This pulse nominally occurs every 6 milliseconds ± 1/584 milliseconds.
68	LOSW3	DI	**Loop 3 Loss of Sync Word Status**. This pin inputs the LOSW status from the Loop 3 transceiver. This pin provides hardware override for the demux TMGSRC control bits, disables Loop 3 error counters, and can force demux E1 Partial-AIS. It has an internal pull up resistor.
69	LP3DTI	DI	**Loop 3 Data In**. This signal inputs demux data, which is sampled on rising edge of ICLK1, from the Loop 3 transceiver. The nominal bit rate of this signal is 1168 kbps.

1. DI = digital input; DO = digital output, DI/O = digital input and output; AI = analog input, AO = analog output.

Table 1: Pin Descriptions – continued

Pin	Symbol	I/O[1]	Description
70	$\overline{\text{RFP3}}$	DI	**Loop 3 Receive Frame Pulse** (Active Low). A Low level on this signal indicates the last bit position of each demux HDSL frame for Loop 3. The position of this pulse is at bit 7006 when no stuffing is added, or bit 7010 when stuffing is added. This pulse nominally occurs every 6 milliseconds ± 1/584 milliseconds.
71	VCC6	-	**+5 Volt Supply**.
72	ICLK3	DI	**Loop 3 Transceiver Interface Clock**. This clock input synchronizes the transfer of HDSL data and frame mark to/from the Loop 3 transceiver. This clock samples the LP3DTI and $\overline{\text{RFP3}}$ inputs on rising edge, and outputs the LP3DTO and $\overline{\text{TFP3}}$ outputs on the falling edge. The nominal frequency of this clock signal is 1168 kHz.
73	GND6	-	**Ground**.
74	FT11	-	**Factory Test**. This pin should not be connected and is reserved for factory test.
75	FT12	-	**Factory Test**. This pin should not be connected and is reserved for factory test.
76	FT13	-	**Factory Test**. This pin should not be connected and is reserved for factory test.
77	BPVI	DI	**BPV Indicator Input**. This pin provides hardware access to the mux HDSL BPV overhead bit on each loop. An active High pulse on this pin activates the BPV indicator bit on each loop in the next frame. This signal is ORed with separate software control bits for each loop that can also activate the BPV bits.
78	LOSDI	DI	**Loss of E1 Signal**. This pin provides hardware access to the mux HDSL LOSD overhead bit on each loop. An active High pulse on this pin activates the LOSD indicator bit on all loops in the next frame. This signal is ORed with separate software control bits for each loop that can also activate the LOSD bits.
79	FRCMXAIS	DI	**Force Mux AIS**. When enabled by the EXTMXAIS control bit, a High on this bit forces the mux E1 to insert AIS.
80	E1FRMO	DO	**E1 Frame Sync Output**. This output identifies the first frame bit position of the demux E1 data. The signal must be High for one E1CLKO period. The nominal frequency of this signal is 8 kHz.
81	E1DATO	DO	**E1 Data Output**. This output signal provides the data to the external E1 framer.
82	FT14	-	**Factory Test**. This pin should not be connected and is reserved for factory test.
83	E1CLKO	DO	**E1 Clock Output**. This output is used to synchronize the transfer of E1 frame mark and data. The output edge of this clock can be inverted by the INVDXCK control bit. The nominal frequency of this clock is 2.048 MHz.
84	FT15	-	**Factory Test**. This pin should not be connected and is reserved for factory test.

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FUNCTIONAL DESCRIPTION

The framer is separated into the following blocks of logic: the multiplexer, demultiplexer, microprocessor interface, E1 interface, and HDSL interface. The following subsections describe each logic function.

The ETSI Technical Report ETR 152 will yield a better understanding of the ETSI HDSL system. Framer related sections include, but are not limited to, the HDSL core specifications, frame structure and Application specific requirements. It is beyond the scope of this document to completely explain all of the details in ETR 152, but some of the directly related HFMA functionality will be covered.

Multiplexer (MX)

The function of the MX block is to split the E1 payload into 2 or 3 parts and then multiplex each part with HDSL overhead (HOH) bits, including CRC6, eoc and Z-bits to be passed on to the individual HDSL data pumps. The MX block controls stuffing into the HDSL data stream. The MX block configuration registers are programmed by the microprocessor. The microprocessor also sets the eoc and Z-bits. Individual loop testing is supported by generating test and error patterns in the MX block.

Sync word generation and data scrambling, as defined by ETR 152, are done by the SK70707 digital transceiver, and therefore are not performed by the HFMA.

Figure 2 shows a simplified logic block of the MX process. The MX_E1_CTL block uses the selected E1 clock to load the E1 data from the E1 Interface into the FIFOs. The E1 clock may be either the derived clock from the E1 data stream, E1CLKI, or an internal nominal clock (E1_NMCK). The MXE1CTL register (see Table 3 on page 17) controls which E1 clock is selected as well as selecting whether E1 data or AIS (all 1s) is clocked into the FIFOs. The NMFMEN bit of the MXE1CTL register, when 0, selects the E1FRMI pin, otherwise an internally generated frame pulse is used. The Loop *n* Time Slot Control Byte registers, L*n*TSCTL*x*, listed in Tables 10 through 21, control which time slots of the E1 data stream are assigned to which HDSL loop. The values loaded in these registers become valid only after setting the LDTABLE bit in the TSCTL register (see Table 9 on page 23). The MX Process HDSL loop data is routed to the HDSL Interface.

HDSL loops 2 and 3 are aligned to loop 1. The HDSL_MX block multiplexes the HOH bits with the payload data as shown in Table 115 on page 56. The HOH bits consist of 19 indicator bits, 13 eoc bits, 14-bit sync word, and 4 stuffing bits (when necessary). Each loop has its own multiplexer. A CRC6 is calculated per frame for each loop excluding the CRC bits, 14-bit sync word and the 4 stuffing bits. The result is stored and transmitted in the following frame.

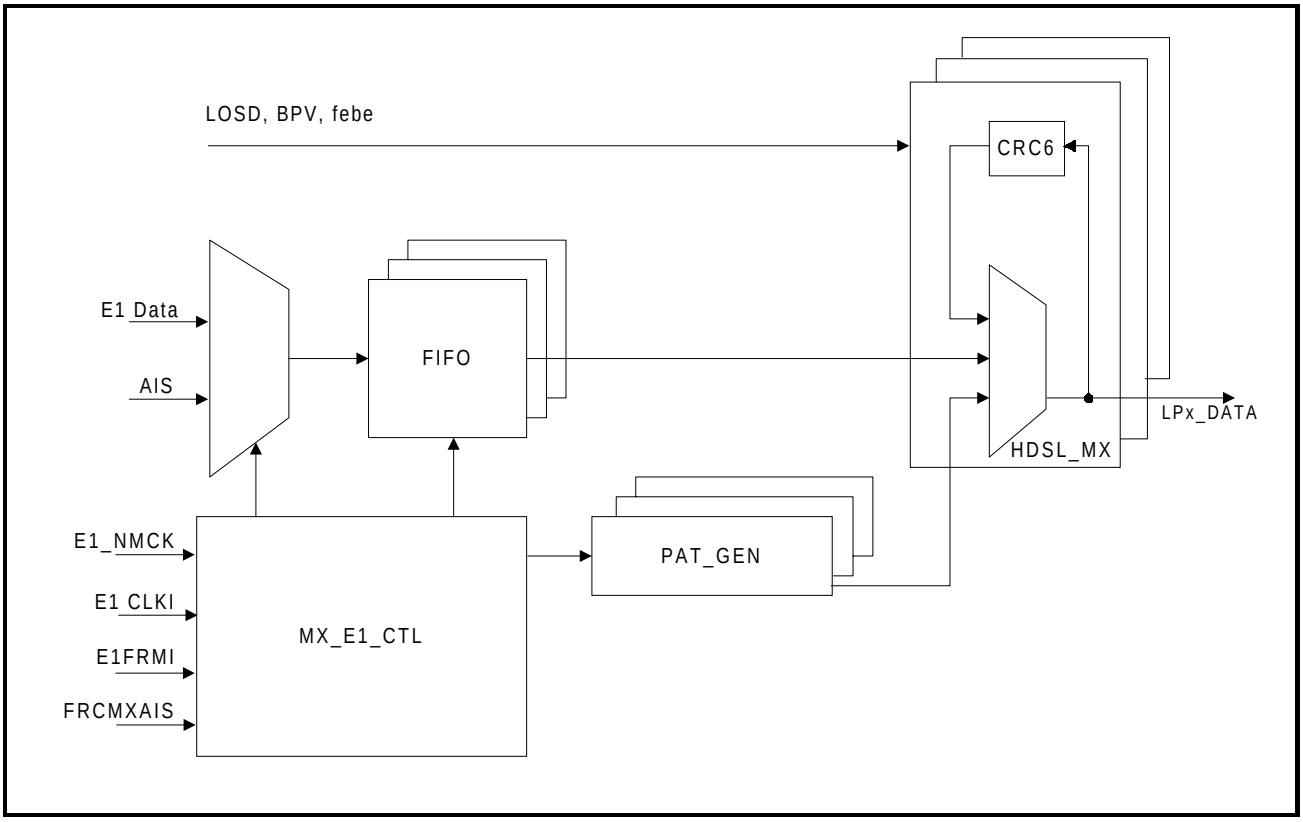
The other indicator bits are febe, losd, bpv, ps1, ps2, hrp, rrbe, rcbe, rega, rta, indc/indr and uib. The febe bit is generated from the DX process and is sent out to the far end HDSL device to indicate that a CRC error occurred in the local received data. The losd bit is from the LOSDI pin for loss of signal at the E1 interface. The bpv bit is from the BPVI pin for a bipolar violation in the E1 data. The bits ps1 and ps2 are Power Status bits from NTU (HTU-R) -> LTU (HTU-C) only. The hrp is the HDSL Repeater Present bit (repeater only). The rrbe, rcbe and rega bits are used for the regenerator/repeater status. The rta is for the remote (NTU) alarm. The 2 uib bits are the Unspecified Indicator Bits.

Several bits can be set for error injection testing on a per loop basis. The outgoing febe and bpv bits can be injected as single bit errors. The CRC can be set for continuous error generation. Registers L*n*OHCTL, listed in Tables 6 through 8, control this activity.

The transmitted Z-bits and eoc bits are set by the microprocessor interface. The Z-bit transmit registers are MXL1Z*x* in Tables 40 through 63, MXL2Z*x* in Tables 64 through 87, MXL3Z*x* in Tables 88 through 111. The eoc transmit registers are MXL1EOC in Tables 46 and 47, MXL2EOC in Tables 70 and 71, MXL3EOC in Tables 94 and 95. In general applications, the eoc is used by the HTU-C to transmit a command continuously to the HTU-R unit until the HTU-R echoes the same command back to the HTU-C three times. ETR 152 recommends some common commands that might be used, but it is up to each vendor to specify detailed implementation. The only defined Z-bits are the first three used for loop identification. Other Z-bits are reserved for vendor use.

The PAT_GEN block generates a QRSS pattern and can be set to generate an error in that pattern. The QRSS is put in place of the E1 data for testing purposes. The QRSS signal is on a per loop basis and is controlled by the PATCTL register as described in Table 23 on page 27.

Figure 2: MX Process



Demultiplexer (DX)

The DX performs the reverse function of the MX by de-multiplexing the HDSL bits into HOH bits and payload data and then combining the 2/3 HDSL payloads into an E1 payload. The HOH bits, eoc and Z-bits, are separated out from the payload, stored into registers for the microprocessor to read. The DX checks the received CRC6 against the data and sets a flag in case of an error condition. The DX also provides the E1 clock based upon an internal PLL.

Figure 3 shows a simplified logic diagram of the DX Process. Each individual loop data is clocked into a separate FIFO. The DX_E1_CTL block controls the Write Enable to the FIFOs by blocking the HOH bits from being loaded into the FIFOs. The DX_E1_CTL selects from which FIFO to load data. The ordering of the time slots is based on the values programmed into the L*n*TSCTL*x* registers as described in Tables 10 through 21. The values loaded in these registers become valid only after setting the LDTABLE bit in the TSCTL register, Table 9. The data is passed through a mux to DX_E1_DATA. The other selection of the mux is AIS. The use of AIS for the outgoing E1 data is controlled by the 4 LSBs of DXE1CTL register (see Table 4).

The DX_E1_CTL block generates a 1168KHz gapped clock as a reference for the E1_TMG_GEN block. The DX_E1_CTL uses the DX_E1_CK from the E1_TMG_GEN to track the current position in the outgoing E1 data stream and to generate the DX_E1_FM, E1 framing pulse.

The E1_TMG_GEN uses the DX_GAP_CK as the reference for the DX_E1_CK. The DX_E1_NMCK is a nominal E1 clock used for E1 AIS, E1 loopback and as the source for the NME1CKO pin to sync an E1 framer when it has no clock.

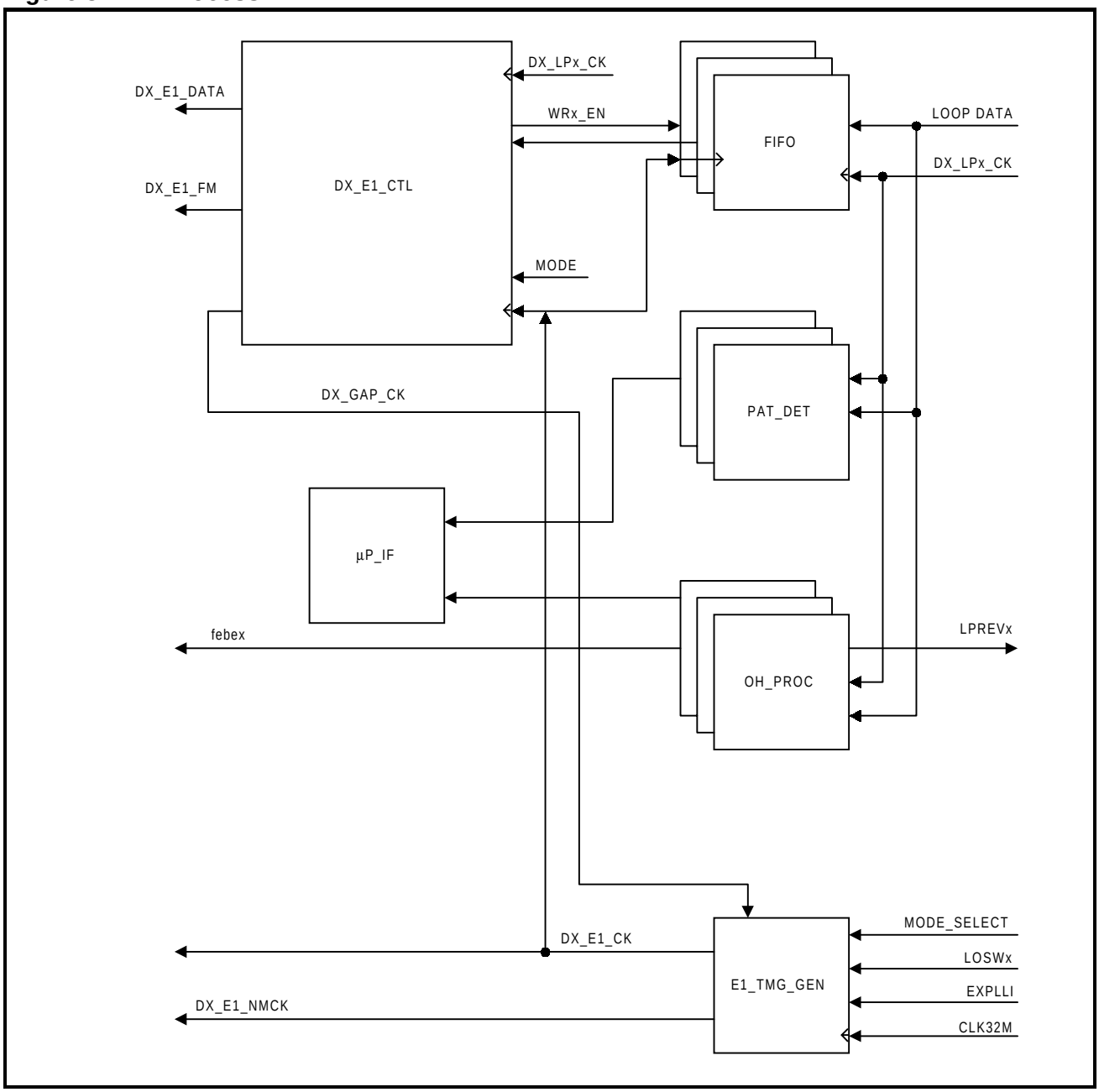
The OH_PROC, overhead processor, looks for all of the HOH bits in the incoming HDSL frames. There is a OH_PROC block for each HDSL loop. The received Z-bits, eoc bits and overhead bits are latched into their respective registers in the UP_IF. A CRC is calculated on the received data and the result is stored for comparison against the CRC bits in the following frame. A CRC error generates the febe bit to the MX Process. The OH_PROC

increments the associated error counters for CRC, febe and bpv. These counters are in the µP_IF section. The sync word bits and stuffing bits are discarded.

The OH_PROC compares the loop ID received from each loop and generates a report to the µP_IF, LPRSTAT register in Table 29, and sends the loop correction bits to the HDSL Interface.

The PAT_DET block, one per loop, generates a Pattern Sync Lost indication bit, PATLOS bit in PATSTAT register (see Table 25 on page 28), when the sync is not present. The PAT_DET increments the appropriate L*n*PATECL (see Tables 61, 85, and 110) counter for each instance of a QRSS pattern bit failure. Overflows of these counters are indicated in PATSTAT register OVERFLOW bits (see Table 25). Overflows may also be set to trigger an interrupt via the µP_IF registers GENINTEN and GENINTSTAT (see Tables 30 and 31).

Figure 3: DX Process



Microprocessor Interface

The microprocessor interface provides access to all of LXP710's registers and routes the interrupt signals to external pins. The MBSE pin configures the LXP710 microprocessor interface for either the Intel or Motorola bus timing. The LXP710 registers are described in Tables 2 through 114.

In the Motorola Mode (MBSE pin set High), the data bus D<0:7>, address bus A<0:6>, $\overline{CS}$, $\overline{DS}$ and R/$\overline{W}$ are used to read or write to the LXP710's internal registers.

In the Intel Mode (MBSE pin set Low), the data bus D<0:7>, address bus A<0:6>, $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$ are used to read or write to the LXP710's internal registers. The board design must include a latch, using ALE, for the address from the Intel multiplexed AD bus. This latch could be shared with the data pumps and other devices on board that have non-multiplexed address pins.

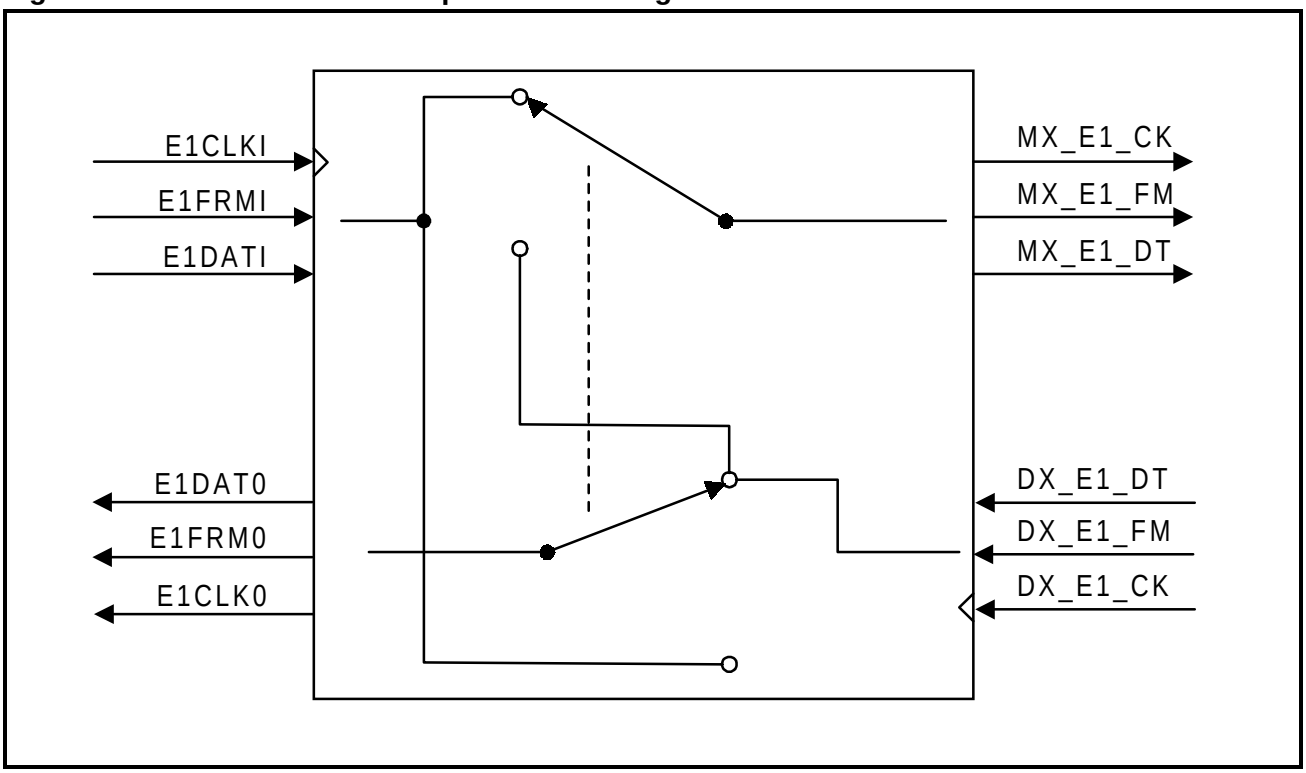
To optimize code execution, Two external interrupt pins, $\overline{INTGEN}$ and $\overline{INT6MS}$, are provided. The $\overline{INTGEN}$ pin is for general purpose interrupts as listed in the GENINTEN and GENINTSTAT registers in Tables 30 and 31. The INDCR bits in the IND_3EOCINTEN and IND_3EOCINTSTAT registers in Tables 34 and 35 are also tied to the $\overline{INTGEN}$ pin.

The $\overline{INT6MS}$ pin is for the 6 ms timing related functions such as when the MX eoc and Z-bits are ready to be loaded to transmit and when the DX eoc and Z-bits have been received. Additionally the EOC Triple-Echo Message Compare Detected bits in the IND_3EOCINTEN and IND_3EOCINTSTAT registers (see Tables 34 and 35) are also tied to the $\overline{INT6MS}$ pin. This feature reduces software processing needed to detect that a message has been received three times.

E1 Interface

The E1 interface connects to an E1 framer device. As shown in Figure 4, the incoming E1 data is routed to the MX and is controlled by signals from the E1 framer. The E1 interface takes E1 data from the DX and provides control signals for the E1 framer. Two loopbacks are available. The first loopback is for E1 input data to E1 output data. The other is the loopback for the internal DX E1 payload back to the MX block. As shown in the diagram, the two loopbacks are tied together. The loopback is achieved by setting the E1LB bit in the DXE1CTL register as described in Table 4.

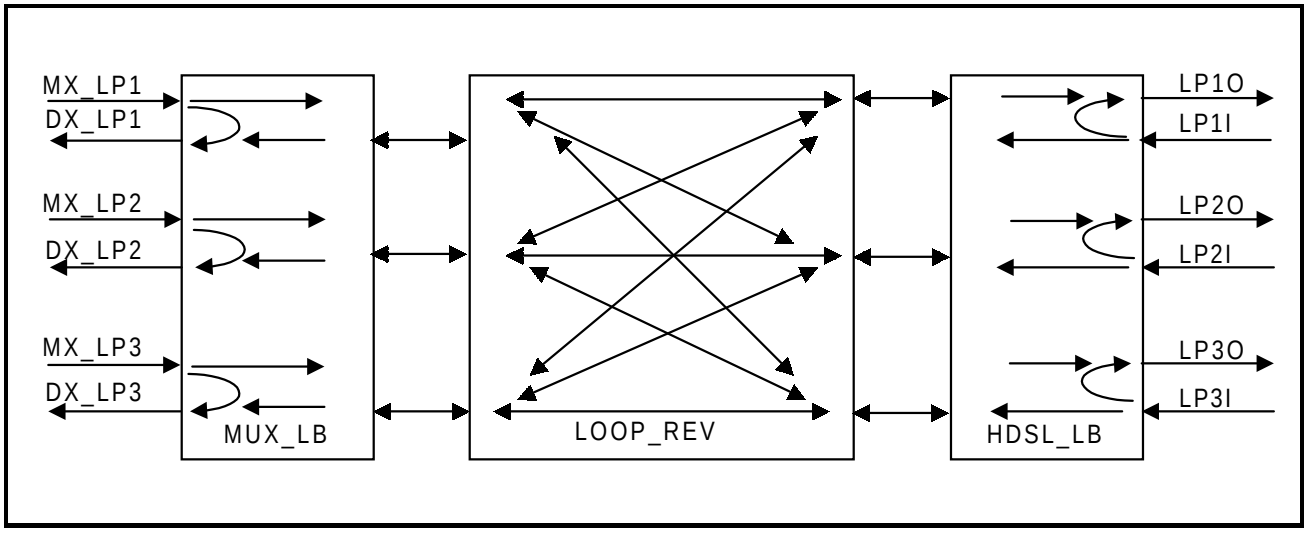
Figure 4: E1 Interface with Loopback Switching



HDSL Interface

The HDSL interface block connects the HDSL loops to the MX and DX blocks. The block can provide loop switching, as well as loopback for each external incoming loop and a loopback for the internal MX signals to the DX block. Figure 5 shows the possible signal routings. When the HDSLLB bit in the LPCTL register (see Table 5) is set, all HDSL Interface loopbacks are set. The LOOP_REV block shows how any loop swap combination can be set by the DX Process in Figure 3. The status of the loop connections can be monitored by reading the LPREV bits in the LPRSTAT register. See Table 29.

Figure 5: HDSL Interface



REGISTER DEFINITIONS

Table 2 provides a summary of the LXP710 registers. Tables 3 through 114 provide detailed descriptions of each of the LXP710 register bits. The specified default values are set when the LXP710 is reset by pin 7.

Table 2: Register Summary

Hex Address	Decimal Address	Symbol	Type	Description
00	0	MXE1CTL	R/W	Mux E1 control register
01	1	DXE1CTL	R/W	Demux E1 control register
02	2	LPCTL	R/W	HDSL loop control register
03	3	L1OHCTL	R/W	HDSL Loop 1 overhead control register
04	4	L2OHCTL	R/W	HDSL Loop 2 overhead control register
05	5	L3OHCTL	R/W	HDSL Loop 3 overhead control register
06	6	TSCTL	R/W	Time slot grouping table control register
07	7	L1TSCTL1	R/W	Loop 1 time slot control byte 1
08	8	L1TSCTL2	R/W	Loop 1 time slot control byte 2
09	9	L1TSCTL3	R/W	Loop 1 time slot control byte 3
0A	10	L1TSCTL4	R/W	Loop 1 time slot control byte 4
0B	11	L2TSCTL1	R/W	Loop 2 time slot control byte 1
0C	12	L2TSCTL2	R/W	Loop 2 time slot control byte 2
0D	13	L2TSCTL3	R/W	Loop 2 time slot control byte 3
0E	14	L2TSCTL4	R/W	Loop 2 time slot control byte 4
0F	15	L3TSCTL1	R/W	Loop 3 time slot control byte 1
10	16	L3TSCTL2	R/W	Loop 3 time slot control byte 2
11	17	L3TSCTL3	R/W	Loop 3 time slot control byte 3
12	18	L3TSCTL4	R/W	Loop 3 time slot control byte 4
13	19	IDLECODE	R/W	Programmable idle code bytes
14	20	PATCTL	R/W	QRSS test pattern control register
15	21	FMSYNC_PLLCTL	R/W	Frame pulse sync & PLL control register
16	22	PATSTAT	R/W	Test pattern error counter status register
17	23	DXPSSTAT	R/W	Demux power status register
18	24	DXHRPSTAT	R/W	Demux HDSL repeater present status register
19	25	DXLOSDSTAT	R/W	Demux loss of signal status register
1A	26	LPRSTAT	R/W	Loop reversal status register
1B	27	GENINTEN	R/W	General interrupt enable register
1C	28	GENINTSTAT	R/W	General interrupt status register
1D	29	6MSINTEN	R/W	6 ms interrupt enable register
1E	30	6MSINTSTAT	R/W	6 ms interrupt status register

Table 2: Register Summary – continued

Hex Address	Decimal Address	Symbol	Type	Description
1F	31	IND_3EOCINTEN	R/W	Indicator bits & triple echo EOC enable register
20	32	IND_3EOCINTSTAT	R/W	Indicator bits & triple echo EOC status register
21	33	GLBCTL	R/W	Global control register
22	34	PLL_BWH	R/W	PLL band width control (high byte)
23	35	PLL_BWL	R/W	PLL band width control (low byte)
24	36	DXRSCNTR	R	Demux loops restart counter
25	37	MXL1Z1	R/W	Mux loop 1 Z bits (LSB)
26	38	MXL1Z2	R/W	Mux loop 1 Z bits
27	39	MXL1Z3	R/W	Mux loop 1 Z bits
28	40	MXL1Z4	R/W	Mux loop 1 Z bits
29	41	MXL1Z5	R/W	Mux loop 1 Z bits
2A	42	MXL1Z6	R/W	Mux loop 1 Z bits (MSB)
2B	43	MXL1EOCH	R/W	Mux loop 1 EOC message (high byte)
2C	44	MXL1EOCL	R/W	Mux loop 1 EOC message (low byte)
2D	45	MXL1UIB	R/W	Mux loop 1 UIB bits
2E	46	DXL1Z1	R	Demux loop 1 Z bits (LSB)
2F	47	DXL1Z2	R	Demux loop 1 Z bits
30	48	DXL1Z3	R	Demux loop 1 Z bits
31	49	DXL1Z4	R	Demux loop 1 Z bits
32	50	DXL1Z5	R	Demux loop 1 Z bits
33	51	DXL1Z6	R	Demux loop 1 Z bits (MSB)
34	52	DXL1EOCH	R	Demux loop 1 EOC message (high byte)
35	53	DXL1EOCL	R	Demux loop 1 EOC message (low byte)
36	54	DXL1UIB	R	Demux loop 1 UIB bits
37	55	DXL1CRCEC	R	Demux loop 1 CRC error count
38	56	DXL1FEBEEC	R	Demux loop 1 FEBE error count
39	57	DXL1BPVEC	R	Demux loop 1 BPV error count
3A	58	L1PATECH	R	Loop 1 QRSS test pattern error counter (High)
3B	59	L1PATECL	R	Loop 1 QRSS test pattern error counter (Low)
3C	60	MX1RSCNTR	R	Loop 1 mux restart counter
3D-3F	61-63	–	–	Unused
40-44	64-68	–	–	Unused
45	69	MXL2Z1	R/W	Mux loop 2 Z bits (LSB)
46	70	MXL2Z2	R/W	Mux loop 2 Z bits
47	71	MXL2Z3	R/W	Mux loop 2 Z bits
48	72	MXL2Z4	R/W	Mux loop 2 Z bits

Table 2: Register Summary – continued

Hex Address	Decimal Address	Symbol	Type	Description
49	73	MXL2Z5	R/W	Mux loop 2 Z bits
4A	74	MXL2Z6	R/W	Mux loop 2 Z bits (MSB)
4B	75	MXL2EOCH	R/W	Mux loop 2 EOC message (High byte)
4C	76	MXL2EOCL	R/W	Mux loop 2 EOC message (Low byte)
4D	77	MXL2UIB	R/W	Mux loop 2 UIB bits
4E	78	DXL2Z1	R	Demux loop 2 Z bits (LSB)
4F	79	DXL2Z2	R	Demux loop 2 Z bits
50	80	DXL2Z3	R	Demux loop 2 Z bits
51	81	DXL2Z4	R	Demux loop 2 Z bits
52	82	DXL2Z5	R	Demux loop 2 Z bits
53	83	DXL2Z6	R	Demux loop 2 Z bits (MSB)
54	84	DXL2EOCH	R	Demux loop 2 EOC message (High byte)
55	85	DXL2EOCL	R	Demux loop 2 EOC message (Low byte)
56	86	DXL2UIB	R	Demux loop 2 UIB bits
57	87	DXL2CRCEC	R	Demux loop 2 CRC error count
58	88	DXL2FEBEEC	R	Demux loop 2 FEBE error count
59	89	DXL2BPVEC	R	Demux loop 2 BPV error counter
5A	90	L2PATECH	R	Loop 2 QRSS test pattern error counter (High byte)
5B	91	L2PATECL	R	Loop 2 QRSS test pattern error counter (Low byte)
5C	92	MX2RSCNTR	R	Loop 2 mux restart counter
5D-5F	93-95	–	–	Unused
60-64	96-100	–	–	Unused
65	101	MXL3Z1	R/W	Mux loop 3 Z bits (LSB)
66	102	MXL3Z2	R/W	Mux loop 3 Z bits
67	103	MXL3Z3	R/W	Mux loop 3 Z bits
68	104	MXL3Z4	R/W	Mux loop 3 Z bits
69	105	MXL3Z5	R/W	Mux loop 3 Z bits
6A	106	MXL3Z6	R/W	Mux loop 3 Z bits (MSB)
6B	107	MXL3EOCH	R/W	Mux loop 3 EOC message (High byte)
6C	108	MXL3EOCL	R/W	Mux loop 3 EOC message (Low byte)
6D	109	MXL3UIB	R/W	Mux loop 3 UIB bits
6E	110	DXL3Z1	R	Demux loop 3 Z bits (LSB)
6F	111	DXL3Z2	R	Demux loop 3 Z bits
70	112	DXL3Z3	R	Demux loop 3 Z bits
71	113	DXL3Z4	R	Demux loop 3 Z bits
72	114	DXL3Z5	R	Demux loop 3 Z bits

Table 2: Register Summary – continued

Hex Address	Decimal Address	Symbol	Type	Description
73	115	DXL3Z6	R	Demux loop 3 Z bits (MSB)
74	116	DXL3EOCH	R	Demux loop 3 EOC message (High byte)
75	117	DXL3EOCL	R	Demux loop 3 EOC message (Low byte)
76	118	DXL3UIB	R	Demux loop 3 UIB bits
77	119	DXL3CRCEC	R	Demux loop 3 CRC error count
78	120	DXL3FEBEEC	R	Demux loop 3 FEBE error count
79	121	DXL3BPVEC	R	Demux loop 3 BPV error count
7A	122	L3PATECH	R	Loop 3 QRSS test pattern error counter (High byte)
7B	123	L3PATECL	R	Loop 3 QRSS test pattern error counter (Low byte)
7C	124	MX3RSCNTR	R	Loop 3 mux restart counter
7D	125	VER	R	HFMA version number
7E	126	MXTEST	R/W	µP mode testing register for mux
7F	127	DXTEST	R/W	µP mode testing register for demux

Mux E1 Control Register

Address: 00
Abbreviation: MXE1CTL
Read/Write

Table 3: Mux E1 Control Register

Bit	Name	Default	Description
7	n/a	0	Not used; Always read Low.
6	n/a	0	Not used; Always read Low.
5	INVMXCK	0	Invert Mux E1 Input Clock. When High, the rising edge of E1CLKI samples the mux E1 data and frame mark. When this bit is Low, the falling edge samples the data and frame mark.
4	NMCKEN	0	Nominal Clock Enable. When High, nominal clock is selected to input the MX_PROCESS block. When Low, E1 recovered clock is selected to input the MX_PROCESS block.
3	NMFMEN	0	Nominal Frame Pulse Enable. When High, nominal frame pulse is selected to input the MX_PROCESS block. When Low, Demux E1 frame pulse is selected to input the MX_PROCESS block.
2	MXSLIDEN	1	MUx Sliding Enable. When High, sliding mode is selected. When Low, jerking mode is selected.
1	SNDMXAIS	0	Send Mux E1 AIS. When High, E1 AIS is inserted into the mux HDSL payload of two/three loops. When Low, the incoming E1 is inserted. This control bit is ORed with the FRCMAIS input pin (when enabled) to control mux AIS.
0	EXTMAIS	0	External Mux AIS Enable. When High, the FRCMAIS input pin is enabled to insert mux E1 AIS. When Low, mux AIS insert is controlled solely by the SNDMAIS control bit.

NOTE: Usage of NMCKEN and NMFMEN are:

Operation	NMCKEN	NMFMEN
Framed service	0	0
Unframed service	0	1
E1 loopback	1	1
E1 loss of signal (LOS) (where E1 framer doesn't provide clock in LOS)	1	1

Demux E1 Control Register

Address: 01
Abbreviation: DXE1CTL
Read/Write

Table 4: Demux E1 Control Register

Bit	Name	Default	Description
7	INVDXCK	0	Invert Demux E1 Output Clock. When High, the demux E1 data and frame mark signals are updated on the falling edge of E1CLKO. When this bit is Low, the data and frame mark are updated on the rising edge.
6	E1LB	0	E1 Loopback. When High, both directions of the E1 NRZ clock, data, and frame mark are looped back. When Low, normal operation is enabled.
5	TMGSRC1	0	Demux E1 Timing Source Select. These two bits can select the ADPLL output or nominal clock as E1CLK0. 00: dependent on the status of input pins LOSWx and software setting in LPCTL register. The loop with first inactive LOSW status will be selected. If all LOSWx are active, force to nominal clock. 01: force to loop 1 10: force to loop 2 11: force to loop 3
4	TMGSRC0	0	
3	DXAIS3	0	Demux Loop 3 AIS Enable. When High, the demux Loop 3 payload is forced to all ones. When Low, normal operation is enabled.
2	DXAIS2	0	Demux Loop 2 AIS Enable. When High, the demux Loop 2 payload is forced to all ones. When Low, normal operation is enabled.
1	DXAIS1	0	Demux Loop 1 AIS Enable. When High, the demux Loop 1 payload is forced to all ones. When Low, normal operation is enabled.
0	EXTDAIS	1	External Demux AIS Enable. When High, the LOSW1 input pin is enabled to force the demux Loop 1 payload to all ones, LOSW2 input pin is enabled to force the demux Loop 2 payload to all ones, and LOSW3 input pin is enabled to force the demux Loop 3 payload to all ones. When EXTDAIS is Low, external demux AIS insertion is disabled.

HDSL Loop Control Register

Address: 02
Abbreviation: LPCTL
Read/Write

Table 5: HDSL Loop Control Register

Bit	Name	Default	Description
7	n/a	0	Not used; Always read Low.
6	HDSLLB	0	HDSL Loopback Enable. When High, both directions of the Loop 1, Loop 2 and Loop 3 frame mark and data signals are looped back. When Low, all HDSL loopbacks are disabled.
5	LOSW3C1	0	LOSW3 S/W Control Normal Operation: 0x Force to Active: 10 Force to Inactive: 11
4	LOSW3C0	0	
3	LOSW2C1	0	LOSW2 S/W Control Normal Operation: 0x Force to Active: 10 Force to Inactive: 11
2	LOSW2C0	0	
1	LOSW1C1	0	LOSW1 S/W Control Normal Operation: 0x Force to Active: 10 Force to Inactive: 11
0	LOSW1C0	0	

HDSL Loop 1 Overhead Control Register

Address: 03
Abbreviation: L1OHCTL
Read/Write

Table 6: HDSL Loop 1 Overhead Control Register

Bit	Name	Default	Description
7	n/a	0	Not used; Always read Low.
6	L1FEBE	0	Mux Loop 1 FEBE Inject (Single-bit). A Low-to-High transition on this bit causes the mux Loop 1 FEBE overhead bit to be activated for one frame. After the FEBE bit has been inserted, this control bit is automatically cleared. The FEBE bit is also activated each time a demux CRC error is detected (on either loop).
5	L1BPV	0	Mux Loop 1 BPV Error Inject (Single-bit). A Low-to-High transition on this bit causes the mux Loop 1 BPV overhead bit to be activated for one frame. After the BPV bit has been transmitted, this control bit is automatically cleared. The mux BPV indicator bit can also be activated by the BPV input pin.
4	L1CRCE	0	Mux Loop 1 CRC Error Inject (Continuous). When High, a continuous error is injected in the mux Loop 1 CRC code until this bit is cleared by the microprocessor.
3	L1LOSD	0	Mux Loop 1 LOSD Alarm Activate. When High, the mux Loop 1 LOSD alarm overhead bit is activated until this bit is reset by the microprocessor. When Low, the LOSD alarm bits are still sent when LOSD input pin is active.
2	L1HRP	0	Mux Loop 1 HDSL Repeater Present Control. When High, the mux Loop 1 HRP overhead bit is activated until this bit is reset by the microprocessor.
1	L1PS1	0	Mux Loop 1 Power Status Bit #1 Control. When High, the mux Loop 1 PS1 overhead bit is activated until this bit is reset by the microprocessor.
0	L1PS2	0	Mux Loop 1 Power Status Bit #2 Control. When High, the mux Loop 1 PS2 overhead bit is activated until this bit is reset by the microprocessor.

NOTE: Although the HDSL overhead indicator bits are active Low on the HDSL data stream, all control bits in this register are active High, i.e., the overhead control bits are inverted before they are transmitted on the loop.

HDSL Loop 2 Overhead Control Register

Address: 04
Abbreviation: L2OHCTL
Read/Write

Table 7: HDSL Loop 2 Overhead Control Register

Bit	Name	Default	Description
7	n/a	0	Not used; Always read Low.
6	L2FEBE	0	Mux Loop 2 FEBE Inject (Single-bit). A Low-to-High transition on this bit causes the mux Loop 2 FEBE overhead bit to be activated for one frame. After the FEBE bit has been inserted, this control bit is automatically cleared. The FEBE bit is also activated each time a demux CRC error is detected (on either loop).
5	L2BPV	0	Mux Loop 2 BPV Error Inject (Single-bit). A Low-to-High transition on this bit causes the mux Loop 2 BPV overhead bit to be activated for one frame. After the BPV bit has been transmitted, this control bit is automatically cleared. The BPV indicator can also be activated by the microprocessor.
4	L2CRCE	0	Mux Loop 2 CRC Error Inject (Continuous). When High, a continuous error is injected in the mux Loop 1 CRC code until this bit is cleared by the microprocessor.
3	L2LOSD	0	Mux Loop 2 LOSD Alarm Activate. When High, the mux Loop 2 LOSD alarm overhead bit is activated until this bit is reset by the microprocessor. When Low, the LOSD alarm is sent if the LOSD input pin is active.
2	L2HRP	0	Mux Loop 2 HDSL Repeater Present Control. When High, the mux Loop 2 HRP overhead bit is activated until this bit is reset by the microprocessor.
1	L2PS1	0	Mux Loop 2 Power Status Bit #1 Control. When High, the mux Loop 2 PS1 overhead bit is activated until this bit is reset by the microprocessor.
0	L2PS2	0	Mux Loop 2 Power Status Bit #2 Control. When High, the mux Loop 2 PS2 overhead bit is activated until this bit is reset by the microprocessor.

NOTE: Although the HDSL overhead indicator bits are active Low on the HDSL data stream, all control bits in this register are active High, i.e., the overhead control bits are inverted before they are transmitted on the loop.

HDSL Loop 3 Overhead Control Register

Address: 05
Abbreviation: L3OHCTL
Read/Write

Table 8: HDSL Loop 3 Overhead Control Register

Bit	Name	Default	Description
7	n/a	0	Not used; Always read Low.
6	L3FEBE	0	Mux Loop 3 FEBE Inject (Single-bit). A Low-to-High transition on this bit causes the mux Loop 3 FEVE overhead bit to be activated for one frame. After the FEBE bit has been inserted, this control bit is automatically cleared. The FEBE bit is also activated each time a demux CRC error is detected (on either loop).
5	L3BPV	0	Mux Loop 3 BPV Error Inject (Single-bit). A Low-to-High transition on this bit causes the mux Loop 3 BPV overhead bit to be activated for one frame. After the BPV bit has been transmitted, this control bit is automatically cleared. The BPV indicator can also be activated by the microprocessor.
4	L3CRCE	0	Mux Loop 3 CRC Error Inject (Continuous). When High, a continuous error is injected in the mux Loop 1 CRC code until this bit is cleared by the microprocessor.
3	L3LOSD	0	Mux Loop 3 LOSD Alarm Activate. When High, the mux Loop 3 LOSD alarm overhead bit is activated until this bit is reset by the microprocessor. When Low, the LOSD alarm is sent if the LOSD input pin is active.
2	L3HRP	0	Mux Loop 3 HDSL Repeater Present Control. When High, the mux Loop 3 HRP overhead bit is activated until this bit is reset by the microprocessor.
1	L3PS1	0	Mux Loop 3 Power Status Bit #1 Control. When High, the mux Loop 3 PS1 overhead bit is activated until this bit is reset by the microprocessor.
0	L3PS2	0	Mux Loop 3 Power Status Bit #2 Control. When High, the mux Loop 3 PS2 overhead bit is activated until this bit is reset by the microprocessor.

NOTE: Although the HDSL overhead indicator bits are active Low on the HDSL data stream, all control bits in this register are active High, i.e., the overhead control bits are inverted before they are transmitted on the loop.

Time Slot Grouping Table Control Register

Address: 06
Abbreviation: TSCTL
Read/Write

Table 9: Time Slot Grouping Table Control Register

Bit	Name	Default	Description
7,6	n/a	0	Not used; Always read Low.
5	LPREN3	0	Loop Reversal Detection Enable. When High, enables loop 3 ID detection operation.
4	LPREN2	0	Loop Reversal Detection Enable. When High, enables loop 2 ID detection operation.
3	LPREN1	0	Loop Reversal Detection Enable. When High, enables loop 1 ID detection operation.
2	SWAPEN	0	Preferred Loop Enable. When High, time slot tables of Loop 1 and Loop 2 are swapped.
1	LDTABLE	0	Load Time Slot Grouping Table. When High, time slot grouping tables are loaded into Mux and Demux blocks and the bit is cleared automatically.
0	FULLE1	0	Full E1/Fractional E1 Control. When High, fractional E1 application is selected. When Low, full E1 is selected.

HDSL Loop 1 Time Slot Control Byte (12 bytes)

Address: 07
Abbreviation: L1TSCTL1
Read/Write

Table 10: Loop 1 Time Slot Control Byte 1

Bit	Name	Default	Description
7	TSG0	1	Loop 1 Time Slot Grouping (Byte 1). Each bit that is set Low blocks transmission of the corresponding DS0 channel in the mux E1 by forcing its bits to idle code.
6	TSG1	1	
5	TSG2	0	
4	TSG3	1	
3	TSG4	0	
2	TSG5	1	
1	TSG6	0	
0	TSG7	1	

Address: 08
Abbreviation: L1TSCTL2
Read/Write

Table 11: Loop 1 Time Slot Control Byte 2

Bit	Name	Default	Description
7	TSG8	0	Loop 1 Time Slot Grouping (Byte 2). Each bit that is set Low blocks transmission of the corresponding DS0 channel in the mux E1 by forcing its bits to idle code.
6	TSG9	1	
5	TSG10	0	
4	TSG11	1	
3	TSG12	0	
2	TSG13	1	
1	TSG14	0	
0	TSG15	1	

Address: 09
Abbreviation: L1TSCTL3
Read/Write

Table 12: Loop 1 Time Slot Control Byte 3

Bit	Name	Default	Description
7	TSG16	1	Loop 1 Time Slot Grouping (Byte 3). Each bit that is set Low blocks transmission of the corresponding DS0 channel in the mux E1 by forcing its bits to idle code.
6	TSG17	0	
5	TSG18	1	
4	TSG19	0	
3	TSG20	1	
2	TSG21	0	
1	TSG22	1	
0	TSG23	0	

Address: 0A
Abbreviation: L1TSCTL4
Read/Write

Table 13: Loop 1 Time Slot Control Byte 4

Bit	Name	Default	Description
7	TSG24	1	Loop 1 Time Slot Grouping (Byte 4). Each bit that is set Low blocks transmission of the corresponding DS0 channel in the mux E1 by forcing its bits to idle code.
6	TSG25	0	
5	TSG26	1	
4	TSG27	0	
3	TSG28	1	
2	TSG29	0	
1	TSG30	1	
0	TSG31	0	

Address: 0B
Abbreviation: L2TSCTL1
Read/Write

Table 14: Loop 2 Time Slot Control Byte 1

Bit	Name	Default	Description
7	TSG0	1	Loop 2 Time Slot Grouping (Byte 1). Each bit that is set Low blocks transmission of the corresponding DS0 channel in the mux E1 by forcing its bits to idle code.
6	TSG1	0	
5	TSG2	1	
4	TSG3	0	
3	TSG4	1	
2	TSG5	0	
1	TSG6	1	
0	TSG7	0	

Address: 0C
Abbreviation: L2TSCTL2
Read/Write

Table 15: Loop 2 Time Slot Control Byte 2

Bit	Name	Default	Description
7	TSG8	1	Loop 2 Time Slot Grouping (Byte 2). Each bit that is set Low blocks transmission of the corresponding DS0 channel in the mux E1 by forcing its bits to idle code.
6	TSG9	0	
5	TSG10	1	
4	TSG11	0	
3	TSG12	1	
2	TSG13	0	
1	TSG14	1	
0	TSG15	0	

Address: 0D
Abbreviation: L2TSCTL3
Read/Write

Table 16: Loop 2 Time Slot Control Byte 3

Bit	Name	Default	Description
7	TSG16	1	Loop 2 Time Slot Grouping (Byte 3). Each bit that is set Low blocks transmission of the corresponding DS0 channel in the mux E1 by forcing its bits to idle code.
6	TSG17	1	
5	TSG18	0	
4	TSG19	1	
3	TSG20	0	
2	TSG21	1	
1	TSG22	0	
0	TSG23	1	

Address: 0E
Abbreviation: L2TSCTL4
Read/Write

Table 17: Loop 2 Time Slot Control Byte 4

Bit	Name	Default	Description
7	TSG24	0	Loop 2 Time Slot Grouping (Byte 4). Each bit that is set Low blocks transmission of the corresponding DS0 channel in the mux E1 by forcing its bits to idle code.
6	TSG25	1	
5	TSG26	0	
4	TSG27	1	
3	TSG28	0	
2	TSG29	1	
1	TSG30	0	
0	TSG31	1	

Address: 0F
Abbreviation: L3TSCTL1
Read/Write

Table 18: Loop 3 Time Slot Control Byte 1

Bit	Name	Default	Description
<7:0>	TSG<0:7>	0	Loop 3 Time Slot Grouping (Byte 1). Each bit that is set Low blocks transmission of the corresponding DS0 channel in the mux E1 by forcing its bits to idle code.

Address: 10
Abbreviation: L3TSCTL2
Read/Write

Table 19: Loop 3 Time Slot Control Byte 2

Bit	Name	Default	Description
<7:0>	TSG<8:15>	0	Loop 3 Time Slot Grouping (Byte 2). Each bit that is set Low blocks transmission of the corresponding DS0 channel in the mux E1 by forcing its bits to idle code.

Address: 11
Abbreviation: L3TSCTL3
Read/Write

Table 20: Loop 3 Time Slot Control Byte 3

Bit	Name	Default	Description
<7:0>	TSG<16:23>	0	Loop 3 Time Slot Grouping (Byte 3). Each bit that is set Low blocks transmission of the corresponding DS0 channel in the mux E1 by forcing its bits to idle code.

Address: 12
Abbreviation: L3TSCTL4
Read/Write

Table 21: Loop 3 Time Slot Control Byte 4

Bit	Name	Default	Description
<7:0>	TSG<24:31>	0	Loop 3 Time Slot Grouping (Byte 4). Each bit that is set Low blocks transmission of the corresponding DS0 channel in the mux E1 by forcing its bits to idle code.

Programmable Idle Code Byte

Address: 13
Abbreviation: IDLECODE
Read/Write

Table 22: Programmable Idle Code Bytes

Bit	Name	Default	Description
<7:0>	IDLE<7:0>	FFh	Programmable Idle Code. This 8 bit code contains the byte used for channel blocking. IDLE7 is the MSB and the first bit of E1 channel shifted out.

QRSS Test Pattern Control

Address: 14
Abbreviation: PATCTL
Read/Write

Table 23: QRSS Test Pattern Control Register

Bit	Name	Default	Description
7, 6	n/a	0	Not used; Always read Low.
5	PATEN3	0	Loop 3 Test Pattern Generation/Detection Enable. When High, the internal pattern is inserted into the mux HDSL payload. When Low, the incoming mux E1 is inserted.
4	PATEN2	0	Loop 2 Test Pattern Generation/Detection Enable. When High, the internal pattern is inserted into the mux HDSL payload. When Low, the incoming mux E1 is inserted.
3	PATEN1	0	Loop 1 Test Pattern Generation/Detection Enable. When High, the internal pattern is inserted into the mux HDSL payload. When Low, the incoming mux E1 is inserted.
2	PATERRI3	0	Loop 3 Test Pattern Error Injection. When High, one bit error is injected into loop payload. When Low, error injection is disabled. After two frame pulses occurs, this bit is cleared.
1	PATERRI2	0	Loop 2 Test Pattern Error Injection. When High, one bit error is injected into loop payload. When Low, error injection is disabled. After two frame pulses occurs, this bit is cleared.
0	PATERRI1	0	Loop 1 Test Pattern Error Injection. When High, one bit error is injected into loop payload. When Low, error injection is disabled. After two frame pulses occurs, this bit is cleared.

Frame Pulse Sync & PLL Control Register

Address: 15
Abbreviation: FMSYNC_PLLCTL
Read/Write

Table 24: Frame Pulse Sync & PLL Control Register

Bit	Name	Default	Description
<7:5>	n/a	0	Not used; Always read Low.
4	SYNCEN	1	Loops Alignment Enable. When High, this bit enables synchronization of the HDSL frames.
3	SYNCFM[1]	0	Frame Pulse Synchronization Select: 00: No frame synchronization 01: Sync with Loop 1 frame pulse 10: Sync with Loop 2 frame pulse 11: Sync with Loop 3 frame pulse
2	SYNCFM[0]	1	
1	E1CLKSRC	0	E1 Clock Source Select; 1 = External Timing Source; 0 = Internal Timing Source.
0	LOCKSEL	0	PLL Locking Time Select; 1 = Slow locking time; 0 = Fast locking time.

Test Pattern Error Counter Status Register

All of the HDSL overhead status bits in this register are latched active High when detected, and remain High until a write is done by the microprocessor.

Address: 16
Abbreviation: PATSTAT
Read/Write

Table 25: Test Pattern Error Counter Status Register

Bit	Name	Default	Description
<7:6>	n/a	0	Not used; Always read Low.
<5:3>	OVERFLOW<3:1>	0	Loop <3:1> Test Pattern Error Counter Status. When High, Pattern Error Counter has overflowed.
<2:0>	PATLOS<3:1>	0	Loop <3:1> Sync Pattern Detector Status. When High, Pattern Sync is lost.

Demux Power Status Register

Address: 17
Abbreviation: DXPSSTAT
Read/Write

Table 26: Demux Power Status Register

Bit	Name	Default	Description
<7:6>	n/a	0	Not used; Always read Low.
5	DL3PS1	0	Demux Loop3 power status bit #1.
4	DL3PS2	0	Demux Loop3 power status bit #2.
3	DL2PS1	0	Demux Loop2 power status bit #1.
2	DL2PS2	0	Demux Loop2 power status bit #2.
1	DL1PS1	0	Demux Loop 1 power status bit #1.
0	DL1PS2	0	Demux Loop 1 power status bit #2.

All of the HDSL overhead status bits in this register are latched active High when detected, and remain High until a write is done by the microprocessor.

NOTE: Although the HDSL overhead indicator bits are active Low on the HDSL data stream, all status bits in this register are active High, i.e., the status bits are inverted from what was received on the loop.

Demux HDSL Repeater Present Status Register

Address: 18
Abbreviation: DXHRPSTAT
Read/Write

Table 27: Demux HDSL Repeater Present Status Register

Bit	Name	Default	Description
<7:3>	n/a	0	Not used; Always read Low.
<2:0>	D<3:1>HRP	0	Demux loop<3:1> HDSL Repeater present status bit.

NOTE: Although the HDSL overhead indicator bits are active Low on the HDSL data stream, all status bits in this register are active High, i.e., the status bits are inverted from what was received on the loop.

Demux Loss of Signal Status Register

Address: 19
Abbreviation: DXLOSDSTAT
Read/Write

Table 28: Demux Loss of Signal Status Register

Bit	Name	Default	Description
<7:3>	n/a	0	Not used; Always read Low.
<2:0>	D<3:1>LOSD	0	Demux loop<3:1> loss of signal status bit.

All of the HDSL overhead status bits in this register are latched active High when detected, and remain High until a write of a logic one is done by the microprocessor.

NOTE: Although the HDSL overhead indicator bits are active Low on the HDSL data stream, all status bits in this register are active High, i.e., the status bits are inverted from what was received on the loop.

Loop Reversal Status Register

Address: 1A
Abbreviation: LPRSTAT
Read/Write

Table 29: Loop Reversal Status Register

Bit	Name	Default	Description
7, 6	n/a	0	Not used; Always read zero.
5	LPRDONE3	0	Loop Reversal Detect. When in HTUC Mode (LTU = 1), Loop *x* has detected the loop identification returned from HTUR. In HTUR Mode (LTU = 0), Loop *x* has detected the same loop identification three times, and the Loop *x* reversal is done.
4	LPRDONE2	0	
3	LPRDONE1	0	
2	LPREV[2]	0	000: Directs Loop 1 data to Loop 1 buffer and Loop 2 data to Loop 2 buffer. 001: Directs Loop 1 data to Loop 2 buffer and Loop 2 data to Loop 1 buffer. 010: Directs Loop 1 data to Loop 2 buffer and Loop 2 data to Loop 3 buffer. 011: Directs Loop 1 data to Loop 3 buffer and Loop 2 data to Loop 2 buffer. 100: Directs Loop 1 data to Loop 3 buffer and Loop 2 data to Loop 1 buffer. 101: Directs Loop 1 data to Loop 1 buffer and Loop 2 data to Loop 3 buffer.
1	LPREV[1]	0	
0	LPREV[0]	0	

General Interrupt Enable Register

Address: 1B
Abbreviation: GENINTEN
Read/Write

Table 30: General Interrupt Enable Register

Bit	Name	Default	Description
7	n/a	0	Not used; Always read Low.
6	EIPATLOS	0	Enable interrupt on pattern sync loss.
5	EIECOVR	0	Enable Interrupt on pattern error counter overflow.
4	EILOSD	0	Enable interrupt on demux loop 1 or loop 2 or loop 3 LOSD.
3	EIPS	0	Enable interrupt on demux loop power status indication.
2	EIL3INDC_R	0	Enable interrupt on demux loop 3 indc/indr bit active.
1	EIL2INDC_R	0	Enable interrupt on demux loop 2 indc/indr bit active.
0	EIL1INDC_R	0	Enable interrupt on demux loop 1 indc/indr bit active.

General Interrupt Vector Status

All of the HDSL overhead status bits in this register are latched active High when detected, and remain High until a write is done by the microprocessor. When a logic '1' is written to these registers, these status bits are cleared unless the associated overhead bit is still active.

Address: 1C
Abbreviation: GENINTSTAT
Read/Write

Table 31: General Interrupt Status Register

Bit	Name	Default	Description
7	n/a	0	Not used; Always read Low.
6	IVPATLOS	0	Pattern sync loss.
5	IVECOVR	0	Pattern error counter overflow.
4	IVLOSD	0	Demux loop 1 or loop 2 or loop 3 LOSD.
3	IVPS	0	Demux loops PS1 or PS2 indication.
2	IVL3INDC_R	0	Demux loop 3 indc/r bit active, new event.
1	IVL2INDC_R	0	Demux loop 2 indc/r bit active, new event.
0	IVL1INDC_R	0	Demux loop 1indc/r bit active, new event.

NOTE: $\overline{\text{INTGEN}}$ interrupt pin corresponds to the interrupt of PATLOS, ECOVR, LOSD, PS, UIB status bits in the GENINSTAT register and the INDC/R status bits in IND_3EOCSTAT register.

6MS Interrupt Enable Register

Address: 1D
Abbreviation: 6MSINTEN
Read/Write

Table 32: 6ms Interrupt Enable Register

Bit	Name	Default	Description
<7:6>	n/a	0	Not used; Always read Low.
5	EIMX36MS	0	Enable interrupt on loop 3 mux 6ms interrupt.
4	EIMX26MS	0	Enable interrupt on loop 2 mux 6ms interrupt.
3	EIMX16MS	0	Enable interrupt on loop 1 mux 6ms interrupt.
2	EIDX36MS	0	Enable interrupt on loop 3 demux 6ms interrupt.
1	EIDX26MS	0	Enable interrupt on loop 2 demux 6ms interrupt.
0	EIDX16MS	0	Enable interrupt on loop 1 demux 6ms interrupt.

6MS Interrupt Vector Status

When a logic ‘1’ is written to these registers, these status bits are cleared unless the associated overhead bit is still active.

Address: 1E
Abbreviation: 6MSINTSTAT
Read/Write

Table 33: 6ms Interrupt Status Register

Bit	Name	Default	Description
<7:6>	n/a	0	Not used; Always read Low.
5	L3MX6MS	0	Loop 3 mux 6ms interrupt.
4	L2MX6MS	0	Loop 2 mux 6ms interrupt.
3	L1MX6MS	0	Loop 1 mux 6ms interrupt.
2	L3DX6MS	0	Loop 3 demux 6ms interrupt.
1	L2DX6MS	0	Loop 2 demux 6ms interrupt.
0	L1DX6MS	0	Loop 1 demux 6ms interrupt.

NOTE: $\overline{\text{INT6MS}}$ interrupt pin corresponds to the interrupt of Mux and Demux 6MS status bits in the 6MSINTSTAT register and triple-echo EOC status bits in IND_3EOCSTAT register.

Indicator and Triple Echo EOC Interrupt Enable Register

Address: 1F
Abbreviation: IND_3EOCINTEN
Read/Write

Table 34: Indicator Bits & Triple Echo EOC Enable Register

Bit	Name	Default	Description
<7:6>	n/a	0	Not used; Always read zero.
<5:3>	EIL<3:1>INDCR	0	Enable interrupt on loop <3:1> ready to receive indicator bit.
<2:0>	EIL<3:1>CMP	0	Enable Interrupt on Loop <3:1> EOC Triple-Echo Message Compare. When High, in addition to enabling the Triple-Echo Message interrupt, the integrated EOC message (which is updated only when a Triple_Echo message is valid) is output. When Low, the non-integrated EOC message (updated every 6 ms) is sent to the receive EOC message register on each loop.

Indicator and Triple Echo EOC Interrupt Status Register

When a logic '1' is written to these registers, these status bits are cleared unless the associated overhead bit is still active.

Address: 20
Abbreviation: IND_3EOCINTSTAT
Read/Write

Table 35: Indicator Bits & Triple EOC Status Register

Bit	Name	Default	Description
<7:6>	n/a	0	Not used; Always read zero.
<5:3>	L<3:1>INDCR	0	Loop <3:1> Ready to Receive Indicator. This status bit is active to indicate to the distant HDSL transceiver that it is ready to receive data.
<2:0>	L<3:1>EOCCMP	0	Loop <3:1> EOC Triple-Echo Message Compare Detected. This status bit is active only when a new message has been received three consecutive times.

Global Control Register

Address: 21
Abbreviation: GLBCTL
Read/Write

Table 36: Global Control Register

Bit	Name	Default	Description
7	n/a	0	Not used; always read zero.
6	LP_CFG[1]	0	HDSL loop configuration for fractional E1 application at central office side. These two bits will control the relationship of DX three data buffer's restart. 00: loops 1, 2 coming from the same remote terminal. 01: loops 1, 3 coming from the same remote terminal. 10: loops 2, 3 coming from the same remote terminal. 11: 3 loops coming from 3 different remote terminals.
5	LP_CFG[0]	0	
4	E1DTLB	0	E1 Data Loopback Enable for fractional E1. When High, both input/ output directions of the E1 NRZ data are loopback, but not the E1 clock or frame pulse. When Low, normal operation.
3	E1FMSEL	0	E1 Framer Select. 0 = Select DS2143; 1 = Select DS2181. If 0, E1FRM0 and E1FRM1 coincide with the first bit of time slot 0 for E1DAT0 and E1DATI respectively. If 1, E1FRM0 and E1FRMI coincide with the last bit of time slot 31 for E1DAT0 and E1DATI respectively.
2	THMODEN	1	1 = Threshold Modulation Enable. 0 = Threshold Modulation Disable.
<1:0>	TMGSTAT	0	Indicates the DX E1 clock loop source status. 00: loop 1 01: loop 2 10: loop 3

PLL Band Width Control Registers (2 bytes)

Address: 22
Abbreviation: PLL_BWH
Read/Write

Table 37: PLL Band Width Control (High Byte)

Bit	Name	Default	Description
<7:0>	PLL_BWH	FC	PLL locking time register High byte. For values greater than 80h, longer locking time to low end frequency, with lower jitter amplitude.

Address: 23
Abbreviation: PLL_BWL
Read/Write

Table 38: PLL Band Width Control (Low Byte)

Bit	Name	Default	Description
<7:0>	PLL_BWL	03	PLL locking time register Low byte. For values less than 80h, longer locking time to High end frequency, with lower jitter amplitude.

Demux Restart Counter Register

Address: 24
Abbreviation: DXRSCNTR
Read only

Table 39: Demux Restart Counter

Bit	Name	Default	Description
<7:0>	n/a	0	E1 Demux Restart Counter. Increments each time the E1 demux loop has been restarted. Primarily used for manufacture testing.

Mux Loop 1 Z Bit Registers (6 Bytes)

Address: 25
Abbreviation: MXL1Z1
Read/Write

Table 40: Mux Loop 1 Z Bits (LSB)

Bit	Name	Default	Description
<7:0>	Z<1:8>	FF	Mux Loop 1 Z bit <1:8>

Address: 26
Abbreviation: MXL1Z2
Read/Write

Table 41: Mux Loop 1 Z Bits

Bit	Name	Default	Description
<7:0>	Z<9:16>	FF	Mux Loop 1 Z bit <9:16>

Address: 27
Abbreviation: MXL1Z3
Read/Write

Table 42: Mux Loop 1 Z Bits

Bit	Name	Default	Description
<7:0>	Z<17:24>	FF	Mux Loop 1 Z bit <17:24>

Address: 28
Abbreviation: MXL1Z4
Read/Write

Table 43: Mux Loop 1 Z Bits

Bit	Name	Default	Description
<7:0>	Z<25:32>	FF	Mux Loop 1 Z bit <25:32>

Address: 29
Abbreviation: MXL1Z5
Read/Write

Table 44: Mux Loop 1 Z Bits

Bit	Name	Default	Description
<7:0>	Z<33:40>	FF	Mux Loop 1 Z bit <33:40>

Address: 2A
Abbreviation: MXL1Z6
Read/Write

Table 45: Mux Loop 1 Z Bits (MSB)

Bit	Name	Default	Description
<7:0>	Z<41:48>	FF	Mux Loop 1 Z bit <41:48>

Mux Loop 1 EOC Transmit Message (2 bytes)

Address: 2B
Abbreviation: MXL1EOCH
Read/Write

Table 46: Mux Loop 1 EOC Message (High Byte)

Bit	Name	Default	Description
<7:5>	n/a	0	Not used; Always read Low.
<4:0>	EOC<1:5>	0	Mux Loop 1 EOC bit <1:5>

Address: 2C
Abbreviation: MXL1EOCL
Read/Write

Table 47: Mux Loop 1 EOC Message (Low Byte)

Bit	Name	Default	Description
<7:0>	EOC<6:13>	0	Mux Loop 1 EOC bit <6:13>

Mux Loop 1 User Indicator Bit Register

Address: 2D
Abbreviation: MXL1UIB
Read/Write

Table 48: Mux Loop 1 UIB Bits

Bit	Name	Default	Description
7	n/a	0	Not used; Always read Low.
6	RRBE	0	Mux loop 1 regenerator remote block error.
5	RCBE	0	Mux loop 1 regenerator central block error.
4	REGA	0	Mux loop 1 internal alarm bit in the regenerator.
3	RTA	0	Mux loop 1 remote terminal alarm.
2	INDC/R	0	Mux loop 1 ready to receive indicator at the LTU/NTU.
1	UIB1	0	Mux loop 1uib bit 1.
0	UIB2	0	Mux loop 1 uib bit 2.

Demux Loop 1 Z Bit Registers (6 Bytes)

Address: 2E
Abbreviation: DXL1Z1
Read

Table 49: Demux Loop 1 Z Bits (LSB)

Bit	Name	Default	Description
<7:0>	Z<1:8>	0	Demux Loop 1 Z bit <1:8>

Address: 2F
Abbreviation: DXL1Z2
Read

Table 50: Demux Loop 1 Z Bits

Bit	Name	Default	Description
<7:0>	Z<9:16>	0	Demux Loop 1 Z bit <9:16>

Address: 30
Abbreviation: DXL1Z3
Read

Table 51: Demux Loop 1 Z Bits

Bit	Name	Default	Description
<7:0>	Z<17:24>	0	Demux Loop 1 Z bit <17:24>

Address: 31
Abbreviation: DXL1Z4
Read

Table 52: Demux Loop 1 Z Bits

Bit	Name	Default	Description
<7:0>	Z<25:32>	0	Demux Loop 1 Z bit <25:32>

Address: 32
Abbreviation: DXL1Z5
Read

Table 53: Demux Loop 1 Z Bits

Bit	Name	Default	Description
<7:0>	Z<33:40>	0	Demux Loop 1 Z bit <33:40>

Address: 33
Abbreviation: DXL1Z6
Read

Table 54: Demux Loop 1 Z Bits (MSB)

Bit	Name	Default	Description
<7:0>	Z<41:48>	0	Demux Loop 1 Z bit <41:48>

Demux Loop 1 EOC Transmit Message (2 bytes)

Address: 34
Abbreviation: DXL1EOCH
Read

Table 55: Demux Loop 1 EOC Message (High Byte)

Bit	Name	Default	Description
<7:5>	n/a	0	Not used; Always read Low.
<4:0>	EOC<1:5>	0	Demux Loop 1 EOC bit <1:5>

Address: 35
Abbreviation: DXL1EOCL
Read

Table 56: Demux Loop 1 EOC Message (Low byte)

Bit	Name	Default	Description
<7:0>	EOC<6:13>	0	Demux Loop 1 EOC bit <6:13>

Demux Loop 1 User Indicator Bit Register

Address: 36
Abbreviation: DXL1UIB
Read

Table 57: Demux Loop 1 UIB Bits

Bit	Name	Default	Description
7	n/a	0	Not used; Always read Low.
6	RRBE	0	Demux loop 1 regenerator remote block error.
5	RCBE	0	Demux loop 1 regenerator central block error.
4	REGA	0	Demux loop 1 internal alarm bit in the regenerator.
3	RTA	0	Demux loop 1 remote terminal alarm.
2	INDC/R	0	Demux loop 1 ready to receive indicator at the LTU/NTU.
1	UIB1	0	Demux loop 1 UIB bit 1.
0	UIB2	0	Demux loop 1 UIB bit 2.

Demux Loop 1 CRC Error Counter

Address: 37
Abbreviation: DXL1CRCEC
Read

Table 58: Demux Loop 1 CRC Error Count

Bit	Name	Default	Description
<7:0>	CRC1EC<7:0>	0	Demux Loop 1 CRC Error Counter. This 8-bit counter increments each time one or more errors are detected on the demux Loop 1 CRC-6 bits. After a microprocessor read, the counter is cleared. This counter is disabled when the LOSW1 signal is High, and automatically stops at 0FFh to prevent overflow.

Demux Loop 1 FEBE Error Counter

Address: 38
Abbreviation: DXL1FEBEEC
Read

Table 59: Demux Loop 1 FEBE Error Count

Bit	Name	Default	Description
<7:0>	FEBE1EC<7:0>	0	Demux Loop 1 FEBE Error Counter. This 8-bit counter increments each time one or more errors are detected on the demux Loop 1 FEBE bits. After a microprocessor read, the counter is cleared. This counter is disabled when the LOSW1 signal is High, and automatically stops at 0FFh to prevent overflow.

Demux Loop 1 BPV Error Counter

Address: 39
Abbreviation: DXL1BPVEC
Read

Table 60: Demux Loop 1 BPV Error Count

Bit	Name	Default	Description
<7:0>	BPV1EC<7:0>	0	Demux Loop 1 BPV Error Counter. This 8-bit counter increments each time one or more errors are detected on the demux Loop 1 BPV bits. After a microprocessor read, the counter is cleared. This counter is disabled when the LOSW1 signal is High, and automatically stops at 0FFh to prevent overflow.

Loop 1 QRSS Test Pattern Error Counter (2 bytes)

Address: 3A
Abbreviation: L1PATECH
Read

Table 61: Loop 1 QRSS Test Pattern Error Counter (High byte)

Bit	Name	Default	Description
<7:0>	PAT1ECH <15:8>	0	Loop 1 Test Pattern Error Counter (High byte). This 16-bit counter increments each time the demux test pattern receiver detects a pattern error. When the upper byte is read, the current count of both bytes is latched and the counter is cleared. This counter is disabled when pattern sync is lost. This counter does not stop counting at 0FFFFh, however, a latched overflow status bit is provided in the General Interrupt Vector Status register.

Address: 3B
Abbreviation: L1PATECL
Read

Table 62: Loop 1 QRSS Test Pattern Error Counter (Low)

Bit	Name	Default	Description
<7:0>	PAT1ECL <7:0>		Loop 1 Test Pattern Error Counter (Low byte). The lower byte is latched when the upper byte is read. Therefore, this byte must be read last when reading the 16-bit Pattern Error Counter.

Loop 1 Mux Restart Counter

Address: 3C
Abbreviation: DX1RSCNTR
Read

Table 63: Loop 1 Mux Restart Counter

Bit	Name	Default	Description
<7:0>	n/a	0	Loop 1 Mux Restart Counter. Increments each time the Mux loop 1 has been restarted. Cleared when read and stops at FFh.

Mux Loop 2 Z Bit Register (6 Bytes)

Address: 45
Abbreviation: MXL2Z1
Read/Write

Table 64: Mux Loop 2 Z Bits (LSB)

Bit	Name	Default	Description
<7:0>	Z<1:8>	FF	Mux Loop 2 Z bit <1:8>

Address: 46
Abbreviation: MXL2Z2
Read/Write

Table 65: Mux Loop 2 Z Bits

Bit	Name	Default	Description
<7:0>	Z<9:16>	FF	Mux Loop 2 Z bit <9:16>

Address: 47
Abbreviation: MXL2Z3
Read/Write

Table 66: Mux Loop 2 Z Bits

Bit	Name	Default	Description
<7:0>	Z<17:24>	FF	Mux Loop 2 Z bit <17:24>

Address: 48
Abbreviation: MXL2Z4
Read/Write

Table 67: Mux Loop 2 Z Bits

Bit	Name	Default	Description
<7:0>	Z<25:32>	FF	Mux Loop 2 Z bit <25:32>

Address: 49
Abbreviation: MXL2Z5
Read/Write

Table 68: Mux Loop 2 Z Bits

Bit	Name	Default	Description
<7:0>	Z<33:40>	FF	Mux Loop 2 Z bit <33:40>

Address: 4A
Abbreviation: MXL2Z6
Read/Write

Table 69: Mux Loop 2 Z Bits (MSB)

Bit	Name	Default	Description
<7:0>	Z<41:48>	FF	Mux Loop 2 Z bit <41:48>

Mux Loop 2 EOC Transmit Message (2 bytes)

Address: 4B
Abbreviation: MXL2EOCH
Read/Write

Table 70: Mux Loop 2 EOC Message (High byte)

Bit	Name	Default	Description
<7:5>	n/a	0	Not used; Always read Low.
<4:0>	EOC<1:5>	0	Mux Loop 2 EOC bit <1:5>

Address: 4C
Abbreviation: MXL2EOCL
Read/Write

Table 71: Mux Loop 2 EOC Message (Low byte)

Bit	Name	Default	Description
<7:0>	EOC<6:13>	0	Mux Loop 2 EOC bit <6:13>

Mux Loop 2 User Indicator Bit Register

Address: 4D
Abbreviation: MXL2UIB
Read/Write

Table 72: Mux Loop 2 UIB Bits

Bit	Name	Default	Description
7	n/a	0	Not used; Always read Low.
6	RRBE	0	Mux loop 2 regenerator remote block error.
5	RCBE	0	Mux loop 2 regenerator central block error.
4	REGA	0	Mux Loop 2 internal alarm bit in the regenerator.
3	RTA	0	Mux loop 2 remote terminal alarm.
2	INDC/R	0	Mux loop 2 ready to receive indicator at the LTU/NTU.
1	UIB1	0	Mux loop 2 UIB bit 1.
0	UIB2	0	Mux loop 2 UIB bit 2.

Demux Loop 2 Z Bit Register (6 Bytes)

Address: 4E
Abbreviation: DXL2Z1
Read

Table 73: Demux Loop 2 Z Bits (LSB)

Bit	Name	Default	Description
<7:0>	Z<1:8>	0	Demux Loop 2 Z bit <1:8>

Address: 4F
Abbreviation: DXL2Z2
Read

Table 74: Demux Loop 2 Z Bits

Bit	Name	Default	Description
<7:0>	Z<9:16>	0	Demux Loop 2 Z bit <9:16>

Address: 50
Abbreviation: DXL2Z3
Read

Table 75: Demux Loop 2 Z Bits

Bit	Name	Default	Description
<7:0>	Z<17:24>	0	Demux Loop 2 Z bit <17:24>

Address: 51
Abbreviation: DXL2Z4
Read

Table 76: Demux Loop 2 Z Bits

Bit	Name	Default	Description
<7:0>	Z<25:32>	0	Demux Loop 2 Z bit <25:32>

Address: 52
Abbreviation: DXL2Z5
Read

Table 77: Demux Loop 2 Z Bits

Bit	Name	Default	Description
<7:0>	Z<33:40>	0	Demux Loop 2 Z bit <33:40>

Address: 53
Abbreviation: DXL2Z6
Read

Table 78: Demux Loop 2 Z Bits (MSB)

Bit	Name	Default	Description
<7:0>	Z<41:48>	0	Demux Loop 2 Z bit <41:48>

Demux Loop 2 EOC Transmit Message (2 bytes)

Address: 54
Abbreviation: DXL2EOCH
Read

Table 79: Demux Loop 2 EOC Message (High byte)

Bit	Name	Default	Description
<7:5>	n/a	0	Not used; Always read Low.
<4:0>	EOC<1:5>	0	Demux Loop 2 EOC bit <1:5>

Address: 55
Abbreviation: DXL2EOCL
Read

Table 80: Demux Loop 2 EOC Message (Low byte)

Bit	Name	Default	Description
<7:0>	EOC<6:13>	0	Demux Loop 2 EOC bit <6:13>

Demux Loop 2 User Indicator Bit Register

Address: 56
Abbreviation: DXL2UIB
Read

Table 81: Demux Loop 2 UIB Bits

Bit	Name	Default	Description
7	n/a	0	Not used; Always read Low.
6	RRBE	0	DemuX loop 2 regenerator remote block error.
5	RCBE	0	Demux loop 2 regenerator central block error.
4	REGA	0	Demux loop 2 internal alarm bit in the regenerator.
3	RTA	0	Demux loop 2 remote terminal alarm.
2	INDC/R	0	Demux loop 2 ready to receive indicator at the LTU/NTU.
1	UIB1	0	Demux loop 2 UIB bit 1.
0	UIB2	0	Demux loop 2 UIB bit 2.

Demux Loop 2 CRC Error Counter

Address: 57
Abbreviation: DXL2CRCEC
Read

Table 82: Demux Loop 2 CRC Error Count

Bit	Name	Default	Description
<7:0>	CRC2EC<7:0>	0	Demux Loop 2 CRC Error Counter. This 8-bit counter increments each time one or more errors are detected on the demux Loop 2 CRC-6 bits. After a microprocessor read, the counter is cleared. This counter is disabled when the LOSW2 signal is High, and automatically stops at 0FFh to prevent overflow.

Loop 2 FEBE Error Counter

Address: 58
Abbreviation: DXL2FEBEEC
Read

Table 83: Demux Loop 2 FEBE Error Count

Bit	Name	Default	Description
<7:0>	FEBE2EC<7:0>	0	Demux Loop 2 FEBE Error Counter. This 8-bit counter increments each time one or more errors are detected on the demux Loop 2 FEBE bits. After a microprocessor read, the counter is cleared. This counter is disabled when the LOSW2 signal is High, and automatically stops at 0FFh to prevent overflow.

Loop 2 BPV Error Counter

Address: 59
Abbreviation: DXL2BPVEC
Read

Table 84: Demux Loop 2 BPV Error Count

Bit	Name	Default	Description
<7:0>	BPV2EC<7:0>	0	Demux Loop 2 BPV Error Counter. This 8-bit counter increments each time one or more errors are detected on the demux Loop 2 BPV bits. After a microprocessor read, the counter is cleared. This counter is disabled when the LOSW2 signal is High, and automatically stops at 0FFh to prevent overflow.

Loop 2 QRSS Test Pattern Error Counter (2 bytes)

Address: 5A
Abbreviation: L2PATECH
Read

Table 85: Loop 2 QRSS Test Pattern Error Counter (High byte)

Bit	Name	Default	Description
<7:0>	PAT2EC<15:8>	0	Loop 2 Test Pattern Error Counter (High byte). This 16-bit counter increments each time the demux test pattern receiver detects a pattern error. When the upper byte is read, the current count of both bytes is latched and the counter is cleared. This counter is disabled when pattern sync is lost. This counter does not stop counting at 0FFFFh, however, a latched overflow status bit is provided in the General Interrupt Vector Status register.

Address: 5B
Abbreviation: L2PATECL
Read

Table 86: Loop 2 QRSS Test Pattern Error Counter (Low byte)

Bit	Name	Default	Description
<7:0>	PAT2EC<7:0>	0	Loop 2 Test Pattern Error Counter (Low byte). The lower byte is latched when the upper byte is read. Therefore, this byte must be read last when reading the 16-bit Pattern Error Counter.

Loop 2 Mux Restart Counter Register

Address: 5C
Abbreviation: MX2RSCNTR
Read

Table 87: Loop 2 Mux Restart Counter

Bit	Name	Default	Description
<7:0>	n/a	0	Loop 2 mux restart counter. Increments each time the mux loop has been restarted.

Mux Loop 3 Z Bit Register (6 Bytes)

Address: 65
Abbreviation: MXL3Z1
Read/Write

Table 88: Mux Loop 3 Z Bits (LSB)

Bit	Name	Default	Description
<7:0>	Z<1:8>	FF	Mux Loop 3 Z bit <1:8>

Address: 66
Abbreviation: MXL3Z2
Read/Write

Table 89: Mux Loop 3 Z Bits

Bit	Name	Default	Description
<7:0>	Z<9:16>	FF	Mux Loop 3 Z bit <9:16>

Address: 67
Abbreviation: MXL3Z3
Read/Write

Table 90: Mux Loop 3 Z Bits

Bit	Name	Default	Description
<7:0>	Z<17:24>	FF	Mux Loop 3 Z bit <17:24>

Address: 68
Abbreviation: MXL3Z4
Read/Write

Table 91: Mux Loop 3 Z Bits

Bit	Name	Default	Description
<7:0>	Z<25:32>	FF	Mux Loop 3 Z bit <25:32>

Address: 69
Abbreviation: MXL3Z5
Read/Write

Table 92: Mux Loop 3 Z Bits

Bit	Name	Default	Description
<7:0>	Z<33:40>	FF	Mux Loop 3 Z bit <33:40>

Address: 6A
Abbreviation: MXL3Z6
Read/Write

Table 93: Mux Loop 3 Z Bits (MSB)

Bit	Name	Default	Description
<7:0>	Z<41:48>	FF	Mux Loop 3 Z bit <41:48>

Mux Loop 3 EOC transmit Message (2 bytes)

Address: 6B
Abbreviation: MXL3EOCH
Read/Write

Table 94: Mux Loop 3 EOC Message (High byte)

Bit	Name	Default	Description
<7:5>	n/a	0	Not used; Always read Low.
<4:0>	EOC<1:5>	0	Mux Loop 3 EOC bit <1:5>

Address: 6C
Abbreviation: MXL3EOCL
Read/Write

Table 95: Mux Loop 3 EOC Message (Low byte)

Bit	Name	Default	Description
<7:0>	EOC<6:13>	0	Mux Loop 3 EOC bit <6:13>

Mux Loop 3 User Indicator Bit Register

Address: 6D
Abbreviation: MXL3UIB
Read/Write

Table 96: Mux Loop 3 UIB Bits

Bit	Name	Default	Description
7	n/a	0	Not used; Always read Low.
6	RRBE	0	Mux loop 3 regenerator remote block error.
5	RCBE	0	Mux loop 3 regenerator central block error.
4	REGA	0	Mux loop 3 internal alarm bit in the regenerator.
3	RTA	0	Mux loop 3 remote terminal alarm.
2	INDC/R	0	Mux Loop 3 ready to receive indicator at the LTU/NTU.
1	UIB1	0	Mux loop 3 UIB bit 1.
0	UIB2	0	Mux loop 3 UIB bit 2.

Demux Loop 3 Z Bit Register (6 Bytes)

Address: 6E
Abbreviation: DXL3Z1
Read

Table 97: Demux Loop 3 Z Bits (LSB)

Bit	Name	Default	Description
<7:0>	Z<1:8>	0	Demux Loop 3 Z bit <1:8>

Address: 6F
Abbreviation: DXL3Z2
Read

Table 98: Demux Loop 3 Z Bits

Bit	Name	Default	Description
<7:0>	Z<9:16>	0	Demux Loop 3 Z bit <9:16>

Address: 70
Abbreviation: DXL3Z3
Read

Table 99: Demux Loop 3 Z Bits

Bit	Name	Default	Description
<7:0>	Z<17:24>	0	Demux Loop 3 Z bit <17:24>

Address: 71
Abbreviation: DXL3Z4
Read

Table 100: Demux Loop 3 Z Bits

Bit	Name	Default	Description
<7:0>	Z<25:32>	0	Demux Loop 3 Z bit <25:32>

Address: 72
Abbreviation: DXL3Z5
Read

Table 101: Demux Loop 3 Z Bits

Bit	Name	Default	Description
<7:0>	Z<33:40>	0	Demux Loop 3 Z bit <33:40>

Address: 73
Abbreviation: DXL3Z6
Read

Table 102: Demux Loop 3 Z Bits

Bit	Name	Default	Description
<7:0>	Z<41:48>	0	Demux Loop 3 Z bit <41:48>

Demux Loop 3 EOC Transmit Message (2 bytes)

Address: 74
Abbreviation: DXL3EOCH
Read

Table 103: Demux Loop 3 EOC Message (High byte)

Bit	Name	Default	Description
<7:5>	n/a	0	Not used; Always read Low.
<4:0>	EOC<1:5>	0	Demux Loop 3 EOC bit <1:5>

Address: 75
Abbreviation: DXL3EOCL
Read

Table 104: Demux Loop 3 EOC Message (Low byte)

Bit	Name	Default	Description
<7:0>	EOC<6:13>	0	Demux Loop 3 EOC bit <6:13>

Demux Loop 3 User Indicator Bit Register

Address: 76
Abbreviation: DXL3UIB
Read

Table 105: Demux Loop 3 UIB Bits

Bit	Name	Default	Description
7	n/a	0	Not used; Always read Low.
6	RRBE	0	Demux loop 1 regenerator remote block error.
5	RCBE	0	Demux loop 1 regenerator central block error.
4	REGA	0	Demux loop 1 internal alarm bit in the regenerator.
3	RTA	0	Demux loop 1 remote terminal alarm.
2	INDC/R	0	Demux loop 1 ready to receive indicator at the LTU/NTU.
1	UIB1	0	Demux loop 1 UIB bit 1.
0	UIB2	0	Demux loop 1 UIB bit 2.

Demux Loop 3 CRC Error Counter

Address: 77
Abbreviation: DXL3CRCEC
Read

Table 106: Demux Loop 3 CRC Error Count

Bit	Name	Default	Description
<7:0>	CRC3EC<7:0>	0	Demux Loop 3 CRC Error Counter. This 8-bit counter increments each time one or more errors are detected on the demux Loop 3 CRC-6 bits. After a microprocessor read, the counter is cleared. This counter is disabled when the LOSW3 signal is High, and automatically stops at 0FFh to prevent overflow.

Demux Loop 3 FEBE Error Counter

Address: 78
Abbreviation: DXL3FEBEEC
Read

Table 107: Demux Loop 3 FEBE Error Count

Bit	Name	Default	Description
<7:0>	FEBE3EC<7:0>	0	Demux Loop 3 FEBE Error Counter. This 8-bit counter increments each time one or more errors are detected on the demux Loop 3 FEBE bits. After a microprocessor read, the counter is cleared. This counter is disabled when the LOSW3 signal is High, and automatically stops at 0FFh to prevent overflow.

Loop 3 BPV Error Counter

Address: 79
Abbreviation: DXL3BPVEC
Read

Table 108: Demux Loop 3 BPV Error Count

Bit	Name	Default	Description
<7:0>	BPV3EC<7:0>	0	Demux Loop 3 BPV Error Counter. This 8-bit counter increments each time one or more errors are detected on the demux Loop 3 BPV bits. After a microprocessor read, the counter is cleared. This counter is disabled when the LOSW3 signal is High, and automatically stops at 0FFh to prevent overflow.

Loop 3 QRSS Test Pattern Error Counter (2 bytes)

Address: 7A
Abbreviation: L3PATECH
Read

Table 109: Loop 3 QRSS Test Pattern Error Counter (High byte)

Bit	Name	Default	Description
<7:0>	PAT3EC<15:8>	0	Loop 3 Test Pattern Error Counter (High byte). This 16-bit counter increments each time the demux test pattern receiver detects a pattern error. When the upper byte is read, the current count of both bytes is latched and the counter is cleared. This counter is disabled when pattern sync is lost. This counter does not stop counting at 0FFFFh, however, a latched overflow status bit is provided in the General Interrupt Vector Status register.

Address: 7B
Abbreviation: L3PATECL
Read

Table 110: Loop 3 QRSS Test Pattern Error Counter (Low byte)

Bit	Name	Default	Description
<7:0>	PAT3EC<7:0>	0	Loop 3 Test Pattern Error Counter (Low byte). The lower byte is latched when the upper byte is read. Therefore, this byte must be read last when reading the 16-bit Pattern Error Counter.

Loop 3 Mux Restart Counter Register

Address: 7C
Abbreviation: MX3RSCNTR
Read

Table 111: Loop 3 Mux Restart Counter

Bit	Name	Default	Description
<7:0>	n/a	0	Loop 3 mux restart counter. Increments each time the mux loop has been restarted.

HFMA Version Number

Address: 7D
Abbreviation: VER
Read

Table 112: HFMA Version Number

Bit	Name	Default	Description
<7:4>	n/a	1	Silicon version h11 for Version 1.1. Other values undefined at time of printing.
<3:0>	n/a	1	

Microprocessor Mode Testing Register For Mux

Address: 7E
Abbreviation: MXTEST
Read/Write

Table 113: Microprocessor Mode Testing Register for Mux

Bit	Name	Default	Description
<7:0>	n/a	0	Defined for manufacturing test only.

Microprocessor Mode Testing Register for Demux

Abbreviations: DXTEST
Address: 7F
Read/Write

Table 114: Microprocessor Mode Testing Register for Demux

Bit	Name	Default	Description
<7:0>	n/a	0	Defined for manufacturing test only.

APPLICATION INFORMATION

Target Applications

The LXP710 HDSL framer/mapper is primarily intended for transporting 2.048 MHz E1 traffic over two loop systems. The data can either be framed (primarily channelized voice), or unframed (primarily data transport). One end of a two-loop HDSL system is shown in Figure 6. E1 service supports 32 64-kbps channels. Details of how the 32 channels are structured can be found in the ITU G.704 document. Definition of the E1 signal is found in the ITU G.703 document.

An unframed data only transport system is shown is Figure 7. If no E1 framing signal is supplied, the HDSL system must be operated in a two line point-to-point mode. Point to multipoint operation is not possible in this mode. The system in Figure 6 can also support unframed operation by setting the LXP710 to unframed mode.

The LXP710 also supports a fractional service mode. Fractional service is defined to be when a customer NTU is supplied with less than 32 channels of service. The E1 signal delivered is still 2.048 kbps with the unused channels filled with an idle code. Multipoint operation is when two or more NTUs are supported (see Figure 8). A multipoint system always operates the loops in a fractional mode, while a fractional service can be one loop to one NTU. Fractional operation must always be in framed E1 mode. Unframed operation can not select which E1 channels go to the appropriate loops.

ETSI Compliant Operation

Many OEMs supply E1 transport systems that must meet the ETSI compliance found in ETR(ETS)-152. The LXP710 supports two loop full 2M E1 and three loop fractional operation. The LXP710 forms the E1 HDSL frame format in Table 115 for each loop and provides access to the overhead bits in all loops independently. This is necessary but not sufficient to make a piece of equipment ETSI compliant. Other issues involve the start up process between the LTU and NTU. The ETR (ETS) 152 document describes this process. Also see the SK70707/8 data sheet for how the data pump activation fits into the ETSI start-up mode. Please contact Level One's Telecom Marketing department for software in assisting developing an E1 HDSL system.

The CRC-6 calculation method used in the LXP710 has been revised in the Rev 1.3 silicon. The earlier revisions do detect CRC-6 errors, but included the stuffing bits, contrary to ETR-152. The new revision corrects this, and is automatically compatible with the older revisions. This is achieved by using the UIB1 bit. (See Table 105 on page 49)

The LTU is the master unit and is typically located in a CO facility, while the NTU is typically located in the CPE facility. In this document there are references to LTU (HTU-C). The LTU is an ETSI designation, where the HTU-C is an ANSI designation. The HTU-x references are given for those readers who may be more familiar with North American equipment nomenclature. Another common name for the LTU is the local unit and the NTU is also known as the remote unit.

User Definable HDSL Overhead Bits

ETSI specifications allocate overhead bits with the intent of command and control between the LTU (HTU-C) and NTU (HTU-R) units. The eoc bits are primarily used for this; plus three Z-bits for loop identification. The remaining 45 Z-bits per 6ms frame per loop are open for any use. This yields a 7.5 kbps channel per loop in both directions for data or low quality voice. If ETSI compliance is not needed, then the additional 13 eoc and 2 uib bits per frame bring this value to 10 kbps. This extra channel is accessible by the microprocessor with interrupts provided at the frame rate per loop to coordinate the writing to and reading of this channel. A point-to-point system could pair up these channels to provide a 15 kbps channel ETSI compliant, and a 20 kbps non ETSI compliant channel.

Figure 6: Two-Loop E1 HDSL System

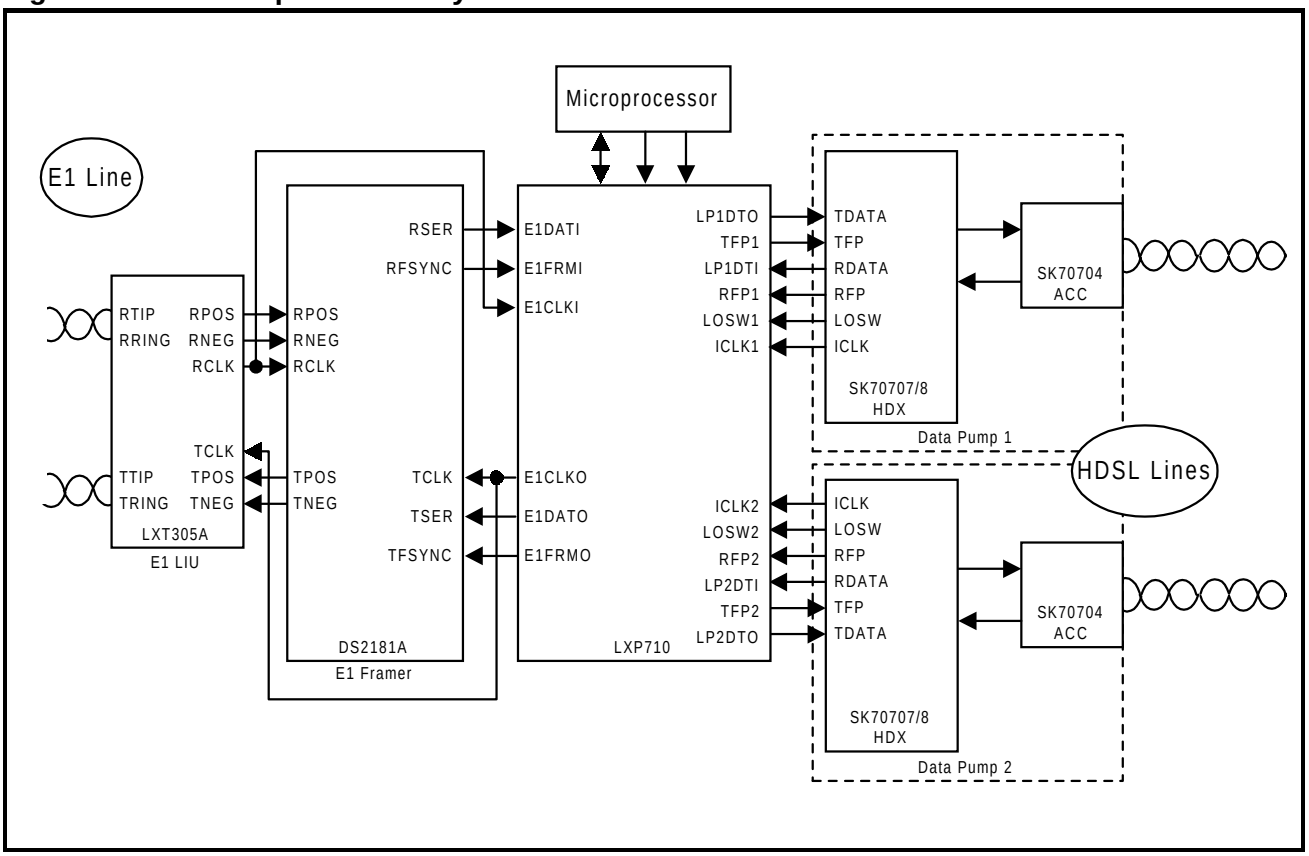


Figure 7: Unframed Data Transport Operation

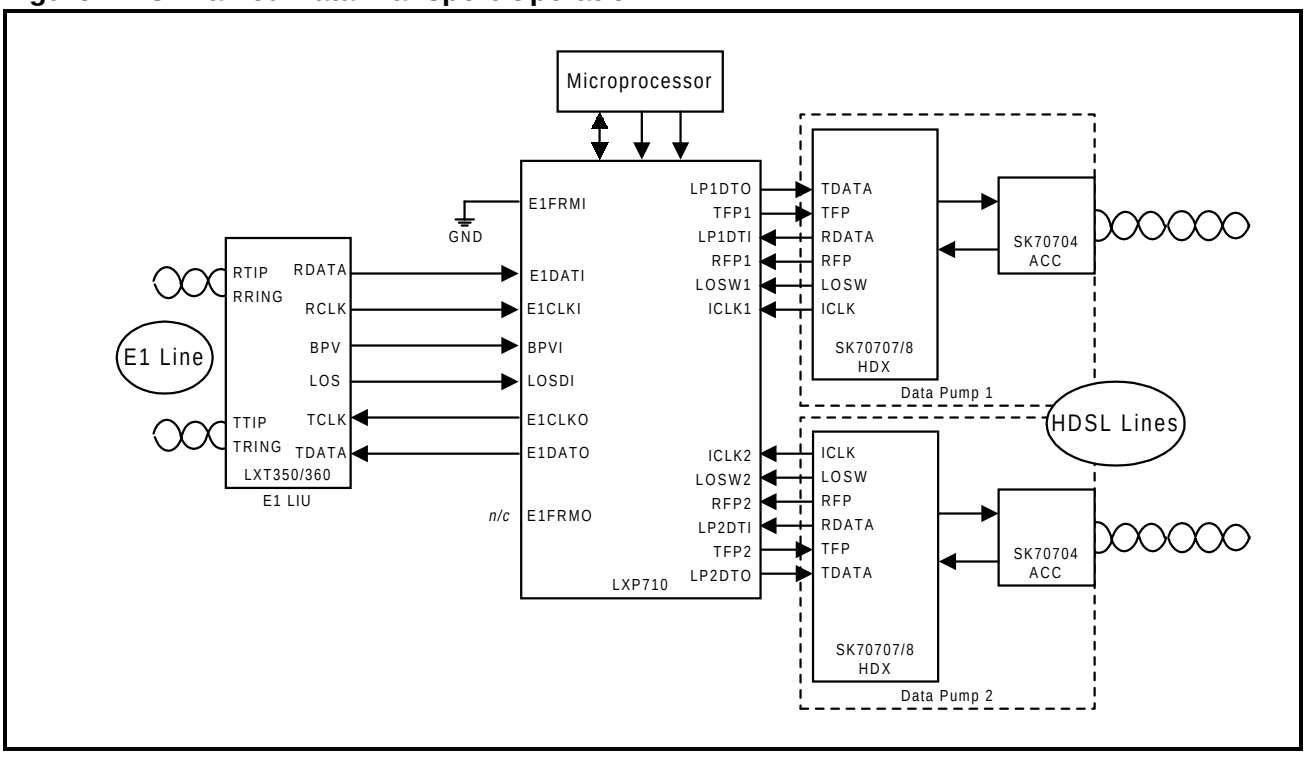
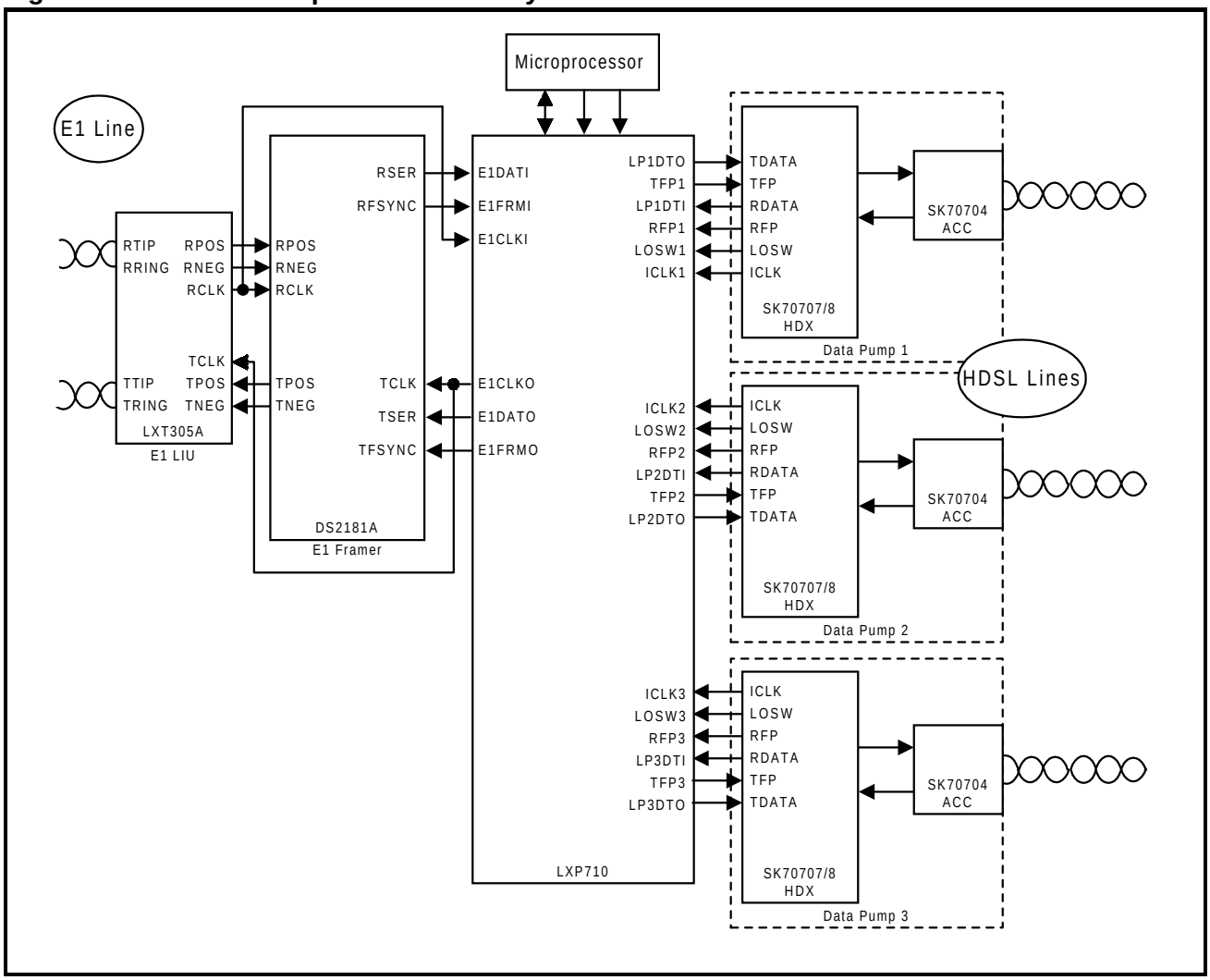


Figure 8: Point-to-Multipoint E1 HDSL System



System Software Guidelines

Many implementations of HDSL systems contain a microprocessor per board which controls the operation of one framer and up to three data pumps. This processor usually also communicates with another in the rack that contains the board. Though there are other possibilities, this is usually a good compromise of providing the necessary computing power and local control of the devices on the board. At first glance the software required run a HDSL system seems complex, but let's break it down to some operational modes. These modes can be: 1.) board initialization, 2.) loop activation, 3.) normal operation, 4.) diagnostic operation and 5.) external communication mode.

The following discussion outlines the major tasks needed for a HDSL system, but not all the details necessary for a complete system.

Board Initialization

This is usually the first code run which initializes the microprocessor which in turn writes the desired starting values to all the registers in the devices on the board. Configuration switches are read to determine whether the board is: a LTU or NTU unit, full 2M or fractional, etc.

After this phase is complete the LTU board can communicate with its master controller in the rack. This is necessary to receive channel configuration and report the status of the loop. The OEM can decide whether the LTU

should automatically activate the loops or wait for a explicit command from the rack controller.

Loop Activation

This phase prepares the loops to carry the payload, in this case E1 data. The data pumps must go through a sophisticated process of training the receivers for echo cancellation, channel equalization and level slicing adjustment. Fortunately Level One data pumps do this automatically by just setting the Activation Request bit in the Control register. When the Active State bit in the Status register is set, this process is complete. Interrupt generation can be used to free the processor from polling to determine completion. Level One data pumps also automatically detect and correct TIP/RING polarity reversal in the wire pair connection.

Once the data pumps are able to pass data, the framers take over to establish communication between the LTU and NTU. The first step is to establish that the loop wire pairs are connected correctly. The LTU sets Z-bits 1 - 3 to indicate loop identification. This is done by writing to the MX Z-bit registers. The NTU receives the loop IDs on the individual loops and checks to see if they are correct, if not then the NTU framer must switch the data paths internally to match and then set its MX loop ID back to the LTU when this process is complete. The loop reversal detect and switch can be done automatically in the LXP710 by setting the LPREN*x* bits in the TSCTL (06h) register during the board initialization phase.

The second step for each side to set its MX indc/r bit when it is ready to receive data.

The loop *x* time slot control bytes must be set. Default values can be stored at the LTU and NTU boards and loaded at power up. Alternately the LTU could receive the assignment from the rack master and, after receiving the indr bit from the NTU, send the configuration to the NTU using the unused Z-bits. Each loop could receive its assignment on its own loop. There is no standard for how the time slot assignments are made remotely so the OEM must take care to be consistent in future equipment designs to maintain interoperability.

Normal Operation

Payload data is transported to both sides in this mode.

Additionally this mode monitors the condition of the HDSL system. Operational characteristics such as signal-to-noise ratio (SNR), loss of signal (LOS) and CRC errors are tracked on each loop to anticipate problems. A LOSW from a data pump is a definite indication that the loop is malfunctioning and corrective action must be taken.

When symptoms indicate that corrective actions are needed, the HDSL system should make changes gracefully to minimize the effect on the E1 link. In the instance of HDSL loop failures the LTU should continually cycle through activation attempts, while the NTU should go QUIET, time-out and then wait for the LTU activation sequence. In instances of local lightning or a cable is cut, the system can recover on its own when the lightning transient dies down, or when the cable is spliced.

Point-to-point systems can program LXP710's automatic loop swap feature to maintain operation of selected E1 channels on a surviving loop when the primary loop is cut.

In rack systems, the LTU should report abnormalities to the rack master. Local unit problems can be defined in terms of errors from either the local E1 or HDSL interface. Remote units can also experience errors. The NTU needs to set the appropriate bits in the HDSL loop. The rta, remote terminal alarm, bit can be used when no other bit is appropriate. Then the LTU can interrogate the NTU through the eoc bits to determine the problem.

The ETR (ETS) 152 defines the eoc protocol and certain actions to be performed, but leaves open many register definitions. Again OEM implementations will differ.

Diagnostic Operation

The diagnostic mode is used when a system is installed to ensure proper operation or to troubleshoot an operational system. The LTU and NTU can be put into loopback modes to isolate sections of the system for performance measurement or troubleshooting. Payload transport operation is shut off or limited in this mode. A HDSL system should be designed to minimize the impact on a properly operating loop when working on the failed one. The LXP710 provides features to change the loop timing source to maintain proper E1 timing.

External Communication

This is usually a background mode for rack systems. The OEM must use a protocol to supply the LTU with configuration information and receive diagnostic data from it. The external system can support remote performance monitoring and command loopbacks, error injections, etc. This also provides the option to upgrade the HDSL system's application software if it is contained in a FLASH EPROM, taking care not to alter the board bootload software.

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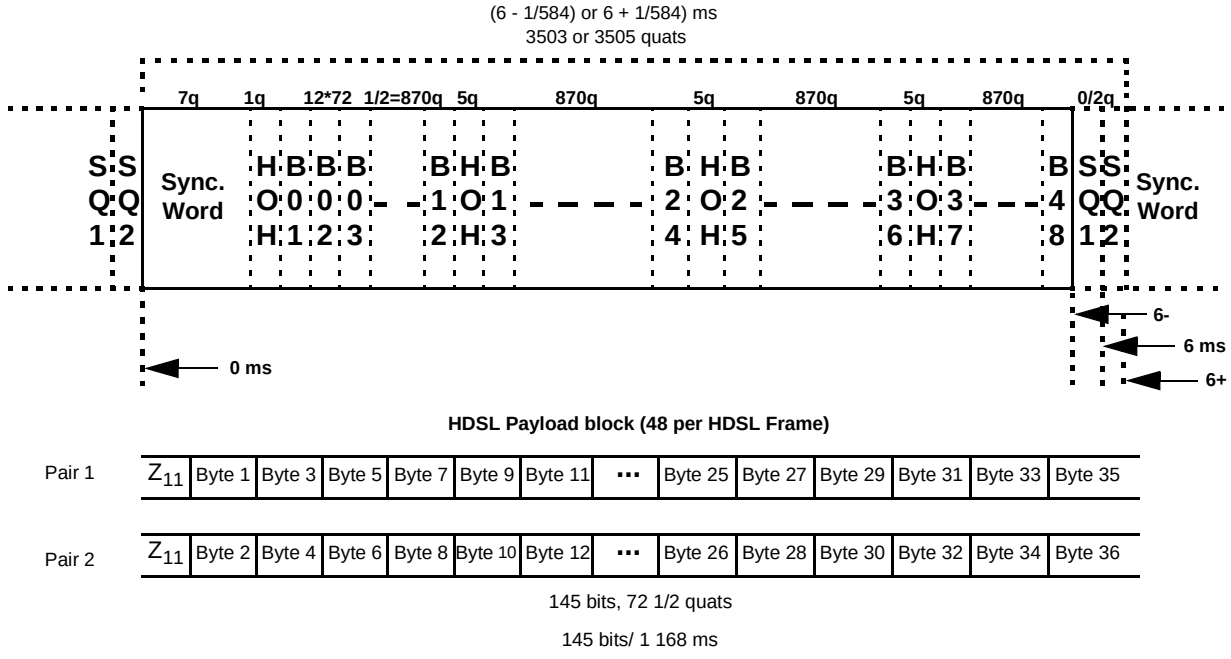
Table 115: HDSL Frame Structure for Two Pair Point-to-Point System

Time	Frame Bit #	HOH Bit #	Symbol	Description	Notes
0 ms	1:14	1:14	SW<1:14>	Sync word	Double barker code
	15	15	losd	Loss of input signal at the far end application interface	
	16	16	febe	Far end block error	
	17:1756	–	B01:B12	Payload block 1:12	HDSL payload including Z_{m1}:Z_{m12}
	1757	17	eoc01	eoc address	
	1758	18	eoc02	eoc address	
	1759	19	eoc03	eoc data/opcode	
	1760	20	eoc04	eoc Odd/Even Byte	
	1761	21	crc1	Cyclic redundancy check	CRC-6
	1762	22	crc2	Cyclic redundancy check	CRC-6
	1763	23	ps1	NTU power status bit 1	NTU → LTU only
	1764	24	ps2	NTU power status bit 2	NTU → LTU only
	1765	25	bpv	Bipolar violation	
	1766	26	eoc05	eoc unspecified	
	1767:3506	–	B13:B24	Payload blocks 13:24	HDSL payload including Z_{m13}:Z_{m24}
	3507	27	eoc06	eoc message bit 1	
	3508	28	eoc07	eoc message bit 2	
	3509	29	eoc08	eoc message bit 3	
	3510	30	eoc09	eoc message bit 4	
	3511	31	crc3	Cyclic redundancy check	CRC-6
	3512	32	crc4	Cyclic redundancy check	CRC-6
	3513	33	hrp	Regenerator present	LTU ← REG → NTU
	3514	34	rrbe	Regenerator remote block error	LTU ← REG → NTU
	3515	35	rcbe	Regenerator central block error	LTU ← REG → NTU
	3516	36	rega	Regenerator alarm	LTU ← REG → NTU
	3517:5256	–	B25:B36	Payload blocks 25:36	HDSL payload including Z_{m25}:Z_{m36}
	5257	37	eoc10	eoc message bit 5	

Table 115: HDSL Frame Structure for Two Pair Point-to-Point System – continued

Time	Frame Bit #	HOH Bit #	Symbol	Description	Notes
0	5258	38	eoc11	eoc message bit 6	
	5259	39	eoc12	eoc message bit 7	
	5260	40	eoc13	eoc message bit 8	
	5261	41	crc5	Cyclic redundancy check	CRC-6
	5262	42	crc6	Cyclic redundancy check	CRC-6
	5263	43	rta	Remote terminal alarm	NTU → LTU only
	5264	44	indc/indr	Ready to receive	indc=LTU → NTU indr=NTU → LTU
	5265	45	uib1	Unspecified indicator bit	
	5266	46	uib2	Unspecified indicator bit	
	5267:7006	–	B37:B48	Payload blocks 37:48	HDSL payload including Z_{m34}:Z_{m48}
6 - 1/584 ms	7007	47	stq1s	Stuff quat 1 sign	Frame stuffing
	7008	48	stq1m	Stuff quat 1 magnitude	Frame stuffing
6 ms nominal	7009	49	stq2s	Stuff quat 2 sign	Frame stuffing
	7010	50	stq2m	Stuff quat 2 magnitude	Frame stuffing
6 + 1/584 ms	The times listed relate to the end of the last bit of the previous line.				

Figure 9: Frame Structure of Two Pair Point-to-Point System



HDSL Payload block (48 per HDSL Frame)

Pair 1	Z_{11}	Byte 1	Byte 3	Byte 5	Byte 7	Byte 9	Byte 11	···	Byte 25	Byte 27	Byte 29	Byte 31	Byte 33	Byte 35
Pair 2	Z_{11}	Byte 2	Byte 4	Byte 6	Byte 8	Byte 10	Byte 12	···	Byte 26	Byte 28	Byte 30	Byte 32	Byte 34	Byte 36

145 bits, 72 1/2 quats

145 bits/ 1 168 ms

Symbol	Description
B01:B48	HDSL system payload blocks.
Byte n	Byte n from core frame (n = 1:144).
HOH	HDSL overhead (sw, eoc, crc,...).
quat	Quaternary symbol.
SQ1 SQ2	Stuff quats.
Sync word	7-symbol Barker codes. “Double Barker” → 14 bits.
6- 6+	6 - 1/584 ms 6 + 1/584 ms
Z_{mn}	Additional overhead bits (Z bits).
m	Indicates corresponding pair (m = 1:2).
n	Indicates number of payload blocks (n = 1:48).

TEST SPECIFICATIONS

NOTE

The minimum and maximum values in Tables 116 through 127 and Figures 10 through 23 represent the performance specifications of the LXP710 and are guaranteed by test except, where noted, by design.

Table 116: Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply voltage	Vcc	-0.3	+6.0	V
Input voltage	–		Vcc +0.3	V
Output current	–	–	±25	mA
Storage temperature	tSTOR	-65	+150	°C

Table 117: Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
DC supply	Vcc	4.75	5.0	5.25	V
Ambient operating temperature	tA	-40	–	+85	°C

Table 118: DC Electrical Characteristics

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Conditions
Supply current (full operation)	ICC	–	45	70	mA	
Input Low voltage	VIL	–	–	0.14 VCC	V	
Input High voltage	VIH	0.64 VCC	–	–	V	
Output Low voltage	VOL	–	–	0.06 VCC	V	IOL < 2 mA
Output High voltage	VOH	0.64 VCC	–	–	V	IOH < -2 mA
Input leakage current[2]	IIL	–	–	±5	µA	0 < VIN < VCC
Tristate leakage current[3]	I3L	–	–	±5	µA	0 < V < VCC
Input capacitance (individual pins)	CIN	–	10	–	pF	
Load capacitance (REFCLK output)	CLREF	–	–	15	pF	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 119: E1 Interface Input Timing Specifications (see Figure 10)

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Conditions
Setup time of E1DATI and E1FRMI	t_{SU}	10	–	–	ns	Referenced from falling edge of E1CLKI.
Hold time of E1DATI and E1FRMI	t_{HT}	20	–	–	ns	Referenced from falling edge of E1CLKI.
E1CLKI period	t_{PW}	–	488	–	ns	
E1CLKI pulse width Low	t_{PWL}	50	–	–	ns	
E1CLKI pulse width High	t_{PWH}	50	–	–	ns	
E1CLKI rise time	t_R	–	–	60	ns	
E1CLKI fall time	t_F	–	–	60	ns	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 10: E1 Interface Input Timing

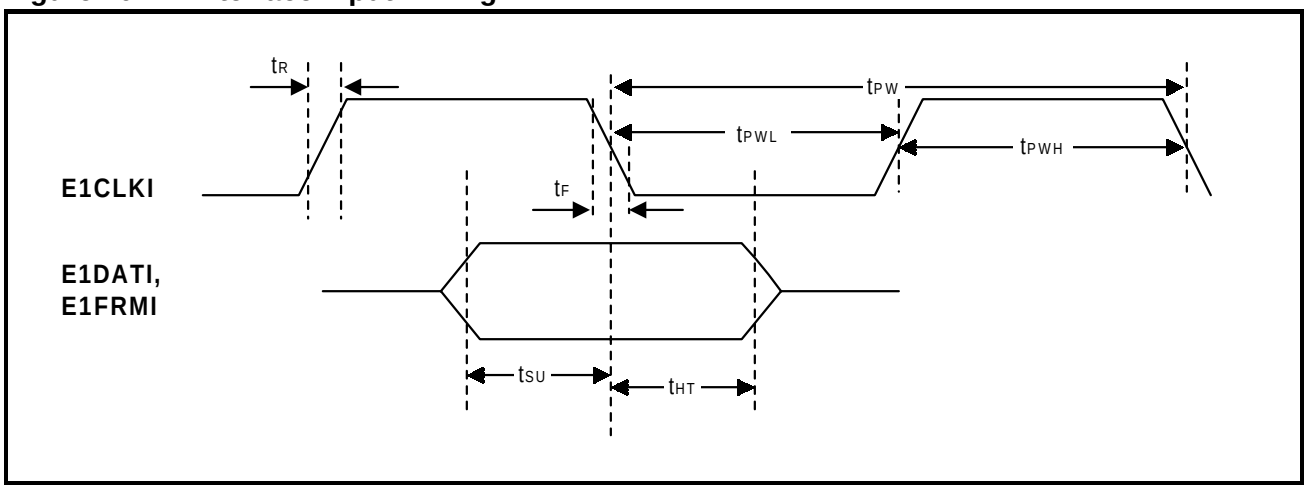


Table 120: E1 Interface Output Timing Specifications (see Figure 11)

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Conditions
Output delay time of E1DATO and E1FRMO	t_D	–	15	30	ns	Referenced from rising edge of E1CLKO.
E1CLKO period	t_{PW}	–	488	–	ns	
E1CLKO pulse width Low	t_{PWL}	50	–	–	ns	
E1CLKO pulse width High	t_{PWH}	50	–	–	ns	
E1CLKO rise time	t_R	–	–	40	ns	
E1CLKO fall time	t_F	–	–	40	ns	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 11: E1 Interface Output Timing

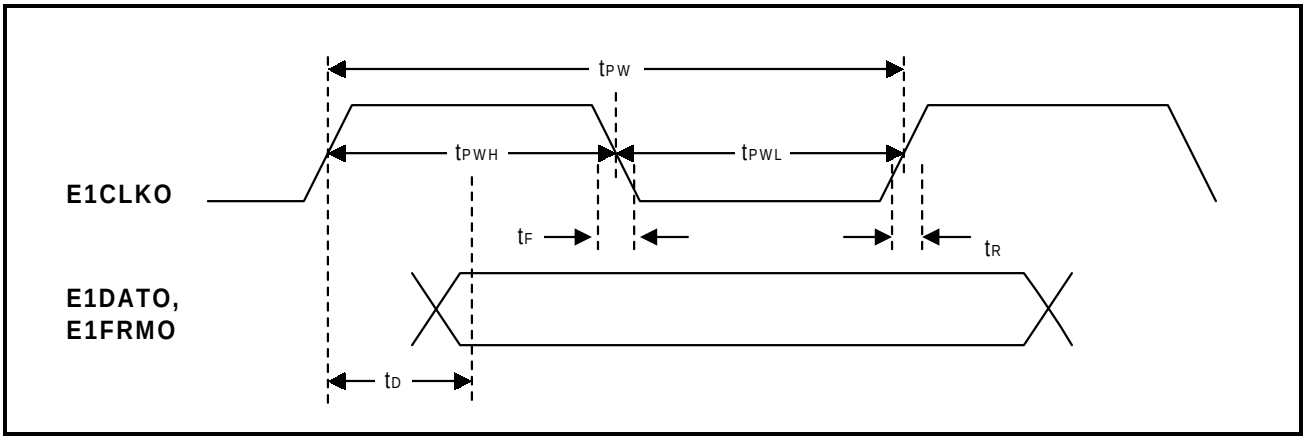


Table 121: HDSL Interface Input Timing Specifications (see Figure)

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Conditions
Setup time of LP<1:3>DTI, RFP<1:3>	t_{SU}	10	–	–	ns	Referenced from rising edge of ICLK1.
Hold time of LP<1:3>DTI, RFP<1:3>	t_{HT}	10	–	–	ns	Referenced from rising edge of ICLK1.

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 12: HDSL Interface Input Timing

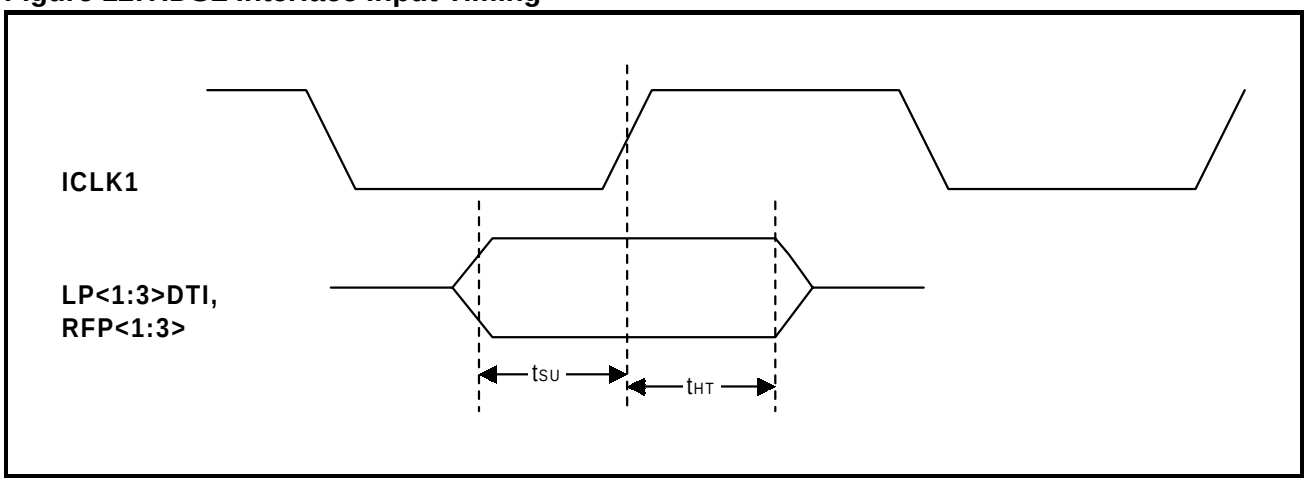


Table 122: HDSL Interface Output Timing Specifications (see Figure 13)

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Conditions
Output delay time of LP<1:3>DTO, TFP<1:3>	t_D	–	–	20	ns	Referenced from falling edge of ICLK1.

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 13: HDSL Interface Output Timing

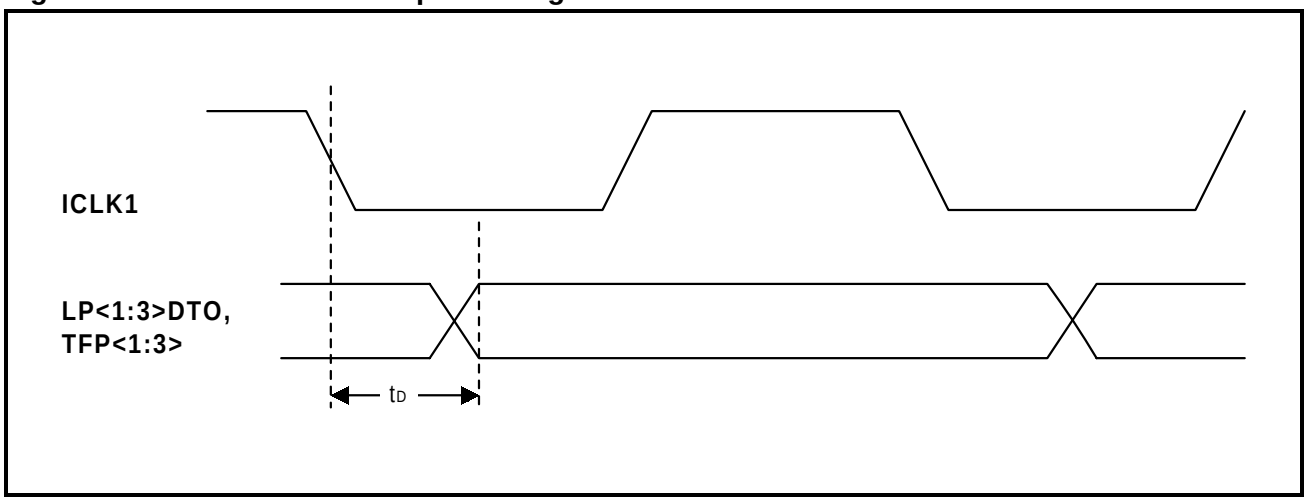


Table 123: Microprocessor Write Cycle Specifications—Motorola Mode (see Figure 14)

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Conditions
Address setup time to $\overline{CS}$, $\overline{DS}$	tASU	10	–	–	ns	
D<0:7> setup time to $\overline{CS}$, $\overline{DS}$	tDSU	10	–	–	ns	
Data-In hold time from $\overline{CS}$, $\overline{DS}$	tDHT	10	–	–	ns	
Allowable $\overline{CS}$ width	tCPW	80	–	–	ns	
Allowable $\overline{DS}$ assertion delay after $\overline{CS}$, R/$\overline{W}$	tRSU	–	–	30	ns	
Allowable $\overline{DS}$ width	tDPW	50	–	–	ns	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 14: Microprocessor Write Cycle—Motorola Mode

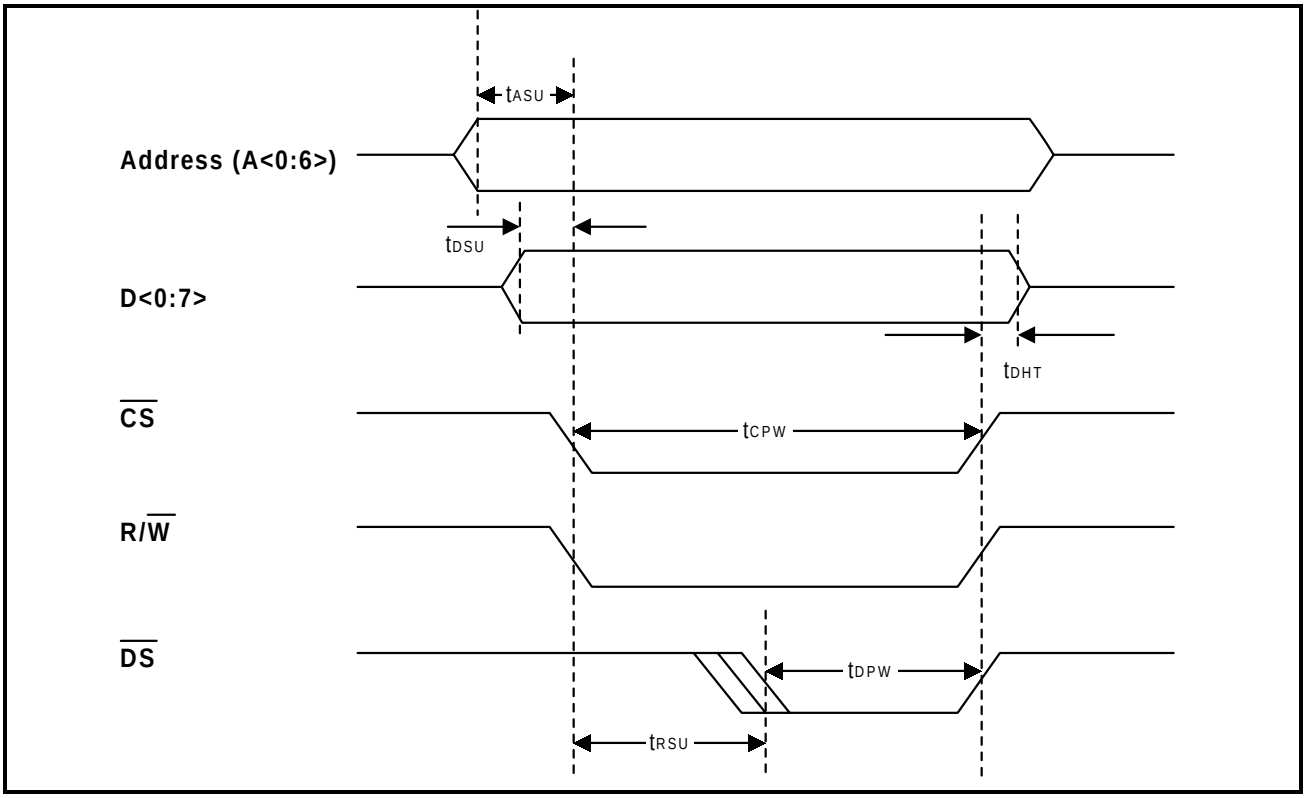


Table 124: Microprocessor Read Cycle Specifications—Motorola Mode (see Figure 15)

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Conditions
D<0:7> valid after $\overline{CS}$, $\overline{DS}$	t1	–	45	60	ns	
D<0:7> keep valid after $\overline{CS}$, $\overline{DS}$ negation	t2	–	–	30	ns	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 15: Microprocessor Read Cycle—Motorola Mode

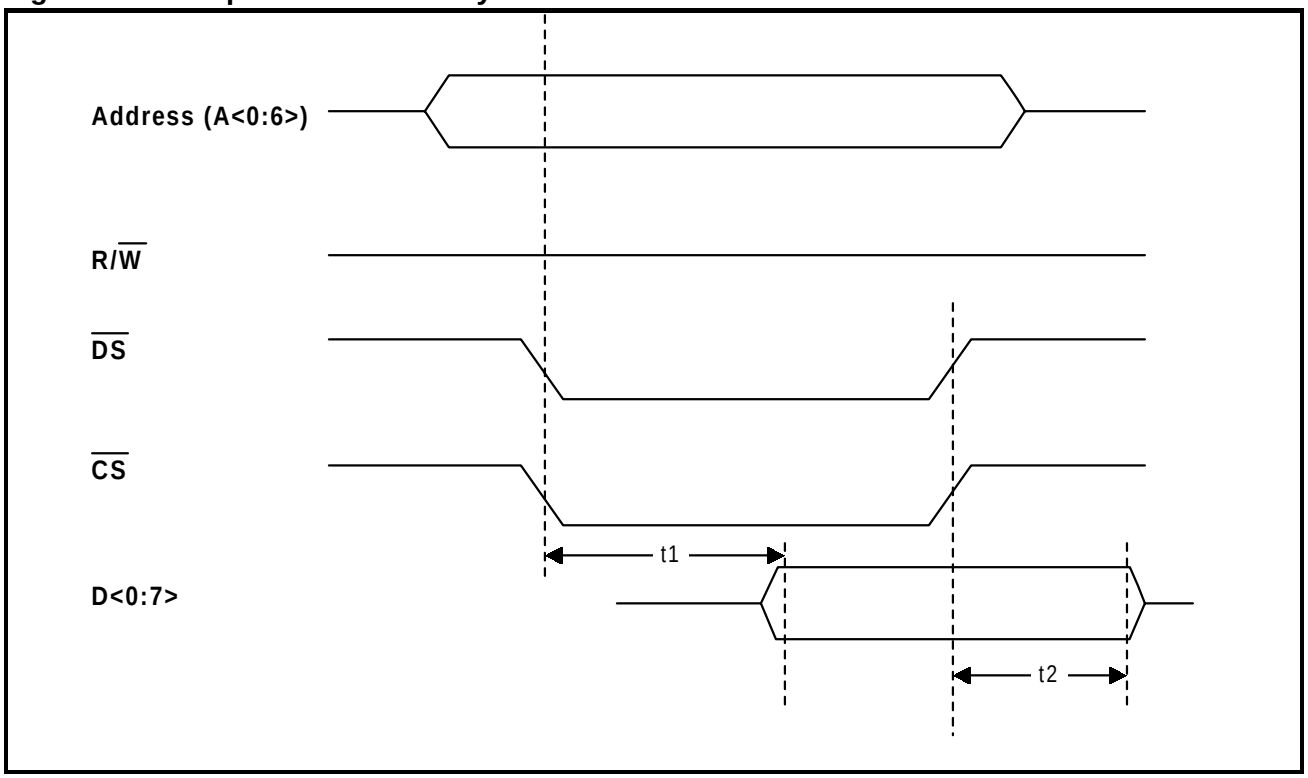


Table 125: Microprocessor Write Cycle Specifications—Intel Mode (see Figure 16)

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Conditions
Address setup time to $\overline{CS}$, $\overline{WR}$	tASU	20	–	–	ns	
D<0:7> setup time to $\overline{CS}$, $\overline{WR}$	tDSU	10	–	–	ns	
D<0:7> hold time after $\overline{CS}$, $\overline{WR}$ rising edge	tDHT	10	–	20	ns	
Allowable $\overline{CS}$ width	tCPW	80	–	–	ns	
Allowable $\overline{WR}$ width	tRPW	80	–	–	ns	
Allowable R/$\overline{W}$ falling edge before $\overline{CS}$ rising	tWSU	50	–	–	ns	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 16: Microprocessor Write Cycle—Intel Mode

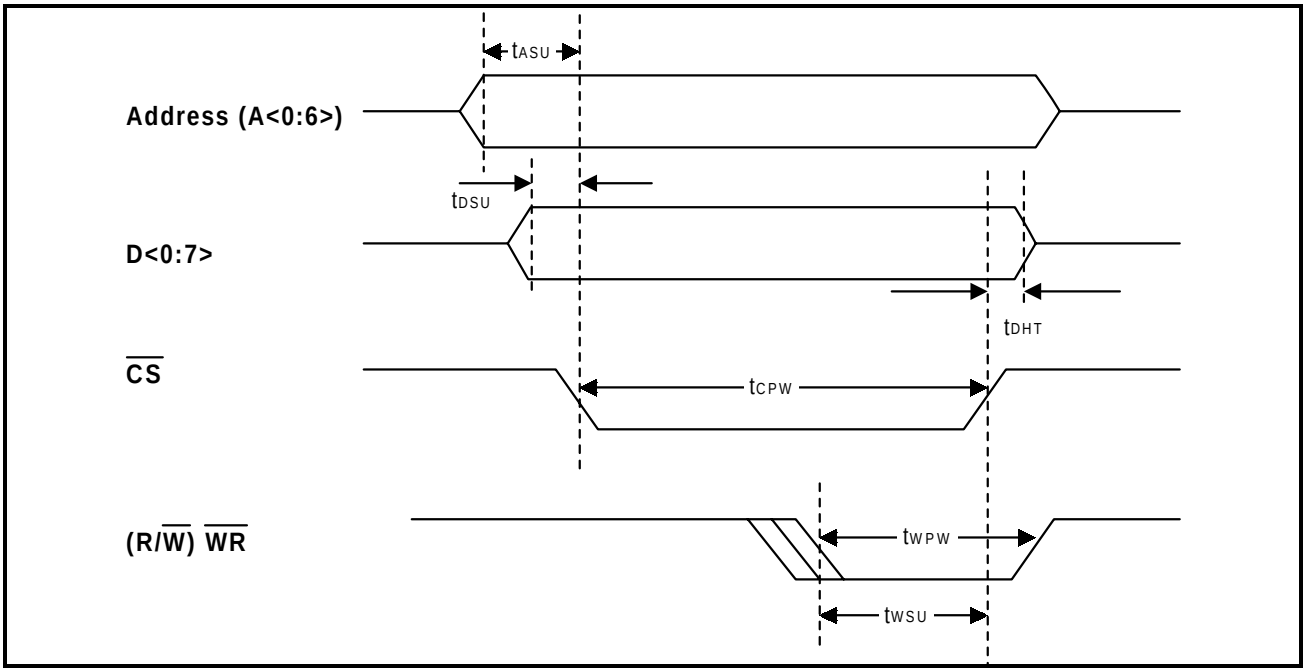


Table 126: Microprocessor Read Cycle Specifications—Intel Mode (see Figure 17)

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Conditions
D<0:7> valid after $\overline{CS}$, $\overline{RD}$ assertion	tDATA	–	45	60	ns	
D<0:7> keep valid after $\overline{CS}$, $\overline{RD}$ negation	tDATN	–	–	20	ns	
Allowed width of $\overline{CS}$	tCPW	80	–	–	ns	
Allowed width of $\overline{RD}$	tRPW	80	–	–	ns	
Address setup time to $\overline{CS}$, $\overline{RD}$ assertion	tASU	50	–	–	ns	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 17: Microprocessor Read Cycle—Intel Mode

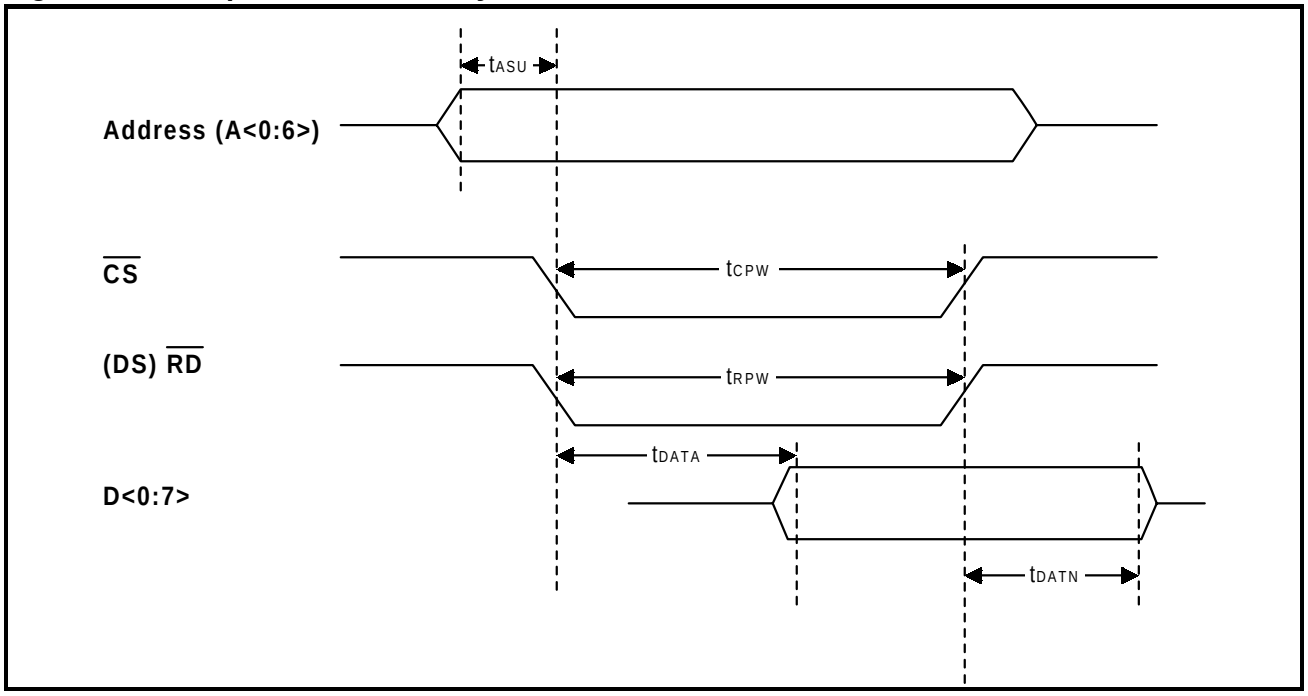


Figure 18: Peak Output Jitter Performance

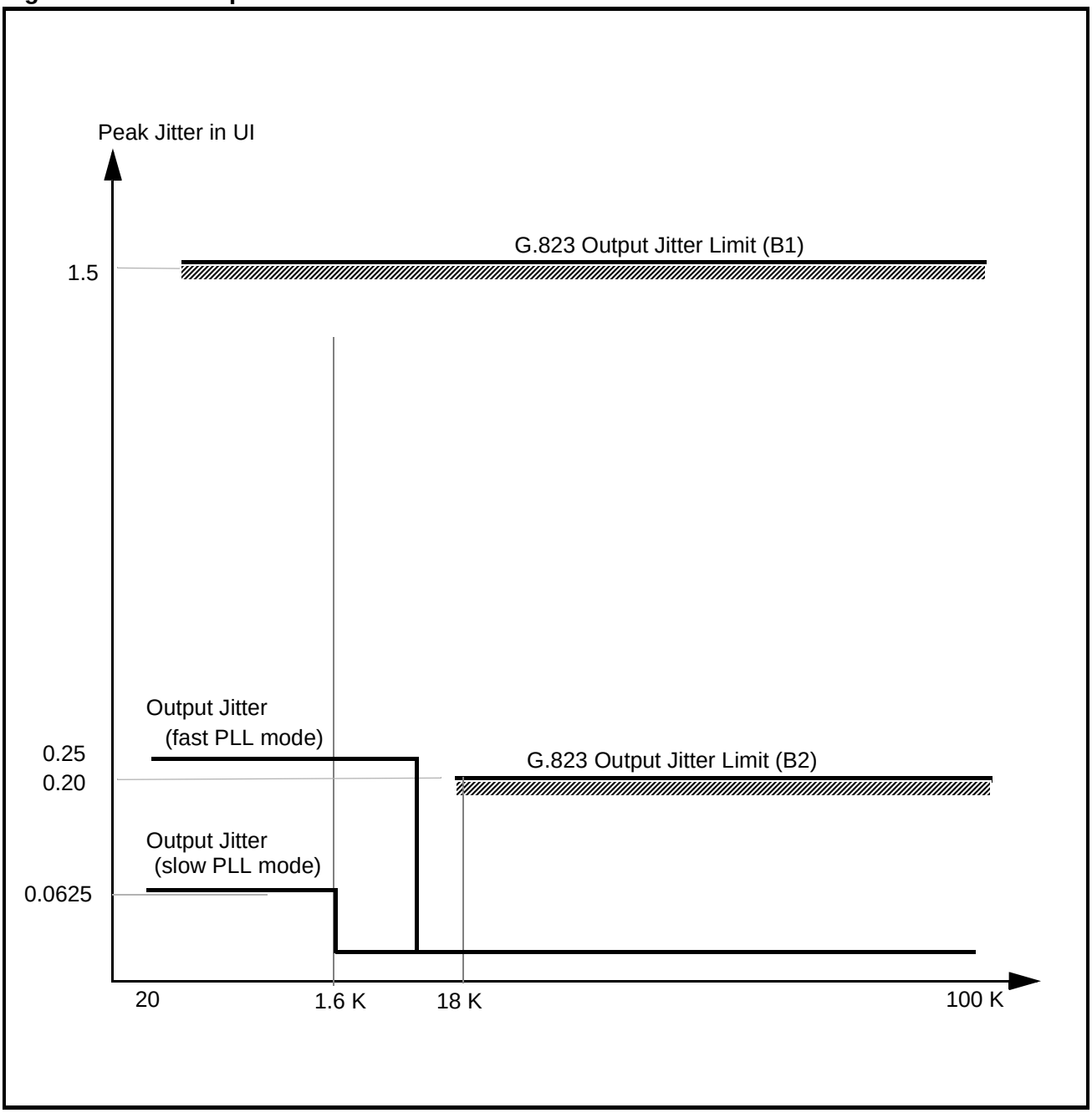
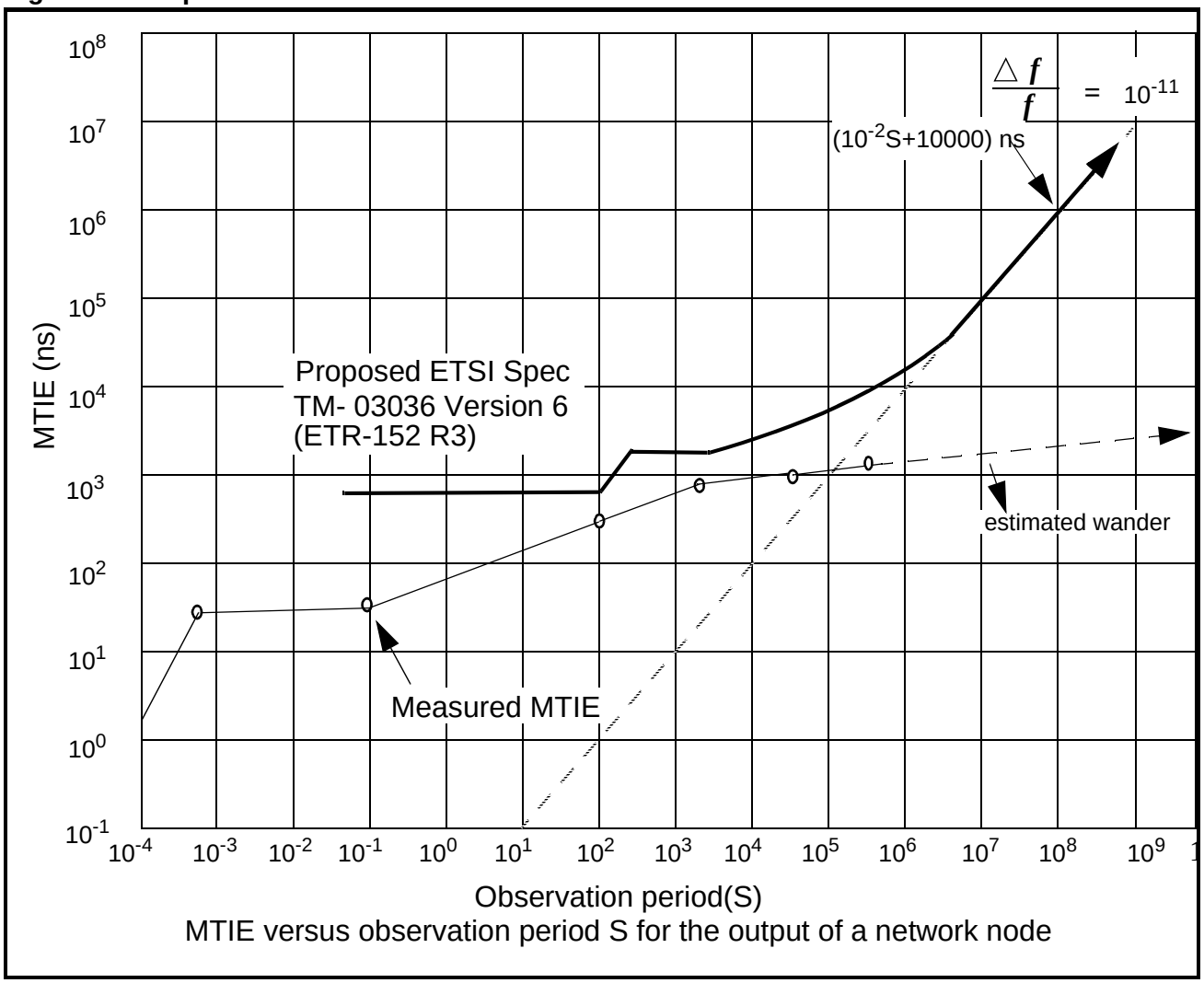


Figure 19: Output Wander Performance

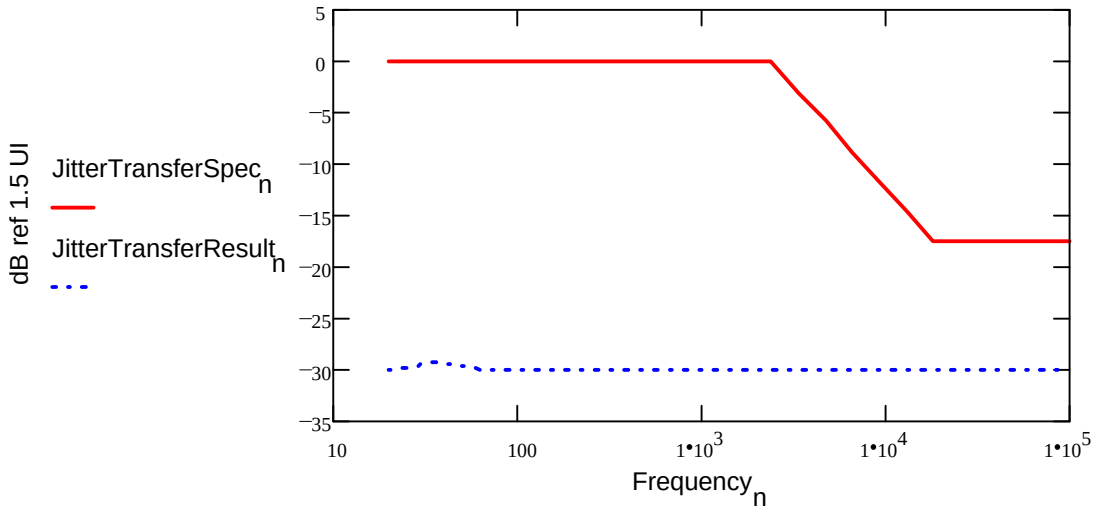


MTIE versus observation period S for the output of a network node

Table 127: ETSI Maximum Wander Values

MTIE	Observation Interval
732 ns	$0.05 < t \leq 100$ s
13t - 568 ns	$100 < t \leq 200$ s
2000 ns	$200 < t \leq 2000$ s
$433t^{0.2} + 0.01t$ ns	$t > 2000$ s

Figure 20: Typical Jitter Transfer Results



Includes the effects of the LIU Jitter Attenuator.

Figure 21: Jitter Transfer Measurement Setup

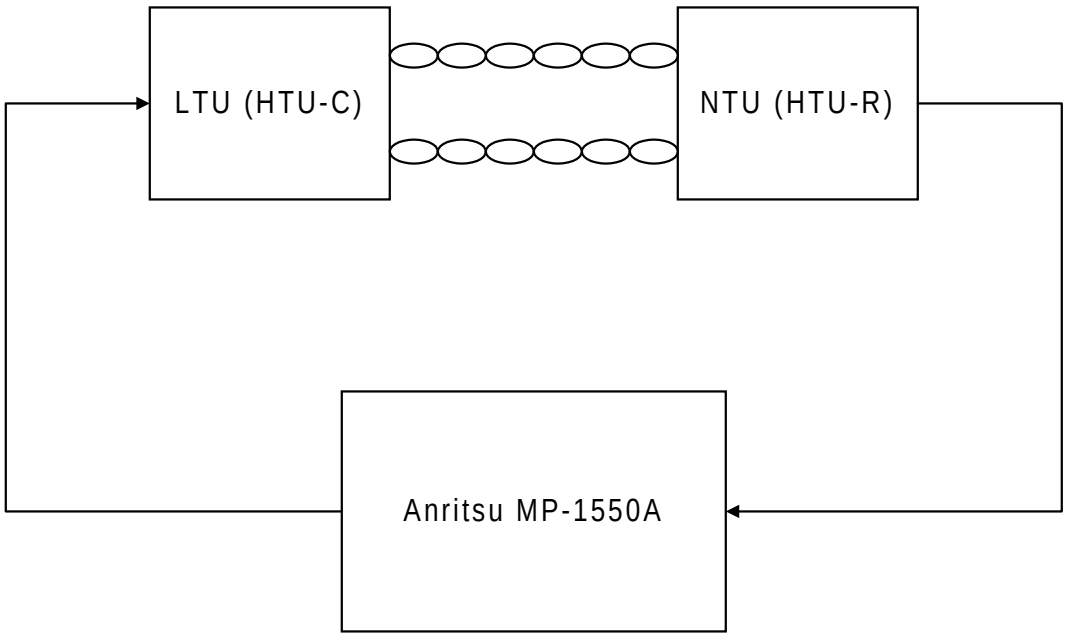
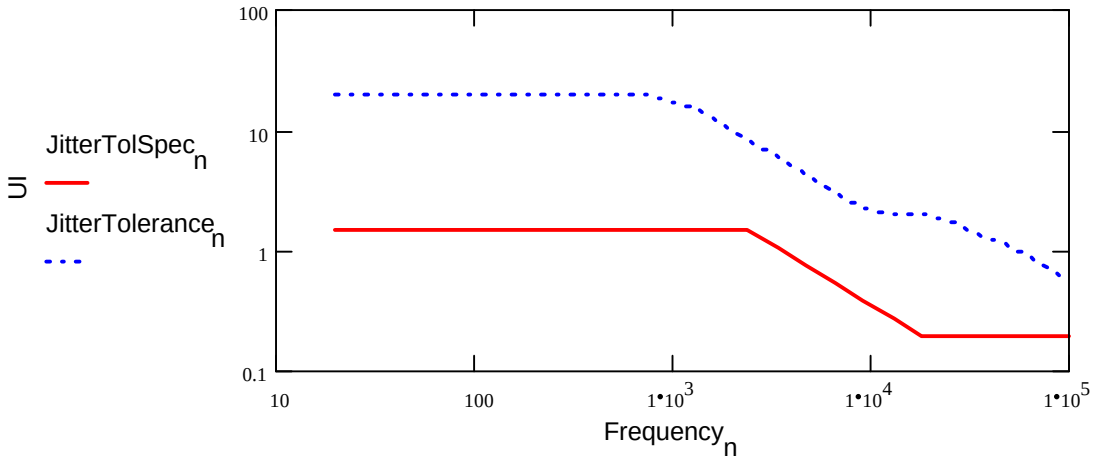
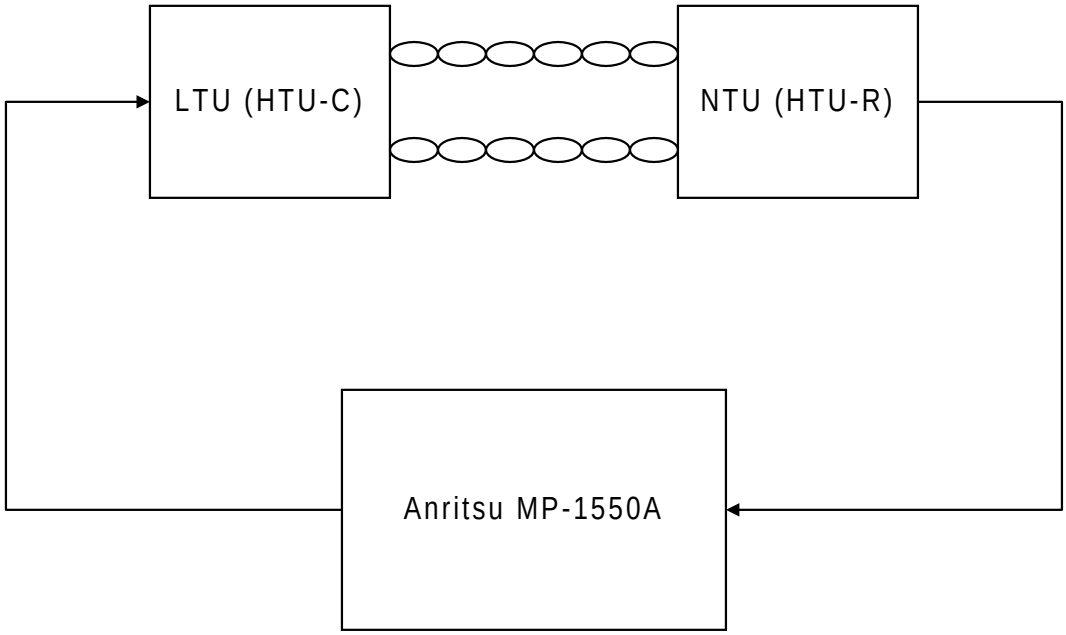


Figure 22: Typical Jitter Tolerance Results



Includes the effects of the LIU Jitter Attenuator.

Figure 23: Jitter Tolerance Measurement Setup

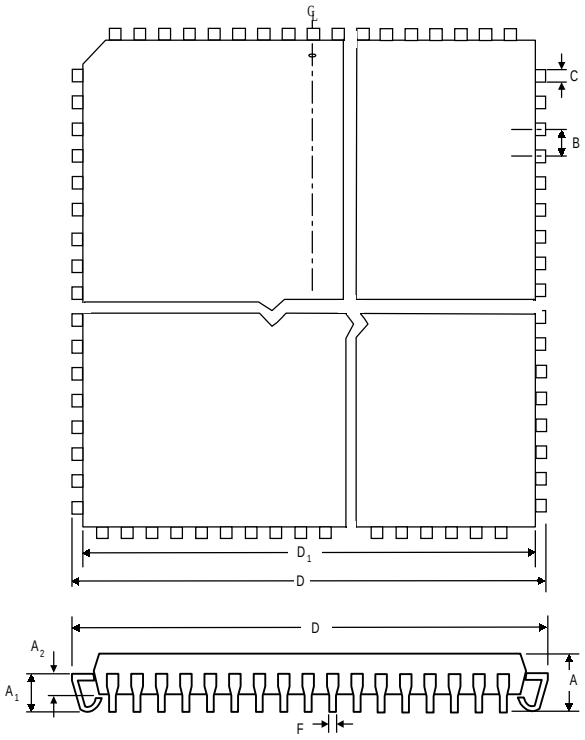


MECHANICAL SPECIFICATIONS

Figure 24: Plastic Leaded Chip Carrier Package Specification

LXP710PE

- 84-pin PLCC
- Extended Temperature Range (-40 °C to 85 °C)



Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	0.167	0.181	4.242	4.598
A1	0.098	0.110	2.490	2.794
A2	–	–	–	–
B	0.050 BSC[1] (nominal)		1.27 BSC[1] (nominal)	
C	0.028		0.711	
D	1.185	1.195	30.099	30.353
D1	1.150	1.158	29.210	29.412
F	0.018		0.457	

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2.0	01/98	Modified test specifications.
1.0	08/97	Product Release.

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5,008,637; 5,028,888; 5,057,794; 5,059,924; 5,068,628; 5,077,529; 5,084,866; 5,148,427; 5,153,875; 5,157,690; 5,159,291; 5,162,746; 5,166,635; 5,181,228; 5,204,880; 5,249,183; 5,257,286; 5,267,269; 5,267,746; 5,461,661; 5,493,243; 5,534,863; 5,574,726; 5,581,585; 5,608,341; 5,671,249; 5,666,129; 5,701,099

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