OKI semiconductor

MSM511002B

1,048,576-Word x 1-Bit DYNAMIC RAM

GENERAL DESCRIPTION

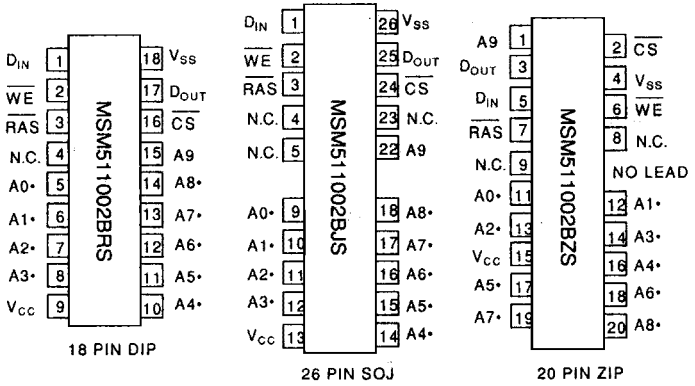
The MSM511002B is a new generation dynamic RAM organized as 1,048,576 words × 1 bit. The technology used to fabricate the MSM511002B is OKI's CMOS silicon gate process technology. The device operates at a single +5V power supply. Its I/O pins are TTL compatible.

FEATURES

- Silicon gate, quardruple polysilicon CMOS, 1-transistor memory cell
- 1,048,576 words × 1 bit
- Single +5V power supply, ±10% tolerance
- Input: TTL compatible, address input, data input latch
- Output: TTL compatible, tristate, nonlatch
- Family organization
- Refresh: 512 cycles/8 ms
- Common I/O capability using Early Write operation
- Static column mode, read/write capability
- $\overline{CS}$ before $\overline{RAS}$ refresh, Hidden refresh, $\overline{RAS}$-only refresh capability
- Gated $\overline{CS}$
- Built-in V_{BB} generator circuit

Family	Access Time (MAX)	Cycle Time (MIN)	Power Dissipation	
			Operating (MAX)	Standby (MAX)
MSM511002B-60	60ns	120ns	495mW	5.5mW
MSM511002B-70	70ns	130ns	440mW	
MSM511002B-80	80ns	150ns	385mW	
MSM511002B-10	100ns	190ns	330mW	

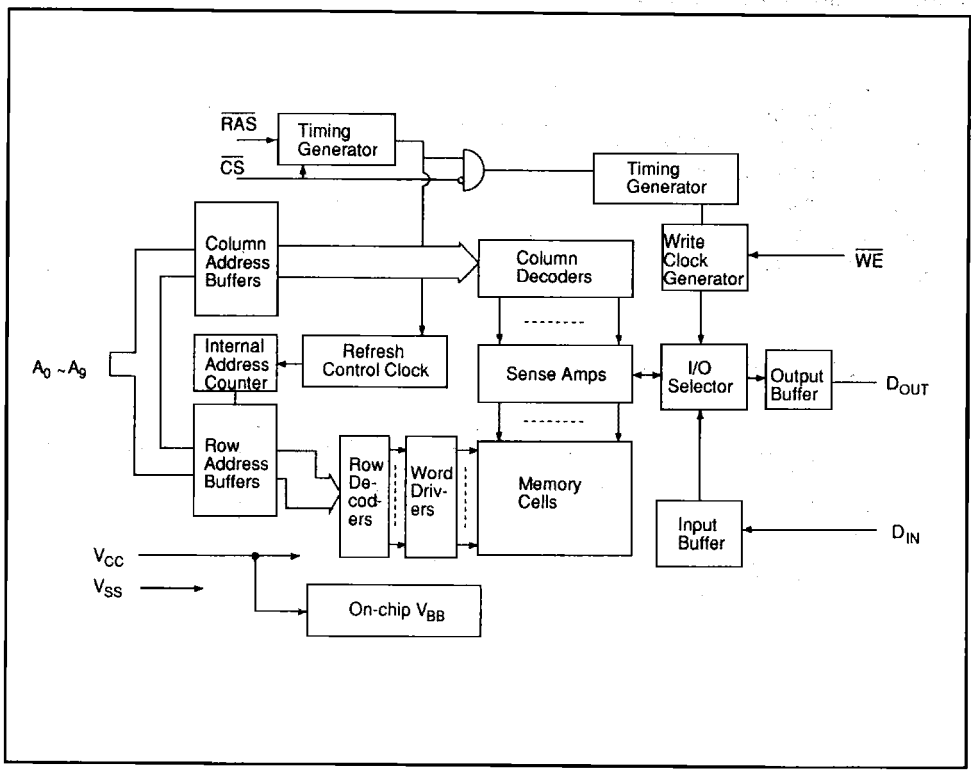
PIN CONFIGURATION (TOP VIEW)



* Refresh Address

Pin Names	Function
A0 to A9	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select Input
DIN	Data Input
DOUT	Data Output
$\overline{WE}$	Write Enable
Vcc	Power Supply (+5V)
Vss	Ground (0V)
N.C.	No Connection

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Conditions	Value	Unit
Voltage on any pin relative to VSS	VT	Ta=25℃	−1.0 to +7.0	V
Short circuit output current	Ios	Ta=25℃	50	mA
Power dissipation	P_D	Ta=25℃	1	W
Operating temperature	Topr	–	0 to +70	℃
Storage temperature	Tstg	–	−55 to +150	℃

RECOMMENDED OPERATING CONDITIONS

(Ta=0 to +70°C)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Supply voltage	V_{CC}	–	4.5	5.0	5.5	V
	V_{SS}	–	0	0	0	V
Input high voltage	V_{IH}	–	2.4	–	6.5	V
Input low voltage	V_{IL}	–	-1.0	–	0.8	V

DC CHARACTERISTICS

(V_{CC} = 5V±10%, Ta = 0 to +70°C)

Parameter	Symbol	Conditions		MSM 511002B-60		MSM 511002B-70		MSM 511002B-80		MSM 511002B-10		Unit	Notes
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Output high voltage	V_{OH}	I_{OH}=-5.0mA		2.4	Vcc	2.4	Vcc	2.4	Vcc	2.4	Vcc	V	
Output low voltage	V_{OL}	I_{OL}=4.2mA		0	0.4	0	0.4	0	0.4	0	0.4	V	
Input leakage current	I_{LI}	0V≦VI≦6.5V; all other pins not under test=0V		−10	10	−10	10	−10	10	−10	10	μA	
Output leakage current	I_{LO}	D_{OUT} disable 0V≦VO≦5.5V		−10	10	−10	10	−10	10	−10	10	μA	
Average power supply current*1, *2 (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CS}$ cycling, t_{RC}=min		−	90	−	80	−	70	−	60	mA	
Power supply current*1 (Standby)	I_{CC2}	$\overline{RAS}$ =V_{IH} $\overline{CS}$=V_{IH} D_{OUT}=HZ	TTL	−	2	−	2	−	2	−	2	mA	
			MOS	−	1	−	1	−	1	−	1	mA	
Average power supply current*1, *2 ($\overline{RAS}$-only refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CS}$=V_{IH} t_{RC}=min		−	90	−	80	−	70	−	60	mA	
Average power supply current*1 ($\overline{CS}$ before $\overline{RAS}$ refresh)	I_{CC6}	$\overline{RAS}$ cycling, $\overline{CS}$ before $\overline{RAS}$		−	90	−	80	−	70	−	60	mA	
Average power supply current*1 (Static column mode)	I_{CC9}	$\overline{RAS}$=V_{IL}, $\overline{CS}$ cycling t_{SC}=min		−	80	−	70	−	60	−	55	mA	

*1 : I_{CC} depends on output loading and cycle rates. Specified values are obtained with the output open.

*2 : Address can be changed less than three times while RAS = V_{IL}.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	TYP	MAX	Unit
Input capacitance(A0 to A9, D_{IN})	CIN1	–	–	6	pF
Input capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{WE}$)	CIN2	–	–	7	pF
Output capacitance (D_{OUT})	COUT	–	–	7	pF

AC CHARACTERISTICS

(V_{CC} = 5V±10%, Ta = 0 to +70°C)

Notes 1, 2, 3

Parameter	Symbol	MSM 511002B-60		MSM 511002B-70		MSM 511002B-80		MSM 511002B-10		Unit	Notes
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Refresh period	t_{REF}	–	8	–	8	–	8	–	8	ms	
Random read or write cycle time	t_{RC}	120	–	130	–	150	–	190	–	ns	
Read/write cycle time	t_{RWC}	140	–	155	–	175	–	220	–	ns	
Static column mode cycle time	t_{SC}	40	–	45	–	50	–	55	–	ns	
Static column mode read/write cycle time	t_{SRWC}	65	–	70	–	80	–	100	–	ns	
Access time from $\overline{RAS}$	t_{RAC}	–	60	–	70	–	80	–	100	ns	4,5,6
Access time from $\overline{CS}$	t_{CAC}	–	15	–	20	–	20	–	25	ns	4,5
Access time from column address	t_{AA}	–	30	–	35	–	40	–	50	ns	4,6,7
Access time from last write	t_{ALW}	–	60	–	65	–	75	–	95	ns	4,7
Output low impedance time from $\overline{CS}$	t_{CLZ}	0	–	0	–	0	–	0	–	ns	4
Data output hold time reference to column address	t_{AOH}	5	–	5	–	5	–	5	–	ns	
Data output enable time reference to $\overline{WE}$	t_{OW}	–	25	–	30	–	30	–	30	ns	
Output buffer turn-off delay	t_{OFF}	0	20	0	20	0	20	0	20	ns	
Transition time	t_T	3	50	3	50	3	50	3	50	ns	3
$\overline{RAS}$ precharge time	t_{RP}	50	–	50	–	60	–	80	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	ns	
$\overline{RAS}$ pulse width (Static column mode cycle only)	t_{RASC}	60	100000	70	100000	80	100000	100	100000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15	–	20	–	20	–	25	–	ns	
$\overline{CS}$ precharge time (Static column mode)	t_{CP}	10	–	10	–	10	–	10	–	ns	
$\overline{CS}$ pulse width	t_{CS}	15	10000	20	10000	20	10000	25	10000	ns	
$\overline{CS}$ pulse width (Static column mode cycle only)	t_{CSC}	15	100000	20	100000	20	100000	25	100000	ns	
$\overline{CS}$ hold time	t_{CSH}	60	–	70	–	80	–	100	–	ns	
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	20	45	20	50	20	60	25	75	ns	5
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	20	50	ns	6
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	5	–	5	–	ns	
Row address set-up time	t_{ASR}	0	–	0	–	0	–	0	–	ns	

AC CHARACTERISTICS (CONT.)

Parameter	Symbol	MSM 511002B-60		MSM 511002B-70		MSM 511002B-80		MSM 511002B-10		Unit	Notes
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Row address hold time	t_{RAH}	10	–	10	–	10	–	15	–	ns	
Column address set-up time	t_{ASC}	0	–	0	–	0	–	0	–	ns	
Column address hold time	t_{CAH}	15	–	15	–	15	–	20	–	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	–	35	–	40	–	50	–	ns	
Column address hold time reference to $\overline{RAS}$ (WRITE CYCLE)	t_{AWR}	50	–	55	–	60	–	75	–	ns	
Column address hold time reference to $\overline{RAS}$	t_{AR}	75	–	85	–	95	–	115	–	ns	
Column address hold time reference to $\overline{RAS}$ precharge	t_{AH}	10	–	10	–	10	–	10	–	ns	
Column address hold time reference to $\overline{WE}$	t_{AHLW}	60	–	65	–	75	–	95	–	ns	
Last write to column address delay	t_{LWAD}	20	30	20	30	20	35	25	45	ns	7
Read command set-up time	t_{RCS}	0	–	0	–	0	–	0	–	ns	
Read command hold time reference to $\overline{CS}$	t_{RCH}	0	–	0	–	0	–	0	–	ns	9
Write command hold time from $\overline{RAS}$	t_{WCR}	50	–	55	–	60	–	75	–	ns	
Write command set-up time	t_{WCS}	0	–	0	–	0	–	0	–	ns	8
Write command pulse width	t_{WP}	10	–	15	–	15	–	20	–	ns	
Write invalid time	t_{WI}	10	–	10	–	10	–	10	–	ns	
Write command hold time (Dout disable)	t_{WCH}	10	–	15	–	15	–	20	–	ns	8
Data-in hold time from $\overline{RAS}$	t_{DHR}	50	–	55	–	60	–	75	–	ns	
Data output hold time reference to $\overline{WE}$	t_{WOH}	0	–	0	–	0	–	0	–	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15	–	20	–	20	–	25	–	ns	
Write command to $\overline{CS}$ lead time	t_{CWL}	15	–	20	–	20	–	25	–	ns	
Data-in set-up time	t_{DS}	0	–	0	–	0	–	0	–	ns	
Data-in hold time	t_{DH}	15	–	15	–	15	–	20	–	ns	
$\overline{CS}$ to $\overline{WE}$ delay	t_{CWD}	15	–	20	–	20	–	25	–	ns	8
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	60	–	70	–	80	–	100	–	ns	8
Column address to $\overline{WE}$ delay time	t_{AWD}	30	–	35	–	40	–	50	–	ns	8
$\overline{RAS}$ to second $\overline{WE}$ delay	t_{RSWD}	75	–	85	–	95	–	115	–	ns	

AC CHARACTERISTICS (CONT.)

Parameter	Symbol	MSM 511002B-60		MSM 511002B-70		MSM 511002B-80		MSM 511002B-10		Unit	Notes
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Read command hold time reference to $\overline{RAS}$	t_{RRH}	0	–	0	–	0	–	0	–	ns	9
RAS to $\overline{CS}$ set-up time (CS before $\overline{RAS}$)	t_{CSR}	10	–	10	–	10	–	10	–	ns	
RAS to $\overline{CS}$ hold time (CS before $\overline{RAS}$)	t_{CHR}	30	–	30	–	30	–	30	–	ns	
$\overline{CS}$ active delay from $\overline{RAS}$ precharge	t_{RPC}	10	–	10	–	10	–	10	–	ns	
$\overline{CS}$ precharge time (Refresh counter test)	t_{CPT}	40	–	40	–	40	–	50	–	ns	
$\overline{CS}$ precharge time	t_{CPN}	10	–	10	–	10	–	15	–	ns	

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Notes: 1. An initial pause of 100 μs is required after power-up followed by any 8RAS cycles (Example: $\overline{RAS}$-only) before proper device operation is achieved.

2. The AC characteristics assume the transition time (t_T)=5ns.

3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring of input signals. Transition times are measured between VIH and V_{IL}.

4. Measured with a load circuit equivalent to 2TTL + 100pF.

5. Operation within the t_{RCD} (max.) limit insures that t_{RCC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, access time is controlled exclusively by t_{CAC}.

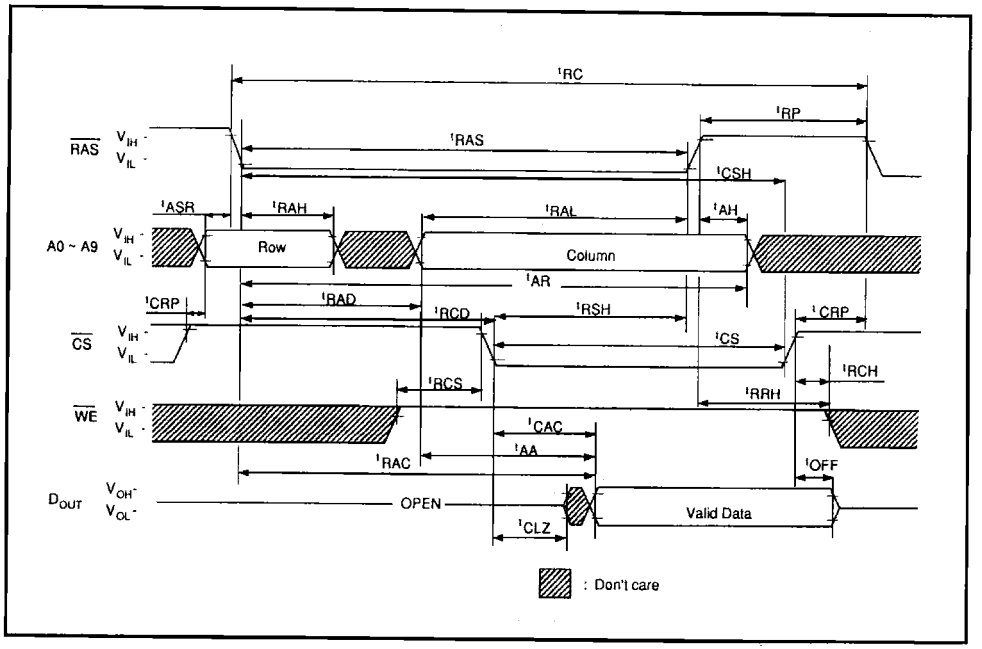
6. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, access time is controlled exclusively by t_{AA}.

7. Operation within the t_{LWAD} (max.) limit insures that t_{ALW} (max.) can be met. t_{LWAD} (max.) is specified as a reference point only; if t_{LWAD} is greater than the specified t_{LWAD} (max.) limit, access time is controlled exclusively by t_{AA}.

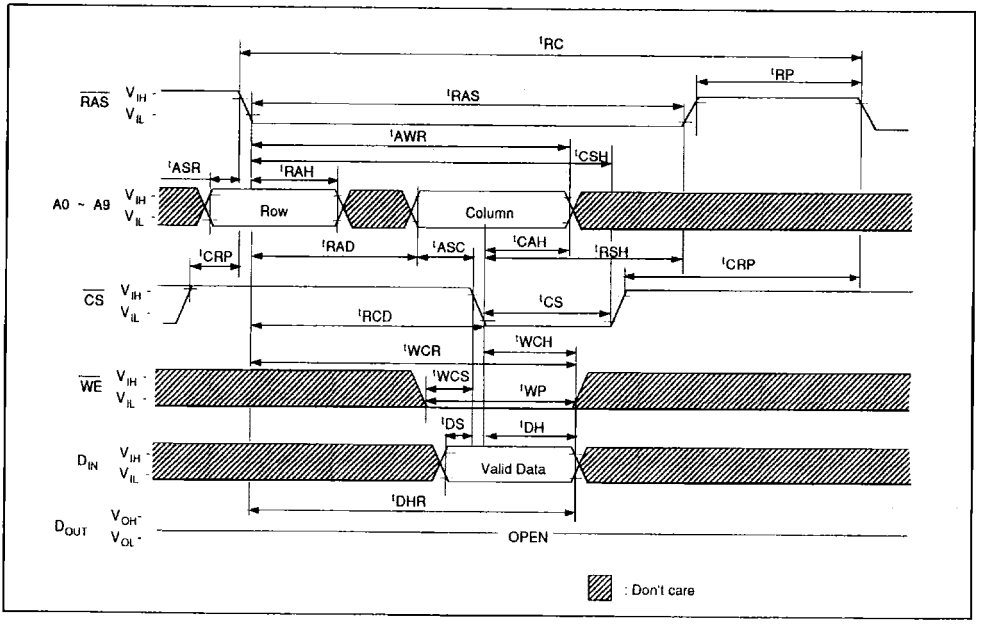
8. t_{WCS}, t_{WH}, t_{CWD}, t_{RWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geqq t_{WCS}$ (min.) and $t_{WH} \geqq t_{WH}$ (min.), the cycle is an Early Write cycle and the data out pin remains open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (min.), $t_{RWD} \geqq t_{RWD}$ (min.) and $t_{AWD} \geqq t_{AWD}$ (min.), the cycle is a read/write cycle and the data out contains data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

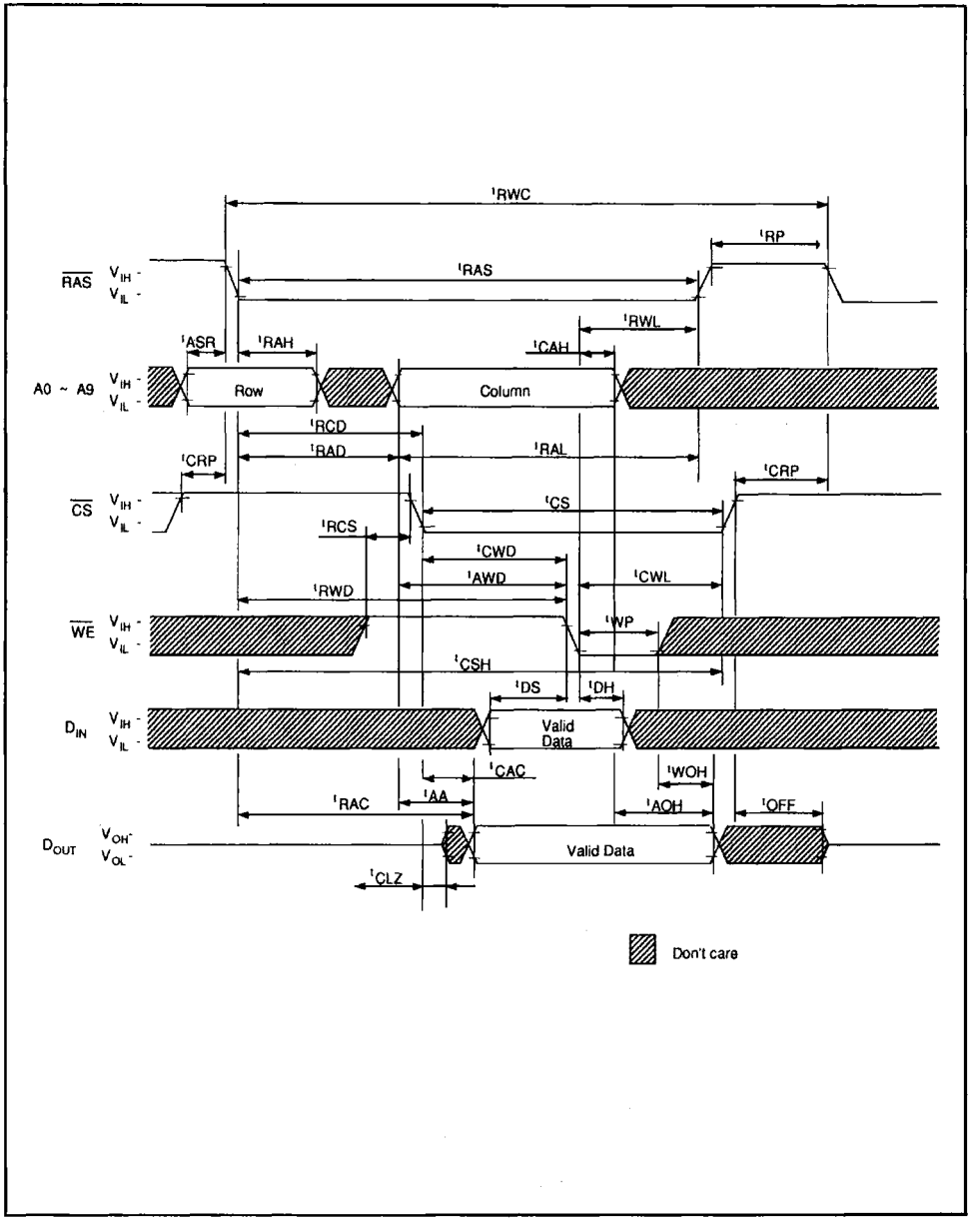
READ CYCLE



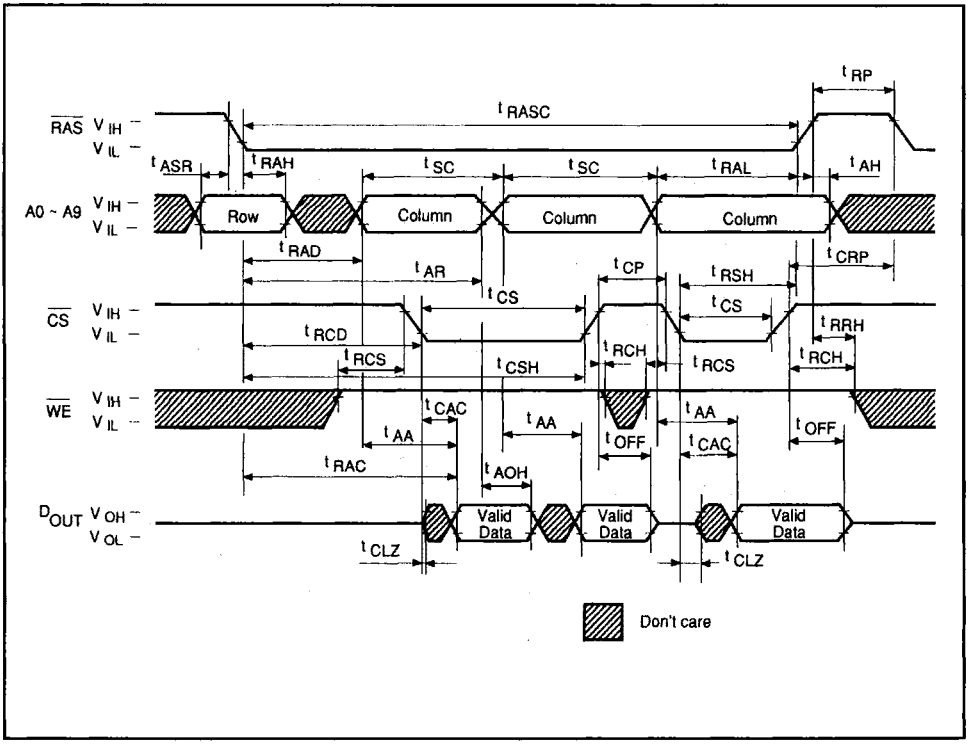
WRITE CYCLE (EARLY WRITE)



READ/WRITE CYCLE



STATIC COLUMN MODE READ CYCLE



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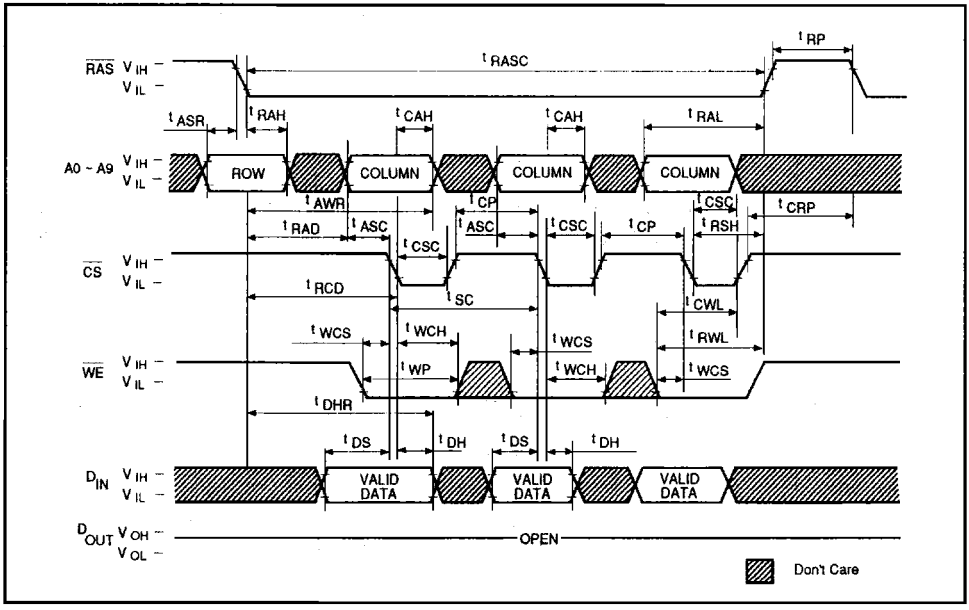
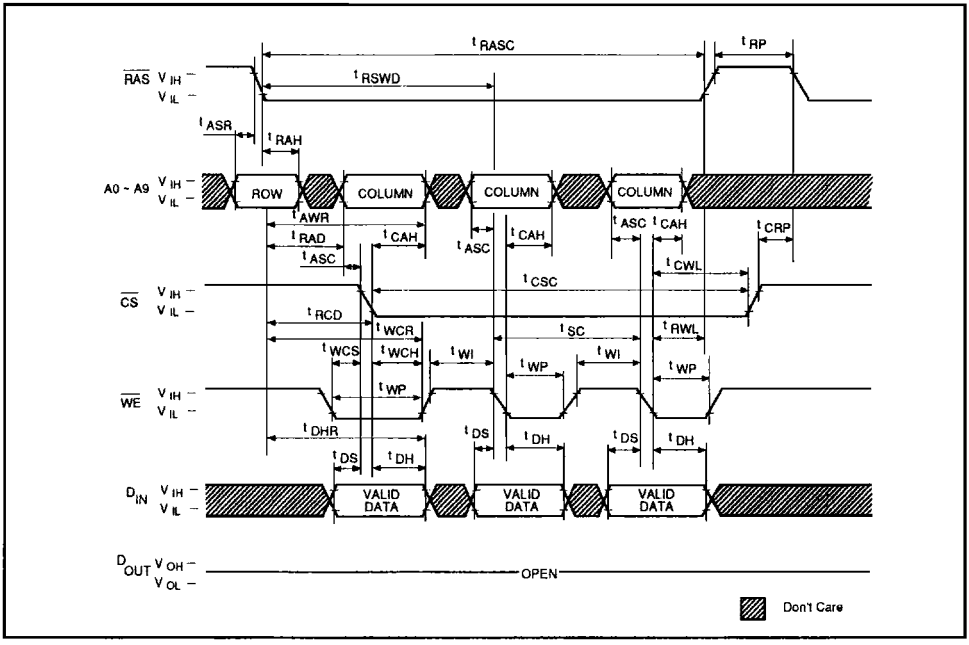
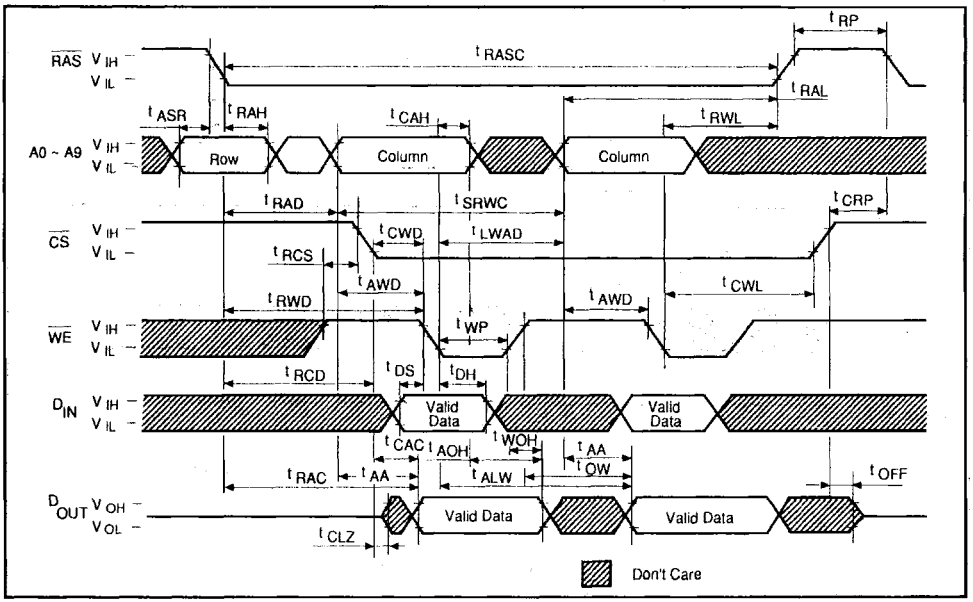
STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



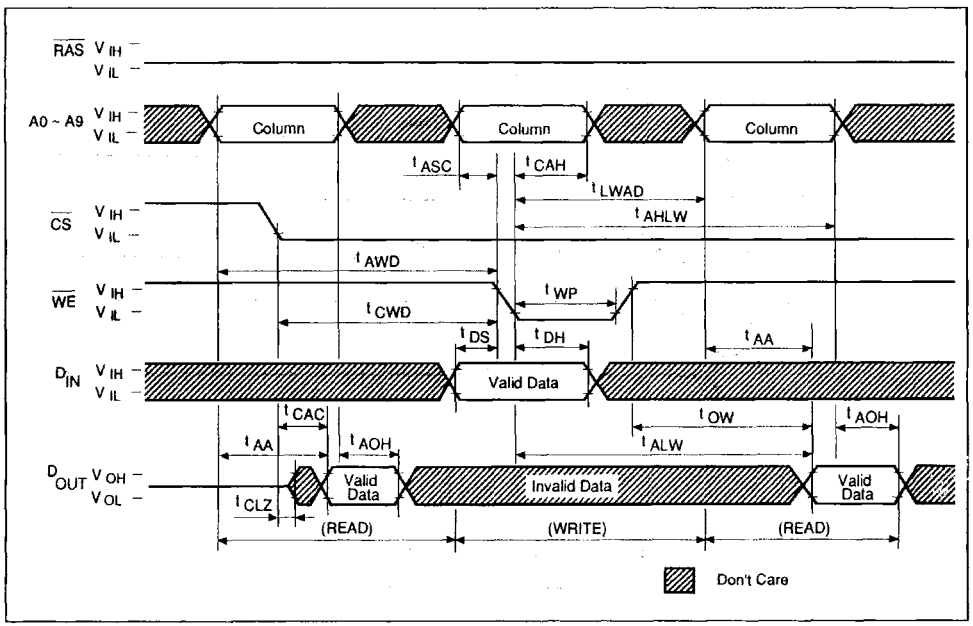
STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



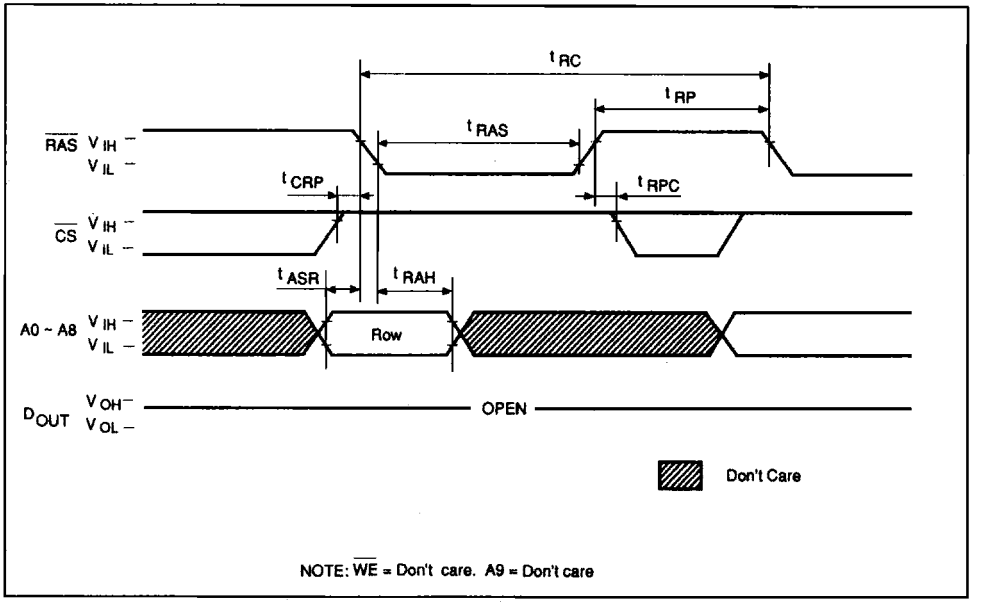
STATIC COLUMN MODE READ/WRITE CYCLE



STATIC COLUMN MODE READ/WRITE MIXED CYCLE

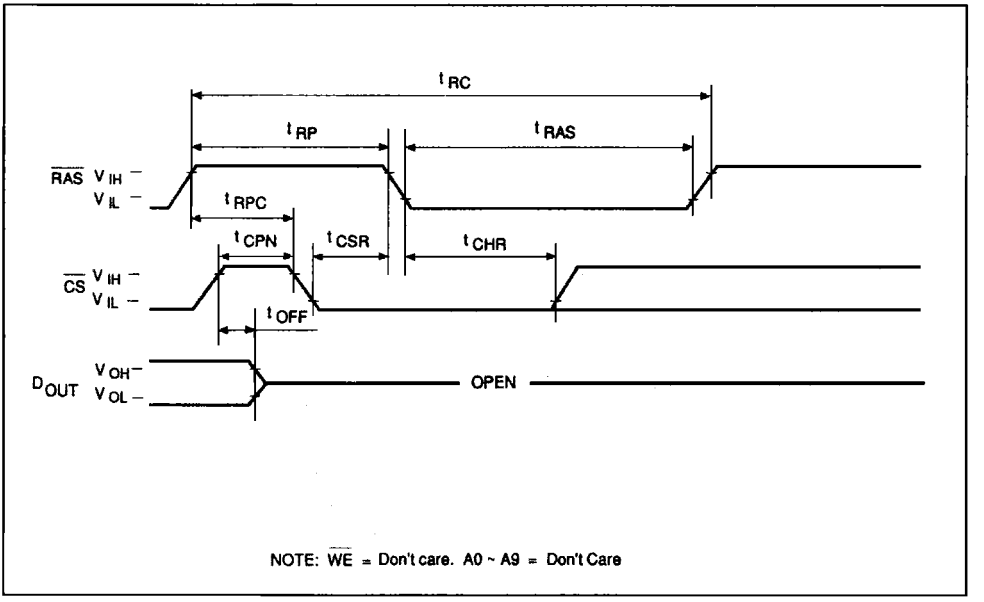


$\overline{RAS}$-ONLY REFRESH CYCLE



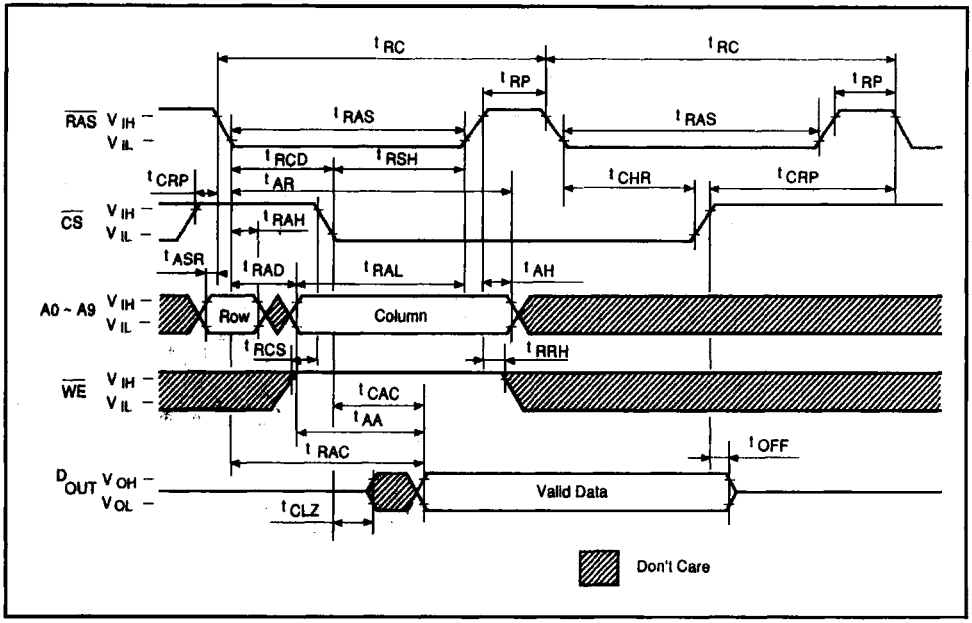
NOTE: $\overline{WE}$ = Don't care. A9 = Don't care

$\overline{CS}$ BEFORE $\overline{RAS}$ AUTO-REFRESH CYCLE

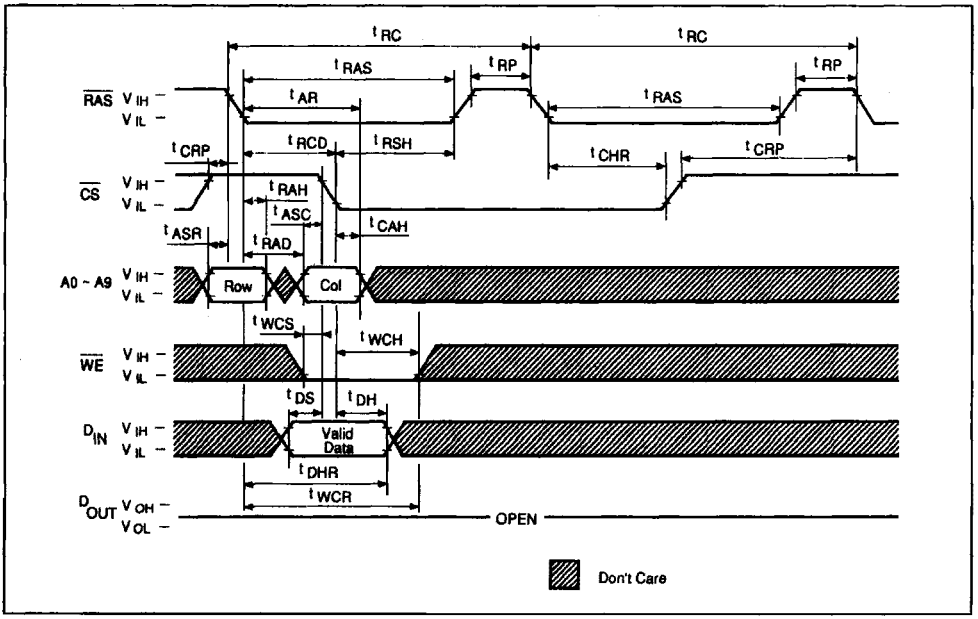


NOTE: $\overline{WE}$ = Don't care. A0 ~ A9 = Don't Care

HIDDEN REFRESH READ CYCLE



HIDDEN REFRESH WRITE CYCLE



$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST