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SSI 32P4741/4744/4744A
Read Channel with 1,7 ENDEC, 4-burst Servo

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DESCRIPTION

The SSI 32P4741/4744/4744A devices are high performance BiCMOS single chip read channel ICs that contain all the functions needed to implement a complete zoned recording read channel for hard disk drive systems. Functional blocks include the pulse detector, programmable filter, 4-burst servo capture, time base generator, and data separator with 1,7 RLL ENDEC. Data rates can be programmed using an internal DAC whose reference current is set by a single external resistor.

Programmable functions of the SSI 32P4741/4744/4744A devices are controlled through a bi-directional serial port and banks of internal registers. This allows zoned recording applications to be supported without changing external component values from zone to zone.

The SSI 32P4741/4744/4744A utilize an advanced BiCMOS process technology along with advanced circuit design techniques which result in high performance devices with low power consumption.

FEATURES

GENERAL

- **DAC controlled programmable data rates from 14 to 40 Mbit/s**
- **Complete zoned recording application support**
- **Low power operation, - 425 mW typical @ 40 Mbit/s at 5V**
- **Bi-directional serial port for register access**
- **Register programmable power management (sleep mode < 0.5 mA)**
- **Power supply range (4.5 to 5.5 volts)**
- **Small footprint 64-lead TQFP package**

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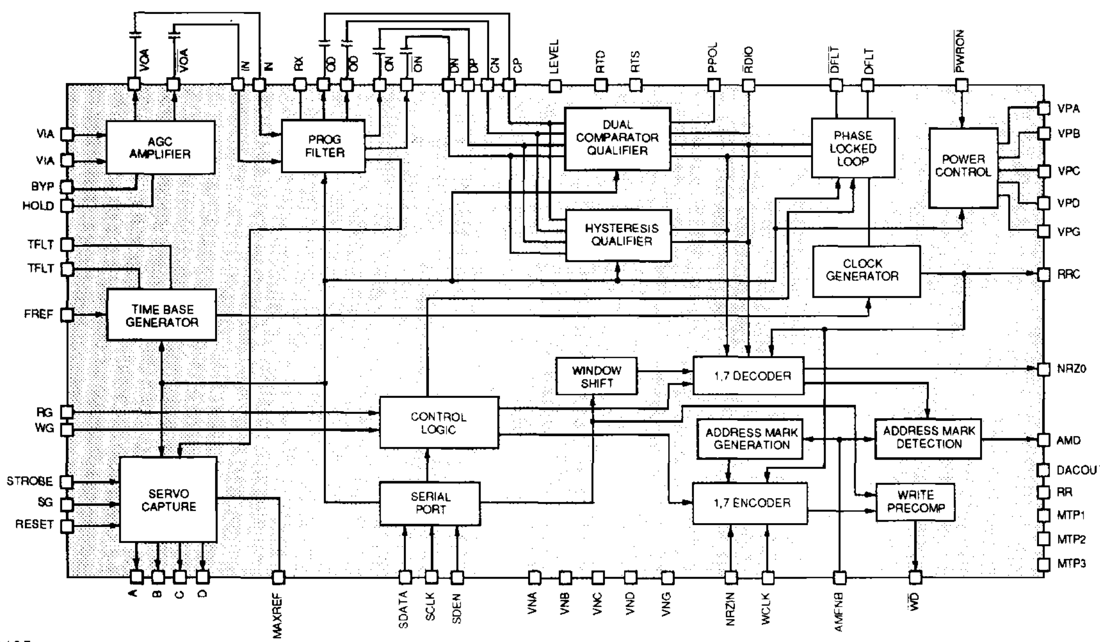
BLOCK DIAGRAM



FEATURES (continued)

PULSE DETECTOR

- Fast attack/decay modes for rapid AGC recovery
- Dual rate charge pump for fast transient recovery
- Low Drift AGC hold circuitry
- Temperature compensated, exponential control AGC
- Wide bandwidth, high precision full-wave rectifier
- Dual mode pulse qualification circuitry (user selectable)
- Register programmable voltage qualification threshold level
- CMOS $\overline{\text{RDIO}}$ signal output for servo timing support
- Internal LOW-Z and fast decay timing
- 0.8 ns max. pulse pairing

SERVO CAPTURE

- 4-burst servo capture with A, B, C, D outputs (4741) and A-B, C-D, A+B outputs (4744/4744A)
- Internal hold capacitors
- Programmable charge current (4-bit DAC)
- Separate registers for FC and VTH during servo mode
- 4-bit DAC for AGC level control (0.75 to 1 Vp-p)

PROGRAMMABLE FILTER

- Programmable cutoff frequency of 6 to 18 MHz
- Programmable boost/equalization of 0 to 13 dB
- Matched normal and differentiated outputs
- ± 15% *fc* accuracy
- ± 2% maximum group delay variation to *fc*
- Less than 1.5% total harmonic distortion
- Low-Z input switch, internally controlled for rapid transient recovery
- No external filter components required

TIME BASE GENERATOR

- Better than 1% frequency resolution
- Up to 75 MHz frequency output
- Independent M and N divide-by registers
- VCO center frequency matched to data synchronizer VCO

DATA SEPARATOR

- Fast acquisition phase lock loop with zero phase restart technique
- Integrated 1,7 RLL Encoder/Decoder
- Fully integrated data separator
  - No external delay lines or active devices required
  - No external active PLL components required
- Programmable decode window symmetry control via serial port
  - Window shift control ± 34.5% (4-bit)
  - Includes delayed read data and VCO clock monitor points
- Programmable write precomp (3-bits each), separate early and late controls
- Hard and soft sector operation
- VCO and Synchronized Read Data test points

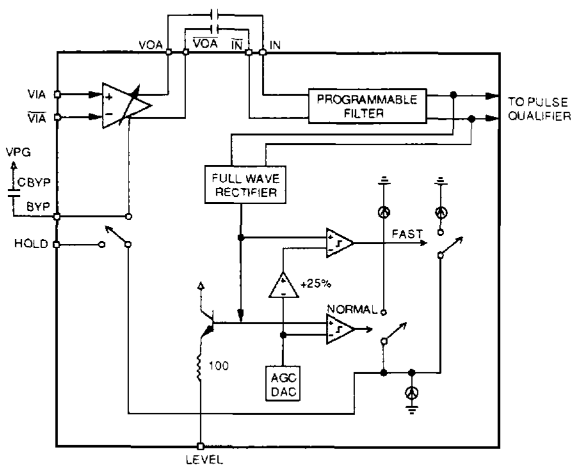


FIGURE 1: AGC Block

FUNCTIONAL DESCRIPTION

The SSI 32P4741/4744/4744A implement a high performance complete read channel, including pulse detector, 4-burst servo capture, programmable active filter, time base generator, and data separator with 1,7 RLL ENDEC, at data rates up to 40 Mbit/s.

PULSE DETECTOR CIRCUIT DESCRIPTION

The pulse detector, in conjunction with the programmable filter, provides all the data processing functions necessary for detection and qualification of encoded read signals. The signal processing circuits include a wide band variable gain amplifier; a wide bandwidth, high precision fullwave rectifier; and a dual rate charge pump. The entire signal path is fully-differential to minimize external noise pick up.

AGC CIRCUIT

The gain of the AGC amplifier is controlled by the voltage (V_{BYP}) stored on the BYP hold capacitor (C_{BYP}), Figure 1. A dual rate charge pump drives C_{BYP} with currents that depend on the instantaneous differential voltage at the DP/DN pins. Attack currents lower V_{BYP} which reduces the amplifier gain, while decay currents increase V_{BYP} which increases the amplifier gain. When the signal at DP/DN is greater than 100% of the programmed AGC level, the nominal attack current of 0.21 mA is used to reduce the amplifier gain. If the signal is greater than 125% of the programmed AGC level, a fast attack current of nine (9) times nominal is used to reduce the gain. This dual rate approach allows AGC gain to be quickly decreased when it is too high yet minimizes distortion when the proper AGC level has been acquired.

A constant decay current of 5 µA acts to increase the amplifier gain when the signal at DP/DN is less than the programmed AGC level. The large ratio (0.21 mA:5 µA) of the nominal attack and nominal decay currents enables the AGC loop to respond to the peak amplitudes of the incoming read signal rather than the average value. A fast decay current mode is provided to allow the AGC gain to be rapidly increased to reduce the recovery time between mode switches.

AGC MODE CONTROL

When write gate (WG) is driven high, the dual rate charge pump is disabled causing the AGC amplifier gain to be held constant. The input impedance of both the AGC amplifier and the programmable filter is reduced. When the WG pin transitions from high to low, the Low-Z mode is activated. In this mode, the input impedance at both the AGC amplifier and the programmable filter remain low to allow for quick recovery of the AC coupling capacitors. Directly following the Low-Z mode is the fast decay mode which allows rapid acquisition of the proper AGC level. In fast decay mode, an internal FET is switched on to drive a high current into the BYP pin. The current remains active until the signal at DP/DN is above 125% of the nominal amplitude, or until an internal timer expires. After the fast decay current is disabled, the normal AGC sequence is enabled. The duration of both the Low-Z and fast decay modes can be set to either 1 µs or 2 µs by programming bit D7 in the N Counter register. A hold/fast decay sequence is also initiated on the edges of servo gate (SG). For the servo sequence the Hold period is nominally 400 ns, during which time the AGC is held to allow for filter settling. The fast decay current is enabled at the end of the Hold period. When the pulse detector is powered-down, V_{BYP} will be held constant subject to leakage currents only. Upon power-up, the Low-Z/fast decay sequence is executed to rapidly recover from any transients or drift which may have occurred on the BYP hold capacitor, refer to Figure 2.

External control for enabling the dual rate charge pump is also provided. Driving the $\overline{\text{HOLD}}$ pin low forces the dual rate charge pump output current to zero. In this mode, V_{BYP} will be held constant subject only to leakage currents.

$\overline{\text{RDIO}}$ Output Pin

A TTL compatible inverted Read Data I/O ($\overline{\text{RDIO}}$) is provided to monitor the pulse detector output. This pin will be held high when SG is low and either RG or WG are high to reduce noise and accompanying jitter during read or write modes. Its falling edge indicates the occurrence of a valid data pulse.

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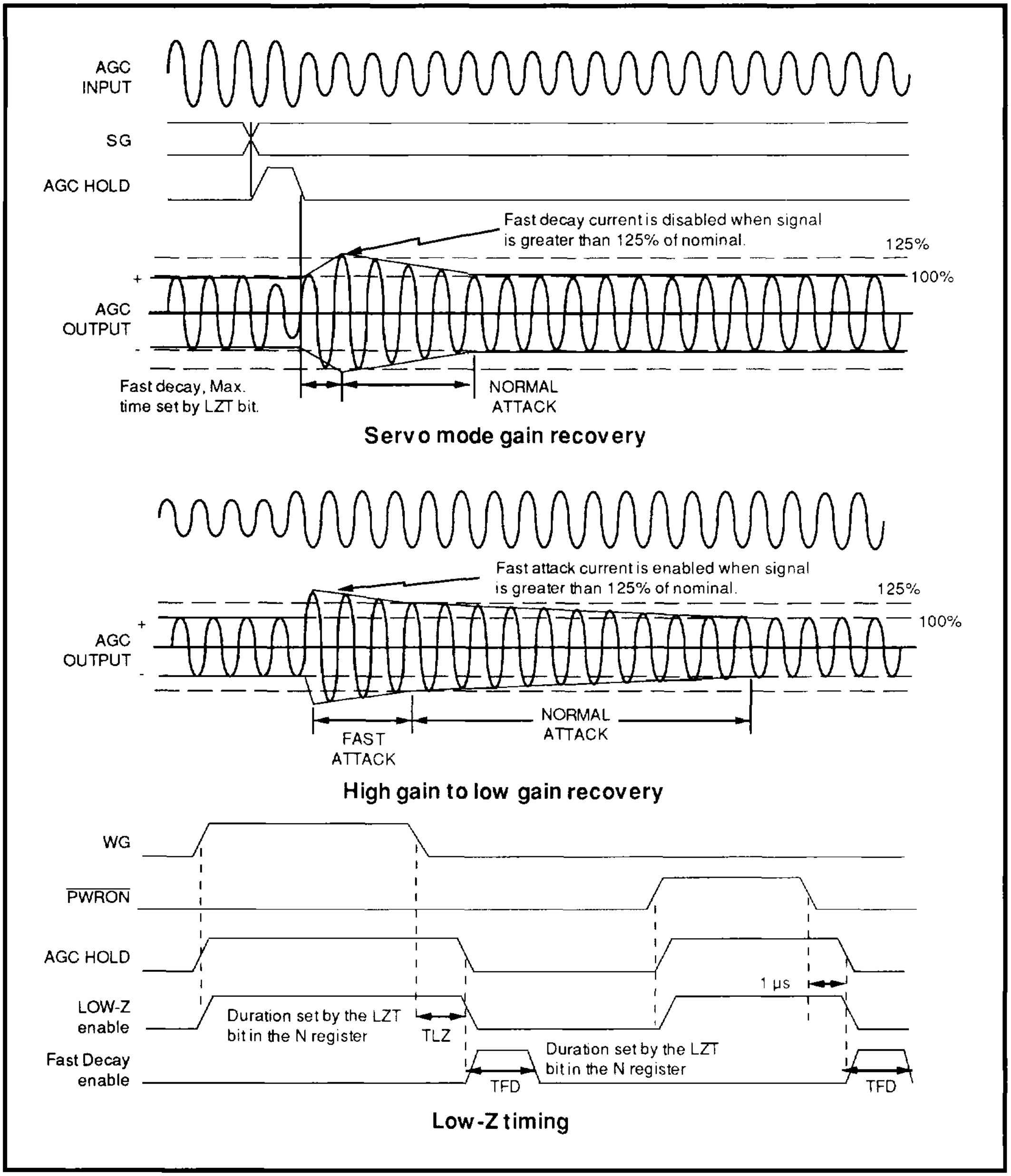

FIGURE 2: AGC Timing Diagrams

FUNCTIONAL DESCRIPTION (continued)

Qualifier Selection

The 32P4741/4744/4744A provide both hysteresis and dual comparator pulse qualification circuits that may be independently selected for read mode and servo mode operation, see Figure 3. For read mode operation the pulse qualifier method is selected by setting the MSB in the data threshold control register (DTCR). The lower 7 bits of the DTCR also set the qualification level of the comparators for read mode. For servo mode operation the pulse qualifier method is selected by setting the MSB in the servo threshold control register (STCR). The lower 7 bits of the STCR set the qualification level of the comparators for servo mode.

DUAL COMPARATOR QUALIFICATION

When in dual comparator mode, independent positive and negative threshold qualification comparators are used to suppress the error propagation of a positive and negative threshold hysteresis comparator. However a slight amount of hysteresis is included to increase the comparator output time when a signal that just exceeds the threshold level is detected. This eases the timing with respect to the zero crossing clock comparator. A differential comparator with programmable hysteresis threshold allows differential signal qualification for noise rejection. The programmable qualification threshold, V_{TH}, is driven by a multiplying DAC which is driven by the LEVEL and referenced to VRC. Qualification thresholds from 30 to 80% may be set with a resolution of better than 1%. A parallel R-C network of RTD and CT sets the qualification threshold time constant when not in the servo mode. A qualified signal zero crossing at the CP-CN inputs triggers the output one shot, Figure 4(a).

HYSTERESIS COMPARATOR QUALIFICATION

When the hysteresis qualification mode is selected, the same threshold qualification comparators and clock comparators are used to implement a polarity checking rule. In this mode, a positive peak that clears the established threshold level will set the hysteresis comparator and trigger the bidirectional one-shot that creates the read data pulses. In order to get another pulse clocked out, a peak of the opposite polarity must clear the negative threshold level to reset the hysteresis comparator and trigger the bidirectional one-shot. Figure 4(b).

SERVO DEMODULATOR CIRCUIT DESCRIPTION

The 32P4741 servo section captures four separate servo bursts and provides A, B, C, and D burst outputs, Figure 5(a). The 32P4744/4744A servo sections capture four separate servo bursts and provide A-B, C-D and A+B burst outputs, Figures 5(b), 5 (c). Internal burst hold capacitors are provided to support low leakage burst capture and reduce external component count. To support embedded servo applications, the 32P4741/4744/4744A provide additional programming registers that set the filter cutoff frequency (fc) and the qualification threshold level (VTH) for servo mode.

SERVO MODE OPERATION

When the servo gate (SG) is asserted, the control DACs for fc and V_{TH} switch from the data mode registers to the servo mode registers and the AGC goes into the hold/fast decay mode. In addition, filter boost is disabled (as determined by the boost control bit), the AGC level is adjusted according to the AGC Level DAC and the RTS servo time constant setting resistor is connected to VRC (VRC is the internal bandgap reference.) By disabling the boost and providing the servo control register for fc the servo signal to noise ratio can be greatly improved. When SG is activated or deactivated there is a nominal 0.3 µs settling time for the internal DACs to recover from the register switching. During servo mode, the AGC circuit remains active. A 4-bit DAC (DACA) is used to set the AGC level over a range of 0.75 to 1 Vp-p as follows:

$$VAGC = 1 - (DACA \times 0.01667)\ Vp\text{-}p$$

where DACA is the value of the AGC Level register.

Typically, a servo preamble is used to achieve the desired AGC level and then the $\overline{HOLD}$ pin is asserted to hold the AGC gain. When SG goes low to terminate the servo mode, the AGC goes into the fast decay mode for 1 µs to allow for fast transition into the read or write mode.

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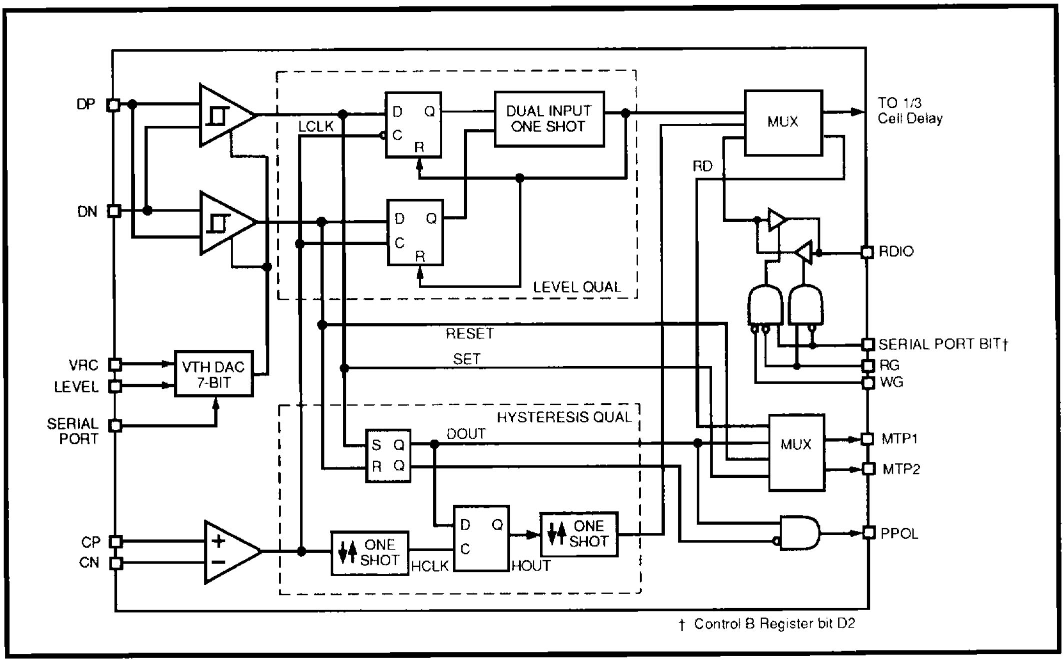

FIGURE 3: Pulse Qualification

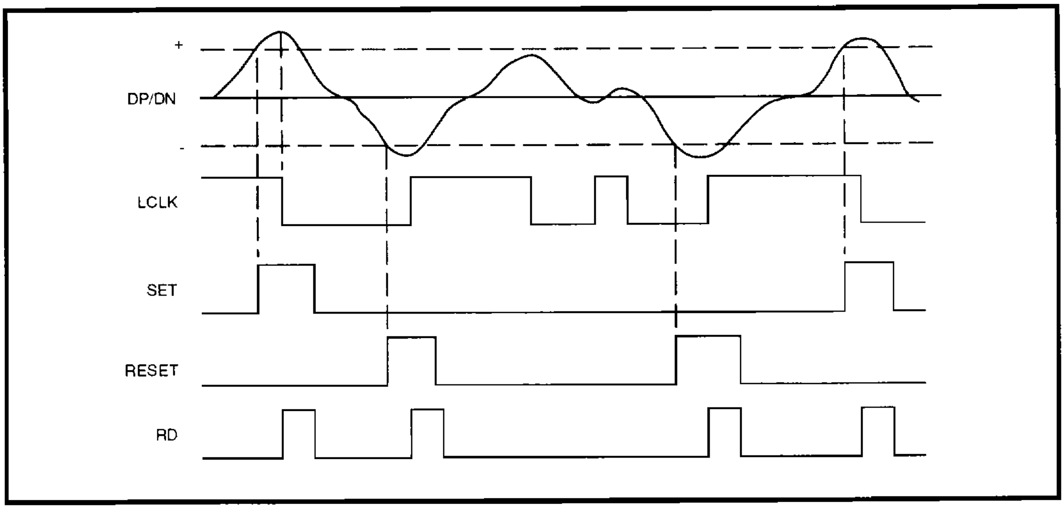

FIGURE 4(a): Dual Comparator Timing Diagram

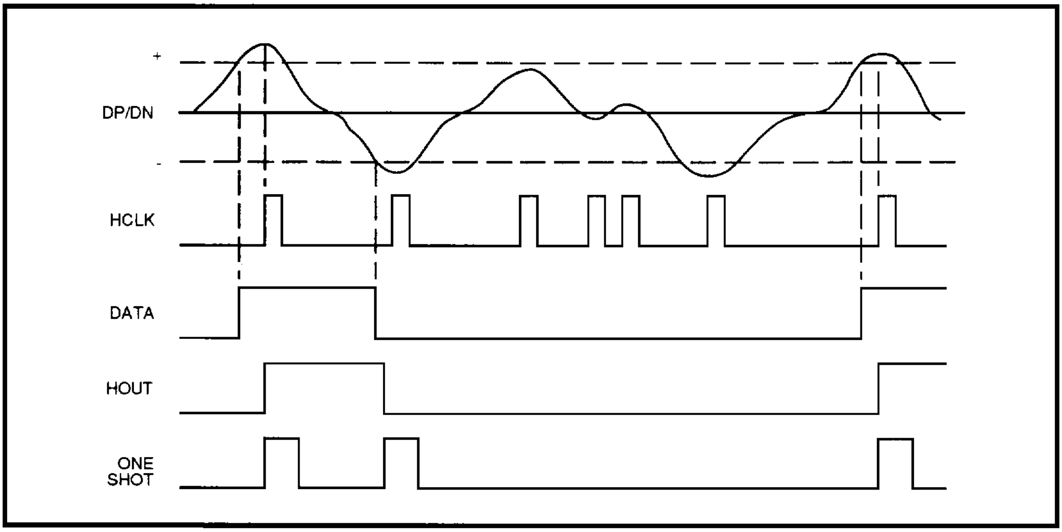

FIGURE 4(b): Hysteresis Comparator Timing Diagram

Burst Capture

The 32P4741 burst capture is controlled by a single external pin designated STROBE and an internal counter. When SG is active, the first pulse on the STROBE pin gates the output of the servo peak detector to the A burst hold capacitor. The capacitor charges for as long as the STROBE pulse is high. On the falling edge of the STROBE signal, the internal counter is incremented. The next STROBE pulse will then gate the servo peak detector output to the B burst hold capacitor. Again, the capacitor charges for as long as the STROBE pulse is high. On the falling edge of STROBE, the counter is incremented again and the C burst is captured on the next STROBE pulse. On the next falling edge of STROBE, the counter is incremented again and the D burst is captured on the next STROBE pulse. After the falling edge of the fourth STROBE pulse, the counter is reset to zero and the burst capture process can be repeated, see Figure 6(a) for timing information. The internal counter is also reset when the SG pin is deactivated. The voltage level on each hold capacitor is then provided to buffer amplifiers which generate the servo output signals. A 1 Vp-p differential voltage at the DP/DN pins will result in a 2.25V peak burst amplitude. The servo output signals (A, B, C, D) are referenced above an internal baseline of 0.5 volts. The output voltage at the MAXREF pin is a nominal 3V, and represents the maximum voltage to which the servo signal outputs will swing. It is typically used as the reference voltage for an external A/D converter. MAXREF is internally reduced to a 0.5 volt level, and establishes the servo zero-signal baseline. All four internal burst hold capacitors are discharged when the RESET pin is driven low.

The 32P4744/4744A burst capture is controlled by four servo control inputs: LATCH0, LATCH1, STROBE and RESET. They control the servo peak sample and hold functions. LATCH0 and LATCH1 are decoded to select one of the four internal burst hold capacitors. Driving the STROBE pin high gates the output of the servo peak detector to the selected internal burst hold capacitor. Reference Figure 6 (b) for servo timing information.

The voltage level on each hold capacitor is then provided to summing amplifiers which generate the servo output signals. For the 32P4744 device, a 1V differential voltage at the DP/DN pins will result in a 2V peak burst amplitude at the A-B, C-D outputs, but only 1V at the A+B output. For the 32P4744A device, a 1V differential voltage at the DP/DN will result in a 1V peak burst amplitude at A-B, C-D and A+B outputs. An input voltage applied to the SREF pin will establish the DC

Burst Capture (continued)

reference voltage for the servo outputs. When A-B = 0, the A-B output will be at SREF. All four hold capacitors are discharged when the $\overline{\text{RESET}}$ pin is driven low.

The $\overline{\text{RESET}}$ control input overrides the STROBE signals. There are two reset modes available. A "0" in the MSB of the Write Precomp/Servo Reset register enables the normal or unidirectional current reset mode. The resulting hold capacitor reset voltage will be slightly less than the zero-signal baseline when observed at the BURST output pins. A "1" written to the MSB location results in a high-resolution, or bi-directional current reset in which the capacitor baseline voltage will be equal to the zero-signal baseline voltage. In general, the high-resolution mode is recommended for most applications.

The drive current of the servo peak detector charge pump is set by a 4-bit word (DACP) addressed through the serial port. The LSB value is 6 µA, and the offset is 1 LSB such that "0000" corresponds to 6 µA and "1111"results in 96 µA. Maximum noise immunity is obtained in the servo peak detector by choosing the smallest value of charge current to charge the internal 10 pF hold capacitor during the burst acquisition time, see Figure 7.

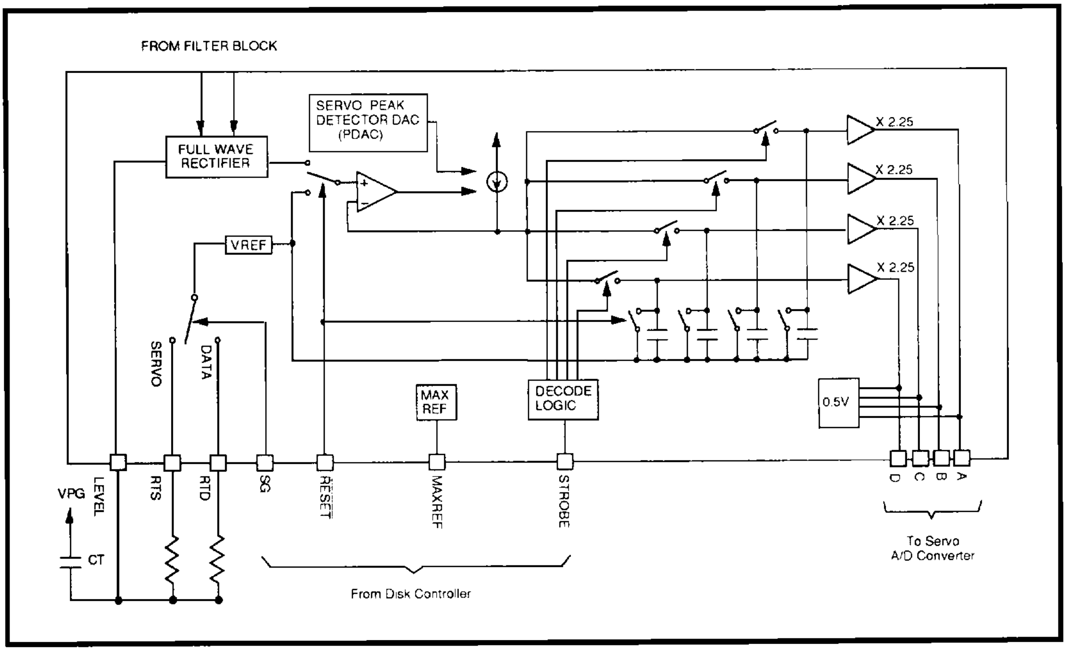

FIGURE 5(a): 32P4741 Servo Capture

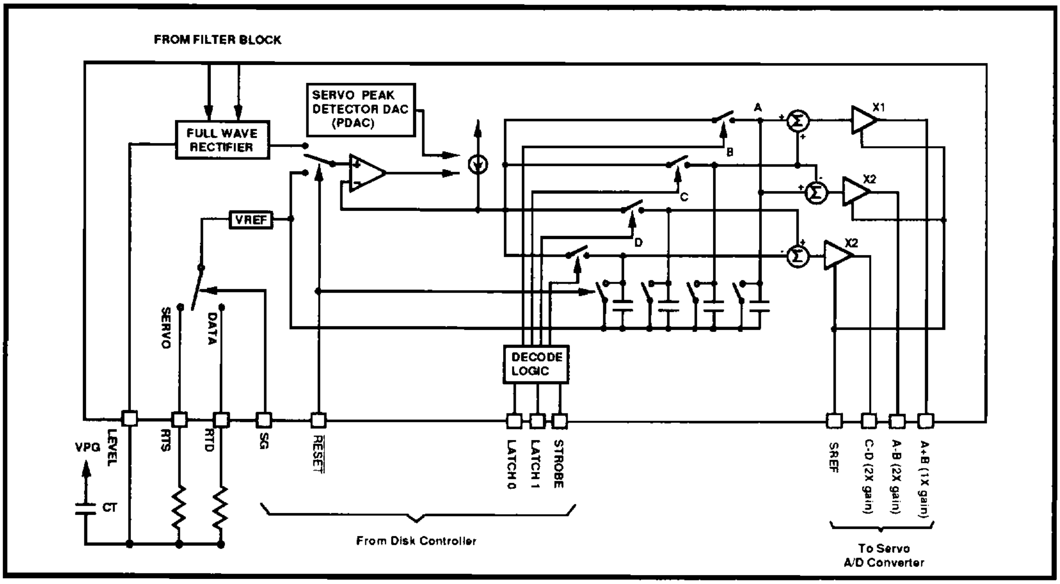

FIGURE 5(b): 32P4744 Servo Capture

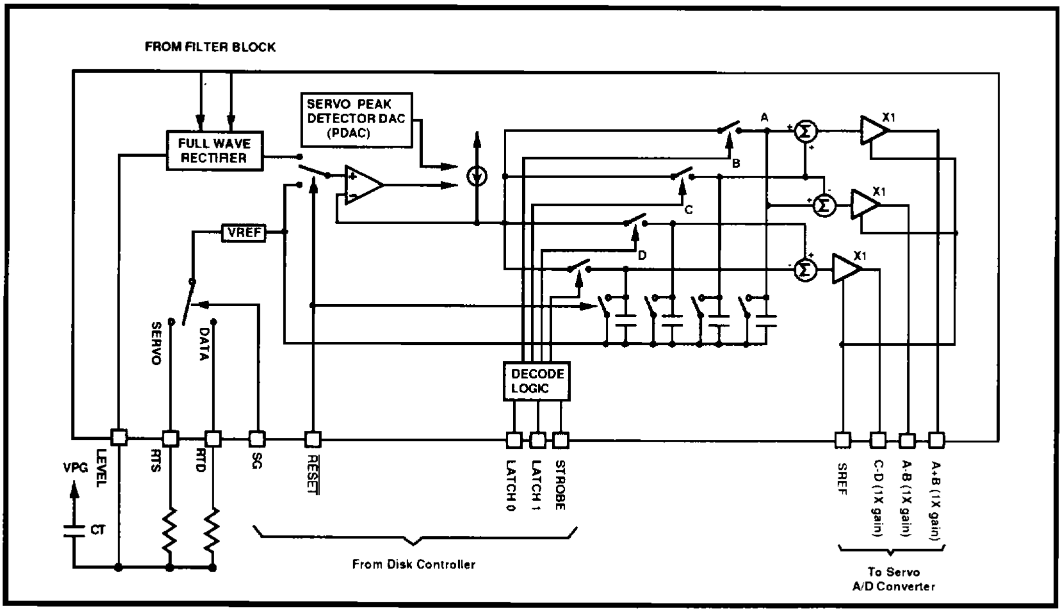

FIGURE 5(c): 32P4744A Servo Capture

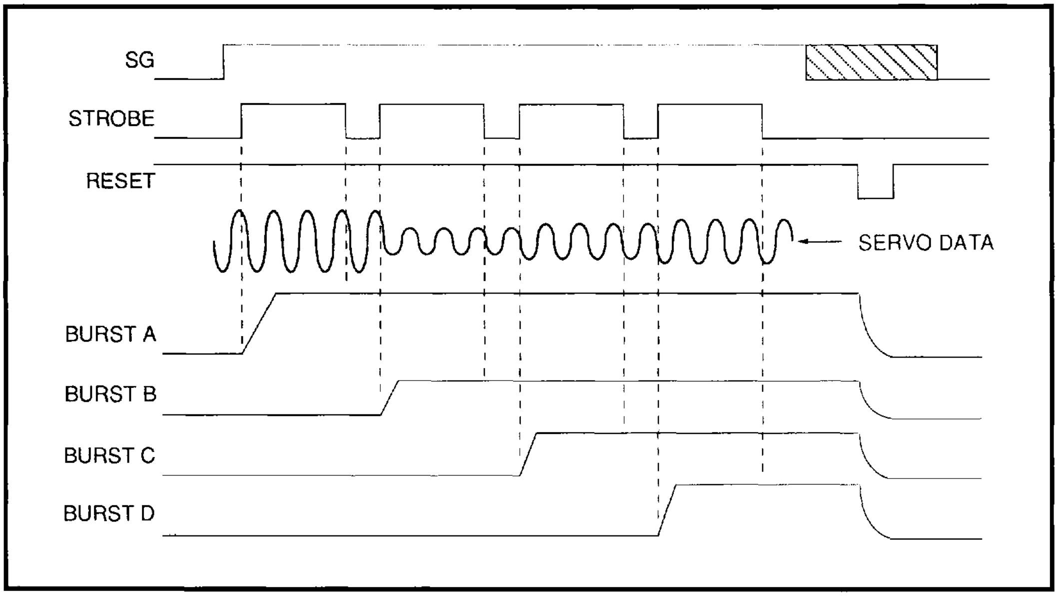

FIGURE 6(a): 32P4741 Servo Capture Timing

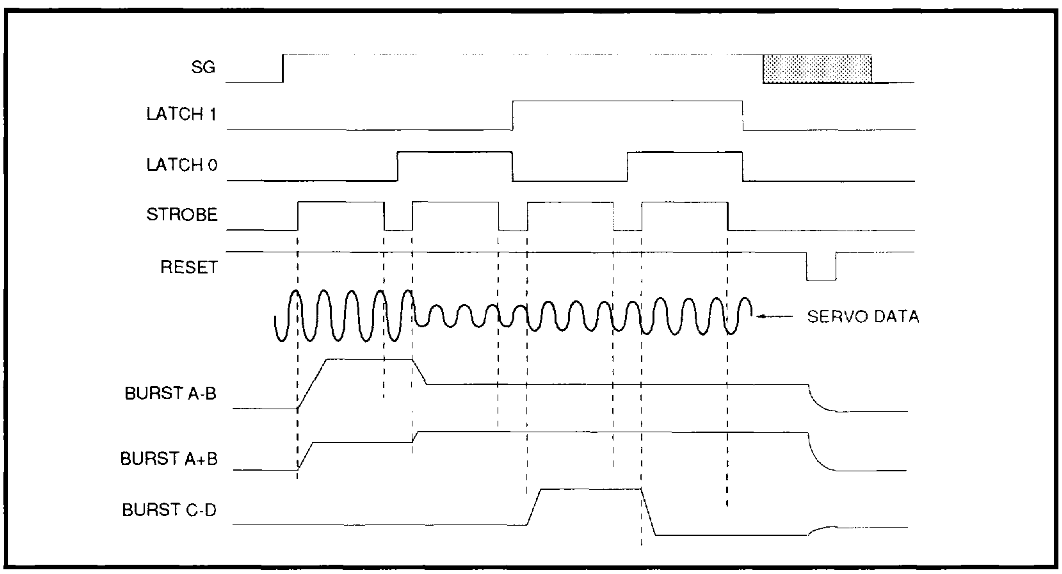

FIGURE 6(b): 32P4744 Servo Capture Timing Diagram

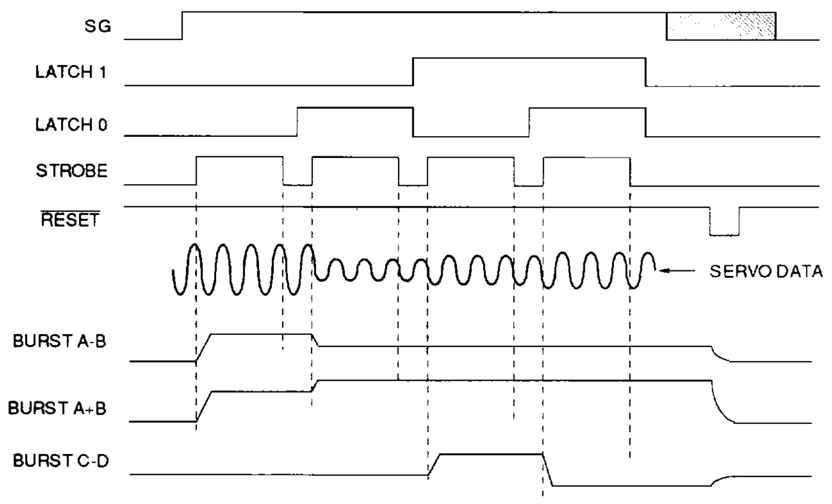

FIGURE 6(c): 32P4744A Servo Capture Timing Diagram

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FUNCTIONAL DESCRIPTION (continued)

Table 1 shows the recommended PDAC settings as a function of the strobe command duration to achieve acquisition to 99.5% of intended final value. These values are calculated with Fservo = 6.66 MHz at DP/DN.

TABLE 1: PDAC Setting vs Strobe Time

PDAC Word	0000	0001	0010	0011	0100	0101	0110	0111	1000
Strobe Time (µs)	6.8	4.8	3.4	2.1	1.5	1.2	0.83	0.77	0.74
PDAC Word	1001	1010	1011	1100	1101	1110	1111		
Strobe Time (µs)	0.71	0.68	0.66	0.64	0.63	0.62	0.61		

The transfer characteristic of the servo demodulator is shown in Figure 8. The peak detector exhibits constant gain for inputs at DP/DN from 0.2 to 1.2 Vp-p with small non-linearities below 0.2V.

TIMING OUTPUTS

To support servo timing recovery, the pulse detector section provides a TTL output of the servo information via the $\overline{\text{RDIO}}$ pin. A negative pulse is generated for each servo peak that is qualified through the pulse detector circuitry. Additional servo timing information is supported by the PPOL output. The PPOL pin provides pulse polarity information for the qualified peaks, where a high level TTL output indicates a positive pulse. To reduce noise progagation, $\overline{\text{RDIO}}$ will be held high and PPOL will be held low when SG is low and either RG or WG are high.

PROGRAMMABLE FILTER CIRCUIT DESCRIPTION

The SSI 32P4741/4744/4744A programmable filter consists of an electronically controlled low-pass filter with a separate differentiated low-pass output. A seven-pole, low-pass filter is provided along with a single-pole, single-zero differentiator. Both outputs have matched group delays (< 1 ns typical.) A fixed delay of 1.25 ns (typ.) is added to the differentiated outputs to guarantee set-up timing in the data qualifier circuit. The delay matching is unaffected by any amount of programmed equalization or bandwidth. Programmable bandwidth and boost/equalization is provided by internal 7-bit control DACs. The programmable characteristics are automatically switched during servo mode to improve signal to noise ratio. Differentiation pulse slimming equalization is accomplished by a two-pole, low-pass with a two-pole, high-pass feedforward section to provide complimentary real axis zeros. A variable attenuator is used to program the zero locations. The filter implements a 0.05 degree equiripple linear phase response.

The normalized transfer functions (i.e., $wc = 2\pi fc = 1$) are:

$$Vnorm/Vi = [(-Ks^2 + 17.98016)/D(s)] \times An$$

and

$$Vdiff/Vi = (Vnorm/Vi) \times (s/0.86133) \times Ad$$

Where D (s)=

$(s^2+1.68495s+1.31703)(s^2+1.54203\ s+2.95139)(s^2+1.14558s+5.37034)(s+0.86133)$,

An and Ad are adjusted for a gain of 2 at $fs=(2/3)fc$.

FILTER OPERATION

AC coupled differential signals from the AGC amplifier are applied to the IN/$\overline{\text{IN}}$ inputs of the filter. To improve settling time of the coupling capacitors, the IN/$\overline{\text{IN}}$ inputs are placed into a Low-Z state for 1 µs when WG goes inactive or when the $\overline{\text{PWRON}}$ pin is brought low. The programmable bandwidth and boost/equalization features are controlled by internal DACs and the registers programmed through the serial port. The current reference for both DACs is set using a single external resistor connected from pin RX to ground. The voltage at pin RX is proportional to absolute temperature (PTAT), hence the current for the DACs is a PTAT reference current. A 1000 pF capacitor should be connected in parallel with RX to reduce harmonic distortion.

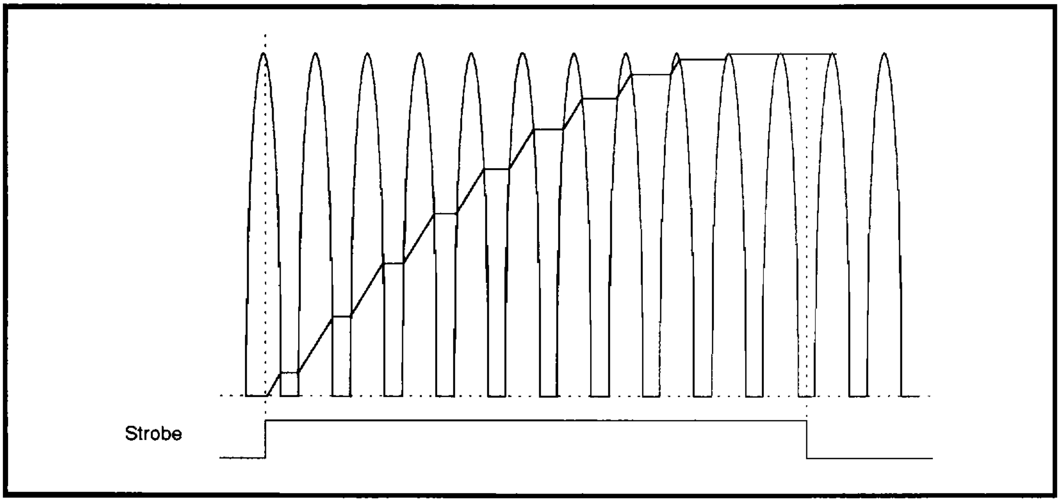

FIGURE 7: Servo Burst Acquisition (SG = $\overline{RESET}$ = 1)

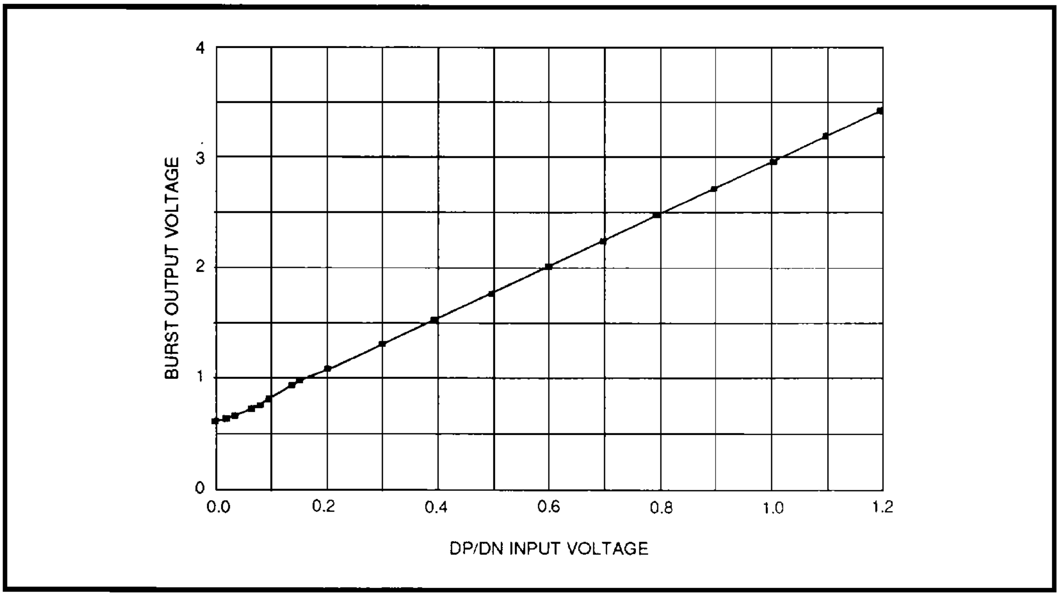

FIGURE 8: Servo Demodulator Transfer Curve

FUNCTIONAL DESCRIPTION (continued)

BANDWIDTH CONTROL

The programmable bandwidth is set by the filter cutoff DAC. This DAC has two separate 7-bit registers that can program the DAC value as follows:

$$fc = 0.1485 \times DACF - 0.9013 \text{ (MHz)}$$

where DACF = DMCR or SMCR value

In the data mode, the Data Mode Cutoff Register (DMCR) is used to determine the filter's 3 dB cutoff frequency. In the servo mode, the Servo Mode Cutoff Register (SMCR) is used. Switching of the registers is controlled by the servo gate (SG) pin. The filter cutoff set by the internal DAC is the unboosted 3 dB frequency. When boost/equalization is added, the actual 3 dB point will move out. Table 2 provides information on boost verses 3 dB frequency.

BOOST/EQUALIZATION CONTROL

The programmable equalization is also controlled by an internal DAC. The 7-bit Filter Boost Control Register (FBCR) determines the amount of equalization that will be added to the 3 dB cutoff frequency, as follows:

$$\text{Boost} = 20 \log[(2.65 \times 10^{-2} \times DACS) + (6 \times 10^{-5} \times DACS \times DACF) + 1] \text{ (dB)}$$

where DACF is the cutoff register and DACS is the boost register.

For example, with the DAC set for maximum output (FBCR = 7F or 127) there will be 13 dB of boost added at the 3 dB frequency. This will result in +10 dB of signal boost above the 0 dB baseline. When SG is active the boost can be disabled by setting bit 7 in FBCR. When bit 7 is "0" and SG is active the boost will automatically be set to 0 dB. If bit 7 is "1" the boost will remain at its programmed value regardless of the state of SG.

TIME BASE GENERATOR CIRCUIT DESCRIPTION

The time base generator, which is a PLL based circuit, provides programmable reference frequency FOUT, see Figure 9. The frequency can be programmed with an accuracy better than 1%. An external passive loop filter is required to control the PLL locking characteristics. The filter is fully-differential and balanced in order to suppress common mode noise.

In read, write and idle modes, the time base generator is programmed to provide a stable reference frequency (FOUT) for the data synchronizer. In write and idle modes, FOUT is the output of the time base generator. In read mode FOUT is disabled after the data synchronizer has achieved lock and switched over to read data as the source for the RRC. This minimizes jitter in the data synchronizer PLL. The reference frequency is programmed using the M and N registers of the time base generator via the serial port, and is related to the external reference clock input, FREF, as follows:

$$FOUT = ((M+1)/(N+1))FREF$$

The VCO center frequency and the phase detector gain of the time base generator are controlled by an internal DAC addressed through the data recovery control register (DRCR). This DAC also sets the 1/3 cell delay, VCO center frequency, and phase detector gain for the data synchronizer circuitry.

TABLE 2: 3 dB Cutoff Frequency versus Boost Magnitude

BOOST (dB)	*fc* Multiplier	BOOST (dB)	*fc* Multiplier
0	1	7	2.42
1	1.21	8	2.51
2	1.50	9	2.59
3	1.80	10	2.66
4	2.04	11	2.73
5	2.20	12	2.80
6	2.32	13	2.86

TIME BASE GENERATOR CIRCUIT DESCRIPTION

Writing to the M and N registers will preload the time base generator for a new FOUT frequency. The actual frequency change is not initiated until data is written to the DRCR, which sets the VCO center frequency. The VCO center frequency equation is:

$$FVCO = [12.5/(RR+0.4)] \times [(0.614 \times IDAC) + 3.84] \text{ MHz}$$

where IDAC is the value in the DRCR and RR is the value (kΩ) of the external RR resistor.

DATA SEPARATOR CIRCUIT DESCRIPTION

The data separator circuit provides complete encoding, decoding, and synchronization for RLL 1,7 format data. In the read mode, the circuit performs sync field search and detect, data synchronization, address mark detection, and data decoding. In the write mode, the circuit provides address mark generation, data encoding, and write precompensation for NRZ data applied to the NRZIN pin. Data rate is established by the time base generator and the internal reference IDAC controlled by the Data Recovery Control Register. The DAC generates a reference current which sets the VCO center frequency, the phase detector gain, and the 1/3 cell delay.

PHASE LOCKED LOOP

The circuit employs a dual mode phase detector; harmonic in the read mode and non-harmonic in the write and idle modes, see Figure 10. In the read mode the harmonic phase detector updates the PLL with each occurrence of a $\overline{\text{DRD}}$ pulse. In the write and idle modes the non-harmonic phase detector is continuously enabled, thus maintaining both phase and frequency lock onto the reference frequency of the internal time base generator. By acquiring both phase and frequency lock to the input reference frequency and utilizing a zero phase restart technique, the VCO transient is minimized and false lock to DRD is eliminated. The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error.

The data synchronizer also requires an external passive loop filter to control its PLL locking characteristics. This filter is also fully-differential and balanced in order to suppress common mode noise.

READ/WRITE MODE CONTROL

The read gate (RG) and write gate (WG) inputs control device operation in data mode. RG is an asynchronous input that must be initiated at the start of a valid preamble field. It can be terminated at any position on the disk. WG is also an asynchronous input. It can be initiated at any time but should not be terminated prior to the last output write data pulse. To ensure that the device will not enter any unknown states, RG overrides WG.

READ MODE

The data synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the decode window. Read gate (RG) initiates the PLL locking sequence and selects the PLL reference input; a high level (read mode) selects the internal $\overline{\text{DRD}}$ signal and a low level selects the reference clock. In the read mode the falling edge of $\overline{\text{DRD}}$ enables the phase detector while the rising edge is phase compared to the rising edge of the VCO reference (VCOR.) As depicted in Figure 11, $\overline{\text{DRD}}$ is a 1/3 NRZ bit cell wide (TVCO) pulse whose leading edge is defined by the falling edge of $\overline{\text{RD}}$. A decode window is developed from the VCOR clock.

READ MODE SOFT SECTOR OPERATION

In soft sector operation the address mark must be detected before RG can be asserted to continue read mode operation. Soft sector operation is entered by driving the AMENB pin high to initiate an address mark search function, see Figure 12. An address mark pattern consists of two 8T patterns followed by two 12T patterns. The address mark detect circuit searches the internal read data ($\overline{\text{RD}}$) for the address mark pattern. First the address mark detect circuit looks for a 6 "0's" within the 8T patterns. Having detected a 6 "0's" the address mark detect circuit then looks for a 9 "0's" within the 12T patterns. If the 9 "0's" pattern is not detected within 5 $\overline{\text{RD}}$ bits after detecting the 6 "0's" pattern, the address mark detect sequence will reset and look for a 6 "0's" pattern again. When the address mark detect circuit has acquired a 6 "0's", 9 "0's" sequence the $\overline{\text{AMD}}$ output transitions low. $\overline{\text{AMD}}$ will remain low until the AMENB input is driven low. Reference Figure 13.

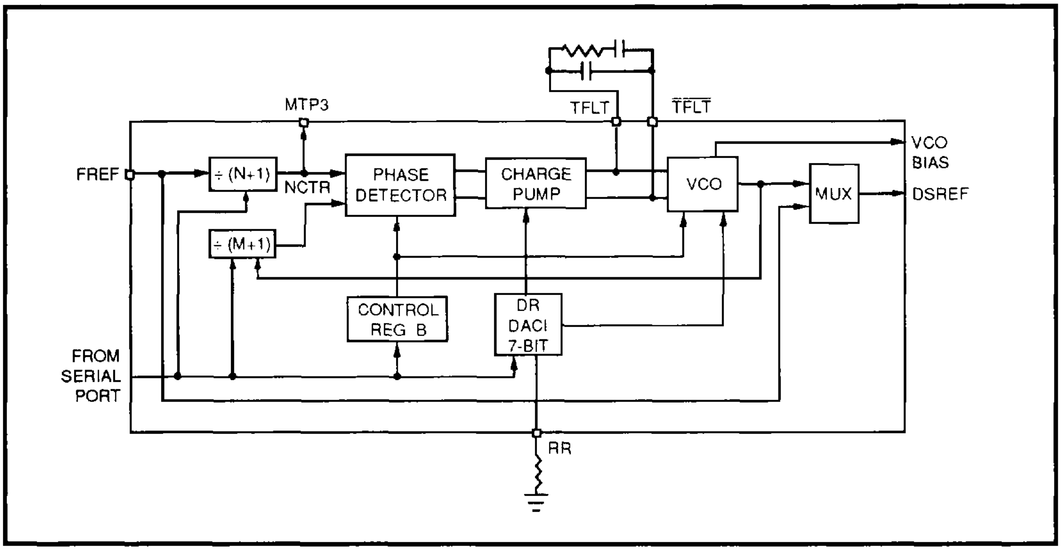

FIGURE 9: Time Base Generator Phase Locked Loop

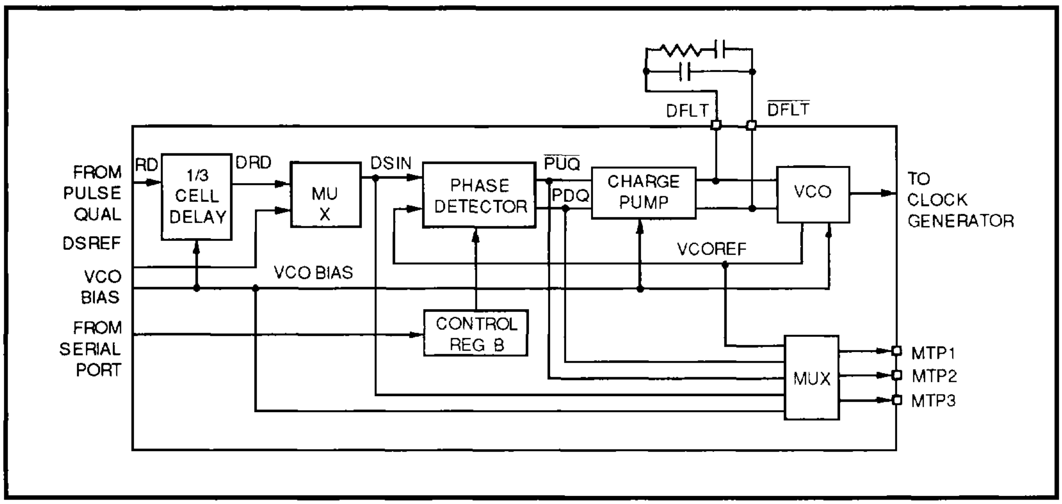

FIGURE 10: Data Separator Phase Locked Loop

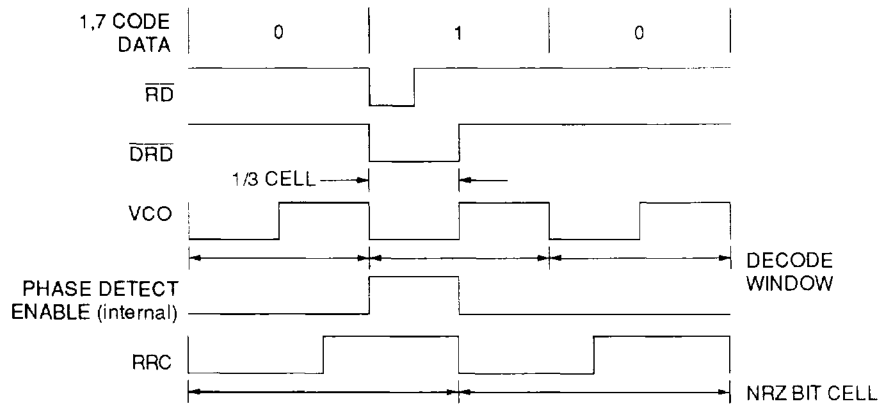

FIGURE 11: Data Synchronization Waveform

FUNCTIONAL DESCRIPTION (continued)

PREAMBLE SEARCH

After the address mark (AM) has been detected, RG can be asserted to initiate the preamble search. When RG is asserted, an internal counter is triggered to count positive transitions of the incoming read data, RD. Once the counter reaches count 3 (3 consecutive 3T patterns detected) the internal read gate is enabled. This switches the phase detector reference from the internal time base to the delayed read data (DRD) signal. At the same time an internal zero phase restart signal restarts the VCO in phase with the DRD. This prepares the VCO to be synchronized to data when the bit sync circuitry is enabled after VCO lock is established, see Figure 14.

VCO LOCK AND BIT SYNC ENABLE

One of two VCO locking modes will be entered depending on the state of the gain shift (GS) bit, or bit 1, in the Control B register. The phase detector will enter a gain shift mode of operation upon the assertion of read gate. The internal read gate is asserted 3 DRD transitions after read gate is asserted. The phase detector then enters a high gain mode of operation to support fast phase acquisition. After an internal counter counts a total of 14 transitions of the internal DRD signal, including the 3 transitions prior to internal read gate, the gain is reduced by a factor of 3 if GS = 1. If GS = 0 the gain remains constant. This gain shift reduction reduces the bandwidth and damping factor of the loop by $\sqrt{3}$ which provides improved jitter performance in the data follow mode. The counter continues to count the next 5 DRD transitions (a total of 19 x 3T from assertion of RG) and then asserts an internal VCO lock signal. The VCO lock signal activates the decoder bit synchronization circuitry to define the proper decode boundaries. The next 2 x 3T patterns are used to set the proper decode window so that VCO is in sync with RRC and RRC is in sync with the data. Following this, the NRZ output is enabled and the data is toggled through the decoder for the duration of the RG.

When the VCO lock signal is asserted, the internal RRC source is also switched from the time base generator to the VCO clock signal that is phase locked to DRD. During the internal RRC switching period the external RRC signal may be held for a maximum of 1 NRZ clock periods, however no short duration glitches will occur.

FUNCTIONAL DESCRIPTION (continued)

Split Field Servo Operation

The data separator circuit supports split field servo operation. For soft sector operation, the AMENB pin is asserted only at the beginning of the data sector (see Figure 15). Within the data sector and following the servo burst, it is not necessary to provide another address mark pattern.

RG can be asserted following the servo burst and the hard sector VCO lock sequence will be initiated. This reduces the overhead required.

READ MODE HARD SECTOR OPERATION

The hard sector operation is entered by holding the AMENB pin low. In hard sector operation, $\overline{AMD}$ remains inactive and the address mark search sequence is not entered. The hard sector read operation starts with assertion of the RG. Once read gate is asserted the VCO lock sequence is identical to the soft sector operation.

WINDOW SHIFT

Shifting the phase of the $\overline{VCO}$ clock effectively shifts the relative position of the $\overline{DRD}$ pulse within the decode window. Decode window control is provided via the WS control bits of the Window Shift Control Register (WSCR). Further description of the WSCR will follow.

NON-READ MODE

In the non-read modes, the PLL is locked to the reference clock. This forces the VCO to run at a frequency which is very close to that required for tracking actual data. When the reference input to the PLL is switched, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse. By minimizing the phase alignment error in this manner, the acquisition time is substantially reduced.

WRITE MODE

In the write mode the circuit converts NRZIN data from the controller into 1,7 RLL formatted data for storage on the disk. In soft sector operation the circuit generates an address mark and a preamble pattern. In hard sector operation the circuit generates the preamble pattern but no preceding address mark. Write mode is entered by asserting WG while the RG is held low. During write mode the VCO and the RRC are referenced to the internal time base generator signal, FOUT.

WRITE MODE SOFT SECTOR OPERATION

In soft sector operation an address mark pattern is written prior to the preamble and encoded data. To initiate the soft sector mode the AMENB is asserted 1 NRZ period after WG is asserted. Once AMENB is asserted, the address mark pattern of two 8T patterns followed by two 12T patterns is automatically generated. Following the address mark pattern, 3T patterns will be generated as long as the NRZIN data is held low. While the address mark and preamble are being written the encoder is active. Therefore, WCLK must be toggling and NRZIN must be held low ("0"). The first non zero NRZIN input bit indicates the end of the preamble pattern. After a delay of 5 NRZIN bit time periods, non-preamble data begins to toggle out of $\overline{WD}$. At the end of the write cycle, 5 bits of blank NRZ time passes to insure the encoder is flushed of data before the WG can be transitioned low. $\overline{WD}$ stops toggling a maximum of 2 NRZ (RRC) time periods after WG goes low. Reference Figures 16 and 17 for detailed timing information.

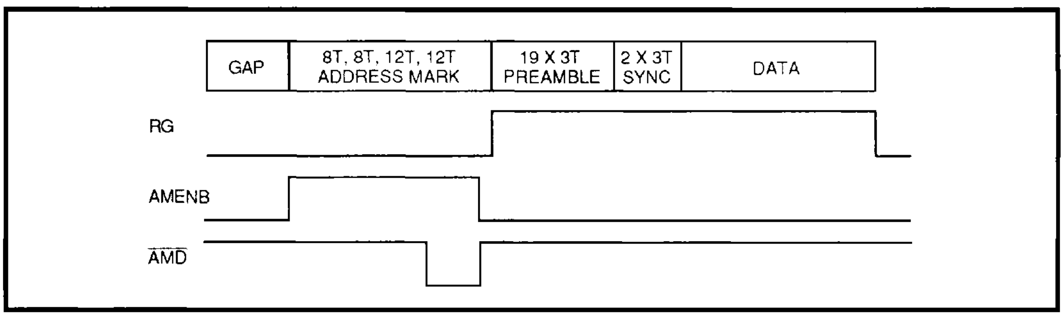

FIGURE 12: Read Mode Soft Sector Operation

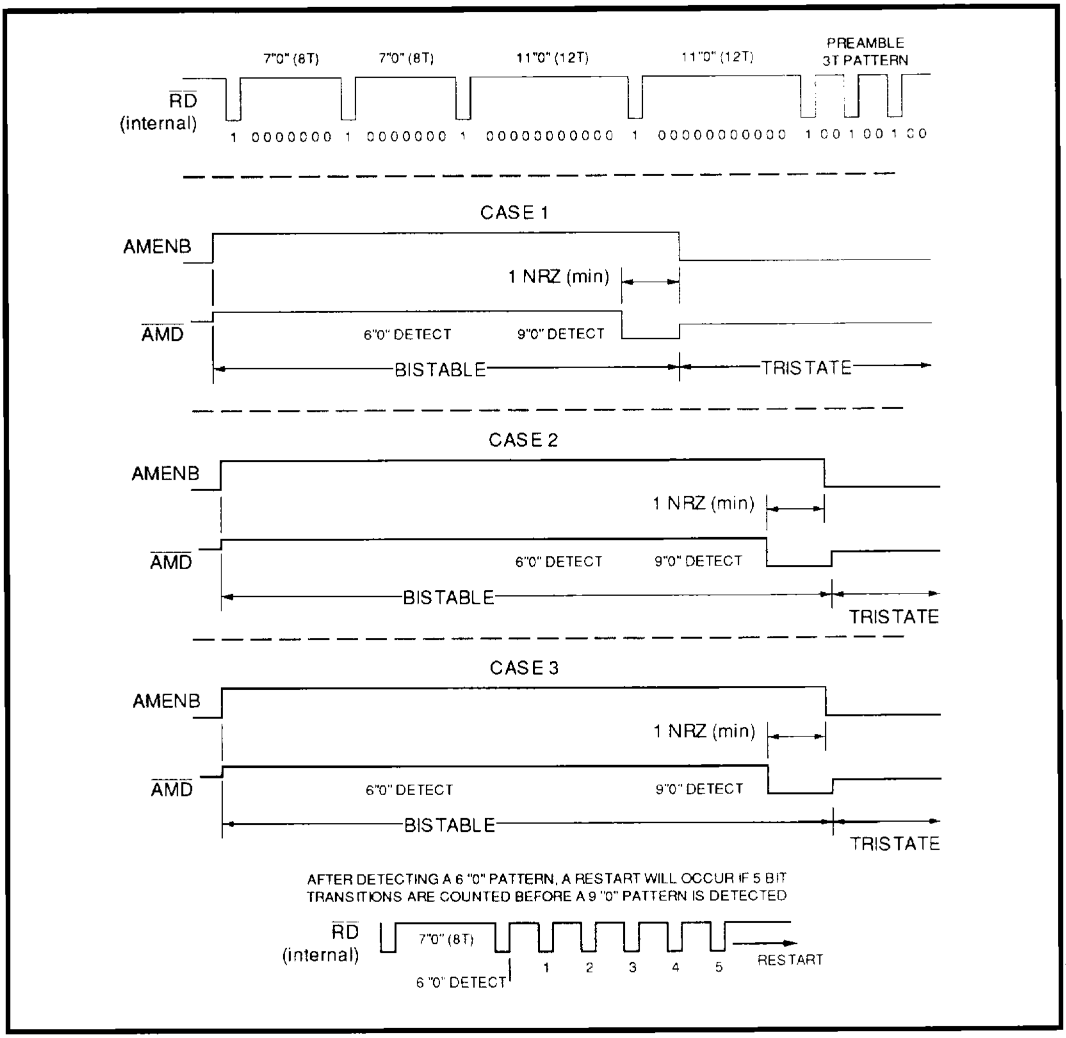

FIGURE 13: Address Mark Search (Soft Sector)

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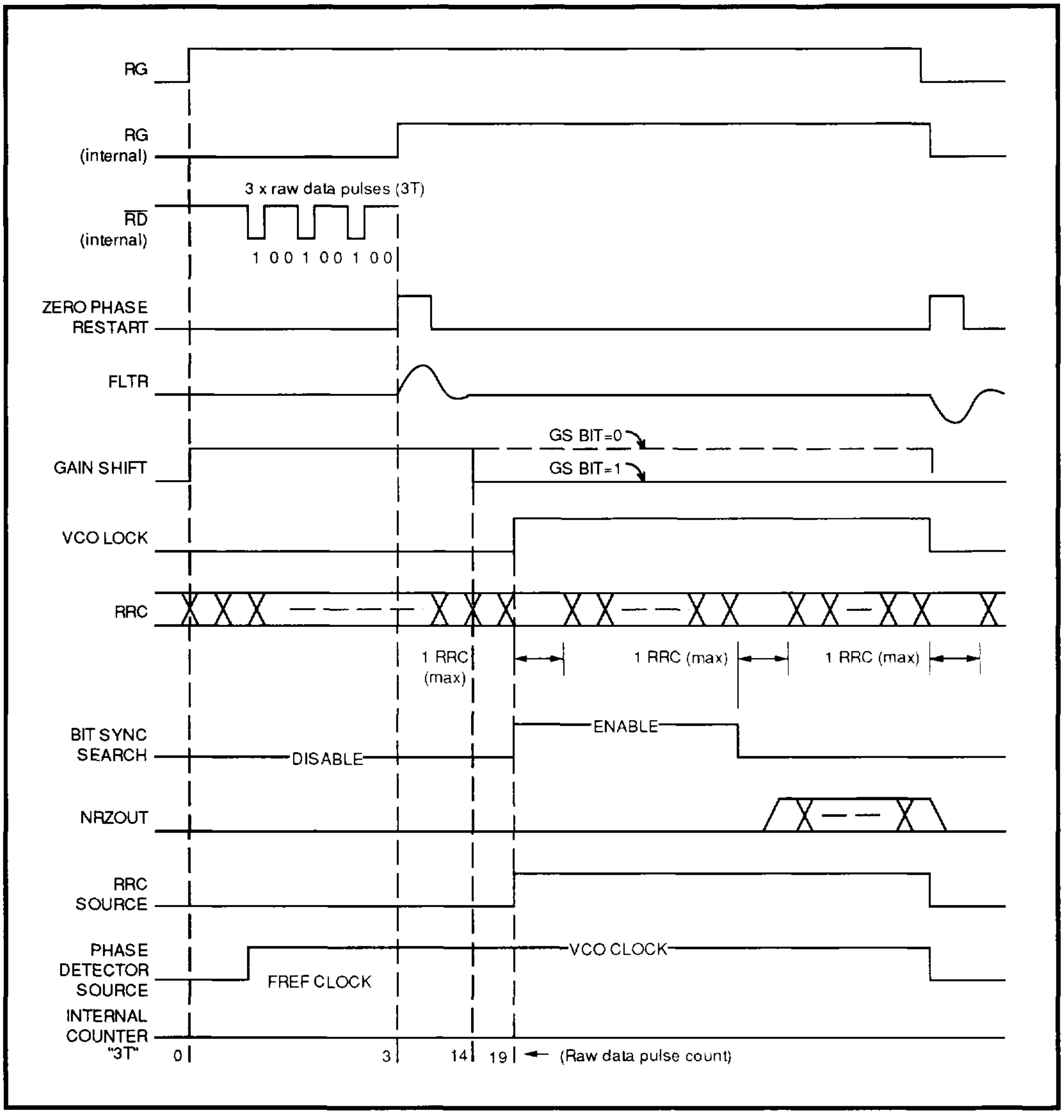

FIGURE 14: Read Mode Locking Sequence

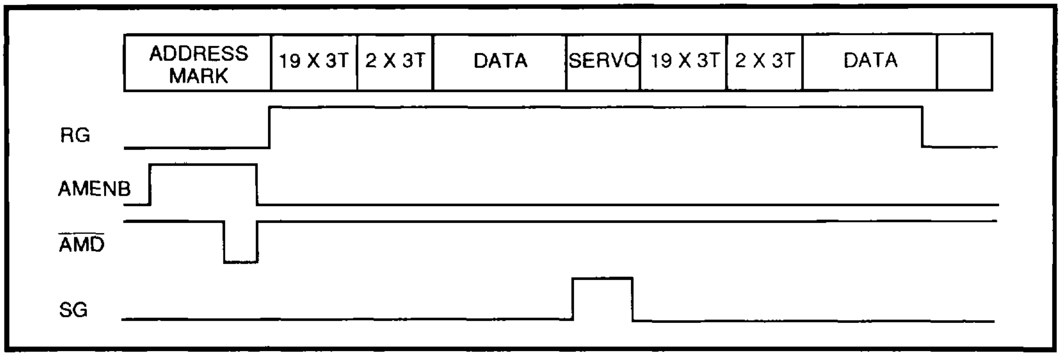

FIGURE 15: Split Field Servo Operation

FUNCTIONAL DESCRIPTION (continued)

WRITE MODE HARD SECTOR OPERATION

In hard sector operation AMENB is held low and no address mark pattern is generated. The preamble pattern is generated in the same sequence as the soft sector operation. During preamble generation the WCLK is toggled and NRZIN data is held low ("0"). Termination of a hard sector write operation follows the same sequence as soft sector mode.

DIRECT WRITE FUNCTION

The 32P4741/4744/4744A include a Direct Write (DW) function that allows the NRZIN data to bypass the encoder and write precomp circuitry. When the DW bit is set in the CBR, the data applied to NRZIN will bypass the encoder and write precomp and directly control the WD output buffer. This allows the user to perform DC erase and media tests.

OPERATING MODES AND CONTROL

The 32P4741/4744/4744A have several operating modes that support read, write, servo, and power management functions. Mode selection is accomplished by controlling the read gate (RG), write gate (WG), servo gate (SG), and $\overline{PWRON}$ pins. Additional modes are also controlled by programming the Power Down Control Register (PDCR), the Control A (CAR) register, and the Control B (CBR) register via the serial port.

EXTERNAL MODE CONTROL

All operating modes of the device are controlled by driving the read gate (RG), write gate (WG), servo gate (SG), and $\overline{PWRON}$ pins with TTL compatible signals. For normal operation the $\overline{PWRON}$ pin is driven low. During normal operation the device is controlled by the read gate (RG), write gate (WG), and servo gate (SG) pins. Servo gate (SG) determines the active mode of the device. When SG is high, the device enters the servo mode, regardless of the state of either RG or WG. When SG is low, RG and WG can be used. When RG is high the device is in read mode regardless of the state of WG. When SG and RG are both low, WG is brought high to enter write mode. If SG, RG, and WG pins are all low the device will be in idle mode (Reference Table 3).

POWER DOWN CONTROL

For power management, the PWRON pin can be used in conjunction with the Power Down Control Register (PDCR) to set the operating mode of the device. The PDCR provides a control bit for each of the functional blocks. When the PWRON pin is brought high ("1") the device is placed into sleep mode (<0.5 mA) and all circuits are powered down except the serial port. This allows the user to program the serial port registers while still conserving power. Register information is retained during the sleep mode so it is not necessary to reprogram the serial port registers after returning to an

FUNCTIONAL DESCRIPTION (continued)

active mode. When the $\overline{\text{PWRON}}$ pin is driven low ("0"), the contents of the PDCR determine which blocks will be active. Register mapping for the PDCR is shown in Table 4. To improve recovery time from the sleep mode, the inputs to the AGC, Filter and DP/DN are placed into a Low-Z mode.

SERIAL INTERFACE OPERATION

The serial interface is a bi-directional port for reading and writing programming data from/to the internal registers of the 32P4741/4744/4744A. For data transfers SDEN is brought high, serial data is presented at the SDATA pin, and a serial clock is applied to the SCLK pin. After the SDEN goes high, the first 16 pulses applied to the SCLK pin will shift the data presented at the SDATA pin into an internal shift register on the rising edge of each clock, see Figure 18(a). An internal counter prevents more than 16 bits from being shifted into the register. The data in the shift register is latched when SDEN goes low. If less than 16 clock pulses are provided before SDEN goes low, the data transfer is aborted.

All transfers are shifted into the serial port LSB first. The first byte of the transfer is address and instruction information. The LSB of this byte is the R/W bit which determines if the transfer is a read (1) or a write (0). The remaining 7-bits determine the internal register to be accessed. Table 4 provides register mapping information. The second byte contains the programming data. In read mode (R/W = 1) the 32P4741/4744/4744A will output the register contents of the selected address. In Write mode the device will load the selected register with data presented on the SDATA pin. At initial power-up, the contents of the internal registers will be in an unknown state and they must be programmed prior to operation. During power down modes, the serial port remains active and register programming data is retained. Detailed timing information is provided in Figure 18(b) and in the electrical specifications.

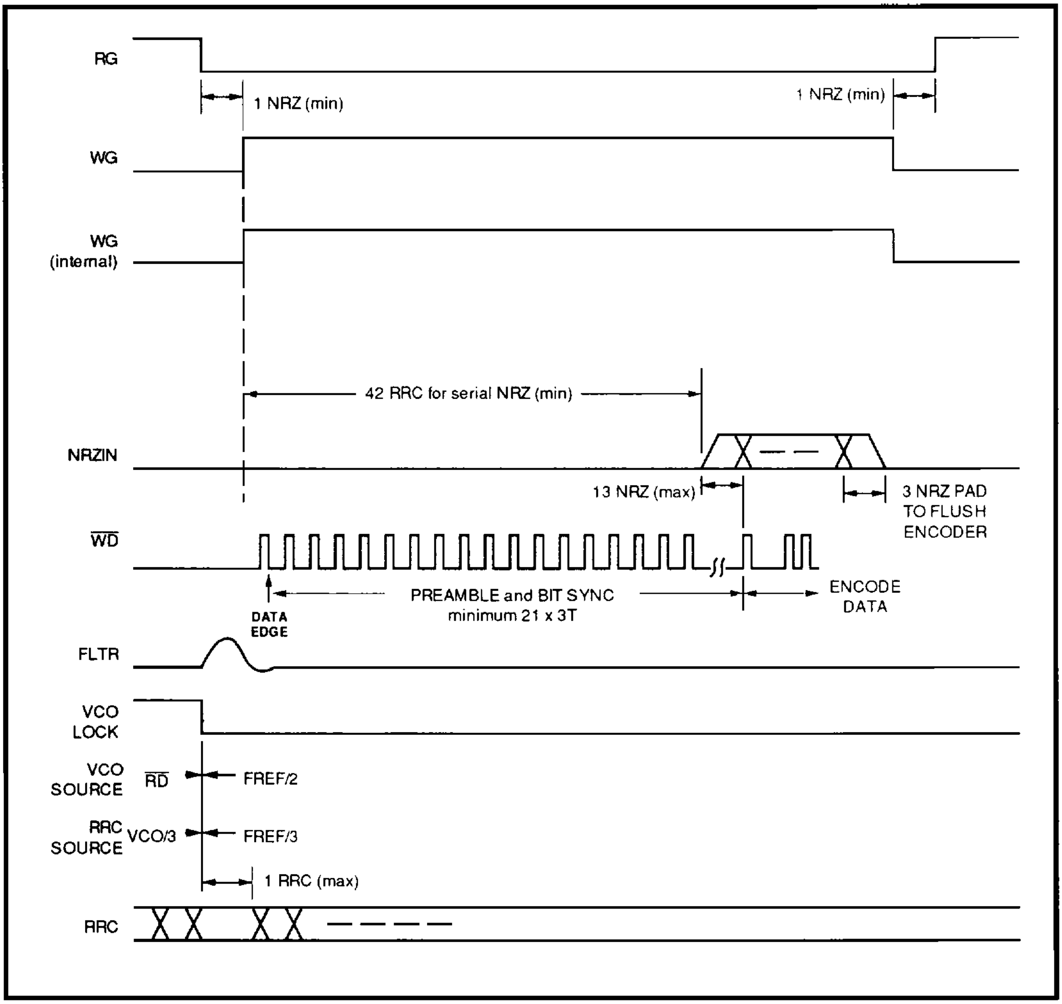

FIGURE 16: Write Data Operation

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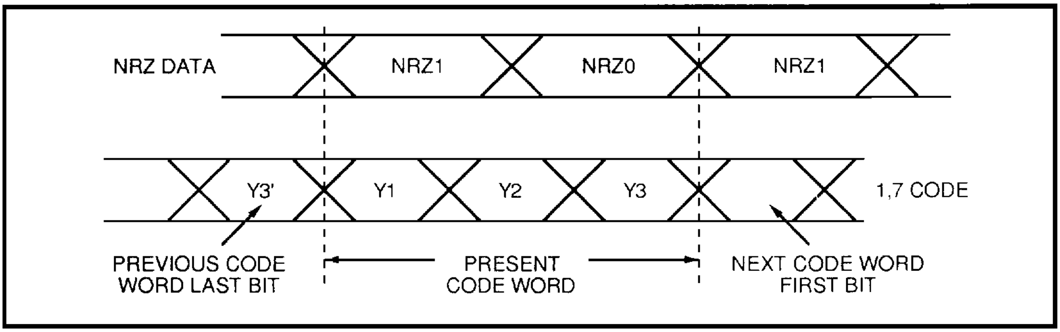

FIGURE 17: NRZ Data Word to 1,7 Code Word Bit Comparison
(Reference Table 4 for decode scheme)

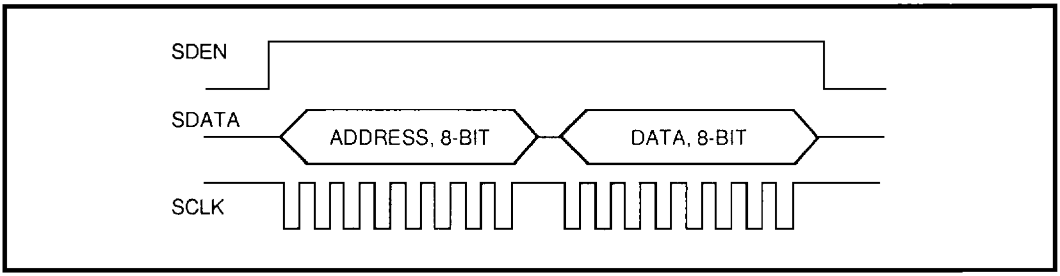

FIGURE 18(a): Serial Port Data Transfer Format

CONTROL REGISTERS

The serial port registers allow the user to configure the device. The register map for the device is shown in Table 4. The bits of these registers are defined as follows:

POWER DOWN CONTROL REGISTER (PDCR)

BIT	NAME	DESCRIPTION
0	PD/SVO	Pulse detector/servo power enable: Determines the state of the pulse detector and servo circuits when $\overline{PWRON}$ pin is low. 0 = Circuits enabled 1 = Circuits powered down
1	TBGKD	Time base KD select: Determines the phase detector gain of the time base generator. 0 = KD is 3x nominal value 1 = KD is 1x nominal value
2	FLTR	Filter power enable: Determines the state of the filter when $\overline{PWRON}$ pin is low. 0 = Filter enabled 1 = Filter powered down
3	DS	Data separator power enable: Determines the state of the data separator circuit when $\overline{PWRON}$ pin is low. 0 = Data separator enabled 1 = Data separator powered down
4	TBG	Time base generator power enable: Determines the state of the time base generator circuit when $\overline{PWRON}$ pin is low. 0 = Time base generator enabled 1 = Time base generator powered down
5-7	N/A	Device ID: These bits are a read only ID code for the device.

DATA MODE CUTOFF (DACF)

0-6	DMC	Filter cutoff setting for data mode. Substitute this value for DACF into the cutoff calculation for the filter in data mode operation.
7	N/A	Not used. Set to zero.

SERVO MODE CUTOFF (DACF)

0-6	SMC	Filter cutoff setting for servo mode. Substitute this value for DACF into the cutoff calculation for the filter in servo mode operation.
7	N/A	Not used. Set to zero

CONTROL REGISTERS (continued)

FILTER BOOST REGISTER (DACS)

BIT	NAME	DESCRIPTION
0-6	FBC	Filter boost setting. Substitute this value for DACS into filter calculations.
7	SBE	Servo boost enable: Determines if boost is enabled when SG is high. 0 = Boost disabled when SG is high 1 = Boost enabled when SG is high

DATA THRESHOLD REGISTER (VTHDAC)

0-6	DTH	Data threshold setting. Substitute this value for VTHDAC into the threshold calculation for data mode operation.
7	DQ	Qualifier select: Determines the type of qualifier used in data mode. 0 = Hysteresis qualifier 1 = Dual comparator qualifier

SERVO THRESHOLD REGISTER (VTHDAC)

0-6	STH	Servo threshold setting. Substitute this value for VTHDAC into the threshold calculation for servo mode operation.
7	SQ	Qualifier select: Determines the type of qualifier used in servo mode. 0 = Hysteresis qualifier 1 = Dual comparator qualifier

CONTROL A REGISTER (CAR)

BIT	NAME	DESCRIPTION
0	EPDT	Enable Phase Detector (Time Base Generator): This bit disables the output of the phase detector to the VCO. An external voltage applied across the TFLT pins drives the VCO to a fixed frequency. 0 = Phase detector charge pump disabled 1 = Phase detector charge pump enabled
1	UT	Enable Pump Up Current (Time Base Generator): This bit enables a test mode for checking the charge pump output current. The charge pump will source a fixed DC current from TFLT and sink the current at $\overline{\text{TFLT}}$. 0 = No current 1 = Pump up current enabled
2	DT	Enable Pump Down Current (Time Base Generator): This bit enables a test mode for checking the charge pump output current. The charge pump will source a fixed DC current from $\overline{\text{TFLT}}$ and sink the current at TFLT. 0 = No current 1 = Pump down current enabled
3	MTP3E	This bit enables the MTP3 test point output buffer. 0 = Test point disabled 1 = Test point enabled
4	BYPT	This bit enables a time base generator bypass mode where the FREF input is connected to the data separator phase detector input. 0 = Time base enabled 1 = Time base bypassed
5/6	TMS0/1	These bits select the test point signal sources (ref Table 7)
7	FDTM	This bit continuously enables the AGC fast decay current. 0 = Fast decay current always on 1 = Normal fast decay operation Set to 1 for normal operation.

CONTROL REGISTERS (continued)

CONTROL B REGISTER (CBR)

BIT	NAME	DESCRIPTION
0	DW	This bit enables the direct write (Bypass Endec) function. 0 = Normal operation 1 = Bypass encoder, NRZ0 buffered to WD (or WD/$\overline{WD}$)
1	GS	This enables the data sep. phase detector gain switch in read mode. 0 = Normal operation 1 = Gain shift until 14 x 3T (read mode only)
2	RDI	This bit enables the $\overline{RDIO}$ pin as an input. 0 = $\overline{RDIO}$ is an output 1 = $\overline{RDIO}$ is an input
3	EPDD	Enable Phase Detector (Data Separator): This bit disables the output of the phase detector to the VCO. An external voltage applied across the DFLT pins drives the VCO to a fixed frequency. 0 = Phase detector charge pump disabled 1 = Phase detector active
4	UD	Enable Pump Up Current (Data Separator): This bit enables a test mode for checking the charge pump output current. The charge pump will source a fixed DC current from DFLT and sink the current at $\overline{DFLT}$. 0 = No current 1 = Pump up current enabled
5	DD	Enable Pump Down Current (Data Separator): This bit enables a test mode for checking the charge pump output current. The charge pump will source a fixed DC current from $\overline{DFLT}$ and sink the current at DFLT. 0 = No current 1 = Pump down current enabled
6	MTP1, 2E	This bit enables the multiplexed test points (MTP1, 2) 0 = Test points disabled 1 = Test points enabled
7	-	Not used. Set to zero.

N COUNTER REGISTER

0-6	N	N counter value.
7	LZT	Low-Z time period: Determines the time period for the Low-Z and fast decay one-shots. 0 = 1 µs nominal time-out (0.4 µs on SG edges) 1 = 2 µs nominal time-out (0.5 µs on SG edges)

M COUNTER REGISTER

0-7	M	M counter value.

DATA RECOVERY REGISTER (DRCR)

BIT	NAME	DESCRIPTION
0-6	IDAC	Center frequency DAC value. Sets the center frequency for the data synchronizer VCO and the TBG VCO.
7	TM	Test mode bit: SSi use only. Set to 0 for normal operation.

WINDOW SHIFT REGISTER (WSR)

0-3	WS	Window shift DAC value.
4	WSD	Window shift direction. 0 = Early 1 = Late
5	WSE	Window shift enable. 0 = Disable 1 = Enable
6-7	TDAC0/1	DACOUT test point select: Selects the DAC output to be provided on the DACOUT test point. The preferred setting when DACOUT is not being monitored is to set TDAC0 = 1 and TDAC1 = 0:

TDAC1	TDAC0	DAC MONITORED
0	0	Filter Fc DAC
0	1	Qualifier threshold DAC (VTH)
1	0	Window shift DAC
1	1	Write precomp DAC; the selection of the early or late DAC is controlled by the WPE bit. WPE = 0 — Late WPE = 1 — Early

WRITE PRECOMP REGISTER (WPR)

0-2	WPE	Write precomp early DAC value.
3	WPE	Write precomp enable. 0 = Disable 1 = Enable
4-6	WPL	Write precomp late DAC value.
7	SRST	Servo reset select. Set to 1 for normal operation.

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CONTROL REGISTERS (continued)

AGC LEVEL REGISTER (ALR)

BIT	NAME	DESCRIPTION
0-3	ADAC	AGC level DAC value. Sets AGC level in servo mode. 0000 = 1 Vp-p 1111 = 0.75 Vp-p
4-7	PDAC	Servo peak detector current DAC value. Sets the servo peak detector current in 6 µA steps. 0000 = 6 µA charge current 1111 = 96 µA charge current

TABLE 3: Mode Control Table

CONTROL LINE: $\overline{PWRON}$	RG	SG	WG	DEVICE MODE	DAC CONTROL: VTH	FC	BOOST	HYSTERESIS
1	X	X	X	**SLEEP MODE:** All functions are powered down. The serial port registers remain active and register programming data is saved.	off	off	off	off
0	0	0	1	**WRITE MODE:** The pulse detector is inactive. The data synchronizaer VCO is locked to the internal time base generator. Write precomp circuit is clocked by internal time base.	DR	DR	DR	DR
0	1	0	X	**READ MODE:** The pulse detector is active. The data synchronizer begins the preamble lock sequence.	DR	DR	DR	DR
0	X	1	X	**SERVO MODE:** The pulse detector is active and the servo control registers are enabled for the Fc DAC and the VTH DAC. $\overline{RDIO}$ is also active. The data synchronizer and time base generator can be disabled using the PDCR.	SR	SR	off (On if SBE = 1)	DR
0	0	0	0	**IDLE MODE:** The contents of the PDCR determine which blocks are powered-up. In normal operation with all blocks powered-up, the pulse detector is active, the data synchronizer VCO is locked to the time base generator, and the data control registers are used for VTH and FC.	DR	DR	DR	DR
				If multiple control signals are active, the priority order will be $\overline{PWRON}$, SG, RG, and WG. For example, if SG and RG are both "1", the Servo mode will be active.				

DAC Control Key: DR = data register, SR = servo register, off = disabled

TABLE 4: Serial Port Register Mapping

REGISTER NAME	A6	ADDRESS					A0	R/W	D7	DATA BIT MAP						D0
POWER DOWN CONTROL	0	0	0	0	0	1	0	0	–	–	–	TBG 1 = Disable 0 = Enable	DATA SEP 1 = Disable 0 = Enable	FILTER 1 = Disable 0 = Enable	TBG KD 1 = 1x KD 0 = 3 x KD	PD/SERVO 1 = Disable 0 = Enable
DATA MODE CUTOFF	0	0	0	0	0	1	1	0	*	F_{CD}DAC BIT 6	F_{CD}DAC BIT 5	F_{CD}DAC BIT 4	F_{CD}DAC BIT 3	F_{CD}DAC BIT 2	F_{CD}DAC BIT 1	F_{CD}DAC BIT 0
SERVO MODE CUTOFF	0	0	1	0	0	1	1	0	*	F_{CS}DAC BIT 6	F_{CS}DAC BIT 5	F_{CS}DAC BIT 4	F_{CS}DAC BIT 3	F_{CS}DAC BIT 2	F_{CS}DAC BIT 1	F_{CS}DAC BIT 0
FILTER BOOST	0	0	0	1	0	1	1	0	Servo Boost 1 = Enable 0 = Disable	F_{B}DAC BIT 6	F_{B}DAC BIT 5	F_{B}DAC BIT 4	F_{B}DAC BIT 3	F_{B}DAC BIT 2	F_{B}DAC BIT 1	F_{B}DAC BIT 0
DATA THRESHOLD	0	0	0	1	0	1	0	0	Data Qual. 1 = Dual 0 = Hys	T_{D}DAC BIT 6	T_{D}DAC BIT 5	T_{D}DAC BIT 4	T_{D}DAC BIT 3	T_{D}DAC BIT 2	T_{D}DAC BIT 1	T_{D}DAC BIT 0
SERVO THRESHOLD	0	0	1	0	0	1	0	0	Servo Qual. 1 = Dual 0 = Hys	T_{S}DAC BIT 6	T_{S}DAC BIT 5	T_{S}DAC BIT 4	T_{S}DAC BIT 3	T_{S}DAC BIT 2	T_{S}DAC BIT 1	T_{S}DAC BIT 0
CONTROL A	0	0	1	1	0	1	0	0	FD Test 1 = Disable 0 = Enable	TMS1	TMS0	TBG 1 = Bypass 0 = Normal	MTP3 1 = Enable 0 = Disable	PUMP DWN 1 = ON 0 = OFF	PUMP UP 1 = ON 0 = OFF	PHASE DET 1 = Enable 0 = Disable
CONTROL B	0	0	0	1	1	0	0	0	*	MTP1/2 1 = Enable 0 = Disable	PUMP DWN 1 = ON 0 = OFF	PUMP UP 1 = ON 0 = OFF	PHASE DET 1 = Enable 0 = Disable	RDI 1 = Input 0 = Output	GAIN SHFT 1 = ON 0 = OFF	DIR WRITE 1 = ON 0 = OFF
N COUNTER	0	0	0	0	1	1	0	0	Low-Z Time 1 = 2 µs 0 = 1 µs	N COUNT BIT 6	N COUNT BIT 5	N COUNT BIT 4	N COUNT BIT 3	N COUNT BIT 2	N COUNT BIT 1	N COUNT BIT 0
M COUNTER	0	0	0	1	1	1	0	0	M COUNT BIT 7	M COUNT BIT 6	M COUNT BIT 5	M COUNT BIT 4	M COUNT BIT 3	M COUNT BIT 2	M COUNT BIT 1	M COUNT BIT 0
DATA RECOVERY	0	0	0	0	1	0	0	0	Test Mode 1 = Reset 0 = Normal	DAC BIT 6	DAC BIT 5	DAC BIT 4	DAC BIT 3	DAC BIT 2	DAC BIT 1	DAC BIT 0
WINDOW SHIFT	0	0	0	0	1	0	1	0	TDAC 1	TDAC 0	WIN SHFT 1 = Enable 0 = Disable	WS DIR 1 = Late 0 = Early	$\overline{WS3}$	$\overline{WS2}$	$\overline{WS1}$	$\overline{WS0}$
WRITE PRECOMP	0	0	0	1	1	0	1	0	Servo Reset 1 = Hi Res 0 = Normal	$\overline{WL2}$	$\overline{WL1}$	$\overline{WL0}$	WR PRCMP 1 = Enable 0 = Disable	$\overline{WE2}$	$\overline{WE1}$	$\overline{WE0}$
AGC LEVEL	0	1	0	0	0	1	0	0	PDAC BIT 3	PDAC BIT 2	PDAC BIT 1	PDAC BIT 0	ADAC BIT 3	ADAC BIT 2	ADAC BIT 1	ADAC BIT 0

* Denotes Silicon Systems internal test bits. These bits should be set to 0 in normal operation.

PIN DESCRIPTION

POWER SUPPLY PINS

NAME	TYPE	DESCRIPTION
VPA	-	Data separator PLL analog power supply pin.
VPB	-	Time base generator PLL analog power supply pin.
VPC	-	Internal ECL, CMOS logic power supply pin.
VPD	-	TTL buffer I/O digital power supply pin.
VPG	-	Pulse detector, filter, servo analog power supply pin.
VNA	-	Data separator PLL analog ground pin.
VNB	-	Time base generator PLL analog ground pin.
VNC	-	Internal ECL, CMOS logic ground pin.
VND	-	TTL buffer I/O digital ground pin.
VNG	-	Pulse detector, filter, servo analog ground pin.

INPUT PINS

VIA, $\overline{VIA}$	I	AGC AMPLIFIER INPUTS: Differential AGC amplifier input pins.
DP, DN	I	ANALOG INPUTS FOR DATA PATH: Differential analog inputs to data comparators, full-wave rectifier.
CP, CN	I	ANALOG INPUTS FOR CLOCK PATH: Differential analog inputs to the clock comparator.
$\overline{PWRON}$	I	Power Enable: TTL compatible power control input. A low level input enables power to circuitry according to the contents of the PDCR. A high level input shuts down all circuitry.
$\overline{HOLD}$	I	HOLD CONTROL: TTL compatible control pin which, when pulled low, disables the AGC charge pump and holds the AGC amplifier gain at its present value.
STROBE	I	BURST STROBE: TTL compatible burst strobe input. A high level TTL input will enable the servo peak detector to charge one of the burst capacitors. The falling edge of STROBE increments an internal counter that determines which burst capacitor will charge on the next STROBE pulse (reference Figure 6 for timing.)
$\overline{RESET}$	I	RESET CONTROL INPUT: TTL compatible reset input. A low level TTL input will discharge the internal servo burst hold capacitors on channels A-D.
IN, $\overline{IN}$	I	FILTER SIGNAL INPUTS: The AGC output signals must be AC coupled into these pins.
FREF	I	REFERENCE FREQUENCY INPUT: Frequency reference input for the time base generator. FREF should be driven by an AC-coupled signal between 1.2 and 2 Vp-p.
LATCH0/1	I	BURST SELECT INPUTS: TTL compatible inputs that are decoded to select one of the three burst outputs: LATCH0 / LATCH1 / OUTPUT 0 / 0 / A-B 1 / 0 / A+B 0 / 1 / C-D

INPUT PINS (continued)

NAME	TYPE	DESCRIPTION
AMENB	I	ADDRESS MARK ENABLE: TTL compatible input. A high level TTL input will enable the address mark generation circuitry in write mode and the address mark detect circuitry in read mode.
NRZIN	I	NRZ INPUT: TTL compatible write data NRZ input. This pin can be connected to the NRZO pin to form a bidirectional data port. Pin NRZIN has an internal pull up resistor.
RG	I	READ GATE: TTL compatible read gate input. A high level TTL input selects the RD input and enables the read mode/address mark detect sequences. A low level selects the FREF input.
SG	I	SERVO GATE: TTL compatible servo gate input. A high level TTL input activates the servo mode by selecting the servo control registers, the RDIO pin, and the RTS resistor.
WCLK	I	WRITE CLOCK: TTL compatible write clock input. Must be synchronous with the Write Data NRZ input. For short cable delays, WCLK may be connected directly to pin RRC. For long cable delays, WCLK should be connected to an RRC return line matched to the NRZ data bus line delay.
WG	I	WRITE GATE: TTL compatible write gate input. A high level TTL input enables the write mode.

OUTPUT PINS

NAME	TYPE	DESCRIPTION
$\overline{\text{AMD}}$	O	ADDRESS MARK DETECT: Address mark detect TTL compatible output. Tristate output pin that is high impedance state when RG is low. When AMENB is high, this output indicates address mark search status. A low level output appears when an address mark has been detected. A low level on the AMENB pin resets $\overline{\text{AMD}}$.
MTP1, 2, 3	O	MULTIPLEXED TEST POINTS: Open emitter ECL output test points. Internal test signals are routed to these test points as determined by the CAR and CBR. External pull up and down resistors are required to use this pin. They should be removed during normal operation to reduce power dissipation.
NRZO	O	NRZ OUTPUT DATA: NRZ data CMOS output. Tristate output pin that is in its high impedance state when RG is low. Read data output when RG is high.
OD, $\overline{\text{OD}}$	O	DIFFERENTIAL DIFFERENTIATED OUTPUTS: Filter differentiated outputs. These outputs are AC coupled into the CP/CN inputs.
ON, $\overline{\text{ON}}$	O	DIFFERENTIAL NORMAL OUTPUTS: Filter normal low pass output signals. These outputs are AC coupled into the DP/DN inputs.
PPOL	O	PULSE POLARITY: Pulse polarity CMOS output. The output is high when the pulse being qualified is positive and it is low when the pulse being qualified is negative.

OUTPUT PINS (continued)

NAME	TYPE	DESCRIPTION
$\overline{\text{RDIO}}$	O	READ DATA I/O: Bi-directional TTL compatible CMOS pin. $\overline{\text{RDIO}}$ is an output when the SG is active or the RDI bit is low in the CBR. $\overline{\text{RDIO}}$ is an input when the RDIO bit is high in the CBR. The SG overrides the bit in the CBR. $\overline{\text{RDIO}}$ is high impedance when SG is low and RG or WG is high.
RRC	O	READ REFERENCE CLOCK: Read clock TTL compatible CMOS output. During a mode change, no glitches are generated and no more than one lost clock pulse will occur. When RG goes high, RRC initially remains synchronized to FOUT. When the Sync Bits are detected, RRC is synchronized to the $\overline{\text{DRD}}$. When RG goes low, RCC is synchronized back to the FOUT.
VOA, $\overline{\text{VOA}}$	O	AGC AMPLIFIER OUTPUT: Differential AGC amplifier output pins. These outputs are ac coupled into the filter inputs (IN/$\overline{\text{IN}}$).
$\overline{\text{WD}}$	O	WRITE DATA: Encoded write data TTL compatible output. The falling edge of $\overline{\text{WD}}$ represents the data bit. $\overline{\text{WD}}$ is internally resynchronized (independent of the delay between RRC and WCLK) to the FREF reference clock. When direct write is active $\overline{\text{WD}}$ is NRZIN data.

ANALOG PINS

A, B, C, D	-	SERVO OUTPUTS: These outputs are processed versions of the voltages captured on the servo hold capacitors. They are referenced to MAXREF.
A-B, C-D, A+B	O	SERVO OUTPUTS: These outputs are processed versions of the voltages captured on the servo hold capacitors. They are referenced to SREF.
BYP	-	The AGC integrating capacitor CBYP, is connected between BYP and VPG.
TFLT/$\overline{\text{TFLT}}$	-	PLL LOOP FILTER: These pins are the connection points for the time base generator loop filter.
DACOUT	-	DAC VOLTAGE TEST POINT: This test point monitors the outputs of the internal DACs. The source DAC is selected by programming the two MSBs of the WSCR register: **TDAC1 TDAC0 DAC MONITORED** 0 0 Filter fc DAC 0 1 Qualifier threshold DAC (VTH) 1 0 Window shift DAC 1 1 Write precomp DAC
DFLT/$\overline{\text{DFLT}}$	-	PLL LOOP FILTER: These pins are the connection points for the data separator loop filter.
LEVEL	-	An NPN emitter output that provides a full-wave rectified signal from the DP, DN inputs. An external capacitor should be connected from LEVEL to VPG to set the qualification threshold time constant in conjunction with RTS and RTD. An internal current source provides 60 µA of pull-down current at this pin.
RR	-	REFERENCE RESISTOR INPUT: An external 1% resistor is connected from this pin to ground to establish a precise internal reference current for the data separator and time base generator.

ANALOG PINS (continued)

NAME	TYPE	DESCRIPTION
RTS	-	SERVO TIME CONSTANT RESISTOR INPUT: An external resistor is connected from this pin to LEVEL to establish the qualification threshold time constant when in servo mode.
RTD	-	DATA TIME CONSTANT RESISTOR INPUT: An external resistor is connected from this pin to LEVEL to establish the hysteresis threshold time constant when not in servo mode.
RX	-	REFERENCE RESISTOR INPUT: An external 1% resistor is connected from this pin to VNG to establish a precise PTAT (proportional to absolute temperature) reference current for the filter. A 1000 pF capacitor should be placed in parallel with this resistor.
MAXREF	-	SERVO REFERENCE: An external voltage output that can be used as the reference for an external A/D converter. This represents the maximum output voltage for the A, B, C, and D outputs.
SREF	I	SERVO REFERENCE: An external voltage is applied to this pin to set the baseline for the servo outputs. When A-B = 0, the A-B output will be SREF.

SERIAL PORT PINS

SDEN	-	SERIAL DATA ENABLE: Serial enable CMOS compatible input. A high level input enables the serial port.
SDATA	-	SERIAL DATA: Serial data CMOS compatible input. NRZ programming data for the internal registers is applied to this input.
SCLK	-	SERIAL CLOCK: Serial clock CMOS compatible input. The clock applied to this pin is synchronized with the data applied to SDATA.

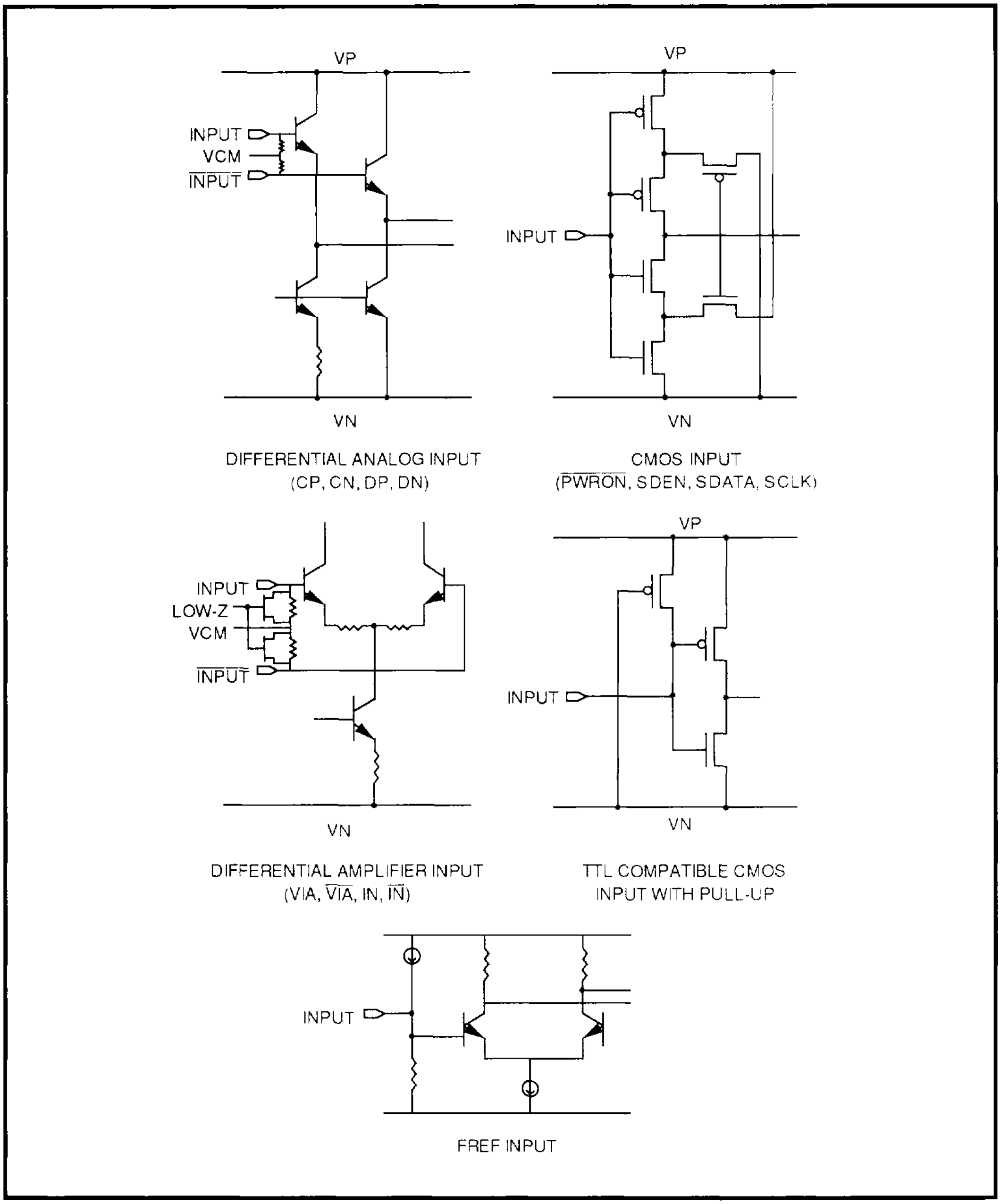

FIGURE 19(a): Input Structures

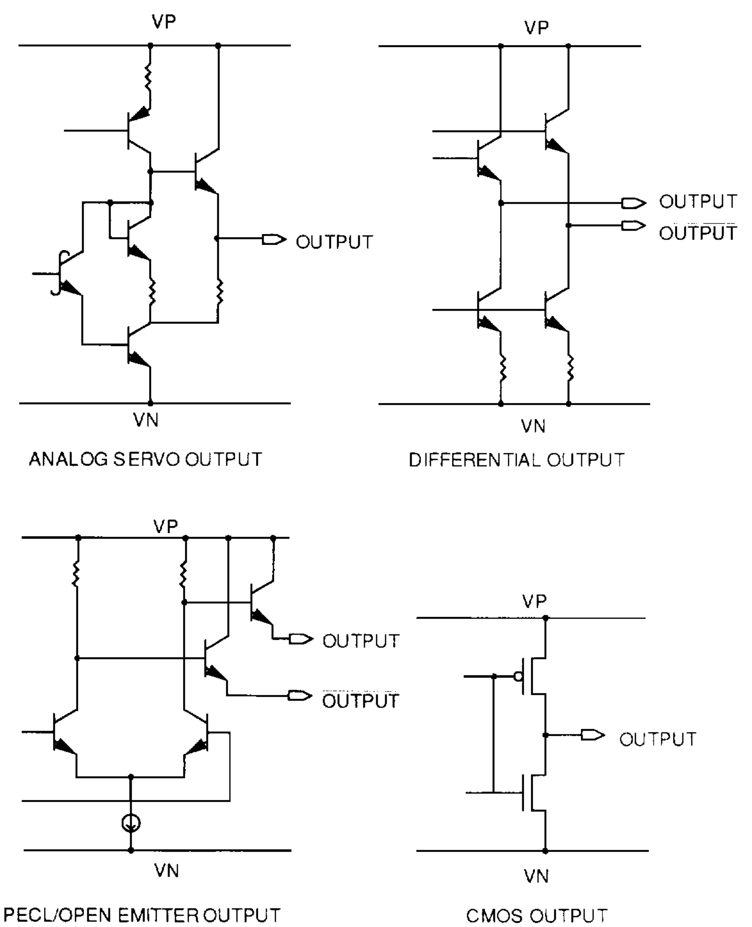

FIGURE 19(b): Output Structures

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, the recommended operating conditions are as follows: 4.5V < POSITIVE SUPPLY VOLTAGE < 5.5V, 0°C < T (ambient) < 70°C, and 0°C < T(junction) < 135°C. Currents flowing into the chip are positive. Current maximums are currents with the highest absolute value. All register DAC settings are in decimal values.

ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may damage the device

PARAMETER	RATING
Storage Temperature	-65 to 150°C
Positive Supply Voltage (Vp)	-0.5 to 7V
Voltage applied to any pin	-0.5V to Vp + 0.5V

POWER SUPPLY CURRENT AND POWER DISSIPATION Unless otherwise specified, Ta = 26°C and data rate = max. All test points and outputs are open. The test points are disabled.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
ICC (VPA, VPB, VPC, VPD, VPG)	$\overline{\text{PWRON}}$ = 0 All blocks enabled		85	135	mA
PWR Power Dissipation	$\overline{\text{PWRON}}$ = 0 All blocks enabled		425	690	mW
Sleep Mode Current	$\overline{\text{PWRON}}$ = 1 SG, RG, WG, STROBE, $\overline{\text{RESET}}$ WCLK = 0 All other CMOS inputs = 1			0.5	mA
Servo Mode Current	$\overline{\text{PWRON}}$ = 0 SG = 1 Power Reg. = 14 hex		45	75	mA

DIGITAL INPUTS AND OUTPUTS

TTL COMPATIBLE INPUTS – Inputs will float high "1" if left open.

Input low voltage	VIL				0.8	V
Input high voltage	VIH		2			V
Input low current	IIL	VIL = 0.4V			-20	µA
Input high current	IIH	VIH = 2.4V			20	µA

CMOS COMPATIBLE INPUTS - Schmitt trigger type, do not leave open. Nominal 1 V hysteresis around VPD/2.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input low voltage	VPC = 5V			1.5	V
Input high voltage	VPC = 5V	3.5			V

CMOS COMPATIBLE OUTPUTS

Output low voltage	IOL = 4 mA, VPD = 5V			0.5	V
Output high voltage	IOH = -4 mA, VPD = 5V	4.5			V
Rise time	$C_L \leq$ 15 pF, 0.8 to 2V			5	ns
Fall time	$C_L \leq$ 15 pF, 2 to 0.8V			5	ns

FREF INPUT

Input level	AC-coupled	1.2		2	Vp-p
Input resistance			11		kΩ

TEST POINT OUTPUT LEVELS (MTP1, MTP2, MTP3) - Termination network: 261Ω to VPA, 402Ω to VNA. For reference use only.

Output high level		VPA-1			V
Output low level				VPA-1.6	V
Output voltage swing		0.35			V

SERIAL PORT

SCLK data clock period TCKL	Write to serial port	100			ns
	Read from serial port	140			ns
SCLK low time, TCKL	Write to serial port	40			ns
	Read from serial port	60			ns
SCLK high time, TCKH	Write to serial port	40			ns
	Read from serial port	60			ns
Enable to SCLK TSENS		35			ns
SCLK to disable TSENH		100			ns
Data set-up time TDS		15			ns
Data hold time TDH		15			ns
SDATA tri-state delay TSENDL				50	ns
SDATA turnaround time TTRN	R/W Bit = 1 (Read)	70			ns
SDEN low time TSL		200			ns
SCLK falls to Valid Data TDSKEW	C load ≤ 15 pf	0		50	ns

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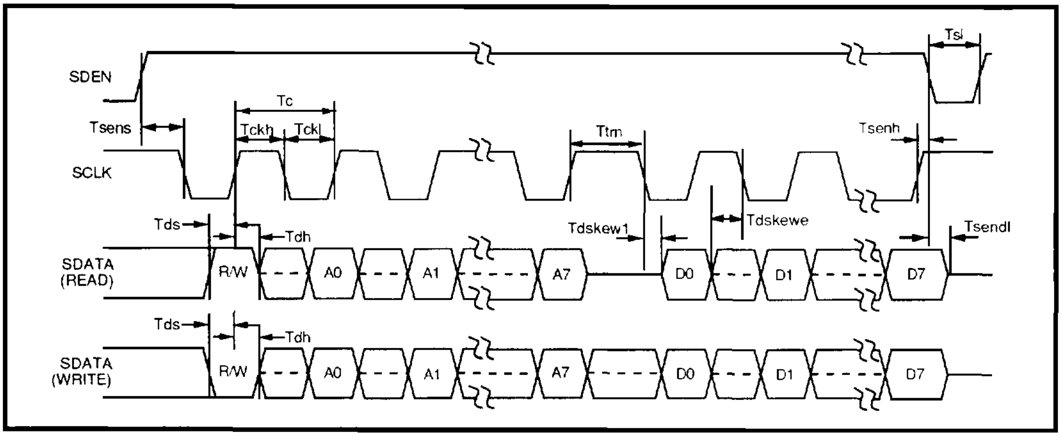

FIGURE 18(b): Serial Port Timing

ELECTRICAL SPECIFICATIONS (continued)

PULSE DETECTOR CHARACTERISTICS

AGC AMPLIFIER

Input signals are AC coupled to VIA/$\overline{VIA}$, VOA/$\overline{VOA}$ outputs are AC coupled toIN/$\overline{IN}$, and ON/$\overline{ON}$ are AC coupled to DP/DN. A 1000 pF capacitor (CBYP) is connected from BYP to VPG. Unless otherwise specified, outputs are measured differentially at VOA/$\overline{VOA}$, FIN = 8 MHz, and filter boost = 0 dB.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input range	Filter boost = 0 dB, Fin = Fc	22		240	mVp-p
	Filter boost = 13 dB	20		100	mVp-p
DP-DN voltage	22 ≤ VIA-$\overline{VIA}$ ≤ 240 mVp-p $\overline{HOLD}$ = 1, boost = 0 dB	0.85		1.15	Vp-p
	20 ≤ VIA-$\overline{VIA}$ ≤ 100 mVp-p, boost = 13 dB	0.85		1.15	Vp-p
DP-DN voltage (servo)	SG = 1, DACA = 0000 Binary SG = 1, DACA = 1111 Binary	0.85 0.60	1 0.75	1.15 0.90	Vp-p Vp-p
AGC gain minimum maximum	$\overline{HOLD}$ = 0 1@ BYP = -50 µA 1@ BYP = 50 µA	 22		 1	 V/V V/V
Gain sensitivity	BYP voltage change	23	28	33	dB/V
AGC output total harmonic distortion	VOA-$\overline{VOA}$ = 0.75 Vp-p VIA = 100 mVp-p			1	%
Differential input impedance	WG = low	4.7	6	8.4	kΩ
	WG = high; or Low-Z	100	350	600	Ω
Single-ended input impedance	WG = low	2.5	3.3	5	kΩ
	WG = high; or Low-Z	150	250	350	Ω

AGC AMPLIFIER (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Bandwidth	Gain = 22, CL ≤ 15 pF	35			MHz
Output offset voltage	Gain = 1 to 22			200	mV
Input noise voltage	Gain = 22, VIA/$\overline{VIA}$ shorted		10	15	nV/√Hz
CMRR	Gain = 22, fc = 5 MHz	40			dB
PSRR	Gain = 22, fc = 5 MHz	45			dB
Single-ended output resistance			125	275	Ω
Gain decay time	VIA-$\overline{VIA}$ = 240 to 120 mV VOA-$\overline{VOA}$ > 0.9 Final Value		50		µs
Gain attack time	VIA-$\overline{VIA}$ = 120 to 240 mV VOA-$\overline{VOA}$ < 1.1 Final Value		1		µs

AGC CONTROL

The input signals are AC coupled into DN/DP, CBYP = 1000 pF to VPG. CT = 10000 pF, RTS = RTD = Open.

Decay current	VBYP = VPG - 2.3V Normal decay mode (I_D) DP-DN = 0V	-3	-5	-7	µA
	Fast decay mode (I_{DF}) DP-DN = 0V	-0.8	-1.3	-1.7	mA
Attack current	VBYP = VPG - 2.3V Normal attack mode (I_{CH}) DP-DN = 0.55V	0.12	0.21	0.29	mA
	Fast attack mode (I_{CHF}) DP-DN = 0.675V	7 x ICH	9 x ICH	11 x ICH	mA
BYP leakage current	$\overline{HOLD}$ = 0, 1 ≤ GAIN ≤ 22	-50		50	nA
Low-Z duration	WG 1 to 0 Low-Z bit = 0	0.5	1	1.5	µs
	Low-Z bit = 1	1	2	3	µs
Fast decay duration	Low-Z bit = 0	0.5	1	1.5	µs
	Low-Z bit = 1	1	2	3	µs
LEVEL output voltage (with respect to RTD/RTS)	FIN = 6 to 18 MHz |DP-DN| = 0.5 Vp-p	0.29	0.33	0.37	V
	|DP-DN| = 1 Vp-p	0.63	0.70	0.77	V
	|DP-DN| = 1.5 Vp-p	0.88	1	1.12	V
LEVEL pull-down current	Vlevel = VPG - 2.3V	40	60	80	µA

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SSI 32P4741/4744/4744A
Read Channel with
1,7 ENDEC, 4-burst Servo

ELECTRICAL SPECIFICATIONS (continued)

DATA COMPARATOR

The input signals are AC coupled into DP/DN.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Differential input resistance	WG = 0	6.5	9	12.5	kΩ
Single ended input resistance	WG = 1	335	500	860	Ω
Threshold (T%) voltage local hysteresis	(% of set value)		20		%
Threshold (T%) accuracy	41 < V_{THDAC} < 109 0.3 < Vlevel - V_{RTHD} < 0.75 T% = V_{THDAC} • 0.7696 - 3.58(%) T% is defined as the 50% error rate point	T%-5	T%	T%+5	%

CLOCK SECTION

The input signals are AC coupled into CP/CN.

Differential input resistance		6.5	9	12.5	kΩ
Pulse pairing	Data rate = 16 Mbit/s Input = 100 mVp-p @ 6 MHz into VIA/$\overline{\text{VIA}}$ Fc = 9 MHZ, 0 dB boost. Measured at falling edge of $\overline{\text{RDIO}}$ Data threshold register = 63 and 196			0.8	ns

SERVO CAPTURE CHARACTERISTICS – Unless otherwise specified: a 4 MHz sine wave is AC-coupled into DP/DN inputs; STROBE and $\overline{\text{RESET}}$ durations are 1 µs; and DACP is set to "1000" with the Servo Reset bit set to "1."

MAXREF output voltage	I_{SOURCE} = 0 mA	2.85	3.05	3.26	V
MAXREF load regulation	I_{SOURCE} = -1 to -4 mA			40	mV
A, B, C, D output low voltage	I_{SINK} = 0.2 mA $\overline{\text{RESET}}$ = 0V (low)	0.14x MAXREF		0.17x MAXREF +0.15	V
MAXREF-A,B,C,D high voltage	I_{SOURCE} = 0 mA	0			V
A, B, C, D output impedance	$I_{SOURCE/SINK}$ = 0.2 mA			50	Ω
A, B, C, D gain	0.2 Vp-p < (DP-DN) ≤ 1 Vp-p 0 Vp-p ≤ (DP-DN) ≤ 0.2 Vp-p	2.05 0		2.35 2.30	V/V V/V
A,B,C,D hold drift	STROBE = 0V, $\overline{\text{RESET}}$ = 1			100	µV/µs
A,B,C,D offset voltage	DP-DN = 1 Vpp, $\overline{\text{RESET}}$ = 1 A-B & C-D A-C, A-D, B-C, & B-D			100 200	mV mV
SREF input range		0.35 • VPG	0.4 • VPG	0.55 • VPG	V
SREF input bias current	0.35 • VPG ≤ SREF ≤ 0.55 • VPG		0.2	1	µA
A-B, C-D, A+B output high voltage		VPG - 1.1			V

SERVO CAPTURE CHARACTERISTICS (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
A-B, C-D, A+B output low voltage				0.5	V
A-B, C-D large signal gain	0.2 Vp-pd < (DP-DN) ≤ 0.8 Vp-pd	1.75	2	2.25	V/Vp-pd
A-B, C-D small signal gain	0 Vp-pd ≤ (DP-DN) ≤ 0.2 Vp-pd	0		2.25	V/Vp-pd
A+B large signal gain	0.2 Vp-pd < (DP-DN) ≤ 0.8 Vp-pd	0.9	1	1.1	V/Vp-pd
A+B small signal gain	0 Vp-pd ≤ (DP-DN) ≤ 0.2 Vp-pd	0		1.1	V/Vp-pd
Output resistance	Isource/sink = 0.2 mA			50	Ω
Burst capture time	DP-DN = 1 Vp-pd, captured burst ≥95% of the final value.			1	µs
Burst reset time	Captured burst ≤ 5% of the final value, $\overline{RESET}$ = 0			1	µs
A-B, C-D hold drift	$\overline{RESET}$ = 1, STROBE = 0V	-100		100	µV/µs
A+B hold drift	$\overline{RESET}$ = 1, STROBE = 0V	-200		200	µV/µs
A-B, C-D offset voltage	DP-DN = 0.5 Vp-pd Offset = |output ($\overline{RESET}$ = 1) - output ($\overline{RESET}$ = 0)|			30	mV
RDIO pulse width	CL = 15 pF Measured at 1.5V crossing	10		15	ns
PPOL to $\overline{RDIO}$ setup time	PPOL rise/fall to $\overline{RDIO}$ fall $\overline{RDIO}$ fall measured @ 1.5V crossing CL ≤ 15 pF	8			ns

PROGRAMMABLE FILTER CHARACTERISTICS – Unless otherwise specified: Rx = 12.1 kΩ, Cx = 1000 pF from Rx pin to VNG. Input signals are AC-coupled into IN/$\overline{IN}$.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Filter cutoff range	*fc* @ 3 dB point *fc* = (0.1485 x DACF) - 0.9013 (MHz) Boost = 0 dB, 46 ≤ DACF 127	6		18	MHz
Filter cutoff accuracy	DACF = 46 and 127	-15		15	%
ON differential gain (AN)	F = 0.67 x *fc*, boost = 0 dB DACF = 46 and 127	1.5	2	2.5	V/V
OD differential gain (AD)	F = 0.67 x *fc*, boost = 0 dB DACF = 46 and 127	0.9 x AN		1.3 x AN	V/V
Boost accuracy	6 dB	-1		1	dB
	9 dB	-1.25		1.25	dB
	13 dB	-1.5		1.5	dB
Group delay variation	F = 0.2 *fc* to *fc* DACF = 46 and 127 Boost = 0 and 3 dB	-2		2	%
	F = *fc* to 1.75 *fc* DACF = 46 and 127 Boost = 3 dB	-3		3	%

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PROGRAMMABLE FILTER CHARACTERISTICS (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
OD output THD @1 Vpp	F = 0.67 *fc*, DACF = 46 and 127			1.5%	Vp-p
Differential input resistance	WG = 0	5	6.5	8	kΩ
	WG = 1	100	300	600	Ω
Single-ended input resistance	WG = 1	600	950	1300	Ω
Single-ended output resistance			100	200	Ω
Output sink current		0.5			mA
Differential output offset change	@ ON/ON, DACF = 46 and 127 |(offset at 127)-(offset at 46)|			200	mV
Output noise voltage	BW = 100 MHz, Rs = 50Ω				
ON/$\overline{ON}$ output	DACF = 127, boost = 0 dB		2.2	3.3	mVRms
ON/$\overline{ON}$ output	DACF = 127, boost = 13 dB		3.2	4.8	mVRms
OD/$\overline{OD}$ output	DACF = 127, boost = 0 dB		3.8	5.7	mVRms
OD/$\overline{OD}$ output	DACF = 127, boost = 13 dB		6.9	10.4	mVRms

TIME BASE GENERATOR CHARACTERISTICS – Unless otherwise specified: RR = 12.1 kΩ. Loop filter values are R = 453Ω, C1 = 0.47 µF, and C2 = 0.047 µF. Clock source is AC coupled into FREF, $1.2 \leq V_{FREF} \leq 2$ Vp-p.

FREF input range	Trise/Tfall ≤ 5 ns	8		20	MHz
FOUT frequency range	FREF = 20 MHz			75	MHz
M counter range		2		255	
N counter range		2		127	
VCO center frequency period (FTBG)	FTBG = [12.5/(RR+0.4)] x [(0.614 x IDAC) + 3.84] (MHz) TFLT-$\overline{TFLT}$ = 0V	0.85x FTBG		1.15x FTBG	MHz
VCO dynamic range	-2V ≤ TFLT-$\overline{TFLT}$ ≤ +2V	±25		±45	%
VCO control gain KVCO	ωi = 2π • FTBG -1V ≤ TFLT-$\overline{TFLT}$ ≤ +1V	0.12 ωi	0.175 ωi	0.24 ωi	rad/(V-S)
Phase detector gain KD	KD = [12.5/(RR + 0.4)] x (0.633 x IDAC + 0.92) PDCR D1 = 1, KD = 1x PDCR D1 = 0, KD = 3x	0.83KD		1.17KD	µA/rad
KVCO x KD product accuracy		-28		28	%
FREF input low time		20			ns
FREF input high time		20			ns

DATA SEPARATOR CHARACTERISTICS

Unless otherwise noted, RR = 12.1 kΩ. Loop filter components are R = 1.82 kΩ, C1 = 270 pF, and C2 = 27 pF. Data Rate = 40 Mbit/s.

READ MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Read clock rise time TRRC	0.8 to 2V CL ≤ 15 pF			5	ns
Read clock fall time TFRC	2 to 0.8V CL ≤ 15 pF			5	ns
RRC duty cycle (TRD/TORC)	1.5V to 1.5V, Cl ≤ 15 pF	40		60	%
NRZ out set-up and hold time (TNS, TNH)		6			ns
NRZ out propagation delay (TPNRZ)		-5		5	ns
Phase window centering	At 16 and 40 Mbit/s Difference between early, late phase reversal points/(TVCO)	-20		20	%
RRC Asymmetry	1/2 the difference between adjacent RRC periods			3	ns

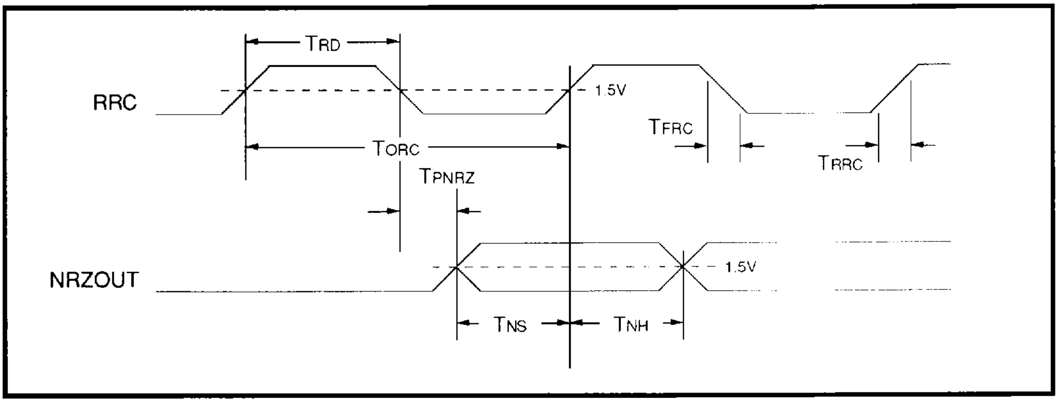

FIGURE 20: NRZ Read Timing

ELECTRICAL SPECIFICATIONS (continued)

WRITE MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Write data rise time (TRWD)	0.8 to 2V CL ≤ 15 pF			5	ns
Write data fall time (TFWD)	2 to 0.8V CL ≤ 15 pF			5	ns
Required WCLK rise time (TRWC)	0.8 to 2V			10	ns
Required WCLK fall time (TFWC)	2 to 0.8V			8	ns
NRZ set-up time (TSNRZ)		5			ns
NRZ hold time (THNRZ)		5			ns
$\overline{\text{WD}}$ jitter	$\overline{\text{WD}}$ out = fixed 2T pattern at 16 Mbit/s at 40 Mbit/s			 1000 500	 ps(RMS) ps(RMS)
$\overline{\text{WD}}$ pulse width (TWD)	Without precomp, TW = 1/FTBG CL ≤ 15 pF	0.82xTW		1.18xTW	ns
Write Precomp magnitude accuracy	TPC = n x TPCO TPCO = 0.04/FTBG for early precomp TPCO = 0.054/FTBG for late precomp 0 ≤ n ≤ 7	0.8xTPC - 1		1.2xTPC + 1	ns

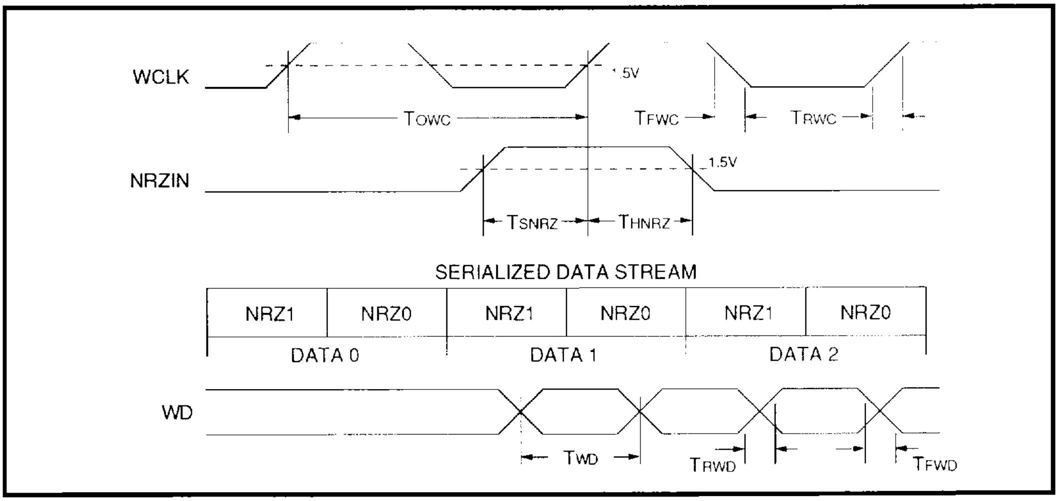

FIGURE 21: $\overline{\text{WD}}$ and NRZ Write Timing

DATA SYNCHRONIZATION

Unless otherwise specified: RR = 12.1 kΩ. Loop filter values are R = 1.82 kΩ, C1 = 270 pF, and C2 = 27 pF. Clock source is AC coupled into FREF, 1.2 ≤ VFREF ≤ 2 Vp-p.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VCO center frequency (FVCO)	FVCO= [12.5/(RR + 0.4)] x [(0.614 x IDAC) + 3.84] MHz DFLT-$\overline{\text{DFLT}}$ = 0V	0.85X FVCO		1.15X FVCO	MHz
VCO dynamic range	-2V ≤ DFLT-$\overline{\text{DFLT}}$ ≤ +2V at 60 MHz	±25		±45	%
VCO control gain KVCO	$\omega i = 2\pi/\text{TVCO}$ -1V ≤ DFLT-$\overline{\text{DFLT}}$ ≤ 1V at 60 MHz	0.12 ωi	0.175 ωi	0.24 ωi	rad/(V-S)
Phase detector gain, KD	Idle mode = 1 x KD Read mode = 3 x KD Read mode after gain shift = 1 x KD KD = [12.5/(RR + 0.4)] x (0.633 x IDAC + 0.92)	0.83 KD		1.17 KD	μA/rad
KVCO x KD product accuracy		-28		28	%
VCO phase restart error		-1		3	ns
Decode window center accuracy	Based on 50% error points at 40 Mbit/s	0.15		1.65	ns
Decode window loss	Based on 50% and 15% error points	-0.75		0.75	ns
Decode window shift magnitude accuracy	TWSO = 0.023/FVCO TWS = nxTWSO 0 ≤ n ≤ 15 for early shifts 0 ≤ n ≤ 9 for late shifts	0.8xTWS - 1		1.2xTWS + 1	ns
Decode window skew		-1		1	ns

ELECTRICAL SPECIFICATIONS (continued)

WINDOW SHIFT CONTROL

Window shift magnitude is set by the value in the Window Shift (WS) register. The WS register bits are as follows:

BIT	NAME	FUNCTION
0	$\overline{WS0}$	
1	$\overline{WS1}$	
2	$\overline{WS2}$	
3	$\overline{WS3}$	
4	WSD	Window shift direction. 0=early, 1=late
5	WSE	Window shift enable
6	TDAC0	Used to route signals to DAC test point
7	TDAC1	Used to route signals to DAC test point

The window shift magnitude is set as a percentage of the decode window, in 2.3 % steps. The tolerance of the window shift magnitude is ±15%. Window shift should be set during idle mode or write mode.

$\overline{WS3}$	$\overline{WS2}$	$\overline{WS1}$	$\overline{WS0}$	Shift Magnitude
1	1	1	1	No shift
1	1	1	0	2.3% (minimum shift)
1	1	0	1	4.6%
1	1	0	0	6.9%
1	0	1	1	9.2%
1	0	1	0	11.5%
1	0	0	1	13.8%
1	0	0	0	16.1%
0	1	1	1	18.4%
0	1	1	0	20.7%
0	1	0	1	23%
0	1	0	0	25.3%
0	0	1	1	27.6%
0	0	1	0	29.9%
0	0	0	1	32.2%
0	0	0	0	34.5% (maximum shift)

WRITE PRECOMP CONTROL

Write precomp magnitude is set by the value in the Write precomp (WP) register. The WP register bits are as follows:

BIT	NAME	FUNCTION
0	$\overline{WE0}$	Early Precomp Magnitude
1	$\overline{WE1}$	Early Precomp Magnitude
2	$\overline{WE2}$	Early Precomp Magnitude
3	WPE	Write Precomp enable, 0 = Disable 1 = Enable
4	$\overline{WL0}$	Late Precomp Magnitude
5	$\overline{WL1}$	Late Precomp Magnitude
6	$\overline{WL2}$	Late Precomp Magnitude
7	–	Not used

The write precomp magnitude is calculated as:

TPC = n x 0.04/FTBG for early precomp
TPC = n x 0.054/FTBG for late precomp

where a = precomp magnitude scaling factor as shown below. TREF is the period of the reference frequency provided by the internal time base generator.

$\overline{WN2}$	$\overline{WN1}$	$\overline{WN0}$	Precomp Magnitude Scaling Factor
1	1	1	No precomp
1	1	0	1X
1	0	1	2X
1	0	0	3X
0	1	1	4X
0	1	0	5X
0	0	1	6X
0	0	0	7X (maximum)

BIT N-2	BIT N-1	BIT N	BIT N+1	BIT N+2	BIT N COMPENSATION
1	0	1	0	1	None
0	0	1	0	0	None
1	0	1	0	0	Early
0	0	1	0	1	Late

Late = Bit N is time shifted toward the N+1 bit by the programmed magnitude

Early = Bit N is time shifted toward the N-1 bit by the programmed magnitude

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TABLE 5: 1,7 RLL Encode Table

NRZ DATA Present D_1 D_2	NRZ DATA Next D_1^* D_2^*		ENCODED WRITE DATA Previous Y_3'	ENCODED WRITE DATA Present Y_1 Y_2^* Y_3^*	
0 0	0 X		X	0 0 1	
0 0	1 X		0	0 0 0	
0 0	1 X		1	0 1 0	
1 0	0 X		X	1 0 1	
1 0	1 X		X	0 1 0	
0 1	0 0		0	0 0 1	
0 1	0 0		1	0 1 0	
0 1	1 0		X	0 0 0	
0 1	0 1		0	0 0 1	
0 1	0 1		1	0 0 0	
0 1	1 1		X	0 0 0	
1 1	0 0		0	0 1 0	
1 1	1 0		0	1 0 0	
1 1	0 1		0	1 0 0	
1 1	1 1		0	1 0 0	

TABLE 6: 1,7 RLL Decode Table

ENCODED READ DATA Previous Y_2' Y_3'	ENCODED READ DATA Present Y_1 Y_2 Y_3	ENCODED READ DATA Next Y_2^* Y_3^*		DECODED DATA D_1 D_2	
0 0	0 0 0	X X		0 1	
1 0	0 0 0	X X		0 0	
0 1	0 0 0	X X		0 1	
X X	1 0 0	X X		1 1	
X 0	0 1 0	0 0		1 1	
X 0	0 1 0	1 0		1 0	
X 0	0 1 0	0 1		1 0	
X 1	0 1 0	0 0		0 1	
X 1	0 1 0	1 0		0 0	
X 1	0 1 0	0 1		0 0	
0 0	0 0 1	X X		0 1	
1 0	0 0 1	X X		0 0	
0 1	0 0 1	X X		0 0	(Preamble)
X X	1 0 1	X X		1 0	

Note: X = Don't Care

ELECTRICAL SPECIFICATIONS (continued)

TABLE 7: 32P4741 Clock Source and Frequency vs. Mode

WG	RG	VCO REF	RCLK	DECODE CLOCK	ENCODE CLOCK	MODE
0	0	FOUT	2FOUT/3	FOUT	FOUT	IDLE
0	1	$\overline{DRD}$	2VCO/3	VCO	FOUT	READ
1	0	FOUT	2FOUT/3	FOUT	FOUT	WRITE

NOTE 1: Until the VCO locks to the new source, the VCO/2 entries will be FOUT.

NOTE 2: Until the VCO locks to the new source, the 2VCO/3 entries will be 2FOUT/3.

NOTE 3: WG = RG = 1 is an indeterminate state.

TABLE 8: Multiplexed Test Point Signal Selection

MTPE	TMS1	TMS0	MTP1	MTP2	MTP3
0	X	X	OFF	OFF	OFF
1	0	0	VCOREF	DS-IN	SRD
1	0	1	RD	DOUT	DSREF
1	1	0	PDQ	$\overline{PUQ}$	SRD
1	1	1	SET	RESET	NCTR

DOUT = Output of the pulse qualifier data comparators
DS-IN = Input to the data synchronizer phase detector
DSREF = Output of the time base generator
NCTR = N counter output of the time base generator
RD = Read data output from the pulse qualifier
RESET = Output of the negative threshold comparator
SET = Output of the positive threshold comparator
VCOREF = Data separator VCO reference clock
PDQ = Data separator phase detector pump down edge
$\overline{PUQ}$ = Data separator phase detector pump up edge (inverted)
SRD = Synchronized read data

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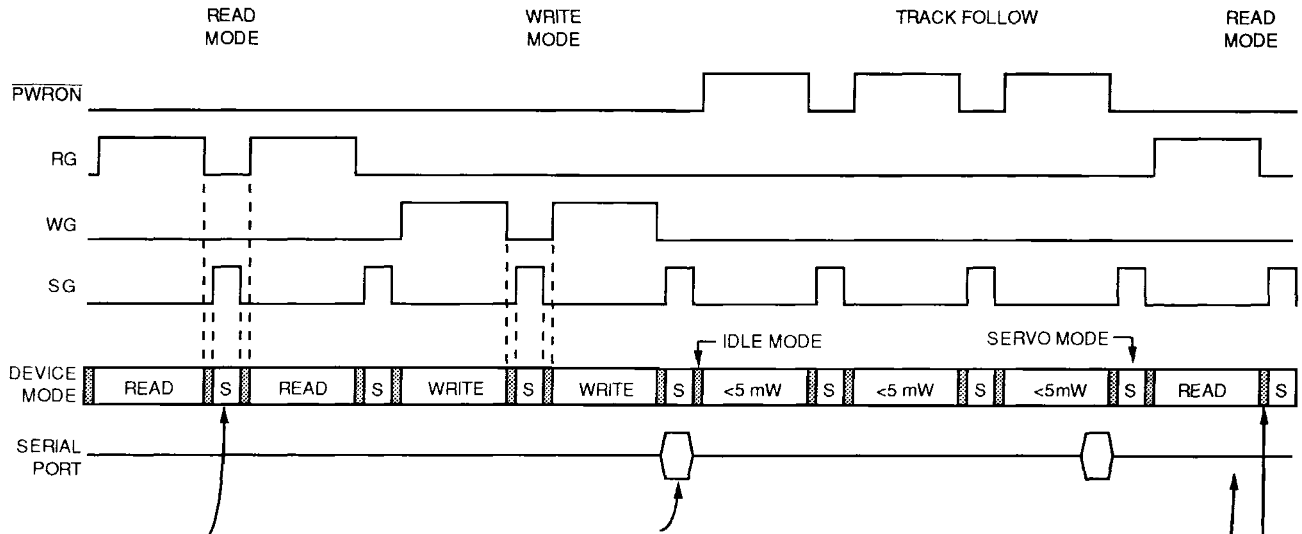

When SG is HIGH the device will switch to the Vs register for the threshold DAC and Fc DAC and the RTS resistor for the LEVEL pin output.

Prior to entering the Track Follow mode, the Power Down Control Register is changed to disable the Data Separator and Time Base Generator blocks. Load data while $\overline{\text{PWRON}}$ is HIGH.

Prior to returning to read mode (or write mode) the Power Down Control Register is changed to enable the Data Separator and Time Base Generator blocks. Load data while $\overline{\text{PWRON}}$ is HIGH.

When both RG and WG are low, the device will enter an idle state where the AGC is active and the data synchronizer is locked to the internal FREF.

NOTES:

1) When the $\overline{\text{PWRON}}$ pin is LOW ("0") the Power Down Control Register is active. All blocks that have their control bit set to "1" will be powered down. When the $\overline{\text{PWRON}}$ pin is HIGH ("1") the device goes into a sleep mode with all blocks powered down except the serial port.

2) When the threshold DAC reference is switched, there is a maximum settling time of 1.5µsec for the DAC.

FIGURE 22: Power Control Timing

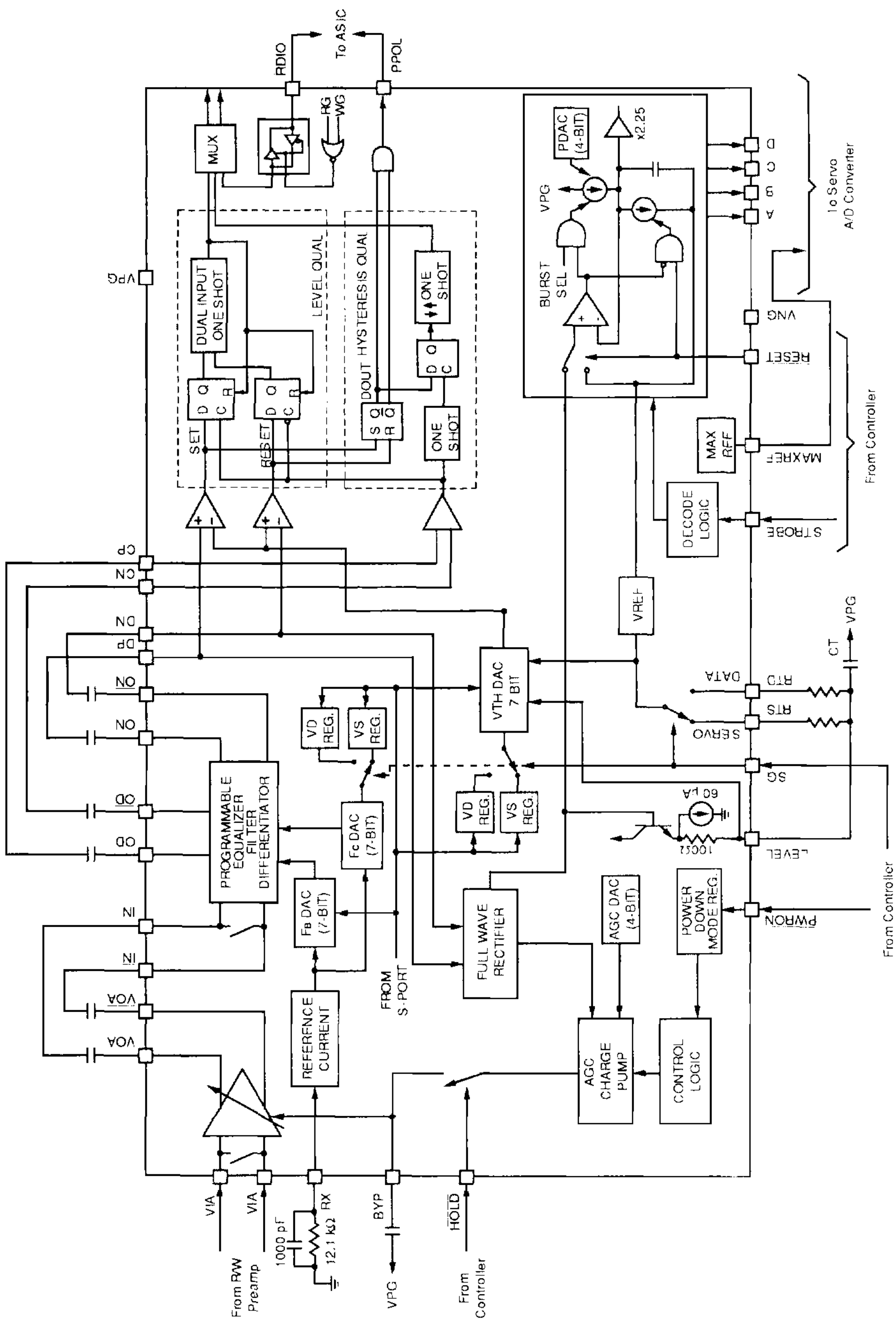

FIGURE 23(a): 32P4741 Application Diagram - Front End

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SSI 32P4741/4744/4744A
Read Channel with
1,7 ENDEC, 4-burst Servo

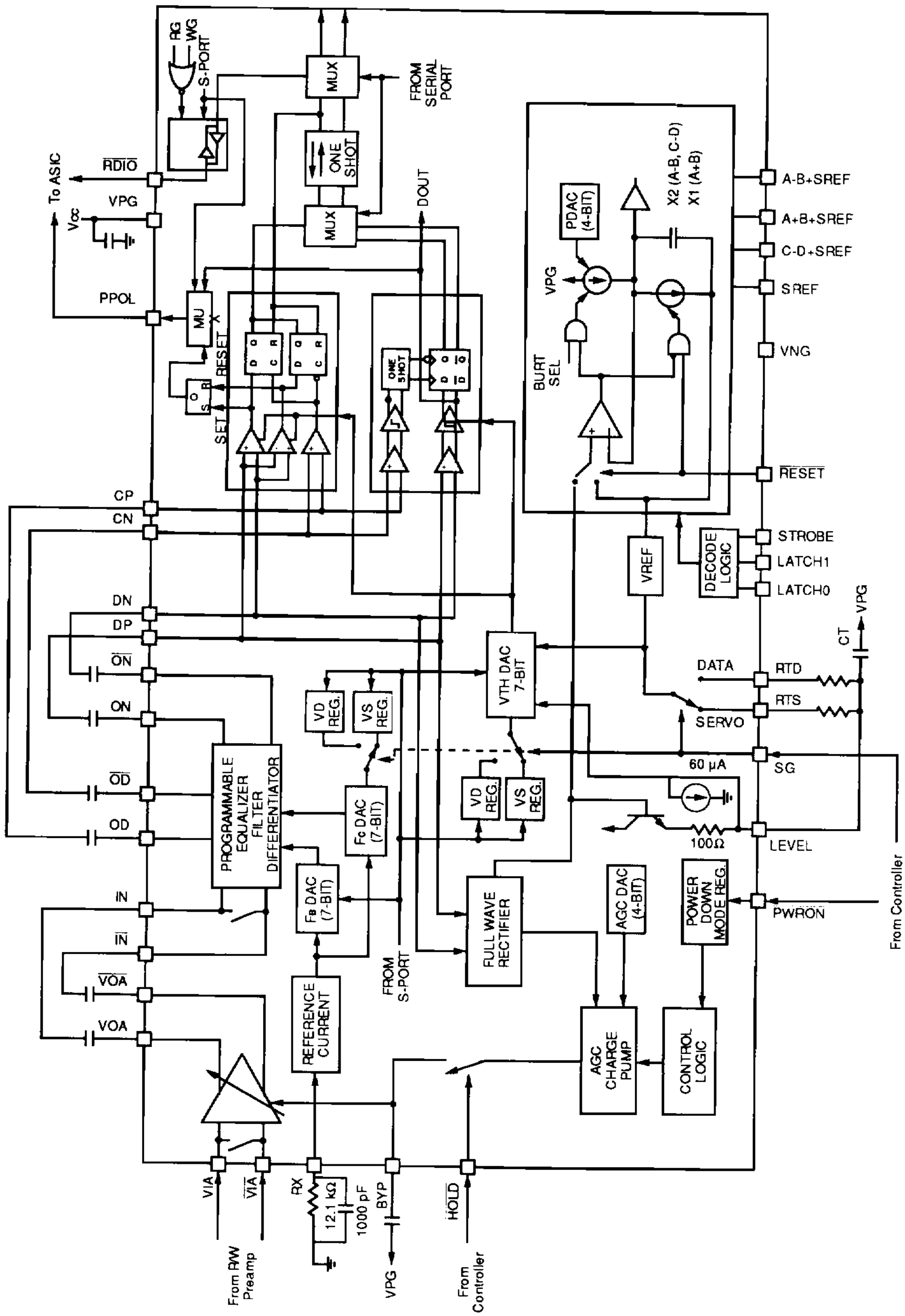


FIGURE 23(b): 32P4744 Application Diagram - Front End

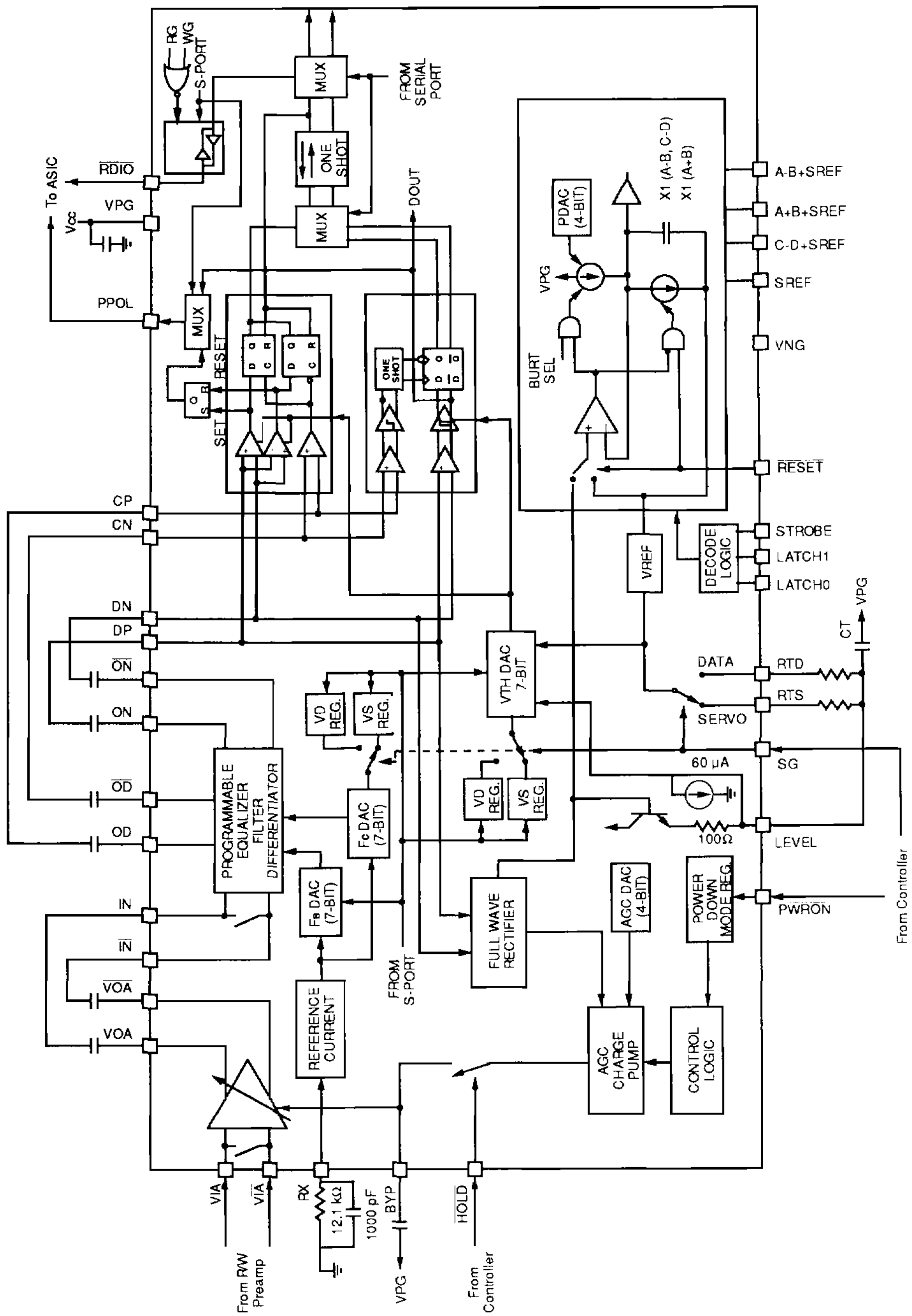


FIGURE 23(c): 32P4744A Application Diagram - Front End

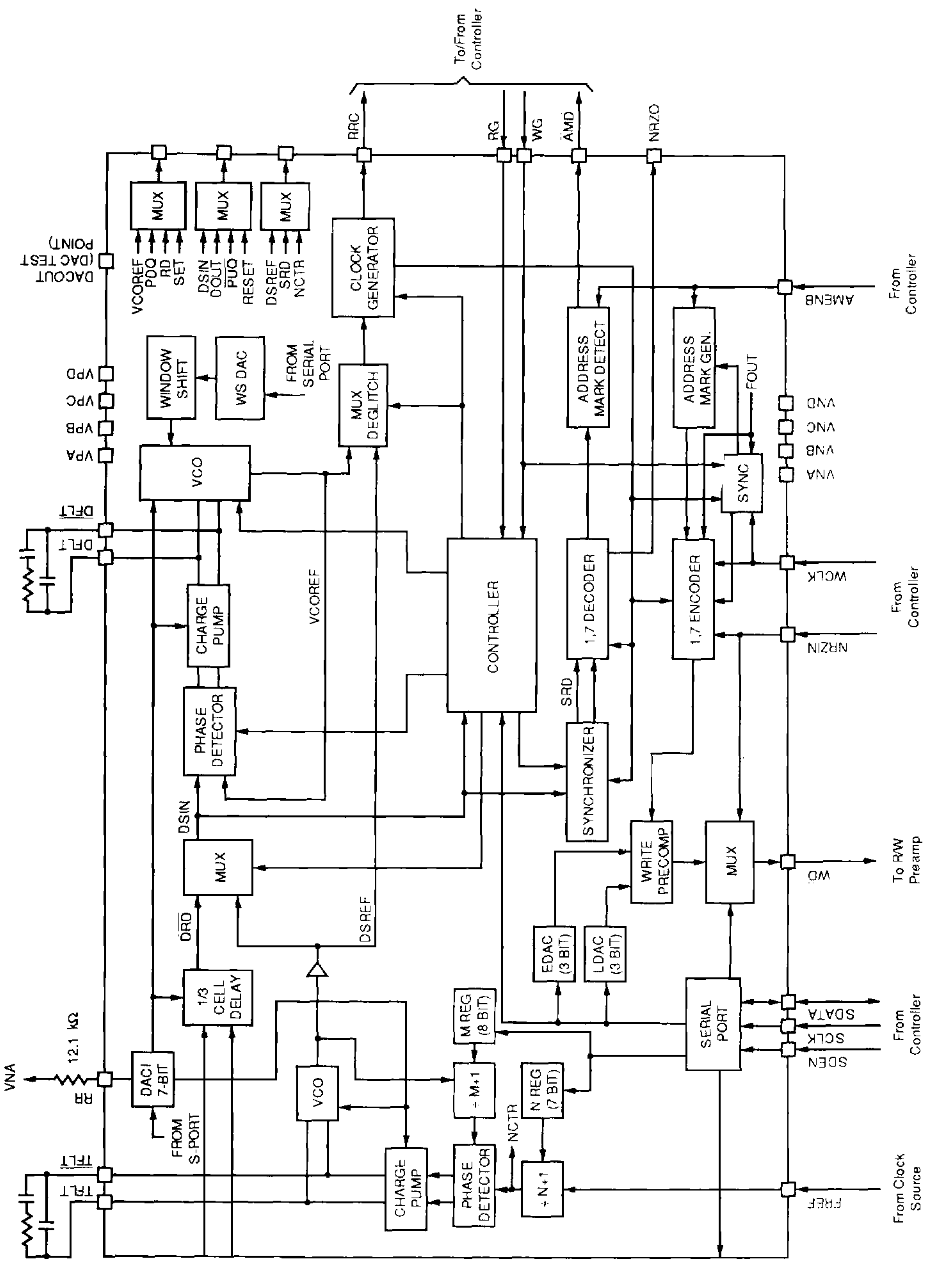
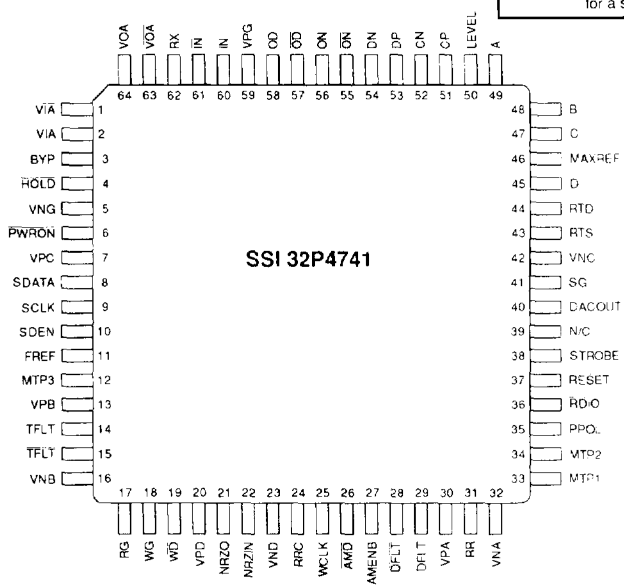


FIGURE 23(d): 32P4741/4744/4744A Application Diagram - Back End

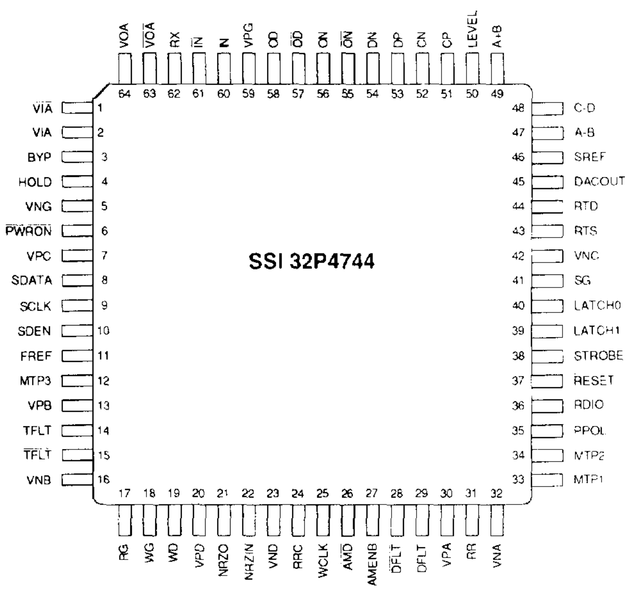
PACKAGE PIN DESIGNATIONS

(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



64-Lead TQFP

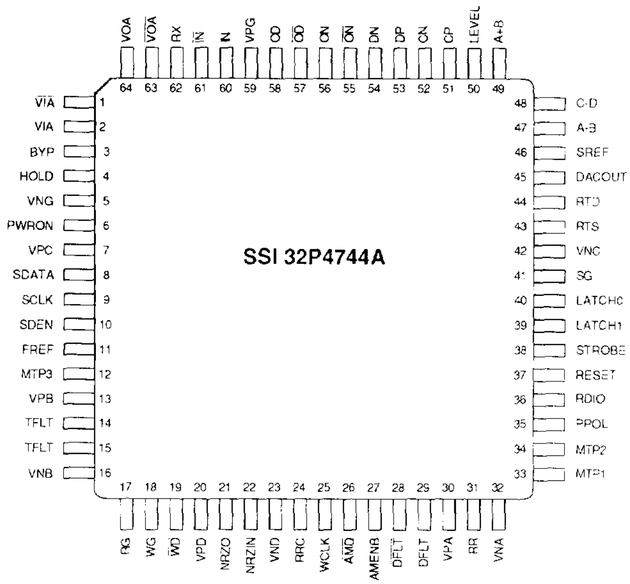


64-Lead TQFP

SSI 32P4741/4744/4744A Read Channel with 1,7 ENDEC, 4-burst Servo

PACKAGE PIN DESIGNATIONS

(Top View)



64-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION		ORDER NUMBER	PACKAGE MARK
SSI 32P4741	64-Lead TQFP	32P4741-CGT	32P4741-CGT
SSI 32P4744	64-Lead TQFP	32P4744-CGT	32P4744-CGT
SSI 32P4744A	64-Lead TQFP	32P4744A-CGT	32P4744A-CGT

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