

4M x 4 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

• Performance range:

	trAC	tcAC	trC	thPC
KM44C4004A/AL/ALL/ASL-5	50ns	13ns	90ns	20ns
KM44C4004A/AL/ALL/ASL-6	60ns	15ns	110ns	24ns
KM44C4004A/AL/ALL/ASL-7	70ns	20ns	130ns	29ns
KM44C4004A/AL/ALL/ASL-8	80ns	20ns	150ns	34ns

- Fast Page Mode with Extended data out
- Self Refresh operation (LL-ver. only)
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$ -only and Hidden Refresh capability
- Fast parallel test mode Capability
- TTL compatible inputs and outputs
- Early write or output enable controlled write
- Single+5.0V \pm 10% power supply
- 4096 cycles/64ms refresh (Normal)
- 4096 cycles/128ms refresh (Low power & Self Ref.)
- 4096 cycles/256ms refresh (Super Low power)
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II)

GENERAL DESCRIPTION

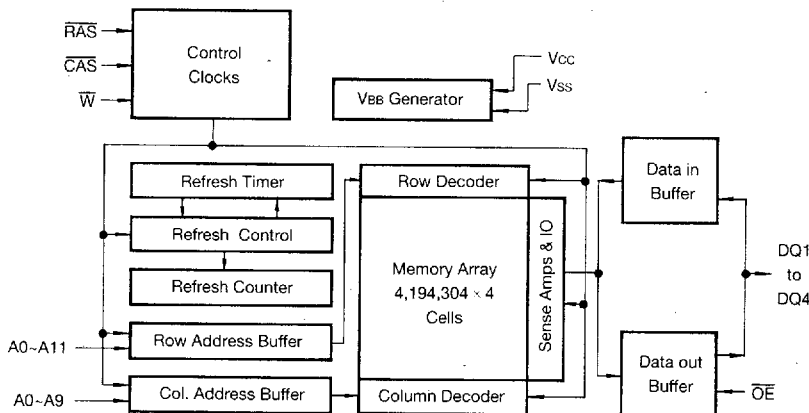
The Samsung KM44C4004A/AL/ALL/ASL is a high speed CMOS 4,194,304 bit x 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM44C4004A/AL/ALL/ASL features EDO Mode operation which allows high speed random access of memory cells within the same row.

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{\text{RAS}}$ -only refresh. All inputs and outputs are fully TTL compatible.

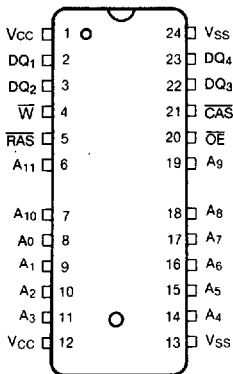
The KM44C4004A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



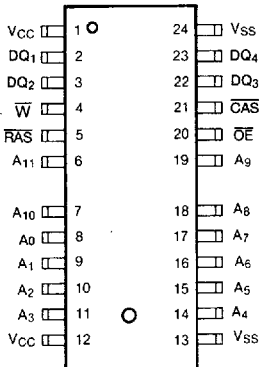
PIN CONFIGURATION (Top Views)

• KM44C4004 AJ/ALJ/ALLJ/ASLJ
AK/ALK/ALLK/ASLK



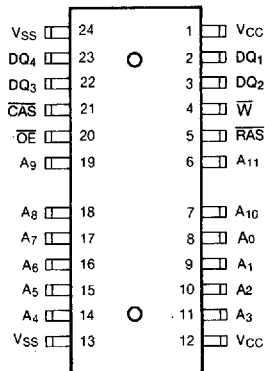
J : 400MIL
K : 300MIL

• KM44C4004 AT/ALT/ALLT/ASLT
AS/ALS/ALLS/ASLS



T : 400MIL(Forward)
S : 300MIL(Forward)

• KM44C4004 ATR/ALTR/ALLTR/ASLTR
ASR/ALSR/ALLSR/ASLSR



TR : 400MIL(Reverse)
SR : 300MIL(Reverse)

Pin Name	Pin Function
A0-A11	Address Inputs
DQ1-4	Data In/Out
Vss	Ground
RAS	Row Address Strobe
CAS	Column Address Strobe
W	Read/Write Input
OE	Data Output Enable
Vcc	Power(+5.0V)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V _{SS}	V _{IN} , V _{OUT}	-1 to + 7.0	V
Voltage on V _{CC} Supply Relative to V _{SS}	V _{CC}	-1 to + 7.0	V
Storage Temperature	T _{stg}	-55 to + 150	°C
Power Dissipation	P _D	1	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	—	V _{CC} + 1	V
Input Low Voltage	V _{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units	
Operating Current* (RAS and CAS Cycling @trc=min.)	KM44C4004A/AL/ALL/ASL-5	I _{CC1}	-	90	mA
	KM44C4004A/AL/ALL/ASL-6			80	mA
	KM44C4004A/AL/ALL/ASL-7			70	mA
	KM44C4004A/AL/ALL/ASL-8			60	mA
Standby Current (RAS=CAS=W=V _{IH})	KM44C4004A	I _{CC2}	-	2	mA
	KM44C4004AL			1	mA
	KM44C4004ALL			1	mA
	KM44C4004ASL			1	mA
RAS-Only Refresh Current* (CAS=V _{IH} , RAS Cycling @trc=min.)	KM44C4004A/AL/ALL/ASL-5	I _{CC3}	-	90	mA
	KM44C4004A/AL/ALL/ASL-6			80	mA
	KM44C4004A/AL/ALL/ASL-7			70	mA
	KM44C4004A/AL/ALL/ASL-8			60	mA
Hyper Page Mode Current* (RAS=V _{IL} , CAS, Address Cycling @tpc=min.)	KM44C4004A/AL/ALL/ASL-5	I _{CC4}	-	100	mA
	KM44C4004A/AL/ALL/ASL-6			90	mA
	KM44C4004A/AL/ALL/ASL-7			80	mA
	KM44C4004A/AL/ALL/ASL-8			70	mA
Standby Current (RAS=CAS=W=V _{CC} -0.2V)	KM44C4004A	I _{CC5}	-	1	mA
	KM44C4004AL			300	μA
	KM44C4004ALL			200	μA
	KM44C4004ASL			200	μA
CAS-Before-RAS Refresh Current* (RAS and CAS Cycling @trc=min.)	KM44C4004A/AL/ALL/ASL-5	I _{CC6}	-	90	mA
	KM44C4004A/AL/ALL/ASL-6			80	mA
	KM44C4004A/AL/ALL/ASL-7			70	mA
	KM44C4004A/AL/ALL/ASL-8			60	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V _{IH})=V _{CC} -0.2V Input Low Voltage(V _{IL})=0.2V CAS=CAS-Before-RAS Cycling or 0.2V DQ1-DQ4=Don't Care trc=31.25μs(L-Ver.) 62.5μs(SL-Ver.), tRAS=tRAS ≤ min-300ns	KM44C4004AL	I _{CC7}	-	450	μA
	KM44C4004ASL			350	μA

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DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Self Refresh Current $\overline{RAS}=\overline{CAS}=0.2V$ $W=\overline{OE}=A_0-A_{11}=V_{CC}-0.2V$ or $0.2V$ $DQ_1-DQ_4=V_{CC}-0.2V, 0.2V$ or Open	l _{ccs}	-	300	μA
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{CC}+0.5V$, all other pins not under test=0 volts.)	I _{I(L)}	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{CC}$)	I _{O(L)}	-10	10	μA
Output High Voltage Level (I _{OH} =-5mA)	V _{OH}	2.4	-	V
Output Low Voltage Level (I _{OL} =4.2mA)	V _{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}=V_{IL}$. In I_{CC4}, Address can be changed maximum once within one Hyper page cycle.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A ₀ -A ₁₁)	C _{IN1}	-	5	pF
Input Capacitance (\overline{RAS} , \overline{CAS} , W, \overline{OE})	C _{IN2}	-	7	pF
Input Capacitance (DQ ₁ -DQ ₄)	C _{DQ}	-	7	pF

AC CHARACTERISTICS (0°C ≤ T_a ≤ 70°C, V_{CC}=5.0V ± 0.5V, See notes 1,2)

Test condition: V_{IH}/V_{IL}=2.4V/0.8V, V_{OH}/V_{OL}=2.0V/0.8V, Output Loading C_L=100pF

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	90		110		130		150		ns	
Read-modify-write cycle time	t _{RWC}	133		155		185		205		ns	
Access time from \overline{RAS}	t _{RAC}		50		60		70		80	ns	3,4,11
Access time from \overline{CAS}	t _{CAC}		13		15		20		20	ns	3,4,5
Access time from column address	t _{AA}		25		30		35		40	ns	3,11
\overline{CAS} to output in Low-Z	t _{CLZ}	3		3		3		3		ns	3
\overline{OE} to output in Low-Z	t _{OLZ}	3		3		2		3		ns	3
Output buffer turn-off delay from \overline{CAS}	t _{CEZ}	3	13	3	15	3	20	3	20	ns	7,15
Transition time (rise and fall)	t _r	2	50	2	50	2	50	2	50	ns	2
\overline{RAS} precharge time	t _{RP}	30		40		50		60		ns	
\overline{RAS} pulse width	t _{RP}	50	10K	60	10K	70	10K	80	10K	ns	
\overline{RAS} hold time	t _{RSH}	13		15		20		20		ns	
\overline{CAS} hold time	t _{CSH}	38		45		50		60		ns	16
\overline{CAS} pulse width	t _{CAS}	8	10K	10	10K	15	10K	20	10K	ns	4
\overline{RAS} to \overline{CAS} delay time	t _{RCD}	20	37	20	45	20	50	20	60	ns	11
\overline{RAS} to column address delay time	t _{RAD}	15	25	15	30	15	35	15	40	ns	



AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
CAS to RAS precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	8		10		15		15		ns	
Column address hold time referenced to RAS	tAR	40		45		55		60		ns	6
Column address to RAS lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to CAS	tRCH	0		0		0		0		ns	9
Read command hold time referenced to RAS	tRRH	0		0		0		0		ns	9
Write command hold time	tWCH	10		10		15		15		ns	
Write command hold time referenced to RAS	tWCR	40		45		55		60		ns	6
Write command pulse width	tWP	10		10		15		15		ns	
Write command to RAS lead time	tRWL	13		15		20		20		ns	
Write command to CAS lead time	tCWL	8		10		15		20		ns	
Data set-up time	tDS	0		0		0		0		ns	10
Data hold time	tDH	10		10		15		15		ns	10
Data hold time referenced to RAS	tDHR	40		45		55		60		ns	6
Refresh period (Normal)	tREF		64		64		64		64	ms	
Refresh period (L-ver)	tREF		128		128		128		128	ms	
Refresh period (SL-ver)	tREF		256		256		256		256	ms	
Write command set-up time	tWCS	0		0		0		0		ns	8
CAS to W delay time	tCWD	36		40		50		50		ns	8
RAS to W delay time	tRWd	73		85		100		110		ns	8
Column address to W delay time	tAWd	48		55		65		70		ns	8
CAS precharge to W delay time	tCPWd	53		60		70		75		ns	8
CAS set-up time (CAS-before-RAS refresh)	tCSR	10		10		10		10		ns	
CAS hold time (CAS-before-RAS refresh)	tCHR	10		10		15		15		ns	
RAS to CAS precharge time	tRPC	5		5		5		5		ns	
CAS precharge time (C-B-R counter test cycle)	tCPT	20		20		30		30		ns	
Access time from CAS precharge	tCPA		30		35		40		45	ns	3
Hyper Page cycle time	tHPC	20		24		29		34		ns	17
Hyper Page read-modify-write cycle time	tHPRWC	62		71		86		96		ns	17
CAS precharge time (Hyper Page Cycle)	tCP	10		10		10		10		ns	
RAS pulse width (Hyper Page Cycle)	tRASP	50	200K	60	200K	70	200K	80	200K	ns	
RAS hold time from CAS precharge	tRHCP	30		35		40		45		ns	
OE access time	tOEA		13		15		20		20	ns	
OE to data delay	tOED	13		15		20		20		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Output buffer turn off delay time from \overline{OE}	toEZ	3	13	3	15	3	20	3	20	ns	7
\overline{OE} command hold time	toEH	13		15		20		20		ns	
Write command set-up time (Test mode in)	twTS	10		10		10		10		ns	12
Write command hold time (Test mode in)	twTH	10		10		10		10		ns	12
\overline{W} to \overline{RAS} precharge time (\overline{C} -B- \overline{R} refresh)	twRP	10		10		10		10		ns	
\overline{W} to \overline{RAS} hold time (\overline{C} -B- \overline{R} refresh)	twRH	10		10		10		10		ns	
Output data hold time	tDOH	5		5		5		5		ns	
Output buffer turn off delay from \overline{RAS}	trEZ	3	13	3	15	3	20	3	20	ns	7,16
Output buffer turn off delay from \overline{W}	twEZ	3	13	3	15	3	20	3	20	ns	7
\overline{W} to data delay	twED	15		15		20		20		ns	
\overline{OE} to \overline{CAS} hold time	toCH	5		5		5		5		ns	
\overline{CAS} hold time to \overline{OE}	tCHO	5		5		5		5		ns	
\overline{OE} precharge time	toEP	5		5		5		5		ns	
\overline{W} pulse width (Hyper Page Cycle)	twPE	5		5		5		5		ns	
\overline{RAS} pulse width (LL-ver)	trASS	100		100		100		100		μ s	15
\overline{RAS} precharge time (LL-ver)	trPS	90		110		130		150		ns	15
\overline{CAS} hold time (LL-ver)	tCHS	-50		-50		-50		-50		ns	15

TEST MODE CYCLE

(Note.12)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trC	95		115		135		155		ns	
Read-modify-write cycle time	trWC	138		160		190		210		ns	
Access time from \overline{RAS}	trAC		55		65		75		85	ns	3,4,11
Access time from \overline{CAS}	trAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,11
\overline{RAS} pulse width	trAS	55	10,000	65	10,000	75	10,000	85	10,000	ns	
\overline{CAS} pulse width	trAS	13	10,000	15	10,000	20	10,000	25	10,000	ns	
\overline{RAS} hold time	trSH	18		20		25		25		ns	
\overline{CAS} hold time	tCSH	43		20		55		65		ns	
Column address to \overline{RAS} lead time	trAL	30		35		40		45		ns	
\overline{CAS} to \overline{W} delay time	trWD	41		45		55		55		ns	8
\overline{RAS} to \overline{W} delay time	trWD	78		90		105		115		ns	8
Column address to \overline{W} delay time	tAWD	53		60		70		75		ns	8
Hyper Page cycle time	trPC	25		29		34		39		ns	
Hyper Page read-modify-write cycle time	trPRWC	67		76		91		101		ns	



TEST MODE CYCLE (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
RAS pulse width (Hyper Page Cycle)	tRASp	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{\text{CAS}}$ precharge	tCPA		35		40		45		50	ns	3
$\overline{\text{OE}}$ access time	tOEA		18		20		25		25	ns	
$\overline{\text{OE}}$ to data delay	tOED	18		20		25		25		ns	
$\overline{\text{OE}}$ command hold time	tOEH	18		20		25		25		ns	

TEST MODE DESCRIPTION

The KM44C4004A/AL/ALL/ASL is the CMOS DRAM organized 4,194,304 words by 4 bit internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A0 is not used. If upon reading, two bits on one I/O pin are equal (all "1" or "0"s) the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In "Test Mode", the 4Mx4 DRAM can be tested as if it were a 1Mx4

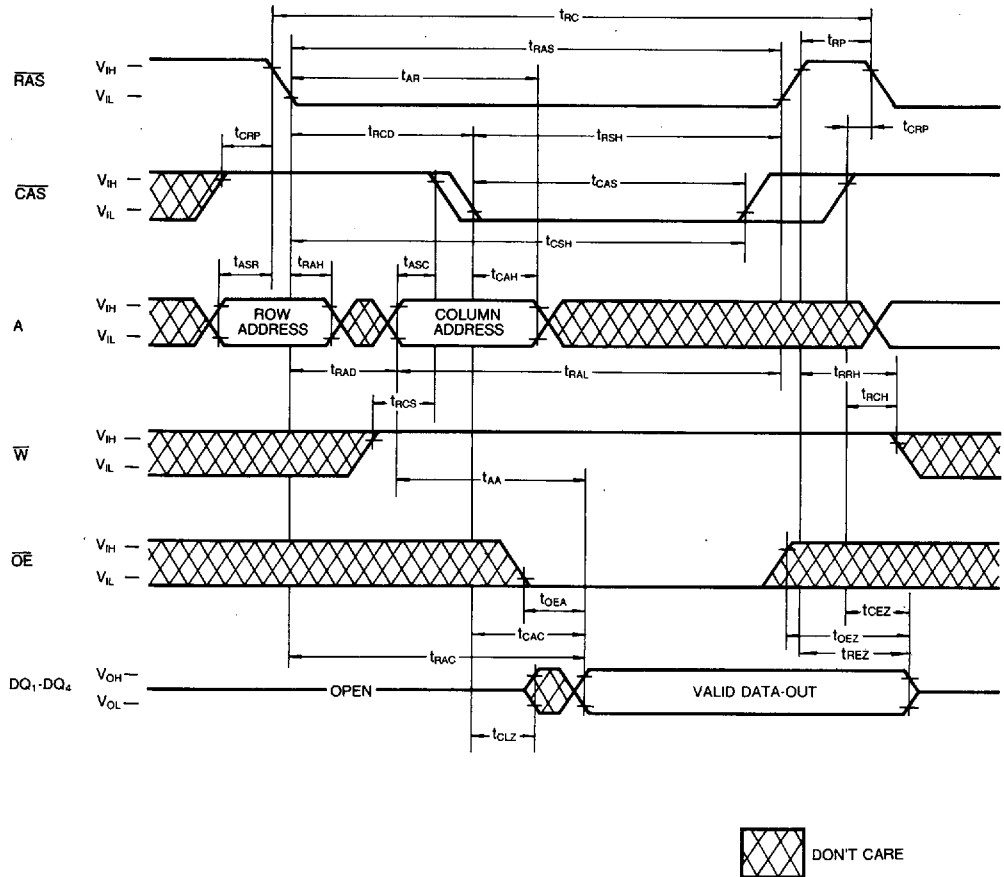
DRAM. $\overline{\text{W}}$ and $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Cycle (WCBR, Test Mode In Cycle) puts the device into "Test Mode", and " $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle" or " $\overline{\text{RAS}}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, " $\overline{\text{W}}$ and $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle" performs the refresh operation with internal CBR refresh address counter. The "Test Mode" function reduces test time(1/4 in cases of N test pattern)

NOTES

1. An initial pause of 200µs is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. VIH(min) and VIL(max) are reference levels for measuring timing of input signals. Transition times are measured between VIH(min) and VIL(max) are assumed to be 5ns for all inputs, without tHPC and tHPRWC.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD ≥ tRCD (max).
6. tAR, tWCR, tDHR are referenced to tRAD(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
8. twcs, trawd, tcwd and tawd are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If twcs ≥ twcs(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tcwd ≥ tcwd(min), trawd ≥ trawd(min) and tawd ≥ tawd(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either tRCH or tRRH must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles and to the $\overline{\text{W}}$ leading edge in read-write cycles.
11. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. tREZ(max), tCEZ(max), tWEZ(max) and tOEZ(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 4096 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.
16. If RAS goes high before CAS high going, the open circuit condition of the output is achieved by $\overline{\text{CAS}}$ high going. If CAS goes high before RAS high going, the open circuit condition of the output is achieved by RAS high going
17. tASC ≥ tCP (min), Assumtn tT=2.0ns

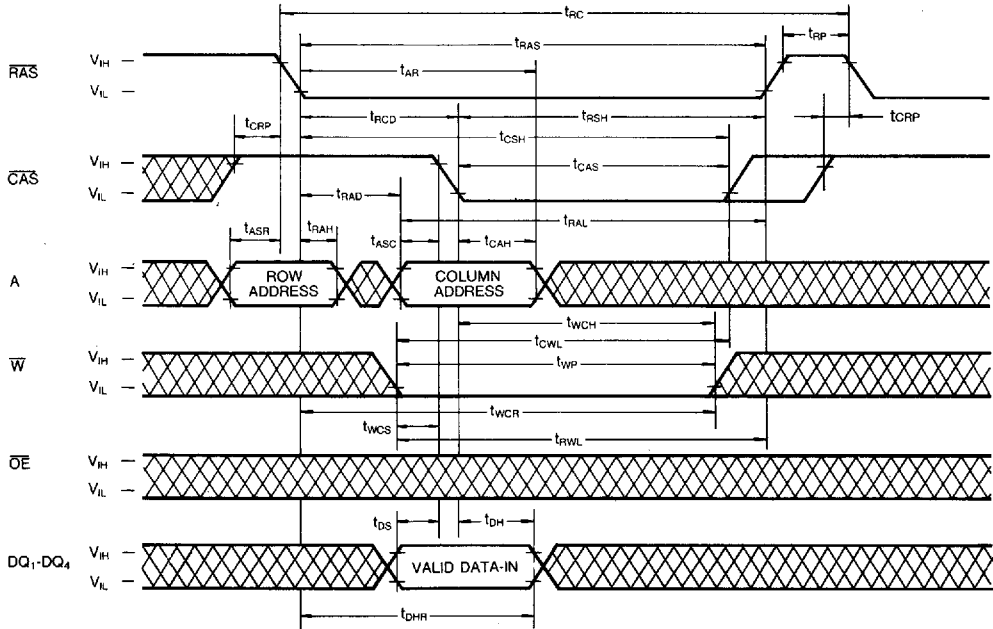


TIMING DIAGRAMS
READ CYCLE

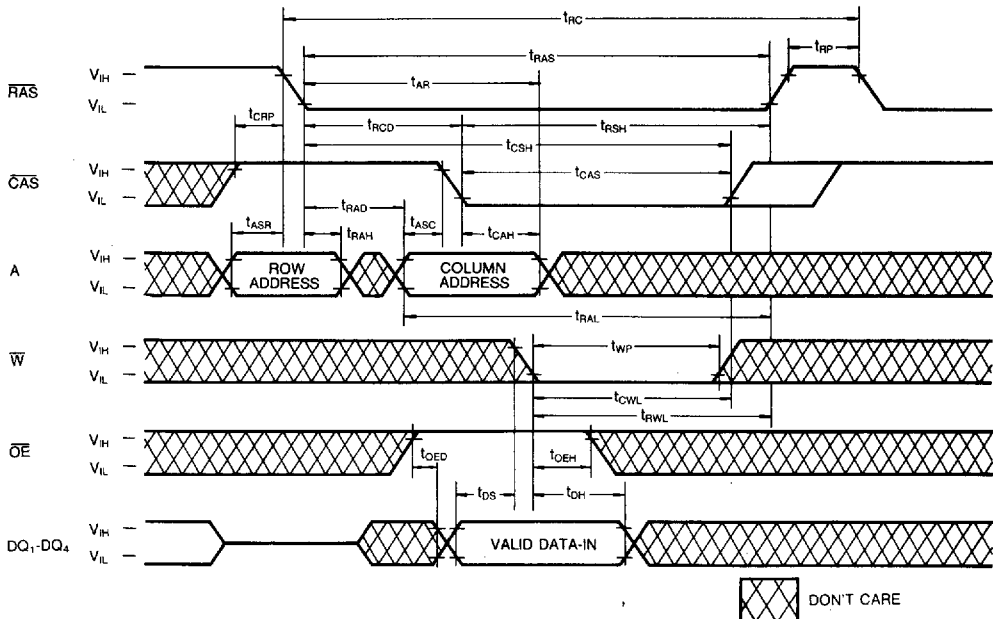


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY CYCLE)



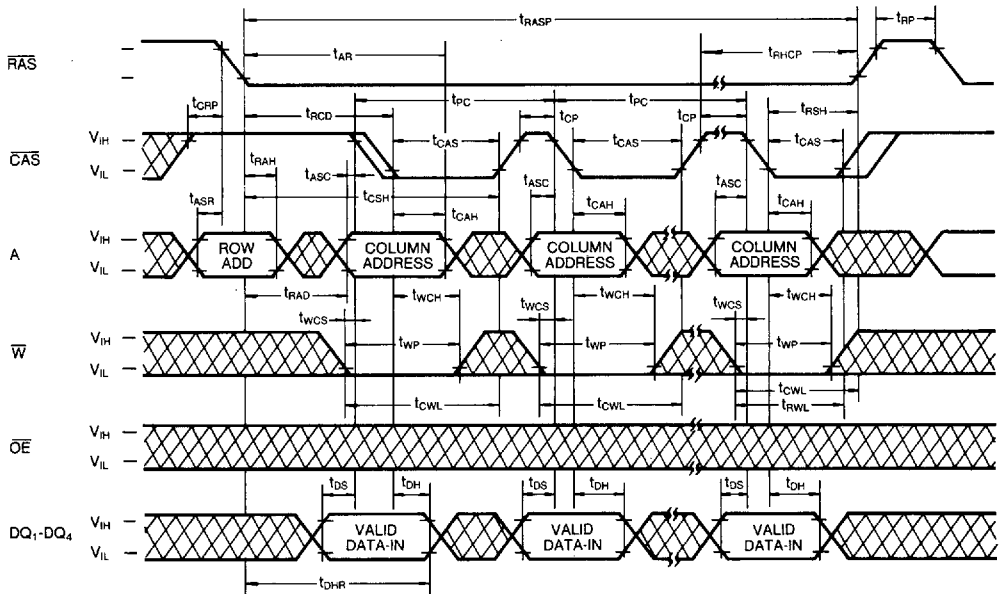
WRITE CYCLE (\overline{OE} CONTROLLED WRITE)



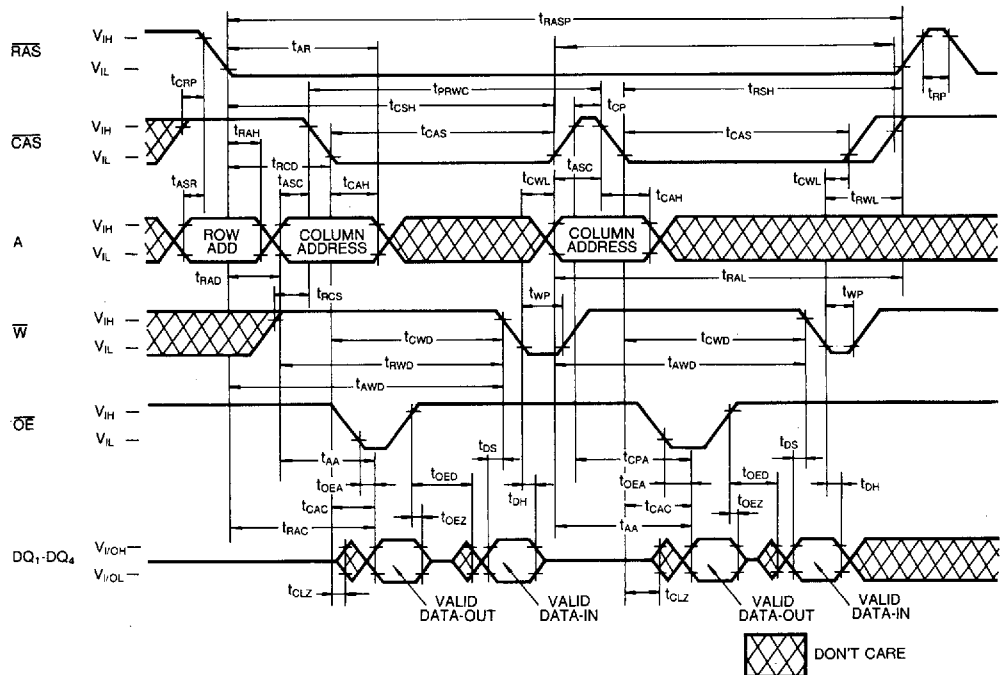
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TIMING DIAGRAMS (Continued)

HYPER PAGE WRITE CYCLE (EARLY WRITE)



HYPER PAGE READ-MODIFY-WRITE CYCLE

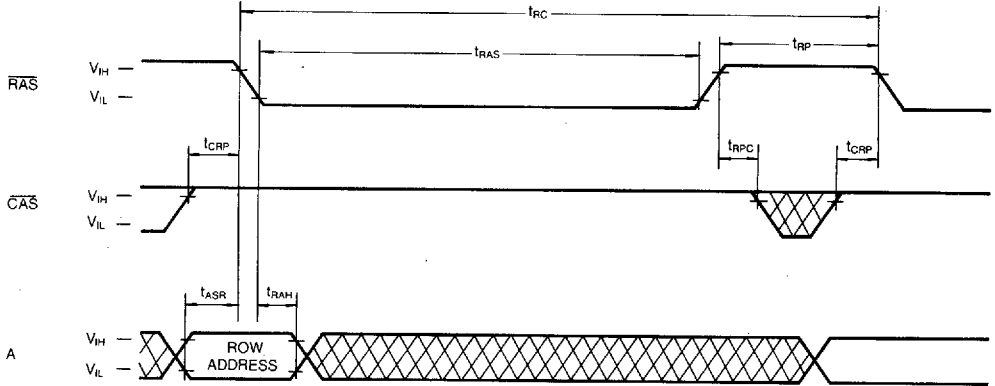


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TIMING DIAGRAMS (Continued)

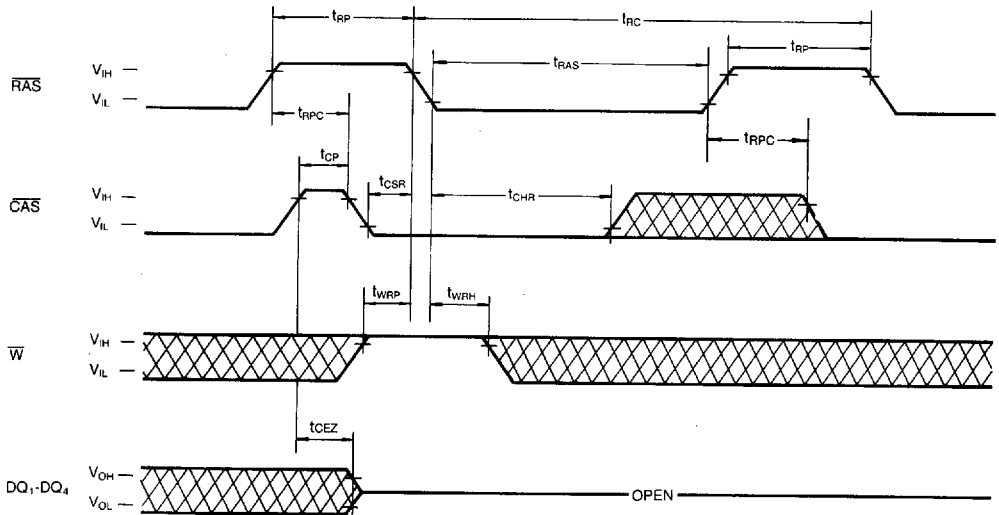
RAS-ONLY REFRESH CYCLE

Note: \overline{W} , \overline{OE} =Don't Care



CAS-BEFORE-RAS REFRESH CYCLE

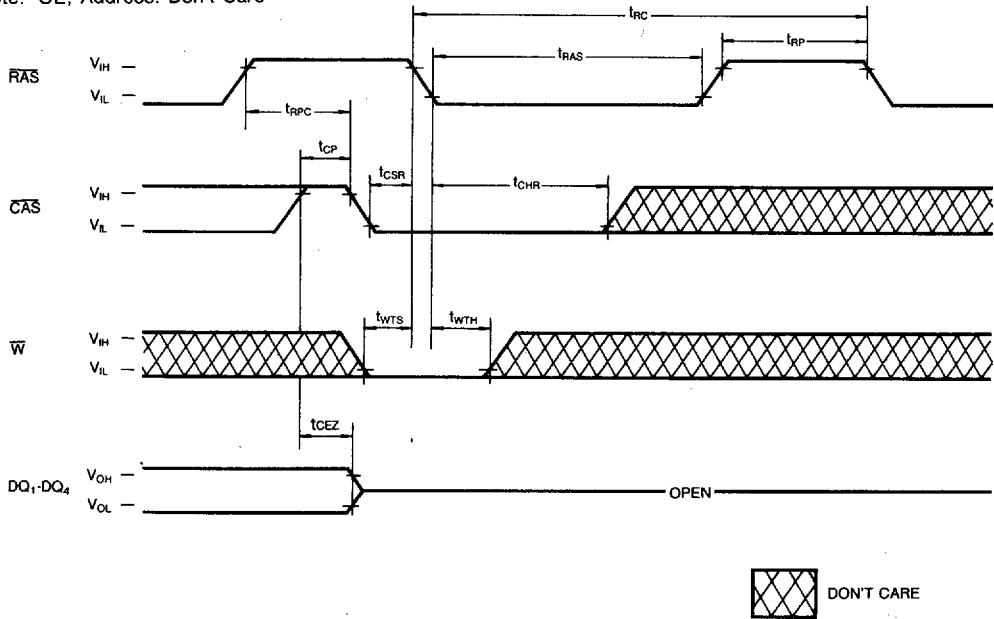
Note: \overline{OE} , Address=Don't Care



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

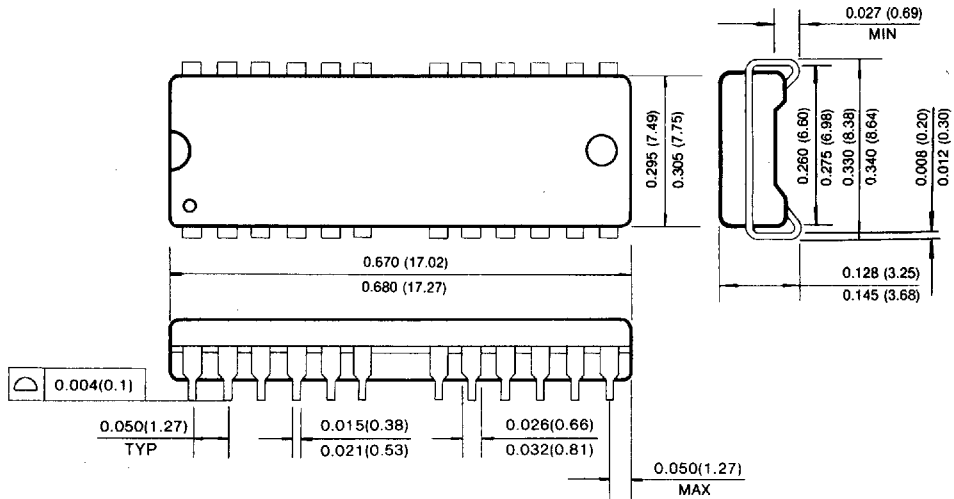
Note: \overline{OE} , Address: Don't Care



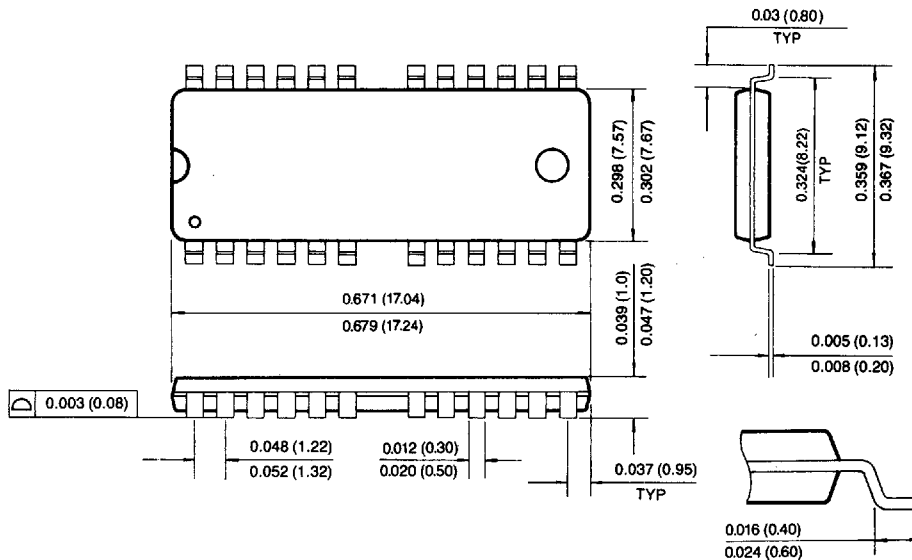
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (300MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II) (300MIL, Forward and Reverse Type)

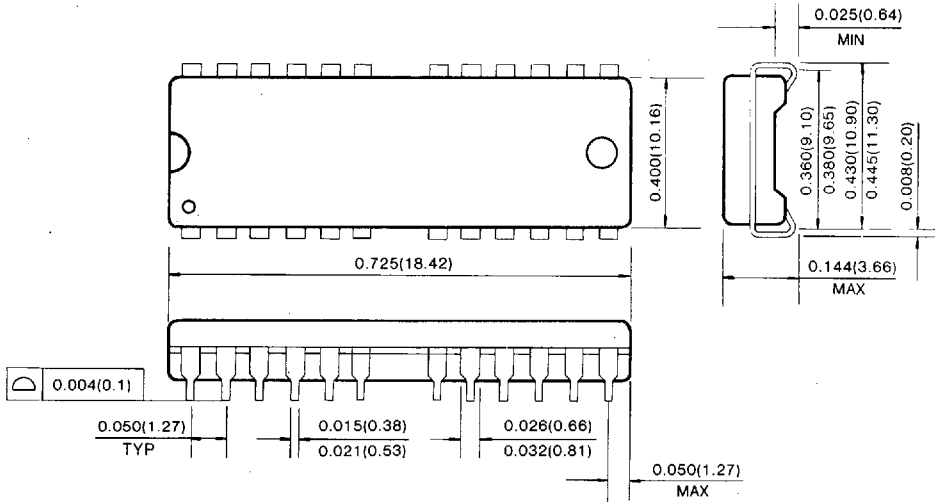


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PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (400MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (400MIL, Forward and Reverse Type)

