

# DRAM MODULE

## 256K x 9 DRAM

FAST PAGE MODE (MT3D2569)  
LOW POWER,  
EXTENDED REFRESH (MT3D2569 L)

### FEATURES

- Industry standard pinout in a 30-pin single-in-line memory module
- High-performance, CMOS silicon-gate process
- Single 5V  $\pm 10\%$  power supply
- Low power, 9mW (.9mW L-version) standby; 625mW active, typical
- All device pins are fully TTL compatible
- FAST PAGE MODE access cycle
- Refresh modes:  $\overline{\text{RAS}}$ -ONLY,  $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$  (CBR) and HIDDEN
- 512-cycle refresh distributed across 8ms or 512-cycle extended refresh distributed across 64ms
- Low CMOS standby current, 60 $\mu$ A maximum (L-version)

### OPTIONS

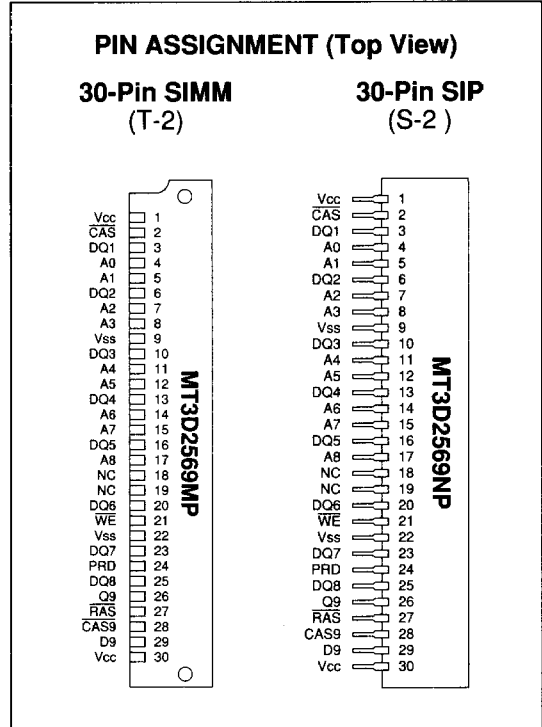
- Timing
  - 60ns access
  - 70ns access
  - 80ns access
- Packages
  - Leadless 30-pin SIMM
  - Leaded 30-pin SIP
- Access Mode
  - FAST PAGE MODE
- Power/Refresh
  - Normal Power/8ms
  - Low Power/64ms

### MARKING

-6  
-7  
-8  
  
M  
N  
  
P  
  
Blank  
L

### GENERAL DESCRIPTION

The MT3D2569 is a randomly accessed solid-state memory containing 262,144 words organized in a x9 configuration. During READ or WRITE cycles, each word is uniquely addressed through the 18 address bits, which are entered nine bits (A0-A8) at a time.  $\overline{\text{RAS}}$  is used to latch the first nine bits and  $\overline{\text{CAS}}$  the latter nine bits. READ or WRITE cycles are selected with the  $\overline{\text{WE}}$  input. A logic HIGH on  $\overline{\text{WE}}$  dictates READ mode while a logic LOW on  $\overline{\text{WE}}$  dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of  $\overline{\text{WE}}$  or  $\overline{\text{CAS}}$ , whichever occurs last. EARLY-WRITE occurs when  $\overline{\text{WE}}$  goes LOW prior to  $\overline{\text{CAS}}$  going LOW, and the output pins remain open (High-Z) until the next  $\overline{\text{CAS}}$  cycle.

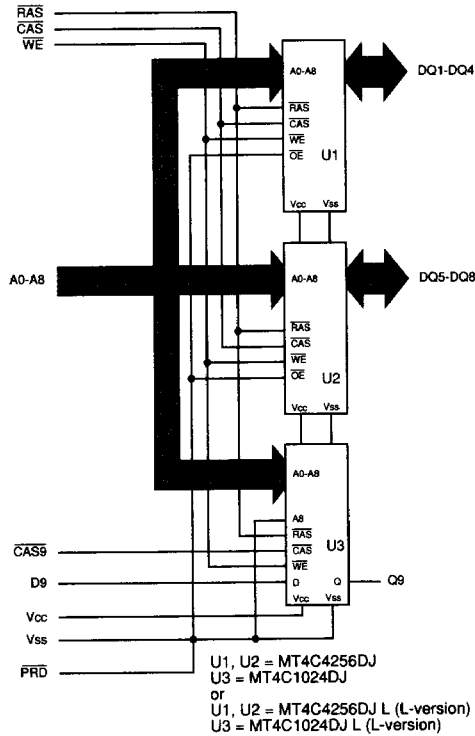


FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by  $\overline{\text{RAS}}$  followed by a column address strobed-in by  $\overline{\text{CAS}}$ .  $\overline{\text{CAS}}$  may be toggled-in by holding  $\overline{\text{RAS}}$  LOW and strobing-in different column addresses, thus executing faster memory cycles.

Returning  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the  $\overline{\text{RAS}}$  high time. Memory cell data is retained in its correct state by maintaining power and executing any  $\overline{\text{RAS}}$  cycle (READ, WRITE,  $\overline{\text{RAS}}$ -ONLY,  $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$  or HIDDEN REFRESH) so that all 512 combinations of  $\overline{\text{RAS}}$  addresses (A0-A8) are executed at least every 8ms (64ms on L-version), regardless of sequence.

**DRAM MODULE**

FUNCTIONAL BLOCK DIAGRAM



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TRUTH TABLE

FUNCTION		RAS	CAS	CAS9	WE	ADDRESSES		DATA IN/OUT
						'R	'C	DQ1-DQ8, D9, Q9
Standby		H	H→X	H→X	X	X	X	High-Z
READ		L	L	L	H	ROW	COL	Data Out
EARLY-WRITE		L	L	L	L	ROW	COL	Data In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H→L	H	ROW	COL	Data Out
	2nd Cycle	L	H→L	H→L	H	n/a	COL	Data Out
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L	H→L	L	ROW	COL	Data In
	2nd Cycle	L	H→L	H→L	L	n/a	COL	Data In
RAS-ONLY REFRESH		L	H	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	L	H	ROW	COL	Data Out
	WRITE	L→H→L	L	L	L	ROW	COL	Data In
CAS-BEFORE-RAS REFRESH		H→L	L	L	X	X	X	High-Z
BATTERY BACKUP REFRESH (L-version)		H→L	L	L	X	X	X	High-Z

**ABSOLUTE MAXIMUM RATINGS\***

Voltage on Vcc Supply Relative to Vss .....	-1V to +7V
Operating Temperature, T <sub>A</sub> (Ambient) .....	0°C to +70°C
Storage Temperature .....	-55°C to +125°C
Power Dissipation .....	3W
Short Circuit Output Current .....	50mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS**

(Notes: 1, 2, 3, 6, 22) (0°C ≤ T<sub>A</sub> ≤ 70°C; V<sub>cc</sub> = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V <sub>cc</sub>	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V <sub>IH</sub>	2.4	V <sub>cc</sub> +1	V	1
Input Low (Logic 0) Voltage, All Inputs	V <sub>IL</sub>	-1.0	0.8	V	1
INPUT LEAKAGE Any Input 0V ≤ V <sub>IN</sub> ≤ V <sub>cc</sub> , (All other pins not under test = 0V)	D9, $\overline{\text{CAS}}$	I <sub>I</sub>	-2	2	μA
	A0-A8, $\overline{\text{RAS}}$ , $\overline{\text{WE}}$	I <sub>I</sub>	-6	6	μA
OUTPUT LEAKAGE (Q is disabled, 0V ≤ V <sub>OUT</sub> ≤ V <sub>cc</sub> )	DQ1-DQ8, Q9	I <sub>OZ</sub>	-10	10	μA
OUTPUT LEVELS Output High (Logic 1) Voltage (I <sub>OUT</sub> = -5mA) Output Low (Logic 0) Voltage (I <sub>OUT</sub> = 5mA)	V <sub>OH</sub>	2.4		V	
	V <sub>OL</sub>		0.4	V	

**DRAM MODULE**

PARAMETER/CONDITION	SYMBOL	MAX			UNITS	NOTES
		-6	-7	-8		
STANDBY CURRENT: (TTL) ( $\overline{\text{RAS}} = \overline{\text{CAS}} = V_{IH}$ )	I <sub>cc1</sub>	6	6	6	mA	
STANDBY CURRENT: (CMOS) ( $\overline{\text{RAS}} = \overline{\text{CAS}} = V_{cc} - 0.2V$ )	I <sub>cc2</sub>	3	3	3	mA	24
		.6	.6	.6	mA	24, 26
OPERATING CURRENT: Random READ/WRITE Average power supply current ( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , Address Cycling: $t^1RC = t^1RC$ (MIN))	I <sub>cc3</sub>	270	240	210	mA	2, 22
		255	225	195	mA	2,22,26
OPERATING CURRENT: FAST PAGE MODE Average power supply current ( $\overline{\text{RAS}} = V_{IL}$ , $\overline{\text{CAS}}$ , Address Cycling: $t^1PC = t^1PC$ (MIN))	I <sub>cc4</sub>	210	180	150	mA	2, 22
		195	165	135	mA	2,22,26
REFRESH CURRENT: $\overline{\text{RAS}}$ -ONLY Average power supply current ( $\overline{\text{RAS}}$ Cycling, $\overline{\text{CAS}} = V_{IH}$ : $t^1RC = t^1RC$ (MIN))	I <sub>cc5</sub>	270	240	210	mA	2
		255	225	195	mA	2, 26
REFRESH CURRENT: $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ Average power supply current ( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , Address Cycling: $t^1RC = t^1RC$ (MIN))	I <sub>cc6</sub>	270	240	210	mA	2, 19
		255	225	195	mA	2,19,26
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: $\overline{\text{CAS}} = 0.2V$ or $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ cycling; $\overline{\text{RAS}} = t^1RAS$ (MIN) to 1μs; $\overline{\text{WE}}$ , A0-A9 and D <sub>IN</sub> = V <sub>cc</sub> - 0.2V or 0.2V (D <sub>IN</sub> may be left OPEN), $t^1RC = 125\mu s$ (512 rows at 125μs = 64ms)	I <sub>cc7</sub>	.6	.6	.6	mA	26

## CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C <sub>I1</sub>		19	pF	17
Input Capacitance: RAS, CAS, WE	C <sub>I2</sub>		25	pF	17
Input Capacitance: D9	C <sub>I3</sub>		10	pF	17
Input/Output Capacitance: DQ1-DQ8	C <sub>I0</sub>		15	pF	17
Output Capacitance: Q9	C <sub>O</sub>		10	pF	17

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) (0°C ≤ T<sub>A</sub> ≤ +70°C; V<sub>CC</sub> = 5V ±10%)

AC CHARACTERISTICS	SYM	-6		-7		-8		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
Random READ or WRITE cycle time	<sup>1</sup> RC	110		130		150		ns	
READ-WRITE cycle time	<sup>1</sup> RWC	n/a		n/a		n/a		n/a	21
FAST-PAGE-MODE READ or WRITE cycle time	<sup>1</sup> PC	40		40		45		ns	
PAGE-MODE READ or WRITE cycle time	<sup>1</sup> PC	n/a		n/a		n/a		ns	
Access time from RAS	<sup>1</sup> RAC		60		70		80	ns	8
Access time from CAS (FAST PAGE MODE)	<sup>1</sup> CAC		20		20		20	ns	9
Output Enable	<sup>1</sup> OE		20		20		20	ns	
Access time from column address	<sup>1</sup> AA		30		35		40	ns	
Access time from CAS precharge	<sup>1</sup> CPA		35		40		45	ns	
RAS pulse width	<sup>1</sup> RAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (FAST PAGE MODE)	<sup>1</sup> RASP	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	<sup>1</sup> RSH	20		20		20		ns	
RAS precharge time	<sup>1</sup> RP	40		50		60		ns	
CAS pulse width	<sup>1</sup> CAS	20	100,000	20	100,000	20	100,000	ns	
CAS hold time	<sup>1</sup> CSH	60		70		80		ns	
CAS precharge time	<sup>1</sup> CPN	10		10		10		ns	18
CAS precharge time (FAST PAGE MODE)	<sup>1</sup> CP	10		10		10		ns	
RAS to CAS delay time	<sup>1</sup> RCD	20	40	20	50	20	60	ns	13
CAS to RAS precharge time	<sup>1</sup> CRP	5		5		5		ns	
Row address setup time	<sup>1</sup> ASR	0		0		0		ns	
Row address hold time	<sup>1</sup> RAH	10		10		10		ns	
RAS to column address delay time	<sup>1</sup> RAD	15	30	15	35	15	40	ns	24
Column address setup time	<sup>1</sup> ASC	0		0		0		ns	
Column address hold time	<sup>1</sup> CAH	15		15		15		ns	
Column address hold time (referenced to RAS)	<sup>1</sup> AR	45		55		60		ns	
Column address to RAS lead time	<sup>1</sup> RAL	30		35		40		ns	
Read command setup time	<sup>1</sup> RCS	0		0		0		ns	
Read command hold time (referenced to CAS)	<sup>1</sup> RCH	0		0		0		ns	25
Read command hold time (referenced to RAS)	<sup>1</sup> RRH	0		0		0		ns	25

# DRAM MODULE

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

(Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) ( $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ ;  $V_{CC} = 5V \pm 10\%$ )

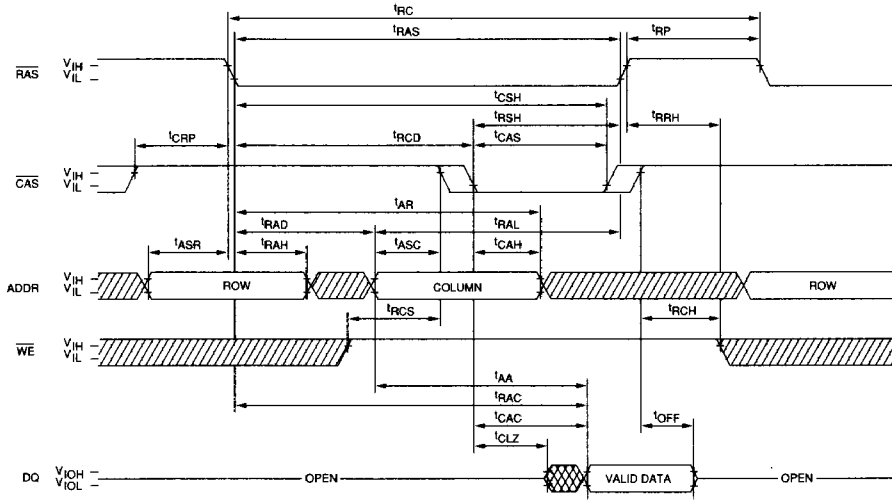
AC CHARACTERISTICS PARAMETER	SYM	-6		-7		-8		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
CAS to output in Low-Z	<sup>t</sup> CLZ	0		0		0		ns	
Output buffer turn-off delay	<sup>t</sup> OFF	0	20	0	20	0	20	ns	12
WE command setup time	<sup>t</sup> WCS	0		0		0		ns	
Write command hold time	<sup>t</sup> WCH	10		15		15		ns	
Write command hold time (referenced to RAS)	<sup>t</sup> WCR	45		55		60		ns	
Write command pulse width	<sup>t</sup> WP	10		15		15		ns	
Write command to RAS lead time	<sup>t</sup> RWL	20		20		20		ns	
Write command to CAS lead time	<sup>t</sup> CWL	20		20		20		ns	
Data-in setup time	<sup>t</sup> DS	0		0		0		ns	15
Data-in hold time	<sup>t</sup> DH	15		15		15		ns	15
Data-in hold time (referenced to RAS)	<sup>t</sup> DHR	45		55		60		ns	
Transition time (rise or fall)	<sup>t</sup> T	3	50	3	50	3	50	ns	5, 16
Refresh period (512 cycles)	<sup>t</sup> REF		8/64		8/64		8/64	ms	3/26
RAS to CAS precharge time	<sup>t</sup> RPC	0		0		0		ns	
CAS setup time (CAS-BEFORE-RAS REFRESH)	<sup>t</sup> CSR	10		10		10		ns	19
CAS hold time (CAS-BEFORE-RAS REFRESH)	<sup>t</sup> CHR	10		15		15		ns	19

**DRAM MODULE**

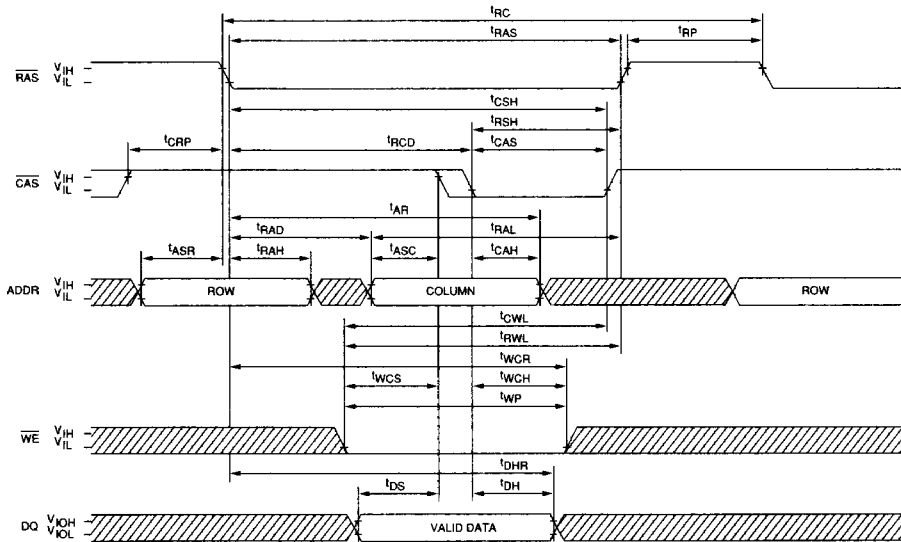
## NOTES

1. All voltages referenced to  $V_{SS}$ .
2.  $I_{CC}$  is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100 $\mu$ s is required after power-up followed by any eight  $\overline{RAS}$  cycles before proper device operation is assured. The eight  $\overline{RAS}$  cycle wake-up should be repeated any time the  $t_{REF}$  refresh requirement is exceeded.
4. AC characteristics assume  $t_T = 5$ ns.
5.  $V_{IH}$  (MIN) and  $V_{IL}$  (MAX) are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ( $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ ) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that  $t_{RCD} < t_{RCD}(\text{MAX})$ . If  $t_{RCD}$  is greater than the maximum recommended value shown in this table,  $t_{RAC}$  will increase by the amount that  $t_{RCD}$  exceeds the value shown.
9. Assumes that  $t_{RCD} \geq t_{RCD}(\text{MAX})$ .
10. If  $\overline{CAS} = V_{IH}$ , data output is High-Z.
11. If  $\overline{CAS} = V_{IL}$ , data output may contain data from the last valid READ cycle.
12.  $t_{OFF}(\text{MAX})$  defines the time at which the output achieves the open circuit condition and is not referenced to  $V_{OH}$  or  $V_{OL}$ .
13. Operation within the  $t_{RCD}(\text{MAX})$  limit ensures that  $t_{RAC}(\text{MAX})$  can be met.  $t_{RCD}(\text{MAX})$  is specified as a reference point only; if  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{MAX})$  limit, then access time is controlled exclusively by  $t_{CAC}$ .
14.  $t_{RCH}$  is referenced to the first rising edge of  $\overline{RAS}$  or  $\overline{CAS}$ .
15. These parameters are referenced to  $\overline{CAS}$  leading edge in EARLY-WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between  $V_{IH}$  and  $V_{IL}$  (or between  $V_{IL}$  and  $V_{IH}$ ) in a monotonic manner.
17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC,  $V_{CC} = 5$ V, DC bias = 2.4V @ 15mV RMS).
18. If  $\overline{CAS}$  is LOW at the falling edge of  $\overline{RAS}$ , data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer,  $\overline{CAS}$  must be pulsed HIGH for  $t_{CP}$ .
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case,  $\overline{WE} = \text{LOW}$ .
21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to  $\overline{OE}$  being grounded on U1 and U2.
22.  $I_{CC}$  is dependent on cycle rates.
23. All other inputs at  $V_{CC} - 0.2$ V.
24. Operation within the  $t_{RAD}(\text{MAX})$  limit ensures that  $t_{RCD}(\text{MAX})$  can be met.  $t_{RAD}(\text{MAX})$  is specified as a reference point only; if  $t_{RAD}$  is greater than the specified  $t_{RAD}(\text{MAX})$  limit, then access time is controlled exclusively by  $t_{AA}$ .
25. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a READ cycle.
26. Applies to L-version only.

READ CYCLE



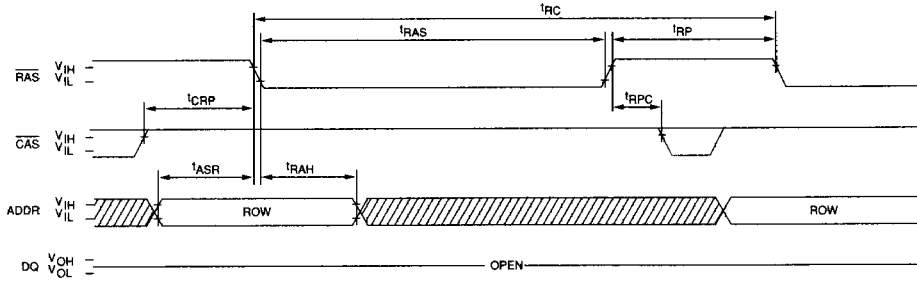
EARLY-WRITE CYCLE



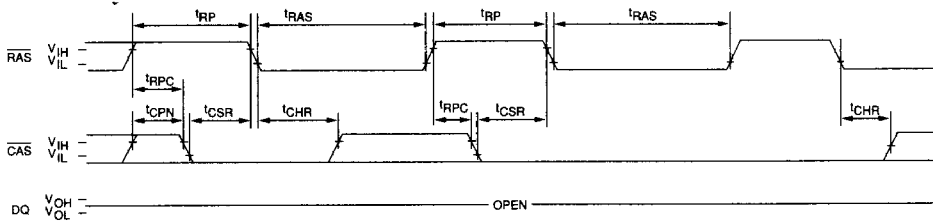
▨ DON'T CARE  
▩ UNDEFINED



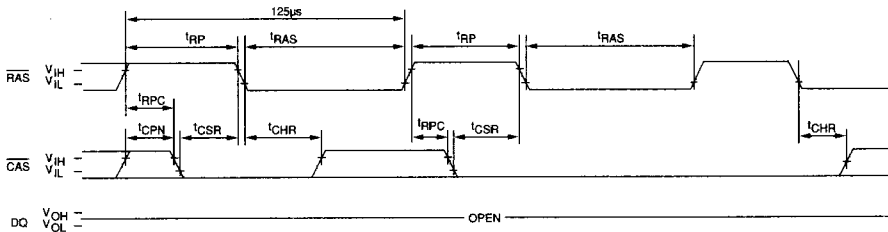
**RAS-ONLY REFRESH CYCLE**  
(ADDR = A0-A8;  $\overline{WE}$  = DON'T CARE)





**CAS-BEFORE-RAS REFRESH CYCLE**  
(A0-A8 and  $\overline{WE}$  = DON'T CARE)

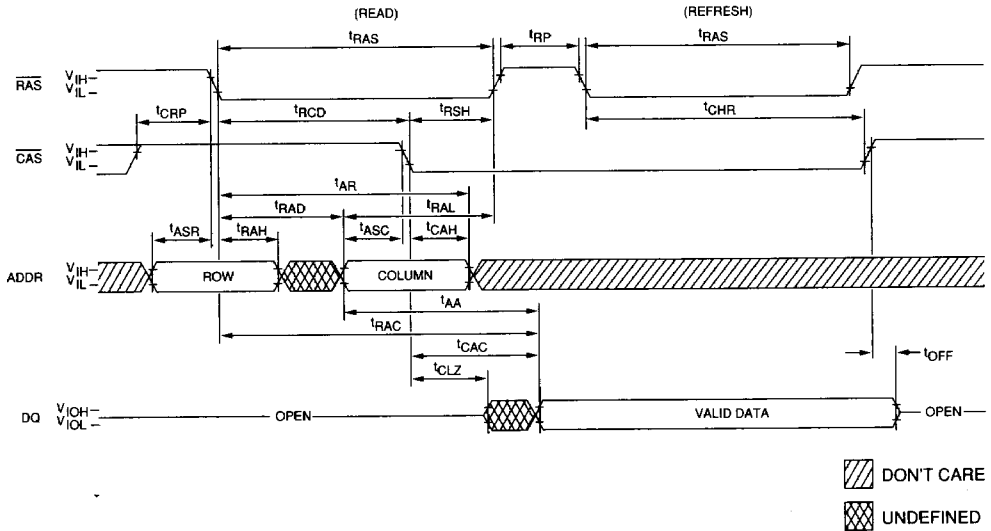


**BATTERY BACKUP REFRESH CYCLE** <sup>26</sup>  
(A0-A8 and  $\overline{WE}$  = DON'T CARE)



 DON'T CARE  
 UNDEFINED

HIDDEN REFRESH CYCLE <sup>20</sup>  
(WE = HIGH)



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