Raytheon

TMC22070 Genlocking Video Digitizer

The TMC22070 Genlocking Video Digitizer converts standard baseband composite NTSC or PAL video into 8-bit digital composite video data. It extracts horizontal and vertical sync signals and generates a pixel clock for the on-board 8-bit A/D converter and a 2x clock for the transfer of data to subsequent video processing such as its companion TMC22090/TMC22190 Digital Video Encoder. It also determines the color subcarrier phase and frequency, and provides this data to the Encoder (for genlocked color NTSC or PAL encoding), or a frame buffer (for frame capture) over the digital composite video port.

The TMC22070 includes a three-channel video input multiplexer, analog clamp, variable gain amplifier, and digital back porch clamp. The on-board oscillator circuitry generates the clock from a 20 MHz crystal or the clock source may be an external oscillator. It is programmable over a microprocessor interface for NTSC or PAL operation. No external component changes and no production tuning or service adjustments are ever required.

The TMC22070 is fabricated in Raytheon's OMICRON-C^{TM} 1μ CMOS process, and is packaged in a 68-lead PLCC. Its performance is guaranteed over the full 0°C to 70°C temperature range.

Applications

- Frame Grabber
- Digital VCR/VTR
- Desktop Video

Features

- Fully Integrated Acquisition
  - 3-Channel Video Input Multiplexer
  - Two-Stage Video Clamp
  - Automatic Gain Adjustment
  - Sync Detection And Separation
  - Genlock to NTSC Or PAL Inputs
  - Clock Generation
  - 8-bit Video A/D Converter
- Microprocessor Interface
- Line-Locked Pixel Rates
  - 12.27 MHz NTSC
  - 13.5 MHz NTSC Or PAL
  - 14.75 MHz And 15.0 MHz PAL
- Direct Interface To TMC22090/TMC22190 Encoders
- Built-In Circuitry For Crystal Oscillator
- No Tuning Or External Voltage Reference Required
- 68 Lead PLCC Package

Related Products

- TMC22090/TMC22190 Digital Video Encoder
- TMC2242/TMC2243/TMC2246 Video Filter
- TMC2249 Digital Mixer
- TMC2255 Convolver
- TMC2272 Colorspace Converter
- TMC2302 Image Manipulation Sequencer

Figure 1. Logic Symbol

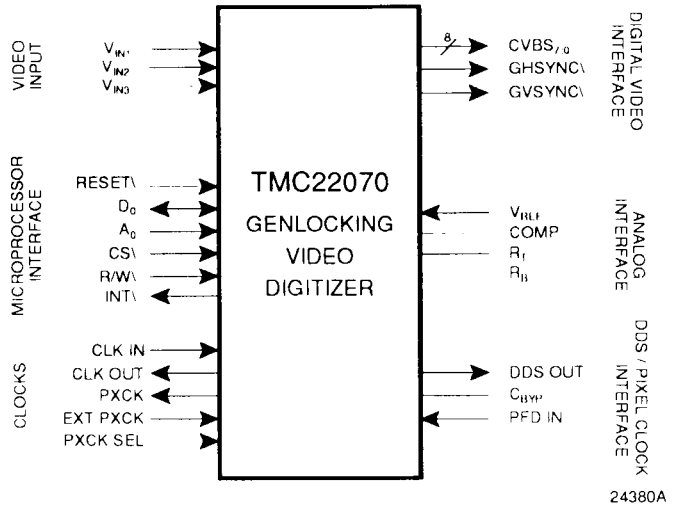

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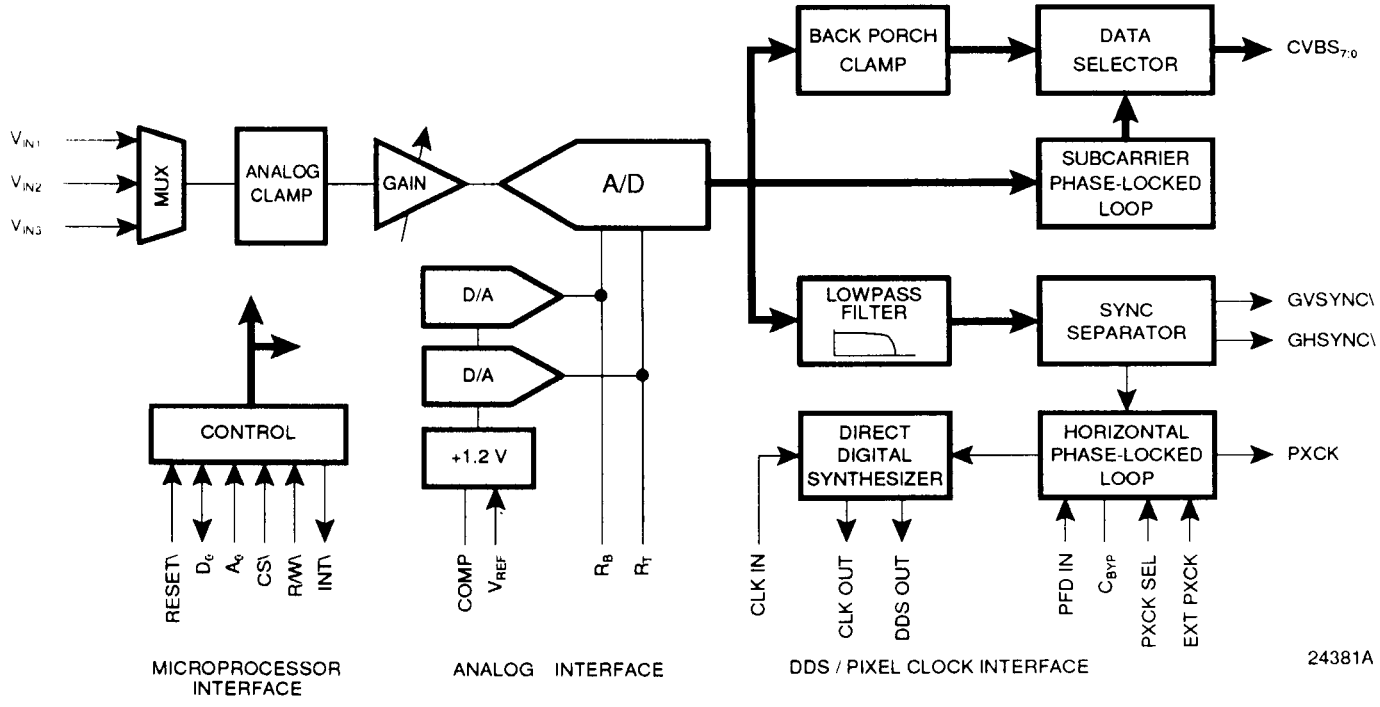
Figure 2. Functional Block Diagram



General Description

The TMC22070 is a fully-integrated genlocking video A/D converter which digitizes NTSC or PAL baseband composite video under program control. It accepts video on three selectable input channels, adjusts gain, clamps to the back porch, and digitizes the video at a multiple of the line rate. It extracts horizontal and vertical sync, identifies odd/even fields, measures the subcarrier frequency and phase (relative to the sampling clock), and provides this data along with digital composite video data over an 8-bit digital video port and two sync outputs (GHSYNC\ and GVSYNC\). It generates a 2x pixel clock (PXCK) for data transfer. PXCK also serves as a master clock for the companion TMC22090/TMC22190 Encoders.

Operating parameters are set up via a standard microprocessor port. Provisions have been made for internal or external voltage reference operation.

Timing

The TMC22070 operates from an internally-synthesized clock, PXCK, which runs at twice the pixel data rate. The nominal pixel rates may be set to 12.27 Mpps for NTSC, 13.5 Mpps for NTSC and PAL, and 14.75 Mpps or 15.0 Mpps for PAL operation.

Video Input

Three high-impedance video inputs are selected by an internal multiplexer under host processor control. The device accepts industry-standard video levels of 1.23 Volts (sync tip to peak color). Good channel-to-channel isolation allows active video on all three inputs simultaneously. Anti-aliasing filtering (if used) and line termination resistors must be provided externally. The input selection is controlled by two bits in the Control Register.

Analog Clamp

The front-end analog clamp ensures that the input video falls within the active range of the A/D converter. The digitized composite video output is clamped to the back porch by a secondary digital clamp.

Automatic Gain Adjustment

Since video signals may vary substantially from nominal levels, the TMC22070 performs an automatic level setting routine to establish correct signal amplitudes for digitizing.

Video signal amplitude errors are usually an artifact of video processing gain, filter losses, cable terminations, etc. The TMC22070 relies upon the presence of the sync tip-to-back porch voltage to determine the gain required for the input video signal.

Sync tip compression or clipping is often affected by APL (Average Picture Level). Rather than tracking minor variations in sync tip amplitude and constantly adjusting video gain, the TMC22070 establishes proper signal amplitudes during initial genlock acquisition, and then (optionally) holds the gain constant. This results in a stable picture under variable signal conditions.

Improper termination of video cables (usually double termination) is handled in the TMC22070 by a selectable gain of +1.0 or +1.5. The higher gain is used to amplify a doubly-terminated signal which are reduced in amplitude by 2/3.

If the input signal levels are well controlled, the automatic gain adjustment can be disabled and the gain held at its nominal value (+1.0 or +1.5).

Analog-to-Digital Converter

The TMC22070 contains a high-performance 8-bit A/D converter. Its gain and offset are automatically set as a part of the automatic gain adjustment process during initial signal acquisition, and require no user attention.

The reference voltages to the A/D converter are set up by internal D/A converters under automatic control during genlock acquisition. These voltages determine the gain and offset of the A/D converter with respect to the video level presented at its input.

Low-pass Filter

The digitized composite video stream is digitally low-pass filtered to remove chrominance components from the sync separator. Filtering provides robust operation by optimizing the signal-to-noise ratio of the synchronizing/blanking portion of the video, improving the accuracy of the back porch blanking level detector.

Sync Separator

A digital sync separator provides the output sync signals and times internal operations. Two detection modes are provided. The normal mode is for video from cameras, VCR's in normal playback, or off-the-air signals.

Horizontal Phase-Locked Loop

A phase-locked loop generates PXCK, at twice the pixel rate. The reference signal for the horizontal phase-locked loop is generated by the Direct Digital Synthesizer (DDS). The DDS output is constructed with an internal D/A converter and is output from the TMC22070 via the DDS OUT pin. This signal is passed through an off-chip filter and input to the horizontal phase-locked loop.

The phase of the DDS output is proportional to the phase difference between PXCK and the horizontal sync of the incoming signal. A 20 MHz clock is required to drive the DDS. This may be input to the TMC22070 via CMOS levels on the CLK IN pin. Alternately, a 20 MHz crystal may be directly connected between CLK IN and CLK\ OUT with tuning capacitors to activate the internal crystal oscillator circuitry.

Subcarrier Phase-Locked Loop

A fully-digital phase-locked loop is used to extract the phase and frequency of the incoming color burst. These frequency and phase values are output over the CVBS bus during the horizontal sync period.

Back Porch Digital Clamp

A digital back-porch clamp is employed to ensure a constant blanking level. It digitally offsets the data from the A/D converter to set the back porch level to precisely 40_h for PAL and $3C_h$ for NTSC.

Digitized Video Output

The digitized 8-bit video output is provided over an 8-bit wide CVBS data port, synchronous with PXCK. Odd/even field identification, subcarrier frequency, and subcarrier phase data are transmitted over $CVBS_{7-0}$ during the horizontal sync tip period.

Microprocessor Interface

Since microprocessor buses are notoriously "noisy" from a wide-band analog point of view, the microprocessor interface bus is only one bit wide, rather than the more customary eight. The operation of this bus is similar to other bus-controlled devices except that the TMC22070 internal Control Register is accessed one bit at a time.

A sequence of 57 bits is written to or read from the LSB of a standard microprocessor port. Writing to or reading from the secondary address results in the transfer of data to or from the internal shift register.

The RESET\ input, when LOW, sets all internal state machines to their initialized conditions. Returning the RESET\ pin HIGH starts the signal acquisition sequence which lasts until locking with the gain-adjusted and clamped video signal is achieved.

Pin Functions

Video Input

V_{IN1-3}	Video inputs, 1.25 Volts peak-to-peak, sync tip to peak color.

Clocks

CLK IN	20 MHz CMOS clock input to DDS. This pin may also be used along with CLK\ OUT for directly connecting crystals.
CLK\ OUT	Inverted DDS clock output. This pin may also be used along with CLK IN for directly connecting a crystal.
PXCK	2x oversampled line-locked clock output.
EXT PXCK	Input for external PXCK clock source.
PXCK SEL	Select input for internal or external PXCK. When HIGH, the internally generated line-locked PXCK is selected. When LOW, the external PXCK source is enabled.

Digital Video Interface

GHSYNC\	When the TMC22070 is locked to incoming video, the GHSYNC\ pin provides a negative-going pulse after the falling edge of the horizontal sync pulse. There is a fixed number of PXCK clock cycles between adjacent falling edges of GHSYNC\.
GVSYNC\	When the TMC22070 is locked to incoming video, the GVSYNC\ pin provides a negative-going edge after the start of a vertical sync pulse.
$CVBS_{7-0}$	8-bit composite video data is output on this bus at 1/2 the PXCK rate. During the horizontal blanking interval, field ID, subcarrier frequency, and subcarrier phase are available on this bus.

Microprocessor Interface

D_0 Microprocessor data port. All control parameters are loaded into and read back from the Control Register over this 1-bit bus.

A_0 Microprocessor address bus. A LOW on this input loads the I/O Port Shift Register with data from D_0 and CS\. A HIGH transfers the I/O Port Shift Register contents into the Control Register on the last falling edge of CS\.

CS\ When CS\ is HIGH, D_0 is in a high-impedance state and ignored. When CS\ is LOW, the microprocessor can read or write D_0 data into the Control Register.

RESET\ Bringing RESET\ LOW forces the internal state machines to their starting states and disables outputs. Bringing RESET\ HIGH restarts the TMC22070.

R/W\ When R/W\ and A_0 are LOW, the microprocessor can write to the Control Register over D_0. When R/W\ is HIGH and A_0 is LOW, the contents of the Control Register are read over D_0.

INT\ This output is LOW after power-up and before horizontal lock has been established for 256 consecutive horizontal lines. After eight lines have been locked, INT\ goes HIGH and remains HIGH until an unlocked condition exists. If Control Register bit 42 is HIGH, INT\ will be HIGH at the beginning of each even fields and LOW during odd fields. If Control Register bit 42 is LOW, INT\ outputs the locked/unlocked status.

Analog Interface

V_{REF} +1.23 Volt reference. When the internal voltage reference is used, this pin should be decoupled to A_{GND} with a 0.1 µF capacitor. An external +1.2 Volt reference may be connected here, overriding the internal reference source.

COMP Compensation for DDS D/A converter circuitry. This pin should be decoupled to V_{DDA} with a 0.1 µF capacitor.

R_T, R_B Decoupling points for A/D converter voltage references. These pins should be decoupled to A_{GND} with a 0.1 µF capacitor.

Loop Filter Interface

DDS OUT Analog output from the internal Direct Digital Synthesizer D/A converter.

PFD IN Analog input to the Phase/Frequency Detector of the horizontal phase-locked loop

C_{BYP} Decoupling point for the internal comparator reference of the Phase/Frequency Detector. This pin should be decoupled to A_{GND} with a 0.1 µF capacitor.

Power Supply

V_{DDA} Positive power supply to analog section.

V_{DD} Positive power supply to digital section.

A_{GND} Ground for analog section.

D_{GND} Ground for digital section.

Table 1. **Package Interconnections**

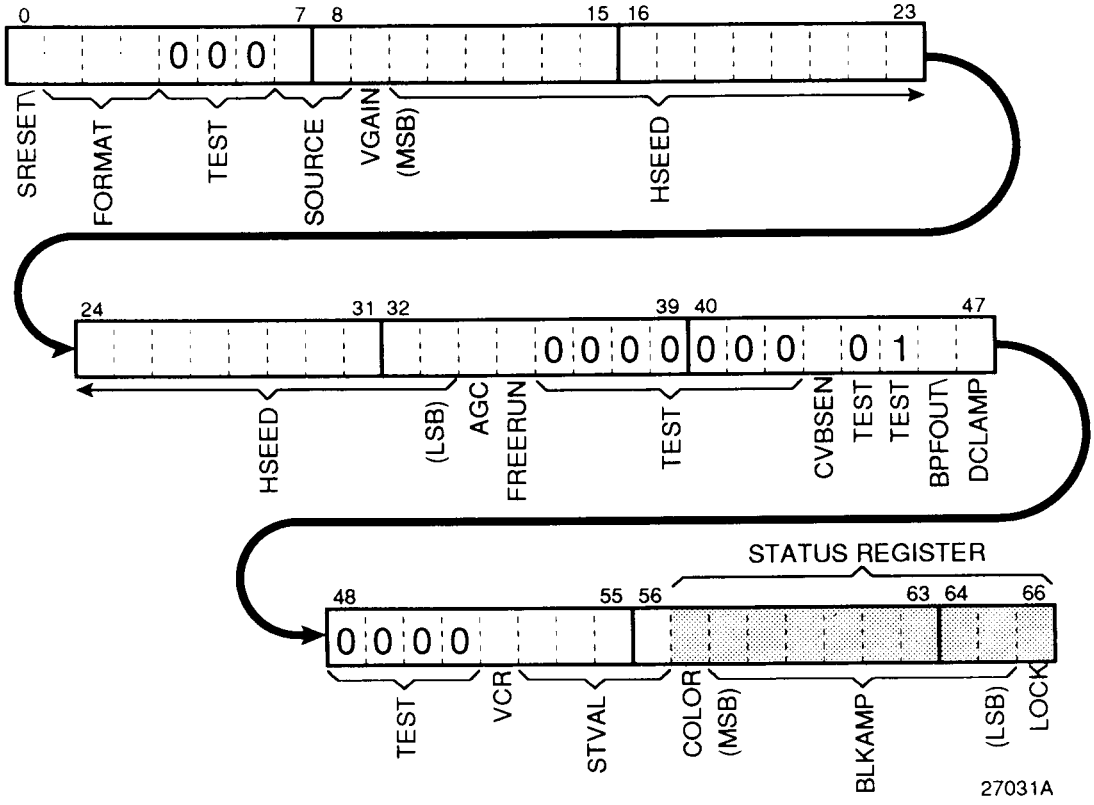
Signal Type	Name	Function	Value	Package Pin
Video Input	V_{IN1-3}	Composite Video Input	1.23Vp-p	34, 31, 29
Clocks	CLK IN	20 MHz DDS clock input	CMOS	51
	CLK\ OUT	Inverted clock output	CMOS	53
	PXCK	Pixel clock output	CMOS	19
	EXT PXCK	External PXCK input	CMOS	54
	PXCK SEL	PXCK source select	CMOS	46
Digital Video	GHSYNC\	Horizontal sync output	CMOS	12
	GVSYNC\	Vertical sync output	CMOS	13
	$CVBS_{7-0}$	Composite output bus	CMOS	11-9, 6-2
µP I/O	D_0	Data I/O port	TTL	66
	A_0	µP port control	TTL	60
	CS\	Chip select	TTL	62
	RESET\	Master reset input	TTL	64
	R/W\	Bus read/write control	TTL	61
	INT\	Interrupt output	TTL	67
Analog	V_{REF}	V_{REF} input/output	+1.23 V	38
	COMP	Compensation capacitor	0.1 µF	48
	R_T,R_B	A/D V_{ref} decoupling	0.1 µF	36, 28
PLL Filter	DDS OUT	Internal DDS output		45
	PFD IN	Horizontal PLL input		43
	C_{BYP}	Comparator bypass	0.1 µF	42
Power	V_{DDA}	Analog power supply	+5 V	23, 25, 26, 30, 33, 40, 47
	V_{DD}	Digital power supply	+5 V	1, 7, 14, 17, 18, 22, 52, 58, 59, 63
Ground	A_{GND}	Analog ground	0.0 V	24, 27, 32, 35, 37, 39, 41, 44, 49,
	D_{GND}	Digital ground	0.0 V	8, 15, 16, 20, 21, 50, 55-57, 65, 68

Control Register Bit Functions

Bit	Mnemonic	Function
0	SRESET	Software reset. When LOW, resets and holds internal state machines and disable output drivers. When HIGH, SRESET starts and runs state machines, PXCK, and enables outputs.
1-3	FORMAT	Input signal format select. When the two FORMAT bits are: 000 NTSC at 12.27 Mpps. 001 NTSC at 13.5 Mpps. 010 PAL_A at 14.75 MPPS. 011 PAL_B at 15.0 Mpps. 1xx PAL at 13.5 Mpps.
4-6	TEST	Factory test control bits. These should be set LOW.
7,8	SOURCE	Video source select. When the two SOURCE bits are: 00 V_{IN1} is selected. 01 $V_{IN2}$is selected. 10 V_{IN3} is selected. 11 V_{IN3} is selected.
9	VGAIN	Video gain. When LOW, gain is set to +1.0. When HIGH, gain is set to +1.5.
10-33	HSEED	24-bit internal DDS seed data. Bit 33 is the MSB.
34	AGC	AGC operation control. The AGC operation is continuous this bit is HIGH. When LOW, AGC is enabled for two fields after acquisition and then held.
35	FRERUN	When HIGH, a free-running PXCK is generated, independent of incoming video. When LOW, PXCK is locked to incoming video.
36-42	TEST	Factory test control bits. These should be set LOW.
43	CVBSEN	CVBS bus enable. When LOW, the $CVBS_{7-0}$, GHSYNC\, and GVSYNC\ outputs are in a high-impedance state. When HIGH, they are enables.
44	TEST	Factory test control bit. This should be set LOW.
45	TEST	Factory test control bit. This should be set HIGH.
46	BPFOUT\	Burst phase / frequency output control. When HIGH, this function is disabled. When LOW, burst phase and frequency information is sent out on the $CVBS_{3-0}$ bus.
47	DCLAMP	Digital clamp enable. The digital clamp is enabled when DCLAMP is HIGH and disabled when LOW.
48-51	TEST	Factory test control bits. These should be set LOW.

Bit	Mnemonic	Function	Bit	Mnemonic	Function
52	VCR	When LOW, time-stable inputs are assumed. When HIGH, input signals with less than ideal time stability (i.e. from VCRs) are assumed.			**Status Bits (read only)**
			57	COLOR	Burst present status bit. This bit is LOW when no burst is present on the input video. It is HIGH when burst is present.
53-56	STVAL	Sync tip value. When DCLAMP is HIGH and STVAL is set to its default value 3_h, the output sync level is 3_h for NTSC and 7_h for PAL. Bit 53 is the MSB.	58-65	BLKAMP	Blanking amplitude status bits. These eight bits report the actual blanking level.
			66	LOCK	Genlocked status bit. When LOW, the TMC22070 is not locked to an input signal. When HIGH, lock has been achieved.

Figure 3. Control Register Map



Control and Status Registers

The TMC22070 is controlled by a single 57-bit long Control Register. Access to the Control Register is via the I/O Port Shift Register arranged as shown in Figure 4. The Control Register can be read and written permitting software modification and examination of its contents. The 10-bit Status Register is read-only and accessed through the same I/O Port Shift Register. Reading the Status Register yields information about blanking level, subcarrier presence, and whether or not PXCK is locked or unlocked with respect to the line rate.

The host processor writes data into the TMC22070 using only one bit of the microprocessor's data and address bus. Once the shift register has input and positioned the 57 bits of desired data (bit 56 first, bit 0 last), a HIGH on A_0 and a LOW on R/W\ when CS\ falls transfers the I/O Port Shift Register contents to the Control Register. The I/O Port Shift Register, Control Register and Status Register are governed by CS\ , R/W\ , and A_0. R/W\ and A_0 are latched by the TMC22070 on the falling edge of CS\ and data input D_0 is latched on the rising edge of CS\. Data read from D_0 is enabled by the falling edge of CS\ and disabled by the rising edge of CS\.

The full sequence of 57 bits of Control Register data must be written each time a change in that data is desired. All or a few of the Control and Status Register bits may be read, but the sequence always begins with bit 66 of the Status Register.

Figure 4. Control and Shift Register Structure

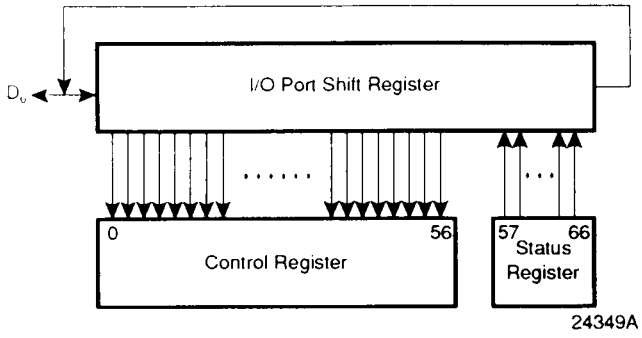


Table 2. Microprocessor Port Control

A_0	R/W\	Action
0	0	Write data from D_0 into I/O Port Shift Register
0	1	Read D_0 data from last stage of I/O Port Shift Register
1	0	Transfer I/O Port Shift Register contents to Control Register
1	1	Enables continuous update of status bits in I/O Port Shift Register

Figure 5. Data Write Sequence

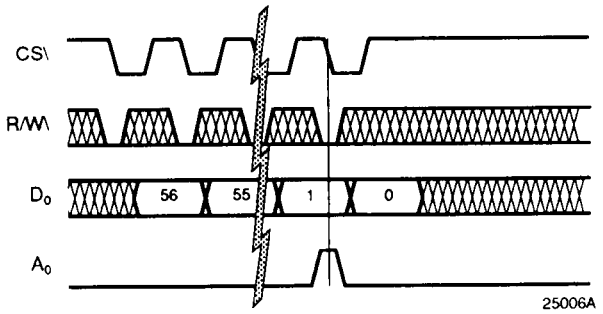
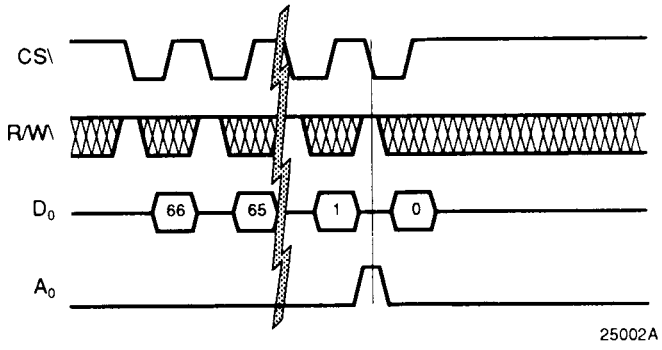


Figure 6. Data Read Sequence



Horizontal Timing

Horizontal line rate is selectable, and is determined by the FORMAT control bits (12.27 Mpps for NTSC, 13.5 Mpps for NTSC and PAL, and either 14.75 or 15.0 Mpps for PAL). Figure 7 illustrates the horizontal blanking interval. Figure 8 completes the definition of timing parameters with vertical blanking interval detail.

Figure 7. Horizontal Sync Timing

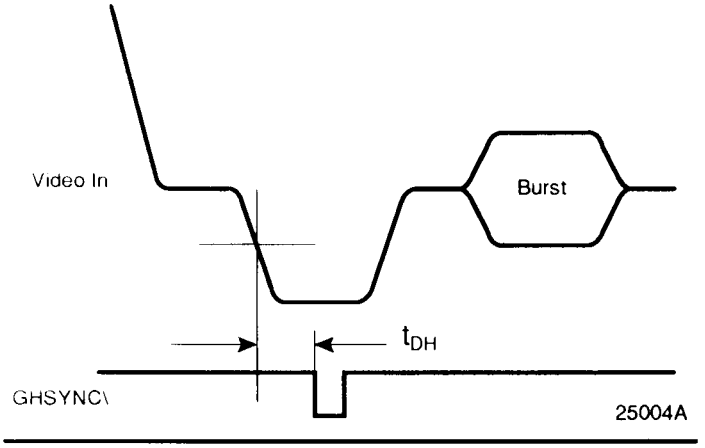


Figure 8. Vertical Sync Timing

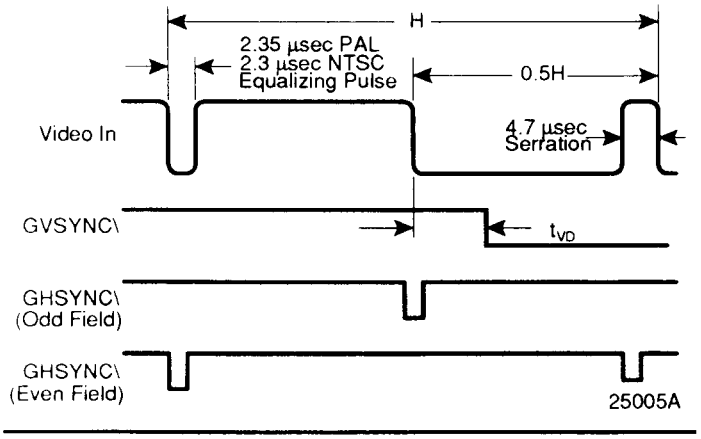


Table 3. Standard Timing Parameters

Standard	Field Rate (Hz)	Line Rate (kHz)	Pixel Rate (Mpps)	PXCK Frequency (MHz)	Pixels Per Line	HSEED (hex)
NTSC	59.94	15.734264	12.2727+	24.54+	780	22E8BA
NTSC-601	59.94	15.734264	13.50	27.0	858	266666
PAL_A	50.00	15.625	14.75	29.5	944	29F49F
PAL_B	50.00	15.625	15.00	30.0	960	2AAAAA
PAL-601	50.00	15.625	13.50	27.0	864	266666

Programming the TMC22070

Upon power-up, the TMC22070 Control Register is set to default values as shown in the top entry of Table 4. These default values do not necessarily render the TMC22070 operational in any specific application. Before the TMC22070 is expected to acquire input video, its Control Register must be loaded with data that is specific to its use.

The Control Register HSEED values shown in Table 3 are calculated from:

$$HSEED = f_{PXCK} \times 0.093206755$$

where f_{PXCK} is twice the expected pixel rate. HSEED, when applied to the DDS will generate the exact horizontal line rate required.

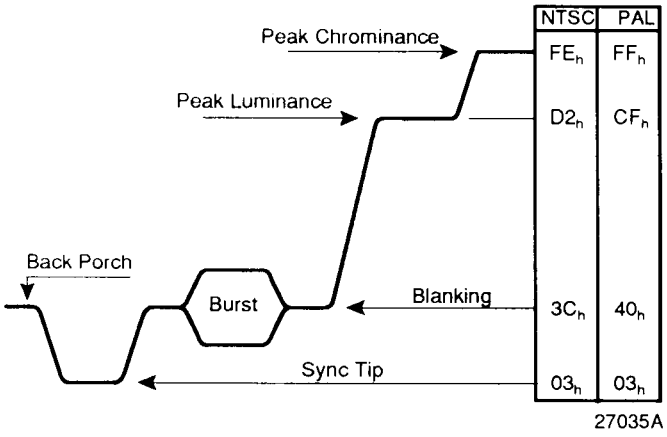
Table 4. Control Register Example Data

Standard	Control Register Data (Bit 56 ..... Bit 0)														
	56	52	48	44	40	36	32	28	24	20	16	12	8	4	0
DEFAULT	0011	1000	0100	0000	0000	0000	0100	0101	1101	0001	0111	0100	0000	0000	1
NTSC	xxxx	x000	0101	0000	0000	0000	0100	0101	1101	0001	0111	0100	xx00	0xxx	1
NTSC-601	xxxx	x000	0101	0000	0000	0000	0100	1100	1100	1100	1100	1100	xx00	0xxx	1
PAL_A	xxxx	x000	0101	0000	0000	0000	0101	0011	1110	1001	0011	1110	xx00	0xxx	1
PAL_B	xxxx	x000	0101	0000	0000	0000	0101	0101	0101	0101	0101	0100	xx00	0xxx	1
PAL-601	xxxx	x000	0101	0000	0000	0000	0100	1100	1100	1100	1100	1100	xx00	0xxx	1

CVBS Bus Data Formats

The CVBS bus outputs a Genlock Reference Signal (GRS) along with the 8-bit digital composite video data. The range of output data versus video input voltage is illustrated in Figure 9 where sync tip and blanking levels are controlled by the digital back-porch clamp of the TMC22070. During horizontal sync, the TMC22070 outputs field identification, subcarrier frequency, and subcarrier phase information on the CVBS bus.

Figure 9. Output Data vs. Input Video Level



Field identification is output on $CVBS_{2-0}$. The LSB, $CVBS_0$, will be LOW during odd fields and HIGH for even fields. When NTSC operation is selected, $CVBS_{1-0}$ count 00,01,10,11 for fields 1 through 4 respectively. When PAL operation is selected, $CVBS_{2-0}$ count 000,001,010, etc. to 111 for fields 1 through 8, respectively.

Subcarrier frequency is sent out in a 24-bit binary representation in six 4-bit nibbles on $CVBS_{3-0}$. Subcarrier frequency data, f_{23-0}, is identical to the pre-programmed BSEED value used in the TMC22070 to lock the subcarrier phase-locked loop to the incoming subcarrier frequency. BSEED is calculated from:

$$BSEED = 2^{24} \times (f_{SUBCAR}) / (f_{PXCK} / 2)$$

where f_{SUBCAR} is the NTSC or PAL subcarrier frequency, $f_{PXCK}/2$ is the expected pixel rate, and f_{23} is the MSB.

Subcarrier phase, Φ_{23-0}, is also sent out in a 24-bit binary representation in six 4-bit nibbles on $CVBS_{3-0}$. Bit Φ_{23} is the MSB. Subcarrier phase is related to the BSEED value by:

$$\Phi = (BSEED / 2^{24}) \times 360 \text{ (degrees)}$$

Figure 10. Genlock Reference Signal (GRS) Format.

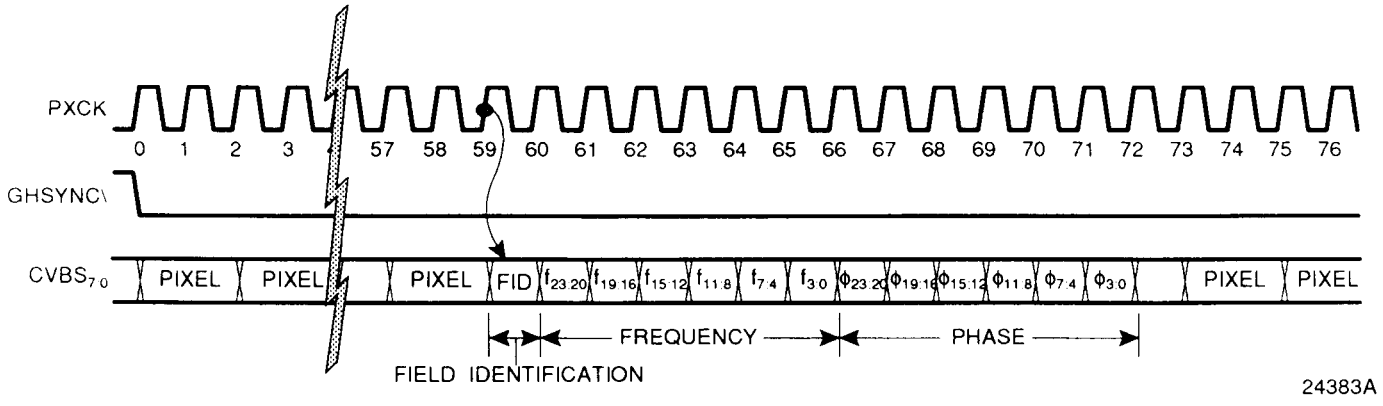


Figure 10. CVBS Bus Video Data Format

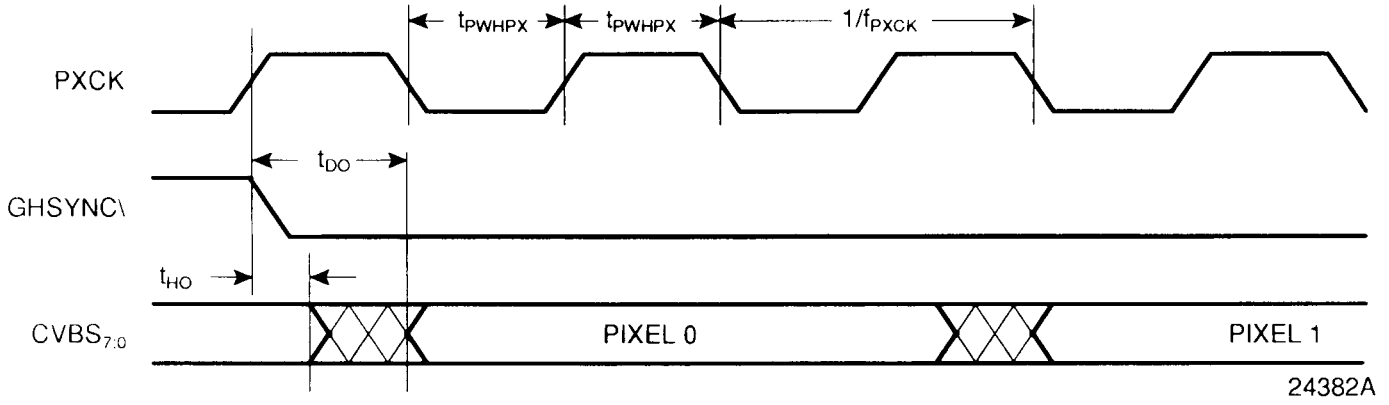


Figure 11. Microprocessor Port - Write Timing

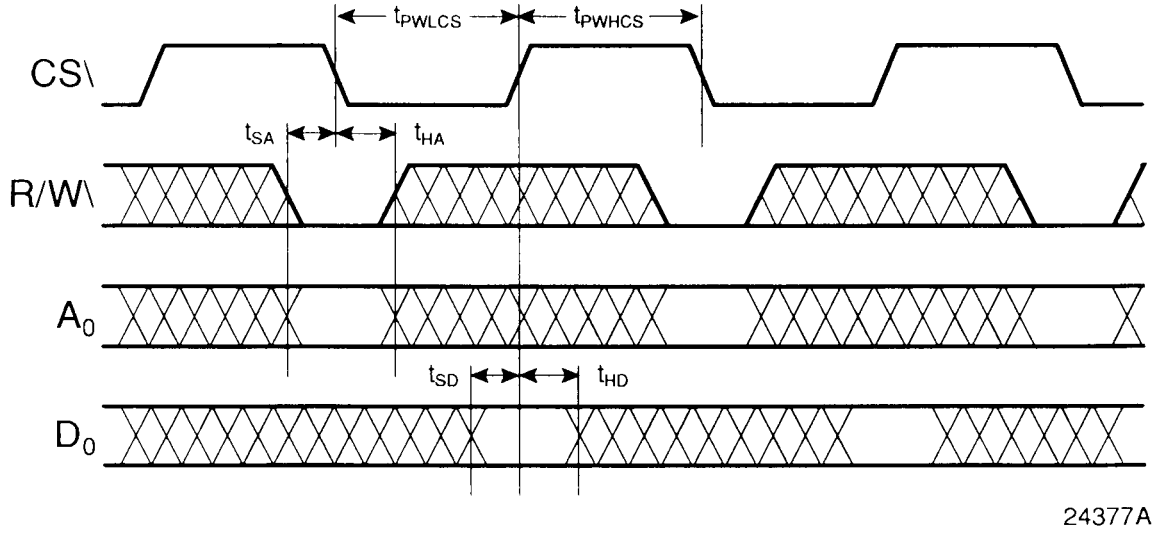


Figure 12. Microprocessor Port - Read Timing

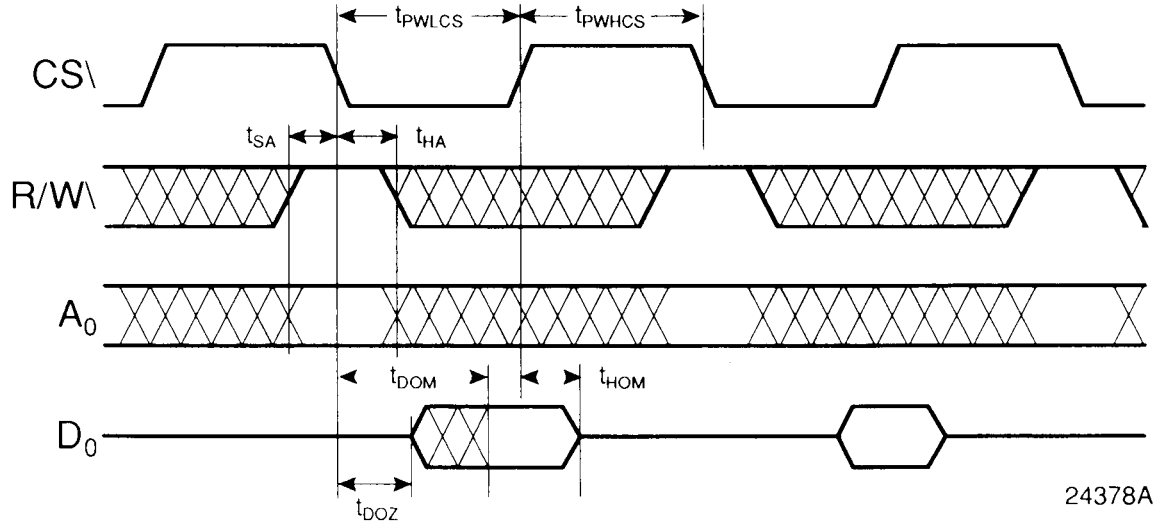


Figure 13. Equivalent PFD IN Circuit

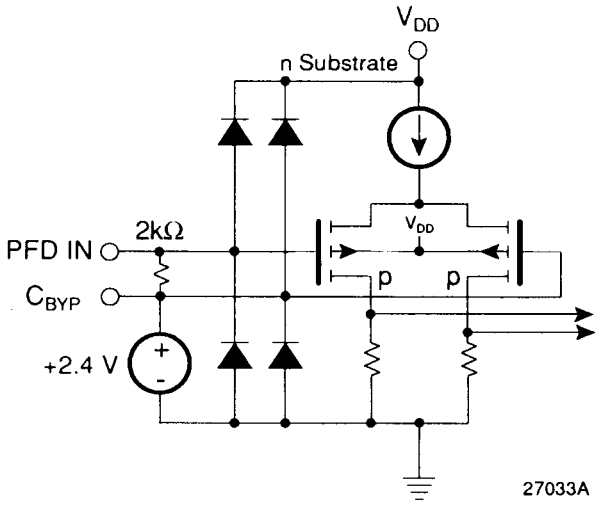


Figure 14. Equivalent Digital Input Circuit

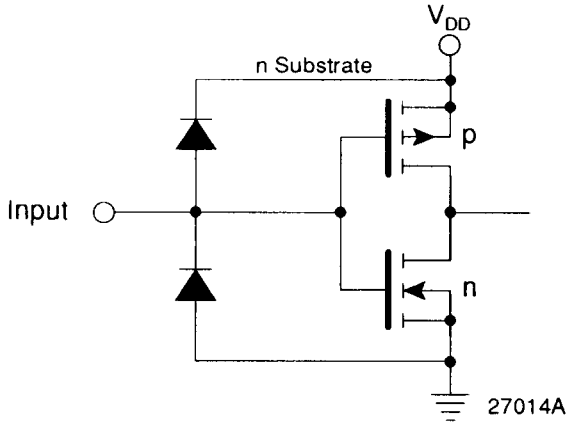


Figure 15. Equivalent DDS OUT Circuit

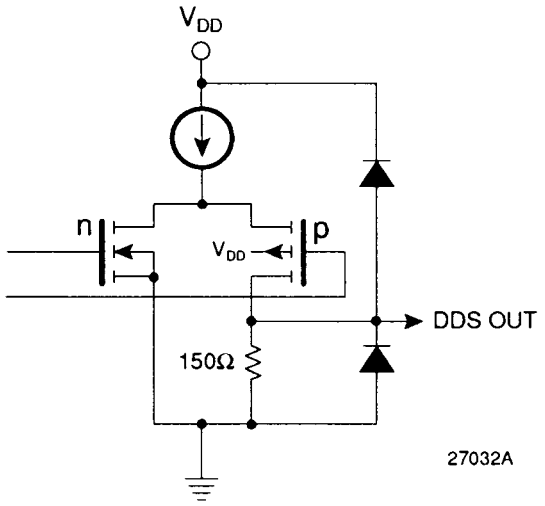


Figure 16. Equivalent Digital Output Circuit

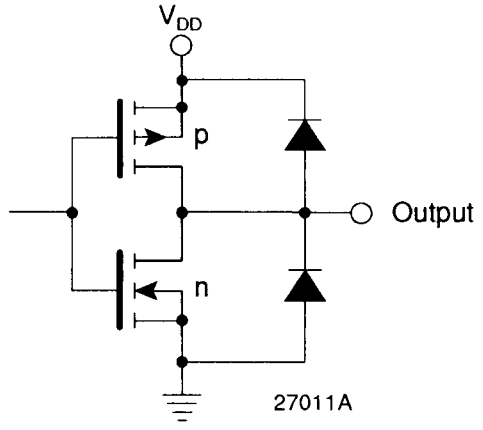
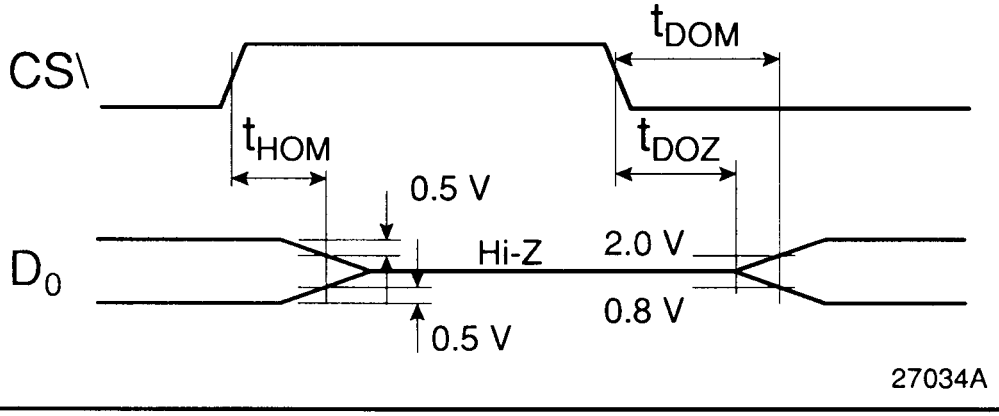


Figure 17. Transition Levels for Three-State Measurements



Absolute maximum ratings (beyond which the device may be damaged)[1]

Power Supply Voltage	-0.5 to +7.0V
Input Voltage	-0.5 to V_{DD}+0.5V
Digital Outputs	
Applied Voltage[2]	-0.5 to V_{DD}+0.5V
Forced Current[3,4]	-6.0 to 6.0 mA
Short Circuit Duration (Single output in HIGH state to GND)	1 second
Temperature	
Operating, case	-60 to +130°C
Operating, Junction	+150°C
Lead, soldering (10 seconds)	+300°C
Vapor phase soldering (1 minute)	+220°C
Storage	-65 to +150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current, flowing into the device.

Operating conditions

Parameter		Temperature Range: Standard Min	Nom	Max	Units
V_{DD}	Power Supply Voltage	4.75	5.0	5.25	V
V_{IH}	Input Voltage, Logic HIGH				
	TTL Inputs	2.0		V_{DD}	V
	CMOS Inputs	2/3 V_{DD}		V_{DD}	V
V_{IL}	Input Voltage, Logic LOW				
	TTL Inputs	D_{GND}		0.8	V
	CMOS Inputs	D_{GND}		1/3 V_{DD}	V
I_{OH}	Output Current, Logic HIGH			-2.0	mA
I_{OL}	Output Current, Logic LOW			4.0	mA
V_{IN}	Video Input Signal Level Sync Tip to Peak White		1.0		V
V_{REF}	External Reference Voltage		1.235		V
T_A	Ambient Temperature, Still Air	0		70	°C
Microprocessor Interface					
t_{PWLCS}	CS\ Pulse Width, LOW	35			ns
t_{PWHCS}	CS\ Pulse Width, HIGH	35			ns
t_{SA}	Address Setup Time	4			ns
t_{HA}	Address Hold Time	25			ns
t_{SD}	Data Setup Time	80			ns
t_{HD}	Data Hold Time	2			ns

Note: 1. Timing reference points are at the 50% level.

Electrical Characteristics

Parameter		Conditions	Temperature Range: Standard Min	Standard Typ	Standard Max	Units
I_{DD}	Power Supply Current[1]	Total Current V_{DD}=Max,f_{PXCK}=30MHz		TBD	TBD	mA
I_{REF}	Reference Input Current	V_{REF} = +1.235V			100	µA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max, V_{IN} = 4.0V			±10	µA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0.4V			±10	µA
V_{OH}	Output Voltage, Logic HIGH	I_{OH} = -2.0 mA	2.4			V
V_{OL}	Output Voltage, Logic LOW	I_{OL} = 4.0 mA			0.4	V
I_{OZH}	Hi-Z Output Leakage current, HIGH	V_{DD}=Max, V_{IN}=V_{DD}			±10	µA
I_{OZL}	Hi-Z Output Leakage current, LOW	V_{DD}=Max, V_{IN}=GND			±10	µA
C_I	Digital Input Capacitance	T_A = 25°C, f = 1MHz		4	15	pF
C_O	Digital Output Capacitance	T_A = 25°C, f = 1MHz		10		pF
C_V	Input Capacitance, V_{IN1-3}	T_A = 25°C, f = 3.58 MHz			15	pF
R_V	Input Resistance, V_{IN1-3}		50			kΩ

Note 1. Typical I_{DD} with V_{DD}=+5.0 Volts and T_A=25°C, Maximum I_{DD} with V_{DD}=+5.25 Volts and T_A=0°C,

Switching Characteristics

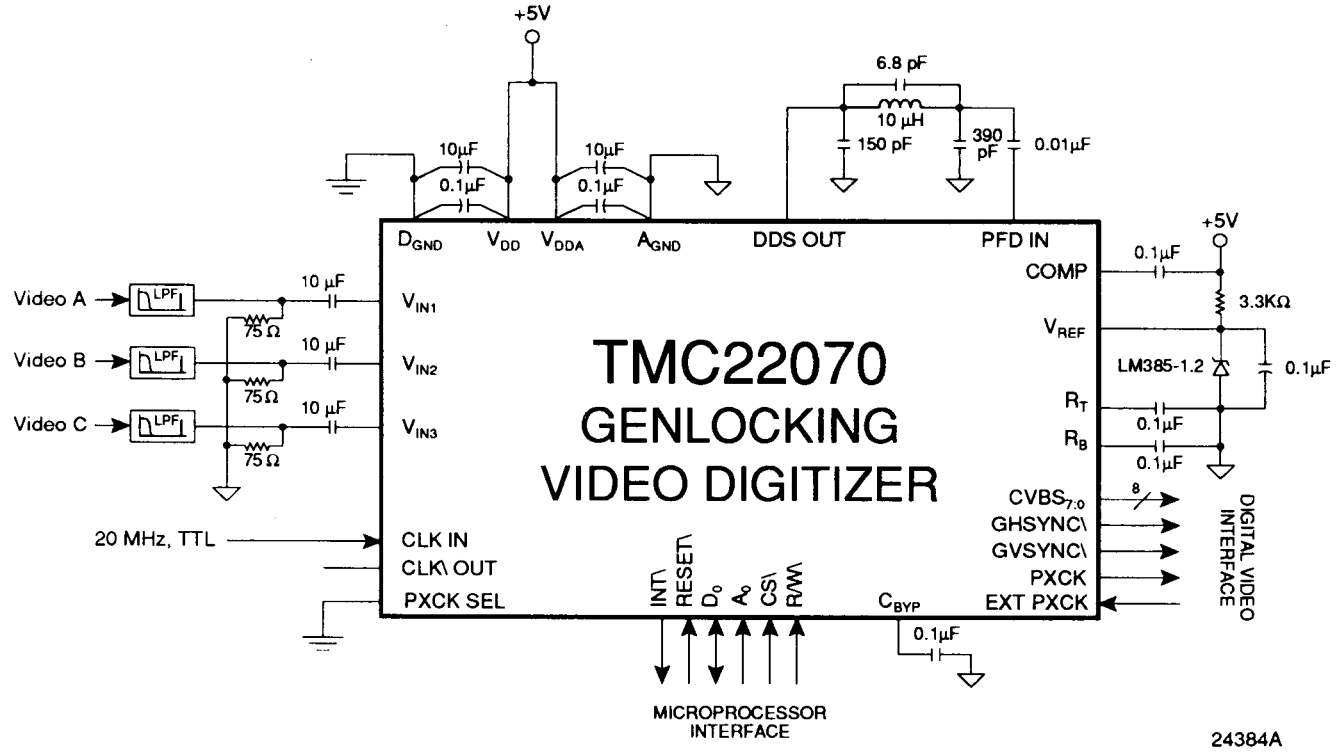
Parameter		Conditions	Temperature Range: Standard Min	Standard Typ	Standard Max	Units
t_{DO}	Output Delay Time	C_{LOAD} = 35 pF	2		15	ns
t_{HO}	Output Hold Time		3		8	ns
f_{PCK}	Pixel Rate		12		15.3	MHz
f_{PXCK}	Master Clock Rate		24		30.6	MHz
t_{PWLPX}	PXCK Pulse Width, LOW		12			ns
t_{PWHPX}	PXCK Pulse Width, HIGH		12			ns
t_{DH}	Horizontal Sync to GHSYNC\			4.5		pixels
t_{VD}	Vertical Sync to GVSYNC\			4.5		pixels
t_{DOM}	D_0 enable time					ns
t_{HOM}	D_0 disable time					ns
t_{DOZ}	CS\ LOW to D_0 output driven					ns

System Performance Characteristics

Parameter		Conditions	Temperature Range: Standard Min	Standard Typ	Standard Max	Units
E_{SCH}	Sync time-base variation[1]				±30	ns
E_{SCP}	Subcarrier Phase Error[1]				±5	degrees
t_{AL}	Line-lock Acquisition Time				2	frames
V_{XT}	Channel-to-Channel Crosstalk @3.58 MHz				-35	dB

Notes 1. NTSC/PAL compliant black burst at nominal input level ±10%, frequencies nominal ± 10 ppm.

Figure 18. Typical Interface Circuit



Application Notes

The TMC22070 is a complex mixed-signal VLSI circuit. It produces CMOS digital signals at clock rates of up to 30 MHz while processing analog video inputs with a resolution of less than a few millivolts. To maximize performance it is important to provide an electrically quiet operating environment. The circuit shown in Figure 18 provides an optional external 1.2V reference to the V_{REF} input of the TMC22070. The internal V_{REF} source is adequate for most applications.

Filtering

Inexpensive low-pass anti-aliasing filters are shown in Figures 19 and 20. These filters would normally be inserted in the video signal path just before the 75Ω terminating resistor and AC-coupling capacitor for each of the three video inputs, V_{IN1-3}. The filter of Figure 19 exhibits a 5th-order Chebyshev response with -3dB bandwidth of 6.7MHz and a group delay of 140 nanoseconds at 5MHz. The filter of Figure 20 has been equalized for group delay in the video signal band. Its -3dB passband is 5.5MHz while the group delay is constant at 220 nanoseconds through the DC to 5MHz frequency band.

Figure 19. Simple Anti-aliasing Filter

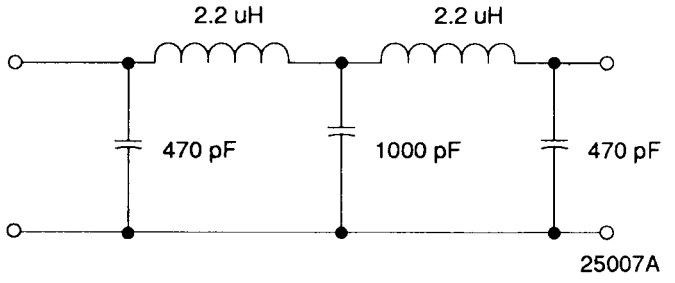
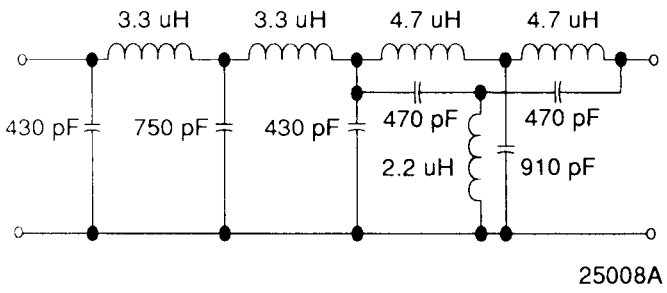


Figure 20. Group Delay Equalized Filter



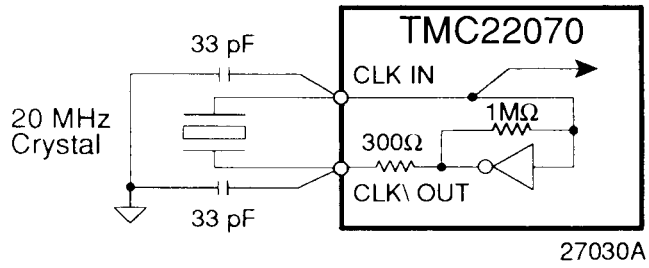
Using a 20 MHz Crystal

In systems where a 20 MHz clock is not available, a crystal may be used to generate the clock to the TMC22070. The crystal must be a 20 MHz "fundamental" type, not overtone." Specific crystal characteristics are listed in Table 5 and the connections are shown in Figure 21.

Table 5. Crystal Parameters

Parameter	Value
Fundamental frequency	20 MHz
Tolerance	±30 ppm @ 25°C
Stability	±50 ppm, 0°C to 70°C
Load Capacitance	20 pF
Shunt Capacitance	7 pF Max.
ESR	50Ω, Max.

Figure 21. Direct Crystal Connections



Grounding

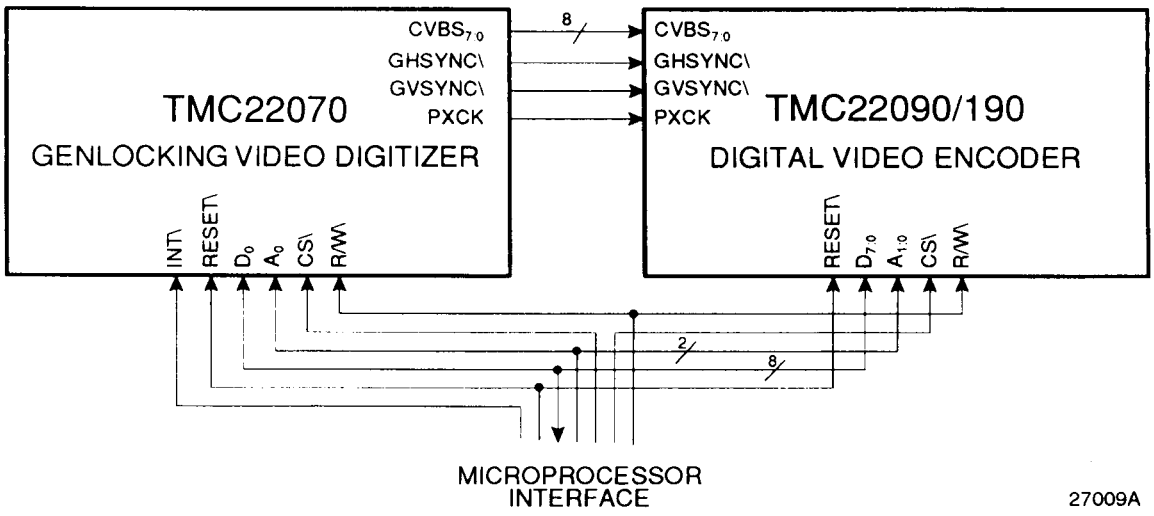
The TMC22070 has separate analog and digital circuits. To minimize digital crosstalk into the analog signals, the power supplies and ground connections are provided over separate pins (V_{DD} and V_{DDA} are digital and analog power supply pins; D_{GND} and A_{GND} are digital and analog ground pins). In general, the best results are obtained by tying all grounds to a solid, low-impedance ground plane. Power supply pins should be individually decoupled at the pin. Power supply noise isolation may be provided between analog and digital supplies via a ferrite bead inductor. Ultimately all +5 Volt power to the TMC22070 should come from the same power source.

Another approach calls for separating analog and digital ground. While some systems may benefit from this strategy, analog and digital grounds must be kept within 0.1V of each other at all times.

Interface to the TMC22090 Encoder

The TMC22090 Digital Video Encoder has been designed to directly interface to the TMC22070 Digital Video Genlock. The TMC22070 is the source for TMC22090/TMC22190 input signals $CVBS_{7-0}$, GHSYNC\, GVSYNC\, and PXCK as shown in Figure 22. These signals directly connect to the TMC22090. The microprocessor interface for TMC22090 and TMC22070 are identical. All W/R\, RESET\, data and address bus signals from the host microprocessor are shared by the TMC22090 and TMC22070. Only CS\ and INT\ signals are separate from the microprocessor bus.

Figure 22. TMC22090/TMC22070 Interface Circuit



Printed Circuit Board Layout

Designing with high-performance mixed-signal circuits demands printed circuits with ground planes. Wire-wrap is not an option. Overall system performance is strongly influenced by the board layout. Capacitive coupling from digital to analog circuits may result in poor picture quality. Consider the following suggestions when doing the layout:

1. Keep the critical analog traces (COMP, V_{REF}, R_T, R_B, DDS OUT, PFD IN, C_{BYP}, and V_{IN1-3}) as short as possible and as far as possible from all digital signals. The TMC22070 should be located near the board edge, close to the analog output connectors.

2. The power plane for the TMC22070 should be separate from that which supplies the rest of the digital circuitry. A single power plane should be used for all of the V_{DD} pins. If the power supply for the TMC22070 is the same as that of the system's digital circuitry, power to the TMC22070 should be decoupled with ferrite beads and 0.1µF capacitors to reduce noise.

3. the ground plane should be solid, not cross-hatched. Connections to the ground plane should have very short leads.

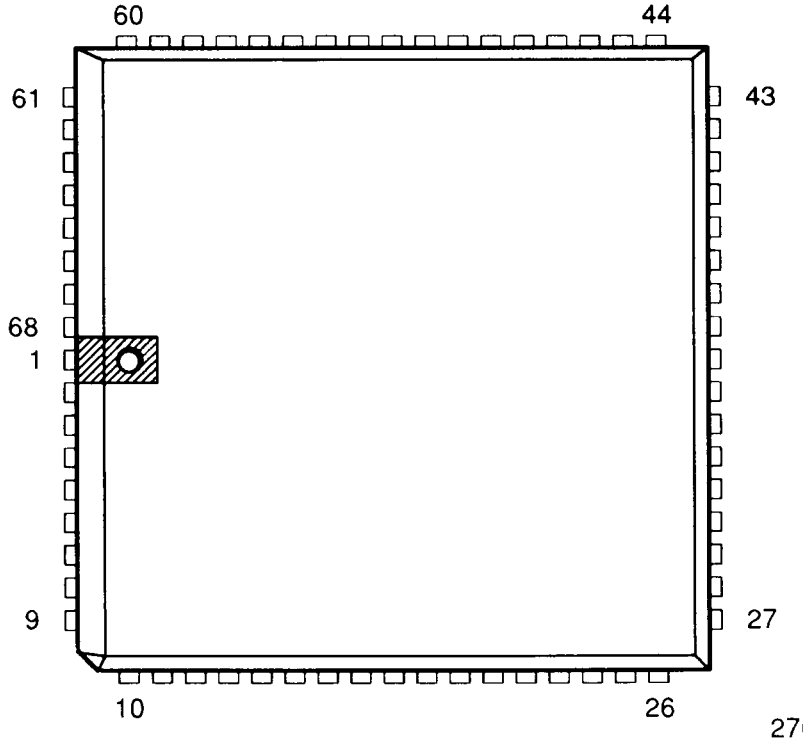
4. Decoupling capacitors should be applied liberally to V_{DD} pins. Remember that not all power supply pins are created equal. They typically supply adjacent circuitry on the device, which generate varying amounts of noise. For best results, use 0.1µF capacitors in parallel with 0.01µF capacitors. Lead lengths should be minimized. Ceramic chip capacitors are the best choice.

5. If the digital power supply has a dedicated power plane layer, it should not overlap the TMC22070, the voltage reference or the analog outputs. Capacitive coupling of digital power supply noise from this layer to the TMC22070 and its related analog circuitry can have an adverse effect on performance.

6. CLK should be handled carefully. Jitter and noise on this clock or its ground reference may degrade performance. Terminate the clock line carefully to eliminate overshoot and ringing.

Pin Assignments

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{DD}	18	V_{DD}	35	A_{GND}	52	V_{DD}
2	$CVBS_0$	19	PXCK	36	R_T	53	CLK\ OUT
3	$CVBS_1$	20	D_{GND}	37	A_{GND}	54	EXT PXCK
4	$CVBS_2$	21	D_{GND}	38	V_{REF}	55	D_{GND}
5	$CVBS_3$	22	V_{DD}	39	A_{GND}	56	D_{GND}
6	$CVBS_4$	23	V_{DDA}	40	V_{DDA}	57	D_{GND}
7	V_{DD}	24	A_{GND}	41	A_{GND}	58	V_{DD}
8	D_{GND}	25	V_{DDA}	42	C_{BYP}	59	V_{DD}
9	$CVBS_5$	26	V_{DDA}	43	PFD IN	60	A_0
10	$CVBS_6$	27	A_{GND}	44	A_{GND}	61	R/W\
11	$CVBS_7$	28	R_B	45	DDS OUT	62	CS\
12	GHSYNC\	29	V_{IN3}	46	PXCK SEL	63	V_{DD}
13	GVSYNC\	30	V_{DDA}	47	V_{DDA}	64	RESET\
14	V_{DD}	31	V_{IN2}	48	COMP	65	D_{GND}
15	D_{GND}	32	A_{GND}	49	A_{GND}	66	D_0
16	D_{GND}	33	V_{DDA}	50	D_{GND}	67	INT\
17	V_{DD}	34	V_{IN1}	51	CLK IN	68	D_{GND}



R1 Package

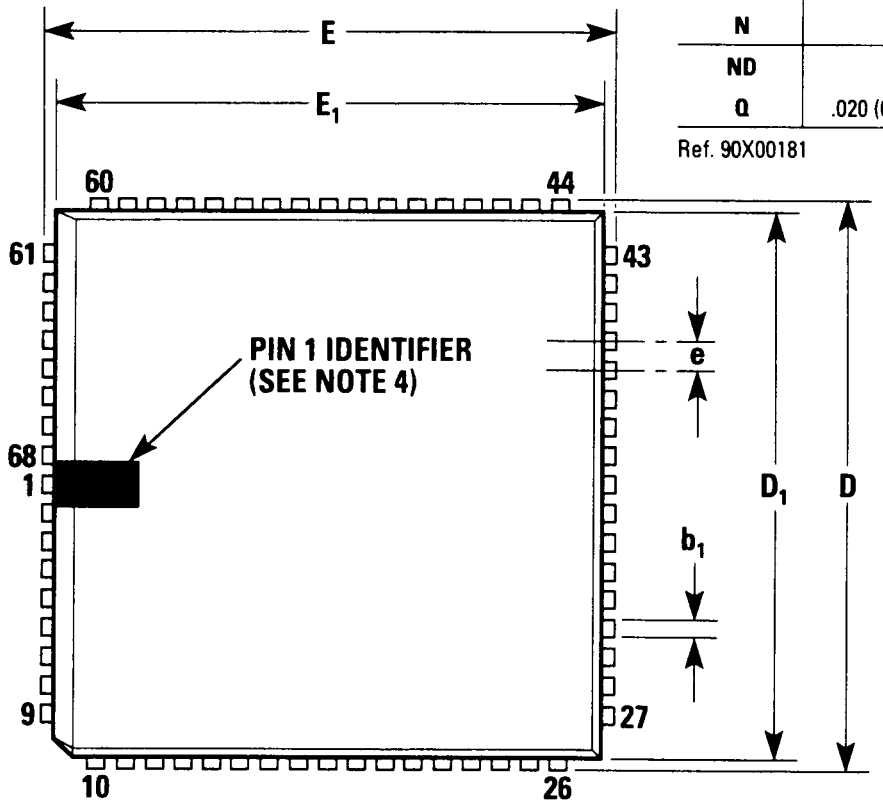
68 Lead Plastic J-Leaded Chip Carrier

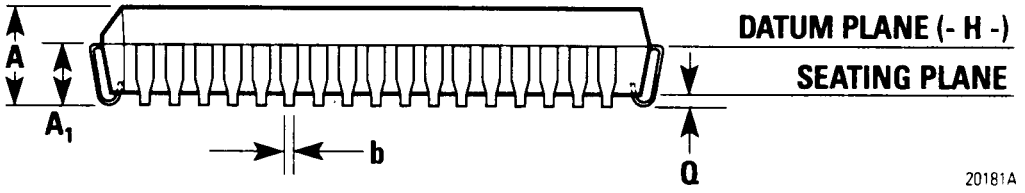
Notes:
1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Datum plane **(–H–)** located at top of mold parting line and coincident with top of lead, where lead exits plastic body.
3. Dimension D_1 and E_1 do not include mold protrusion. Allowable protrusion is .010 inch (0.25mm).
4. Details of pin 1 identifier are optional but must be located within the zone indicated.
5. Dimension N: number of terminals.
6. Dimension ND: number of terminals per package edge.
7. Controlling dimension: inch.

Dimensions

Inches (Millimeters)			
Sym	**Min**	**Max**	**Notes**
A	.165 (4.20)	.200 (5.08)	
A_1	.090 (2.29)	.130 (3.30)	
b	.013 (0.33)	.021 (0.53)	
b_1	.026 (0.66)	.032 (0.81)	
D	.985 (25.02)	.995 (25.27)	
D_1	.950 (24.13)	.958 (24.33)	Note 3
E	.985 (25.02)	.995 (25.27)	
E_1	.950 (24.13)	.958 (24.33)	Note 3
e			.050 (1.27) Basic
N			68, Note 5
ND			17, Note 6
Q	.020 (0.51)		

Ref. 90X00181





20181A

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC22070R1C	T_A = 0°C to 70°C	Commercial	68-Lead PLCC	22070R1C

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