FEATURES

- **High Gain ..... 200V/mV Typ**
- **Single or Dual Supply Operation**
- **Input Voltage Range Includes Ground**
- **Low Power Consumption (1.5mW/Comparator)**
- **Low Input Bias Current ..... 100nA Max**
- **Low Input Offset Current ..... 10nA Max**
- **Low Offset Voltage ..... 1mV Max**
- **Low Output Saturation Voltage ..... 250mV @ 4mA**
- **Logic Output Compatible with TTL, DTL, ECL, MOS and CMOS**
- **Directly Replaces LM139/239/339 Comparators**
- **Available in Die Form**

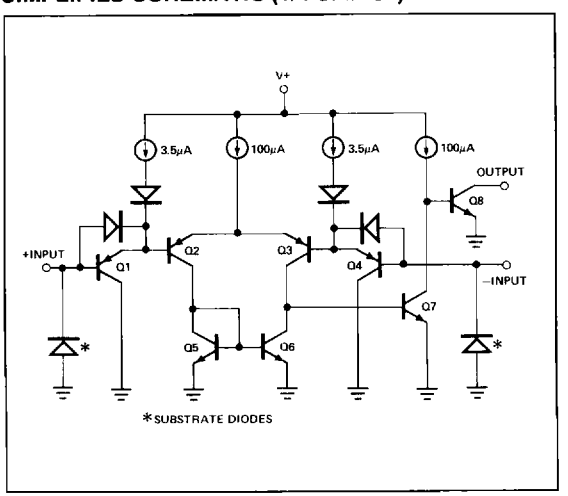
ORDERING INFORMATION †

T_A = +25°C	PACKAGE			OPERATING
V_{OS} (mV)	CERDIP 14-PIN	PLASTIC 14-PIN	SO 14-PIN	TEMPERATURE RANGE
1	CMP04BY*	–	–	MIL
1	CMP04FY	CMP04FP	CMP04FS	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages. For ordering information, see PMI's Data Book, Section 2.

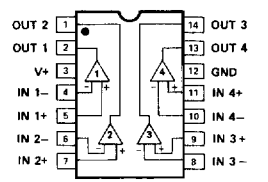
SIMPLIFIED SCHEMATIC (1/4 CMP-04)



GENERAL DESCRIPTION

Four precision independent comparators comprise the CMP-04. Performance highlights include a very low offset voltage, low output saturation voltage and high gain in a single supply design. The input voltage range includes ground for single supply operation and V– for split supplies. A low power supply current of 2mA, which is independent of supply voltage, makes this the preferred comparator for precision applications requiring minimal power consumption. Maximum logic interface flexibility is offered by the open-collector TTL output.

PIN CONNECTIONS

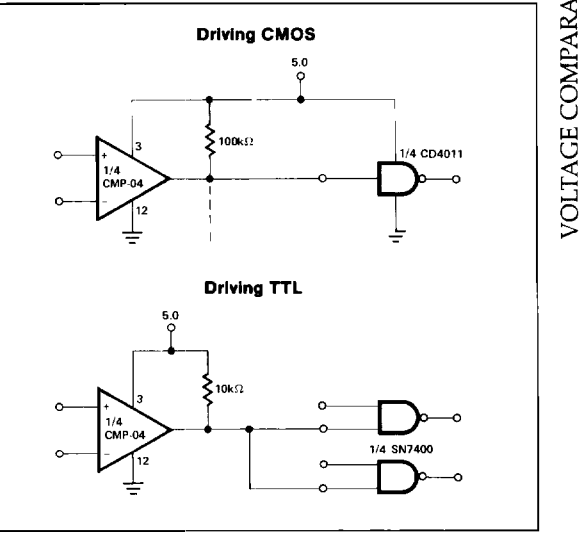


14-PIN HERMETIC DIP (Y-Suffix)

14-PIN EPOXY DIP (P-Suffix)

14-PIN SO (S-Suffix)

TYPICAL INTERFACE



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... 36V or ±18V
Differential Input Voltage ..... $36V_{DC}$
Input Voltage ..... –0.3V to +36V
Operating Temperature Range
CMP-04FY ..... –25°C to +85°C
CMP-04BY ..... –55°C to +125°C
CMP-04FP, FS ..... –40°C to +85°C
Junction Temperature (T_J) ..... –65°C to +150°C
Storage Temperature Range ..... –65°C to +150°C
P-Suffix) ..... –65°C to +125°C
Input Current (V_{IN} < –3.0V) 50mA
Output Short-Circuit to GND ..... Continuous
Lead Temperature (Soldering, 60 sec) ..... 300°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
14-Pin Hermetic DIP (Z)	110	26	°C/W
14-Pin Plastic DIP (P)	83	39	°C/W
14-Pin SO (S)	120	36	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at V+ = +5V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-04B/F MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	R_S = 0Ω, R_L = 5.1kΩ V_O = 1.4V, (Note 1)	—	0.4	1	mV
Input Offset Current	I_{OS}	$I_{IN}(+) - I_{IN}(-)$ R_L = 5.1kΩ V_O = 1.4V	—	2	10	nA
Input Bias Current	I_B	$I_{IN}(+)$ or $I_{IN}(-)$	—	25	100	nA
Voltage Gain	A_V	$R_L \geq$ 15kΩ, V+ = 15V, (Note 5)	80	200	—	V/mV
Large-Signal Response Time	t_r	V_{IN} = TTL Logic Swing V_{REF} = 1.4V, (Note 4) V_{RL} = 5V, R_L = 5.1kΩ	—	300	—	ns
Small-Signal Response Time	t_r	V_{IN} = 100mV Step, (Note 4) 5mV Overdrive V_{RL} = 5V, R_L = 5.1kΩ	—	1.3	—	µs
Input Voltage Range	CMVR	(Note 2)	0	—	V+ –1.5	V
Common-Mode Rejection Ratio	CMRR	(Notes 3, 5)	80	100	—	dB
Power Supply Rejection Ratio	PSRR	V+ = +5V to 18V, (Note 5)	80	100	—	dB
Saturation Voltage	V_{OL}	$V_{IN}(-) \geq$ 1V, $V_{IN}(+)$ = 0, $I_{SINK} \leq$ 4mA	—	250	400	mV
Output Sink Current	I_{SINK}	$V_{IN}(-) \geq$ 1V, $V_{IN}(+)$ = 0, $V_O \leq$ 1.5V	6	16	—	mA
Output Leakage Current	I_{LEAK}	$V_{IN}(+) \geq$ 1V, $V_{IN}(-)$ = 0, V_O = 30V	—	0.1	100	nA
Supply Current	I+	R_L = ∞, All Comps V+ = 30V	—	0.8	2.0	mA

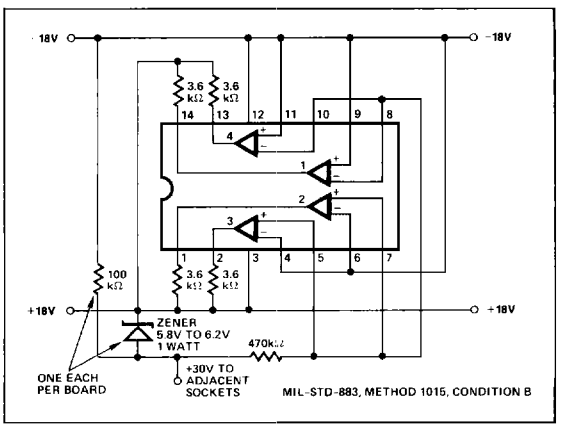
NOTES:
1. At output switch point, V_O = 1.4V, R_S = 0Ω with V+ from 5V; and over the full input common-mode range (0V to V+ – 1.5V).
2. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ – 1.5V, but either or both inputs can go to +30V without damage.
3. $R_L \geq$ 15kΩ, V+ = 15V, V_{CM} = 1.5V to 13.5V.
4. Sample tested.
5. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at V+ = +5V, $-55°C \le T_A \le +125°C$ for CMP-04BY, $-40°C \le T_A \le +85°C$ for CMP-04FY/FP/FS, unless otherwise noted.

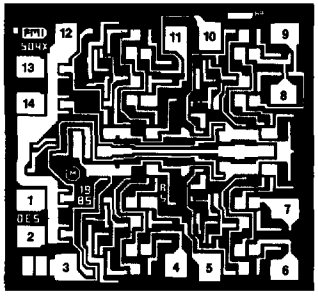
PARAMETER	SYMBOL	CONDITIONS	CMP-04B/F (Note 3) MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S = 0\Omega$, $R_L = 5.1k\Omega$ $V_O = 1.4V$, (Note 1)	—	1	2	mV
Input Offset Current	I_{OS}	$I_{IN}(+) - I_{IN}(-)$ $R_L = 5.1k\Omega$ $V_O = 1.4V$	—	4	20	nA
Input Bias Current	I_B	$I_{IN}(+)$ or $I_{IN}(-)$	—	40	200	nA
Voltage Gain	A_V	$R_L \ge 15k\Omega$, V+ = 15V, (Note 5)	70	125	—	V/mV
Large-Signal Response Time	t_r	V_{IN} = TTL Logic Swing $V_{REF} = 1.4V$, (Note 4) $V_{RL} = 5V$, $R_L = 5.1k\Omega$	—	300	—	ns
Small-Signal Response Time	t_r	V_{IN} = 100mV Step, (Note 4) 5mV Overdrive $V_{RL} = 5V$, $R_L = 5.1k\Omega$	—	1.3	—	µs
Input Voltage Range	CMVR	(Note 2)	0	—	V+ −1.5	V
Common-Mode Rejection Ratio	CMRR	(Notes 3, 5)	60	100	—	dB
Power Supply Rejection Ratio	PSRR	V+ = +5V to 18V	80	100	—	dB
Saturation Voltage	V_{OL}	$V_{IN}(-) \ge 1V$, $V_{IN}(+) = 0$, $I_{SINK} \le 4mA$	—	250	700	mV
Output Sink Current	I_{SINK}	$V_{IN}(-) \ge 1V$, $V_{IN}(+) = 0$, $V_O \le 1.5V$	5	16	—	mA
Output Leakage Current	I_{LEAK}	$V_{IN}(+) \ge 1V$, $V_{IN}(-) = 0$, $V_O = 30V$	—	0.1	200	nA
Supply Current	I+	$R_L = \infty$, All Comps V+ = 30V	—	1.2	3.0	mA

NOTES:
1. At output switch point, $V_O = 1.4V$, $R_S = 0\Omega$ with V+ from 5V; and over the full input common-mode range (0V to V+ − 1.5V).
2. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ − 1.5V, but either or both inputs can go to +30V without damage.
3. $R_L \ge 15k\Omega$, V+ = 15V, $V_{CM} = 1.5V$ to 13.5V.
4. Sample tested.
5. Guaranteed by design.

BURN-IN CIRCUIT



DICE CHARACTERISTICS



DIE SIZE 0.058 × 0.055 inch, 3190 sq. mils
(1.47 × 1.40 mm, 2.058 sq. mm)

1. OUTPUT (2)
2. OUTPUT (1)
3. POSITIVE SUPPLY
4. INVERTING INPUT (1)
5. NONINVERTING INPUT (1)
6. INVERTING INPUT (2)
7. NONINVERTING INPUT (2)
8. INVERTING INPUT (3)
9. NONINVERTING INPUT (3)
10. INVERTING INPUT (4)
11. NONINVERTING INPUT (4)
12. GROUND (SUBSTRATE)
13. OUTPUT (4)
14. OUTPUT (3)

For additional DICE ordering information, refer to 1990/91 Data Book, Section 2.

WAFER TEST LIMITS at V+ = +5V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-04N LIMIT	CMP-04G LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S = 0\Omega$, $R_L = 5.1k\Omega$ $V_O = 1.4V$, (Note 1)	1	2	mV MAX
Input Offset Current	I_{OS}	$I_{IN}(+) - I_{IN}(-)$ $R_L = 5.1k\Omega$ $V_O = 1.4V$	10	25	nA MAX
Input Bias Current	I_B	$I_{IN}(+)$ or $I_{IN}(-)$, (Note 1)	100	100	nA MAX
Voltage Gain	A_V	$R_L \geq 15k\Omega$, V+ = 15V, (Note 3)	80	50	V/mV MIN
Input Voltage Range	CMVR	(Notes 2, 3)	V+ − 1.5	V+ − 1.5	V MAX
Common-Mode Rejection Ratio	CMRR	(Note 4)	80	80	dB MIN
Power Supply Rejection Ratio	PSRR	V+ = 5V to +18V	80	80	dB MIN
Saturation Voltage	V_{OL}	$V_{IN}(-) \geq 1V$, $V_{IN}(+) = 0$, $I_{SINK} \leq 4mA$	400	400	mV MAX
Output Sink Current	I_{SINK}	$V_{IN}(-) \geq 1V$, $V_{IN}(+) = 0$, $V_O \leq 1.5V$	6	6	mA MIN
Output Leakage Current	I_{LEAK}	$V_{IN}(+) \geq 1V$, $V_{IN}(-) = 0$, $V_O = 30V$	100	100	nA MAX
Supply Current	I+	$R_L = \infty$, All Comps V+ = 30V	2	2	mA MAX

NOTES:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

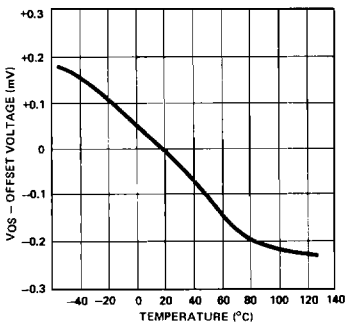
TYPICAL ELECTRICAL CHARACTERISTICS at V+ = +5V, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-04N TYPICAL	CMP-04G TYPICAL	UNITS
Large-Signal Response Time	t_r	V_{IN} = TTL Logic Swing V_{REF} = 1.4V, (Note 5) V_{RL} = 5V, $R_L = 5.1k\Omega$	600	600	ns
Small-Signal Response Time	t_r	V_{IN} = 100mV Step, (Note 5) 5mV Overdrive V_{RL} = 5V, $R_L = 5.1k\Omega$	1.3	1.3	μs

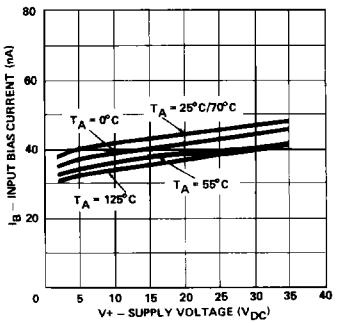
NOTES:
1. At output switch point, $V_O = 1.4V$, $R_S = 0\Omega$ with V+ from 5V; and over the full input common-mode range (0V to V+ − 1.5V).
2. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ − 1.5V, but either or both inputs can go to +30V without damage.
3. Guaranteed by design.
4. $R_L \geq 15k\Omega$. $V_{CM} = 1.5V$ to 13.5V.
5. Sample tested.

TYPICAL PERFORMANCE CHARACTERISTICS

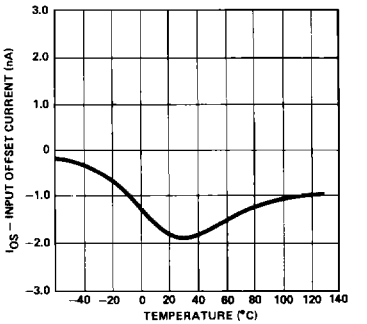
OFFSET VOLTAGE vs TEMPERATURE



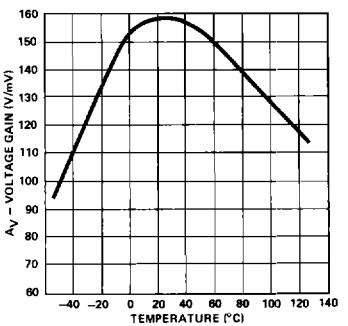
INPUT BIAS CURRENT vs V+ AND TEMPERATURE



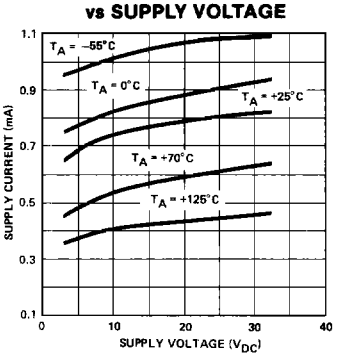
INPUT OFFSET CURRENT vs TEMPERATURE



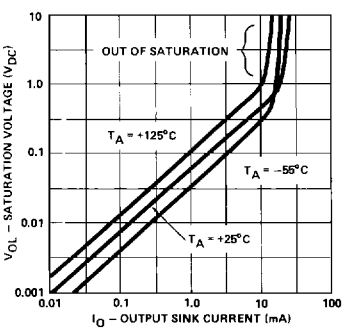
VOLTAGE GAIN vs TEMPERATURE



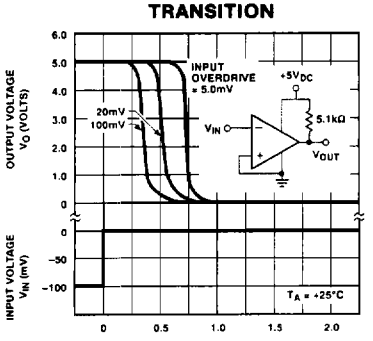
SUPPLY CURRENT vs SUPPLY VOLTAGE



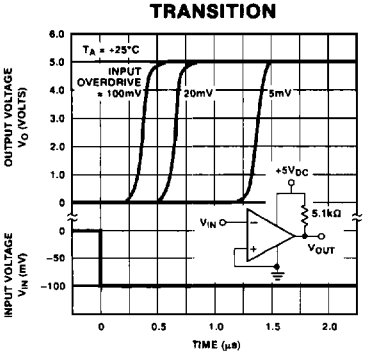
OUTPUT VOLTAGE vs OUTPUT CURRENT AND TEMPERATURE



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES — NEGATIVE TRANSITION

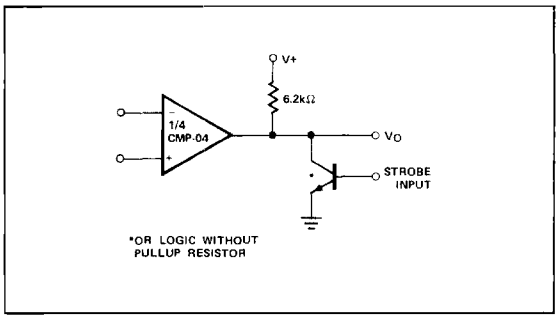


RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES — POSITIVE TRANSITION

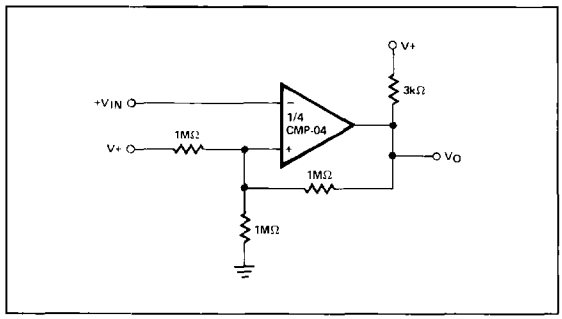


TYPICAL APPLICATIONS

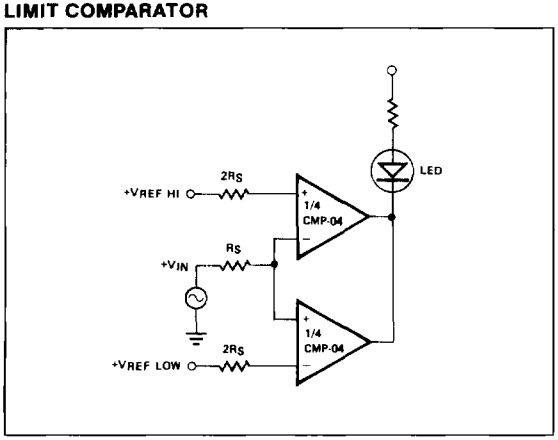
OUTPUT STROBING



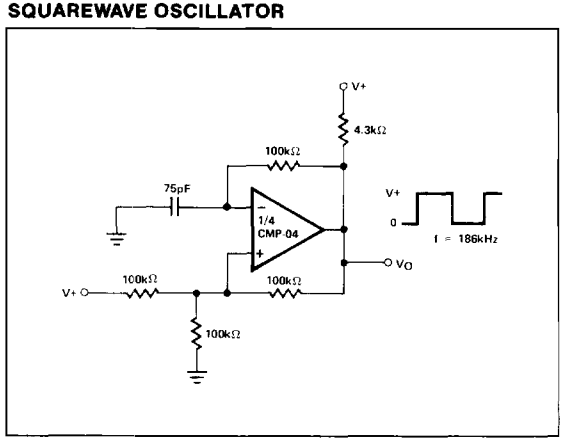
INVERTING COMPARATOR WITH HYSTERESIS



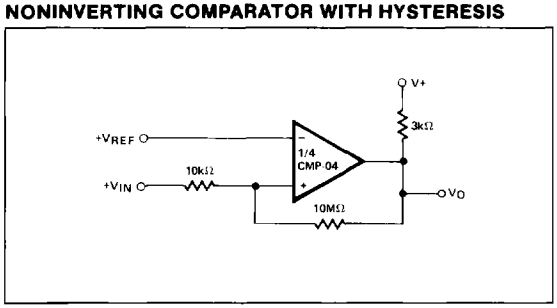
LIMIT COMPARATOR



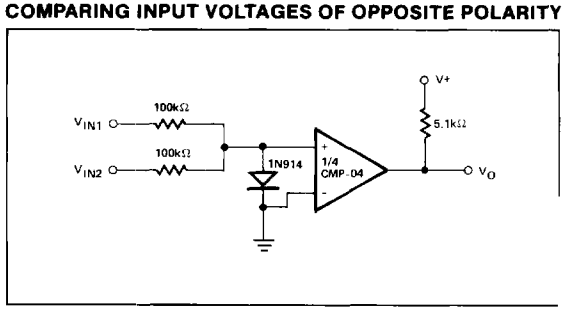
SQUAREWAVE OSCILLATOR



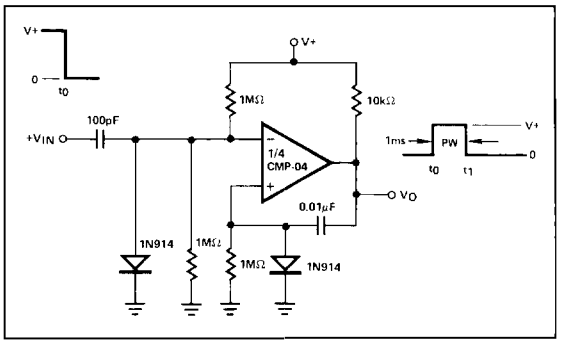
NONINVERTING COMPARATOR WITH HYSTERESIS



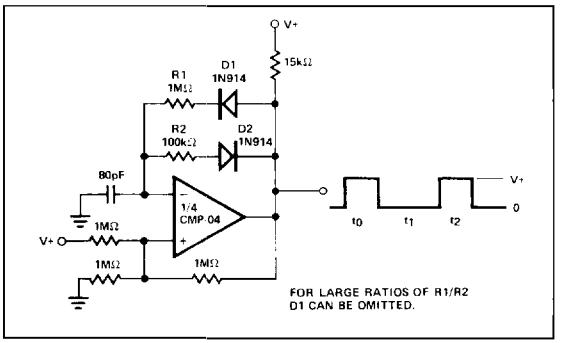
COMPARING INPUT VOLTAGES OF OPOSITE POLARITY



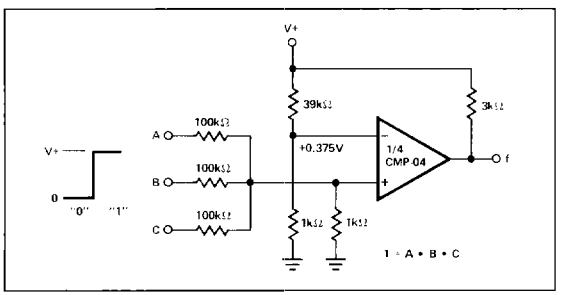
ONE-SHOT MULTIVIBRATOR



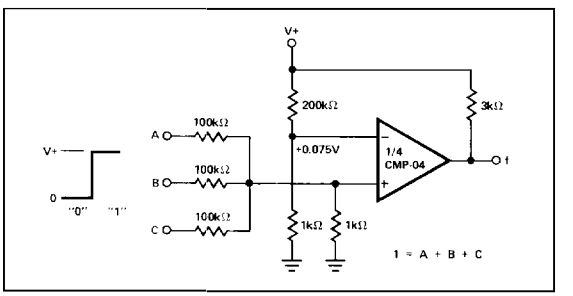
PULSE GENERATOR



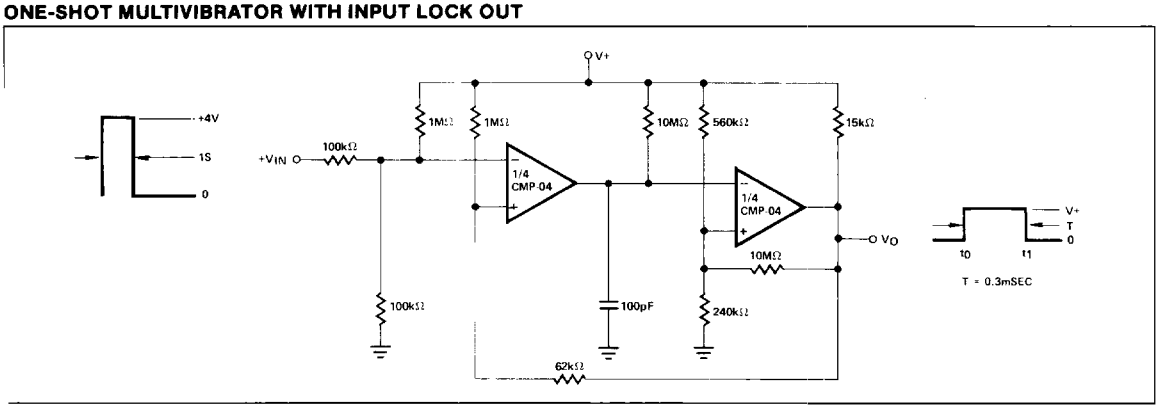
AND GATE



OR GATE



ONE-SHOT MULTIVIBRATOR WITH INPUT LOCK OUT



TYPICAL APPLICATIONS

TIME DELAY GENERATOR