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# HM51W17400B Series

4,194,304-word × 4-bit Dynamic Random Access Memory

# HITACHI

ADE-203-370A (Z)

Rev. 1.0

Nov. 17, 1995

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## Description

The Hitachi HM51W17400B is a CMOS dynamic RAM organized 4,194,304-word × 4-bit. It employs the most advanced CMOS technology for high performance and low power. The HM51W17400B offers Fast Page Mode as a high speed access mode.

## Features

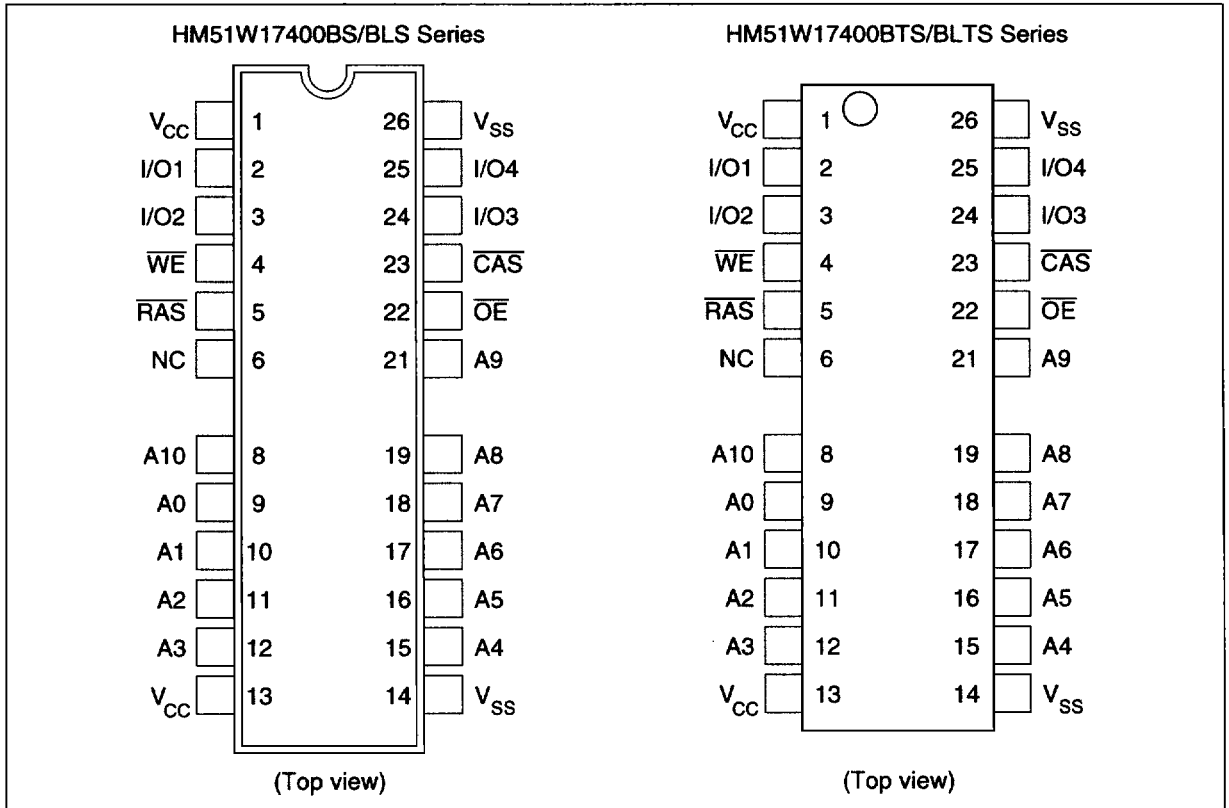
- Single 3.3 V ( $\pm 0.3$  V)
- High speed
  - Access time : 60 ns/ 70 ns/ 80 ns (max)
- Low power dissipation
  - Active mode : 396 mW/360 mW/324 mW(max)
  - Standby mode : 7.2 mW (max)
    - : 0.36 mW (max) (L-version)
- Fast page mode capability
- Long refresh period
  - 2048 refresh cycles : 32 ms
    - : 128 ms (L-version)
- 4 variations of refresh
  - $\overline{\text{RAS}}$ -only refresh
  - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh
  - Hidden refresh
  - Self refresh (L-version)
- Battery backup operation (L-version)
- Test function
  - 16-bit parallel test mode

This specification is fully compatible with the 16-Mbit DRAM specifications from TEXAS INSTRUMENTS.

## Ordering Information

Type No.	Access Time	Package
HM51W17400BS-6	60 ns	300-mil 26-pin plastic SOJ (CP-26/24DB)
HM51W17400BS-7	70 ns	
HM51W17400BS-8	80 ns	
HM51W17400BLS-6	60 ns	300-mil 26-pin plastic TSOP II (TTP-26/24DA)
HM51W17400BLS-7	70 ns	
HM51W17400BLS-8	80 ns	
HM51W17400BTS-6	60 ns	300-mil 26-pin plastic TSOP II (TTP-26/24DA)
HM51W17400BTS-7	70 ns	
HM51W17400BTS-8	80 ns	
HM51W17400BLTS-6	60 ns	300-mil 26-pin plastic TSOP II (TTP-26/24DA)
HM51W17400BLTS-7	70 ns	
HM51W17400BLTS-8	80 ns	

## Pin Arrangement



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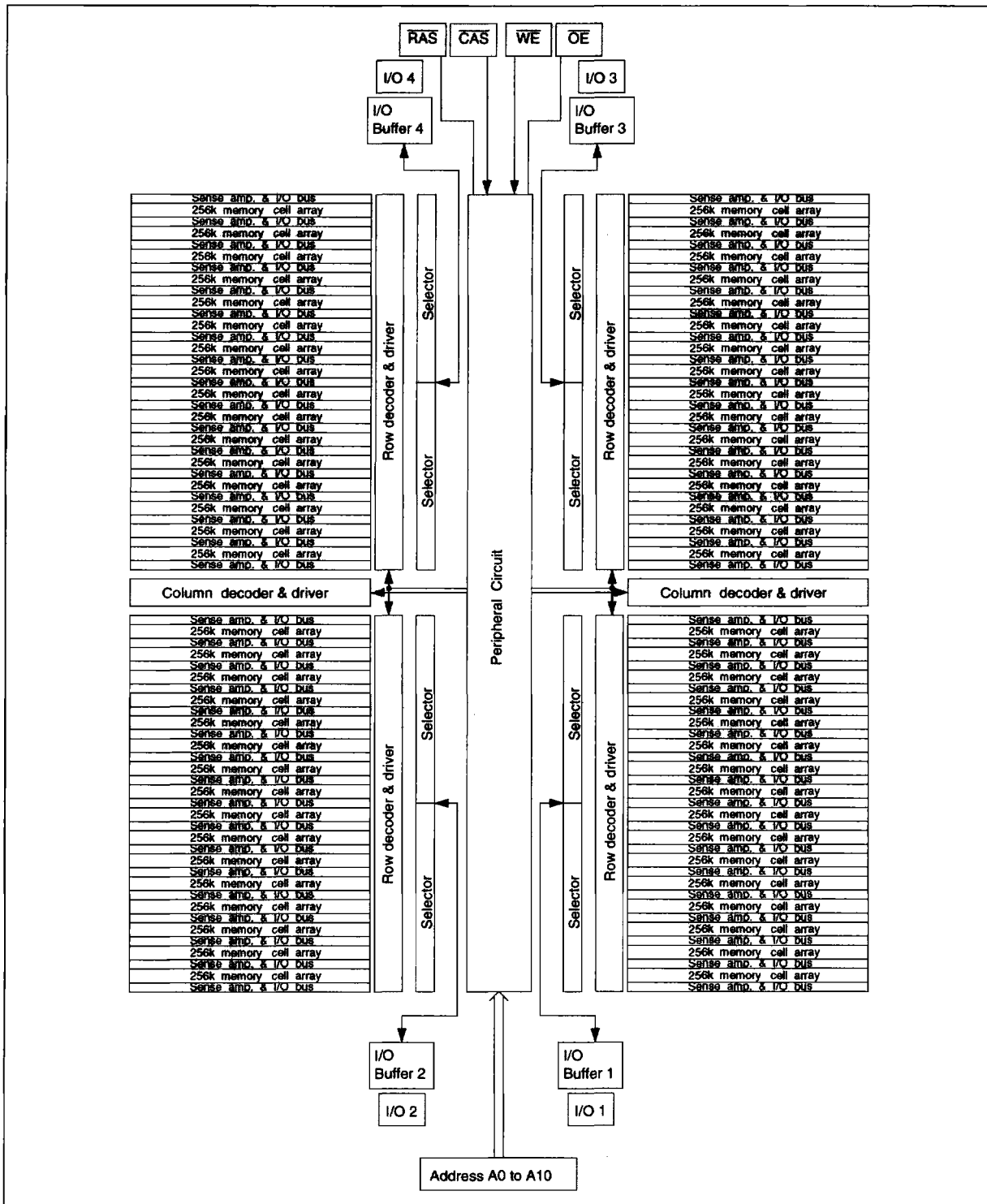
## HM51W17400B Series

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### Pin Description

Pin Name	Function
A0 to A10	Address input
A0 to A10	Refresh address input
I/O1 to I/O4	Data input/data output
$\overline{\text{RAS}}$	Row address strobe
$\overline{\text{CAS}}$	Column address strobe
$\overline{\text{WE}}$	Write enable
$\overline{\text{OE}}$	Output enable
$V_{\text{CC}}$	Power supply (+3.3 V)
$V_{\text{SS}}$	Ground
NC	No connection

Block Diagram



## HM51W17400B Series

### Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to $V_{SS}$	$V_T$	$-0.5$ to $V_{CC} + 0.5$ ( $\leq 4.6$ V (max))	V
Supply voltage relative to $V_{SS}$	$V_{CC}$	$-0.5$ to $+4.6$	V
Short circuit output current	$I_{out}$	50	mA
Power dissipation	$P_T$	1.0	W
Operating temperature	$T_{opr}$	0 to $+70$	$^{\circ}$ C
Storage temperature	$T_{stg}$	$-55$ to $+125$	$^{\circ}$ C

### Recommended DC Operating Conditions ( $T_a = 0$ to $+70^{\circ}$ C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	$V_{CC}$	3.0	3.3	3.6	V	1
Input high voltage	$V_{IH}$	2.0	—	$V_{CC} + 0.3$	V	1
Input low voltage	$V_{IL}$	$-0.3$	—	0.8	V	1

Note: 1. All voltage referred to  $V_{SS}$ .

### DC Characteristics ( $T_a = 0$ to $+70^{\circ}$ C, $V_{CC} = 3.3$ V $\pm$ 0.3 V, $V_{SS} = 0$ V)

Parameter	Symbol	HM51W17400B						Unit	Test Conditions
		-6		-7		-8			
		Min	Max	Min	Max	Min	Max		
Operating current <sup>1, 2</sup>	$I_{CC1}$	—	110	—	100	—	90	mA	$t_{RC} = \min$
Standby current	$I_{CC2}$	—	2	—	2	—	2	mA	TTL interface $\overline{RAS}, \overline{CAS} = V_{IH}$ Dout = High-Z
		—	1	—	1	—	1	mA	CMOS interface $\overline{RAS}, \overline{CAS} \geq V_{CC} - 0.2$ V Dout = High-Z
Standby current (L-version)	$I_{CC2}$	—	100	—	100	—	100	$\mu$ A	CMOS interface $\overline{RAS}, \overline{CAS} \geq V_{CC} - 0.2$ V Dout = High-Z

## DC Characteristics (Ta = 0 to +70°C, V<sub>CC</sub> = 3.3 V ± 0.3 V, V<sub>SS</sub> = 0 V) (cont)

Parameter	Symbol	HM51W17400B						Unit	Test Conditions
		-6		-7		-8			
		Min	Max	Min	Max	Min	Max		
RAS-only refresh current <sup>2</sup>	I <sub>CC3</sub>	—	110	—	100	—	90	mA	t <sub>RC</sub> = min
Standby current <sup>1</sup>	I <sub>CC5</sub>	—	5	—	5	—	5	mA	RAS = V <sub>IH</sub> , CAS = V <sub>IL</sub> Dout = enable
CAS-before-RAS refresh current	I <sub>CC6</sub>	—	110	—	100	—	90	mA	t <sub>RC</sub> = min
Fast page mode current <sup>1, 3</sup>	I <sub>CC7</sub>	—	80	—	70	—	65	mA	t <sub>PC</sub> = min
Battery backup current (Standby with CBR refresh) (L-version)	I <sub>CC10</sub>	—	300	—	300	—	300	μA	CMOS interface Dout = High-Z CBR refresh: t <sub>RC</sub> = 62.5 μs t <sub>RAS</sub> ≤ 0.3 μs
Self refresh mode current (L-version)	I <sub>CC11</sub>	—	200	—	200	—	200	μA	CMOS interface RAS, CAS ≤ 0.2 V Dout = High-Z
Input leakage current	I <sub>LI</sub>	-10	10	-10	10	-10	10	μA	0 V ≤ Vin ≤ 4.6 V
Output leakage current	I <sub>LO</sub>	-10	10	-10	10	-10	10	μA	0 V ≤ Vout ≤ 4.6 V Dout = disable
Output high voltage	V <sub>OH</sub>	2.4	V <sub>CC</sub>	2.4	V <sub>CC</sub>	2.4	V <sub>CC</sub>	V	High Iout = -2 mA
Output low voltage	V <sub>OL</sub>	0	0.4	0	0.4	0	0.4	V	Low Iout = 2 mA

Notes: 1. I<sub>CC</sub> depends on output load condition when the device is selected. I<sub>CC</sub> max is specified at the output open condition.

2. Address can be changed once or less while RAS = V<sub>IL</sub>.

3. Address can be changed once or less while CAS = V<sub>IH</sub>.

## Capacitance (Ta = 25°C, V<sub>CC</sub> = 3.3 V ± 0.3 V)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C <sub>I1</sub>	—	5	pF	1
Input capacitance (Clocks)	C <sub>I2</sub>	—	7	pF	1
Output capacitance (Data-in, Data-out)	C <sub>I/O</sub>	—	7	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. CAS = V<sub>IH</sub> to disable Dout.

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AC Characteristics ( $T_a = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ ) \*1, \*2, \*18, \*19

### Test Conditions

- Input rise and fall time : 5 ns
- Input timing reference levels : 0.8 V, 2.0 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load : 1 TTL gate +  $C_L$  (100 pF) (Including scope and jig)

### Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

Parameter	Symbol	HM51W17400B						Unit	Notes
		-6		-7		-8			
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	$t_{RC}$	110	—	130	—	150	—	ns	
$\overline{\text{RAS}}$ precharge time	$t_{RP}$	40	—	50	—	60	—	ns	
$\overline{\text{CAS}}$ precharge time	$t_{CP}$	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ pulse width	$t_{RAS}$	60	10000	70	10000	80	10000	ns	
$\overline{\text{CAS}}$ pulse width	$t_{CAS}$	15	10000	18	10000	20	10000	ns	
Row address setup time	$t_{ASR}$	0	—	0	—	0	—	ns	
Row address hold time	$t_{RAH}$	10	—	10	—	10	—	ns	
Column address setup time	$t_{ASC}$	0	—	0	—	0	—	ns	
Column address hold time	$t_{CAH}$	10	—	15	—	15	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	$t_{RCD}$	20	45	20	52	20	60	ns	3
$\overline{\text{RAS}}$ to column address delay time	$t_{RAD}$	15	30	15	35	15	40	ns	4
$\overline{\text{RAS}}$ hold time	$t_{RSH}$	15	—	18	—	20	—	ns	
$\overline{\text{CAS}}$ hold time	$t_{CSH}$	60	—	70	—	80	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	$t_{CRP}$	5	—	5	—	5	—	ns	
$\overline{\text{OE}}$ to Din delay time	$t_{OED}$	15	—	18	—	20	—	ns	5
$\overline{\text{OE}}$ delay time from Din	$t_{DZO}$	0	—	0	—	0	—	ns	6
$\overline{\text{CAS}}$ delay time from Din	$t_{DZC}$	0	—	0	—	0	—	ns	6
Transition time (rise and fall)	$t_T$	3	50	3	50	3	50	ns	7

**Read Cycle**
**HM51W17400B**

		-6		-7		-8			
		Min	Max	Min	Max	Min	Max		

Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Access time from $\overline{\text{RAS}}$	$t_{\text{RAC}}$	—	60	—	70	—	80	ns	8, 9, 20
Access time from $\overline{\text{CAS}}$	$t_{\text{CAC}}$	—	15	—	18	—	20	ns	9, 10, 17, 20
Access time from address	$t_{\text{AA}}$	—	30	—	35	—	40	ns	9, 11, 17, 20
Access time from $\overline{\text{OE}}$	$t_{\text{OEA}}$	—	15	—	18	—	20	ns	9, 20
Read command setup time	$t_{\text{RCS}}$	0	—	0	—	0	—	ns	
Read command hold time to $\overline{\text{CAS}}$	$t_{\text{RCH}}$	0	—	0	—	0	—	ns	12
Read command hold time to $\overline{\text{RAS}}$	$t_{\text{RRH}}$	0	—	0	—	0	—	ns	12
Column address to $\overline{\text{RAS}}$ lead time	$t_{\text{RAL}}$	30	—	35	—	40	—	ns	
Column address to $\overline{\text{CAS}}$ lead time	$t_{\text{CAL}}$	30	—	35	—	40	—	ns	
$\overline{\text{CAS}}$ to output in low-Z	$t_{\text{CLZ}}$	0	—	0	—	0	—	ns	
Output data hold time	$t_{\text{OH}}$	3	—	3	—	3	—	ns	
Output data hold time from $\overline{\text{OE}}$	$t_{\text{OHO}}$	3	—	3	—	3	—	ns	
Output buffer turn-off time	$t_{\text{OFF}}$	—	15	—	15	—	15	ns	13
Output buffer turn-off to $\overline{\text{OE}}$	$t_{\text{OEZ}}$	—	15	—	15	—	15	ns	13
$\overline{\text{CAS}}$ to Din delay time	$t_{\text{CDD}}$	15	—	18	—	20	—	ns	5

**Write Cycle**
**HM51W17400B**

		-6		-7		-8			
		Min	Max	Min	Max	Min	Max		

Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Write command setup time	$t_{\text{WCS}}$	0	—	0	—	0	—	ns	14
Write command hold time	$t_{\text{WCH}}$	10	—	15	—	15	—	ns	
Write command pulse width	$t_{\text{WP}}$	10	—	10	—	10	—	ns	
Write command to $\overline{\text{RAS}}$ lead time	$t_{\text{RWL}}$	15	—	18	—	20	—	ns	
Write command to $\overline{\text{CAS}}$ lead time	$t_{\text{CWL}}$	15	—	18	—	20	—	ns	
Data-in setup time	$t_{\text{DS}}$	0	—	0	—	0	—	ns	15
Data-in hold time	$t_{\text{DH}}$	10	—	15	—	15	—	ns	15

# HM51W17400B Series

## Read-Modify-Write Cycle

Parameter	Symbol	HM51W17400B						Unit	Notes
		-6		-7		-8			
		Min	Max	Min	Max	Min	Max		
Read-modify-write cycle time	$t_{RWC}$	155	—	181	—	205	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	$t_{RWD}$	85	—	98	—	110	—	ns	14
$\overline{CAS}$ to $\overline{WE}$ delay time	$t_{CWD}$	40	—	46	—	50	—	ns	14
Column address to $\overline{WE}$ delay time	$t_{AWD}$	55	—	63	—	70	—	ns	14
$\overline{OE}$ hold time from $\overline{WE}$	$t_{OEH}$	15	—	18	—	20	—	ns	

## Refresh Cycle

Parameter	Symbol	HM51W17400B						Unit	Notes
		-6		-7		-8			
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ setup time (CBR refresh cycle)	$t_{CSR}$	5	—	5	—	5	—	ns	
$\overline{CAS}$ hold time (CBR refresh cycle)	$t_{CHR}$	10	—	10	—	10	—	ns	
$\overline{WE}$ setup time (CBR refresh cycle)	$t_{WRP}$	0	—	0	—	0	—	ns	
$\overline{WE}$ hold time (CBR refresh cycle)	$t_{WRH}$	10	—	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	$t_{RPC}$	0	—	0	—	0	—	ns	

## Fast Page Mode Cycle

Parameter	Symbol	HM51W17400B						Unit	Notes
		-6		-7		-8			
		Min	Max	Min	Max	Min	Max		
Fast page mode cycle time	$t_{PC}$	40	—	45	—	50	—	ns	
Fast page mode $\overline{RAS}$ pulse width	$t_{RASP}$	—	100000	—	100000	—	100000	ns	16
Access time from $\overline{CAS}$ precharge	$t_{CPA}$	—	35	—	40	—	45	ns	9, 17, 20
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	$t_{CPRH}$	35	—	40	—	45	—	ns	

## Fast Page Mode Read-Modify-Write Cycle

		HM51W17400B							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Fast page mode read-modify-write cycle time	$t_{PRWC}$	85	—	96	—	105	—	ns	
$\overline{WE}$ delay time from $\overline{CAS}$ precharge	$t_{CPW}$	60	—	68	—	75	—	ns	14

## Test Mode Cycle<sup>\*19</sup>

		HM51W17400B							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Test mode $\overline{WE}$ setup time	$t_{WTS}$	0	—	0	—	0	—	ns	
Test mode $\overline{WE}$ hold time	$t_{WTH}$	10	—	10	—	10	—	ns	

## Refresh

Parameter	Symbol	Max	Unit	Note
Refresh period	$t_{REF}$	32	ms	2048 cycles
Refresh period (L-version)	$t_{REF}$	128	ms	2048 cycles

## Self Refresh Mode (L-version)

		HM51W17400BL							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{RAS}$ pulse width (Self refresh)	$t_{RASS}$	100	—	100	—	100	—	$\mu$ s	
$\overline{RAS}$ precharge time (Self refresh)	$t_{RPS}$	110	—	130	—	150	—	ns	
$\overline{CAS}$ hold time (Self refresh)	$t_{CHS}$	-50	—	-50	—	-50	—	ns	

Notes: 1. AC measurements assume  $t_T = 5$  ns.

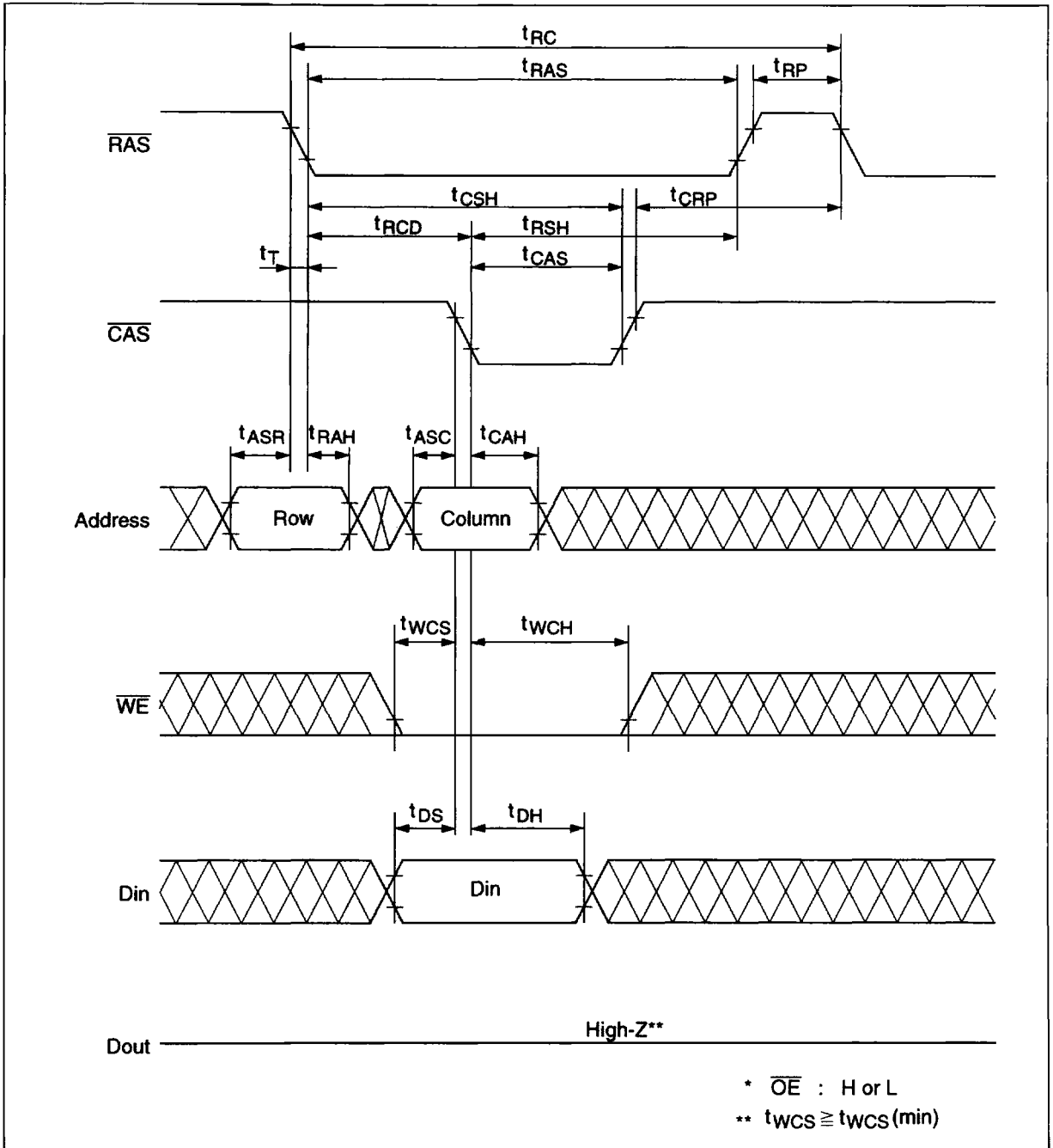
- An initial pause of 200  $\mu$ s is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing  $\overline{RAS}$ -only refresh or  $\overline{CAS}$ -before- $\overline{RAS}$  refresh). If the internal refresh counter is used, a minimum of eight  $\overline{CAS}$ -before- $\overline{RAS}$  refresh cycles are required.
- Operation with the  $t_{RCD}$  (max) limit insures that  $t_{RAC}$  (max) can be met,  $t_{RCD}$  (max) is specified as a reference point only; if  $t_{RCD}$  is greater than the specified  $t_{RCD}$  (max) limit, then access time is controlled exclusively by  $t_{CAC}$ .

4. Operation with the  $t_{RAD}$  (max) limit insures that  $t_{RAC}$  (max) can be met,  $t_{RAD}$  (max) is specified as a reference point only; if  $t_{RAD}$  is greater than the specified  $t_{RAD}$  (max) limit, then access time is controlled exclusively by  $t_{AA}$ .
5. Either  $t_{OED}$  or  $t_{CDD}$  must be satisfied.
6. Either  $t_{DZO}$  or  $t_{DZC}$  must be satisfied.
7.  $V_{IH}$  (min) and  $V_{IL}$  (max) are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  (min) and  $V_{IL}$  (max).
8. Assumes that  $t_{RCD} \leq t_{RCD}$  (max) and  $t_{RAD} \leq t_{RAD}$  (max). If  $t_{RCD}$  or  $t_{RAD}$  is greater than the maximum recommended value shown in this table,  $t_{RAC}$  exceeds the value shown.
9. Measured with a load circuit equivalent to 1 TTL loads and 100 pF. ( $V_{OH} = 2.0$  V,  $V_{OL} = 0.8$  V)
10. Assumes that  $t_{RCD} \geq t_{RCD}$  (max) and  $t_{RCD} + t_{CAC}$  (max)  $\geq t_{RAD} + t_{AA}$  (max).
11. Assumes that  $t_{RAD} \geq t_{RAD}$  (max) and  $t_{RCD} + t_{CAC}$  (max)  $\leq t_{RAD} + t_{AA}$  (max).
12. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycles.
13.  $t_{OFF}$  (max) and  $t_{OEZ}$  (max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
14.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$ ,  $t_{AWD}$  and  $t_{CPW}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if  $t_{WCS} \geq t_{WCS}$  (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if  $t_{RWD} \geq t_{RWD}$  (min),  $t_{CWD} \geq t_{CWD}$  (min), and  $t_{AWD} \geq t_{AWD}$  (min), or  $t_{CWD} \geq t_{CWD}$  (min),  $t_{AWD} \geq t_{AWD}$  (min) and  $t_{CPW} \geq t_{CPW}$  (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. These parameters are referred to  $\overline{CAS}$  leading edge in early write cycles and to  $\overline{WE}$  leading edge in delayed write or read-modify-write cycles.
16.  $t_{RASP}$  defines  $\overline{RAS}$  pulse width in fast page mode cycles.
17. Access time is determined by the longest among  $t_{AA}$ ,  $t_{CAC}$  and  $t_{CPA}$ .
18. In delayed write or read-modify-write cycles,  $\overline{OE}$  must disable output buffer prior to applying data to the device. After  $\overline{RAS}$  is reset, if  $t_{OEH} \geq t_{CWL}$ , the I/O pin will remain open circuit (high impedance); if  $t_{OEH} < t_{CWL}$ , invalid data will be out at each I/O.
19. The 16M DRAM offers a 16-bit time saving parallel test mode. Address CA0 and CA1 for the 4M  $\times$  4 are don't care during test mode. Test mode is set by performing  $\overline{WE}$ -and- $\overline{CAS}$ -before- $\overline{RAS}$  (WCBR) cycle. In 16-bit parallel test mode, data is written into 4 bits in parallel at each I/O (I/O1 to I/O4) and read out from each I/O.  
 If 4 bits of each I/O are equal (all 1s or 0s), data output pin is a high state during test mode read cycle, then the device has passed. If they are not equal, data output pin is a low state, then the device has failed.  
 Refresh during test mode operation can be performed by normal read cycles or by WCBR refresh cycles.  
 To get out of test mode and enter a normal operation mode, perform either a regular  $\overline{CAS}$ -before- $\overline{RAS}$  refresh cycle or  $\overline{RAS}$ -only refresh cycle.
20. In a test mode read cycle, the value of  $t_{RAC}$ ,  $t_{AA}$ ,  $t_{CAC}$  and  $t_{CPA}$  is delayed by 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
21. XXX: H or L (H:  $V_{IH}$  (min)  $\leq V_{IN} \leq V_{IH}$  (max), L:  $V_{IL}$  (min)  $\leq V_{IN} \leq V_{IL}$  (max))  
 //////////////: Invalid Dout



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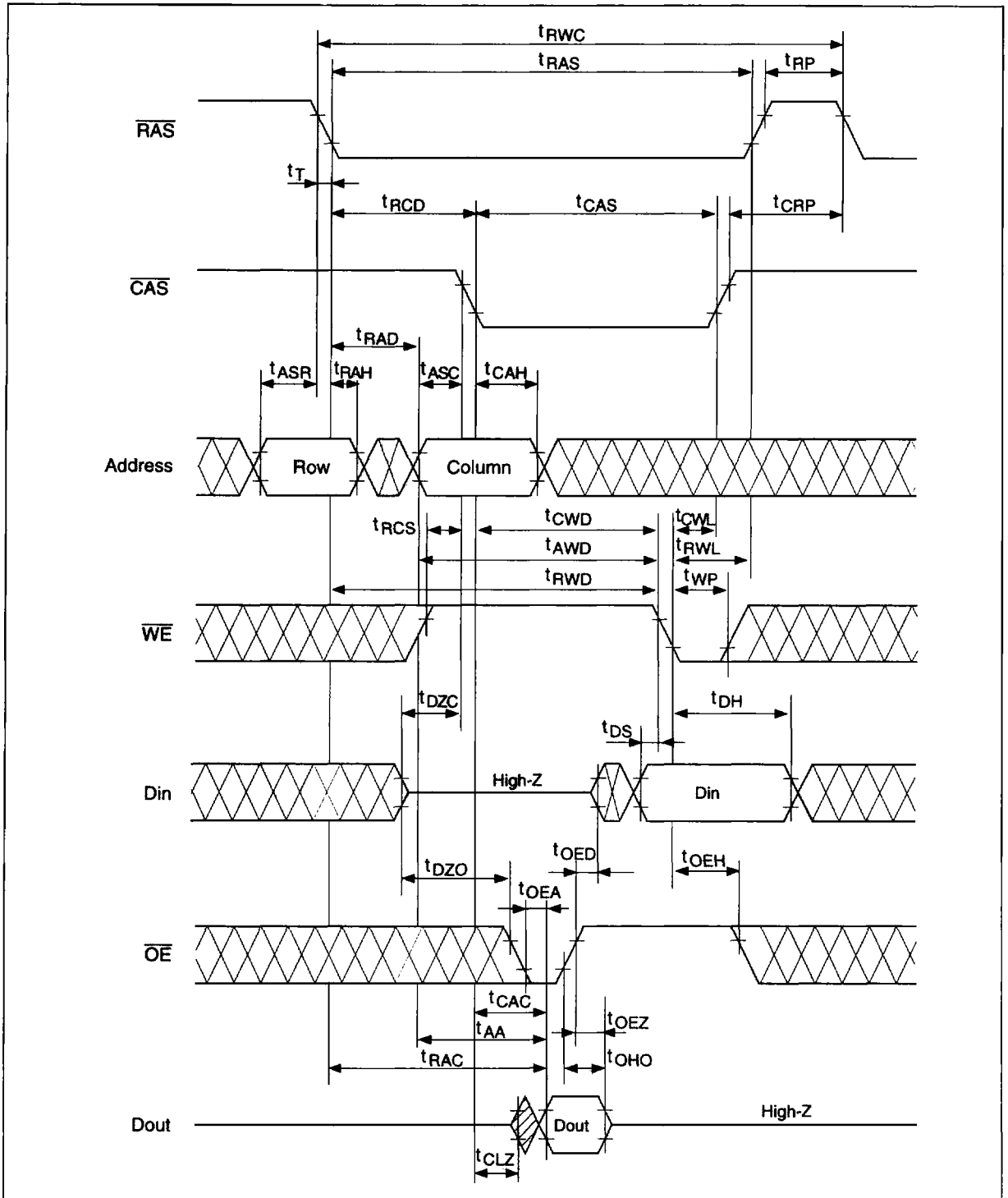
## Early Write Cycle



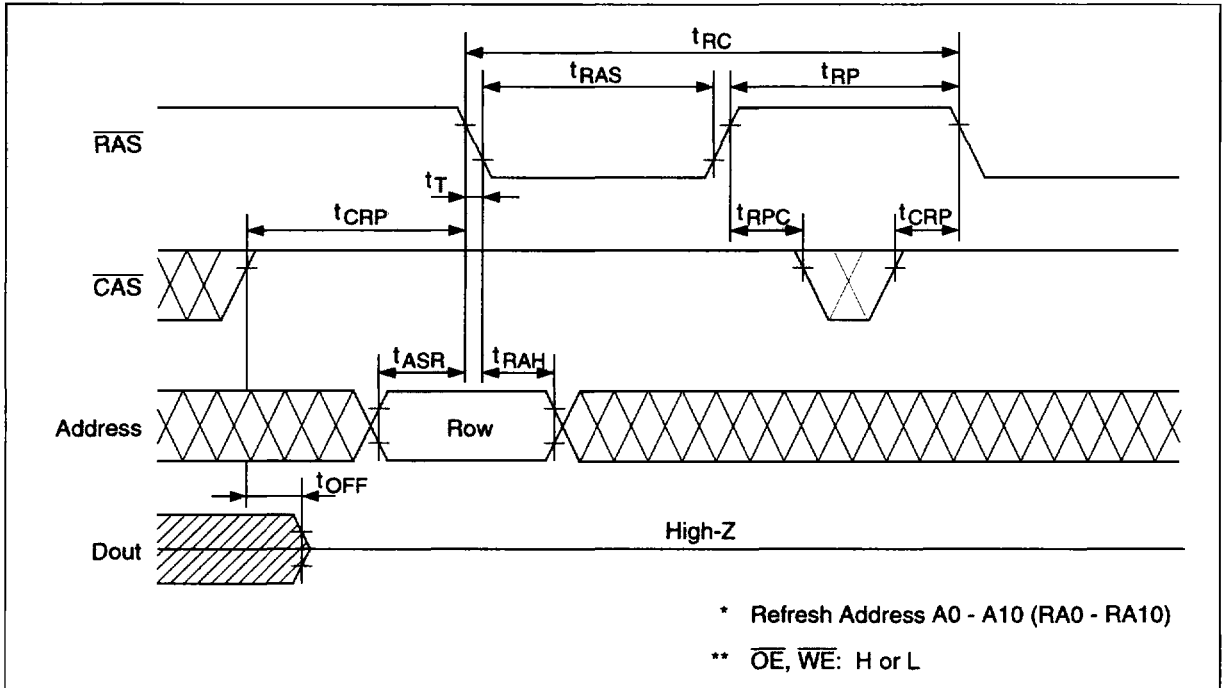


# HM51W17400B Series

## Read-Modify-Write Cycle<sup>\*18</sup>

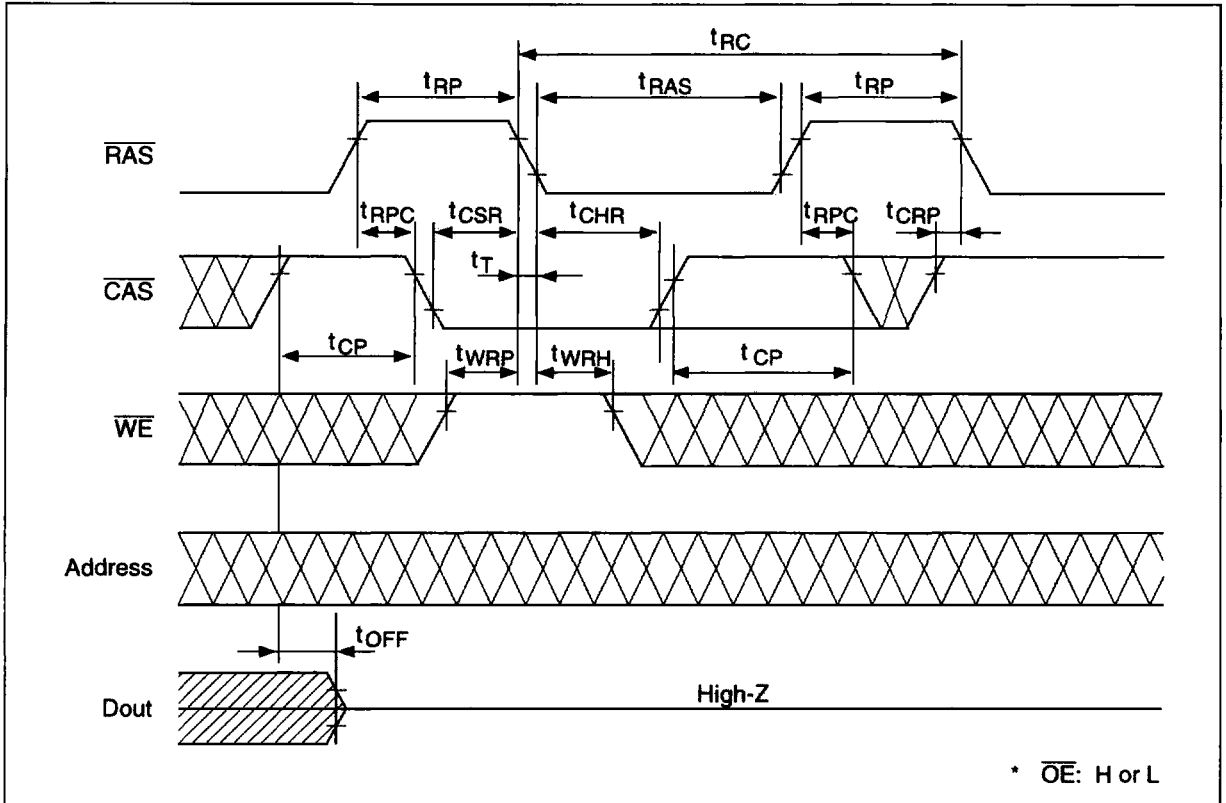


RAS-Only Refresh Cycle

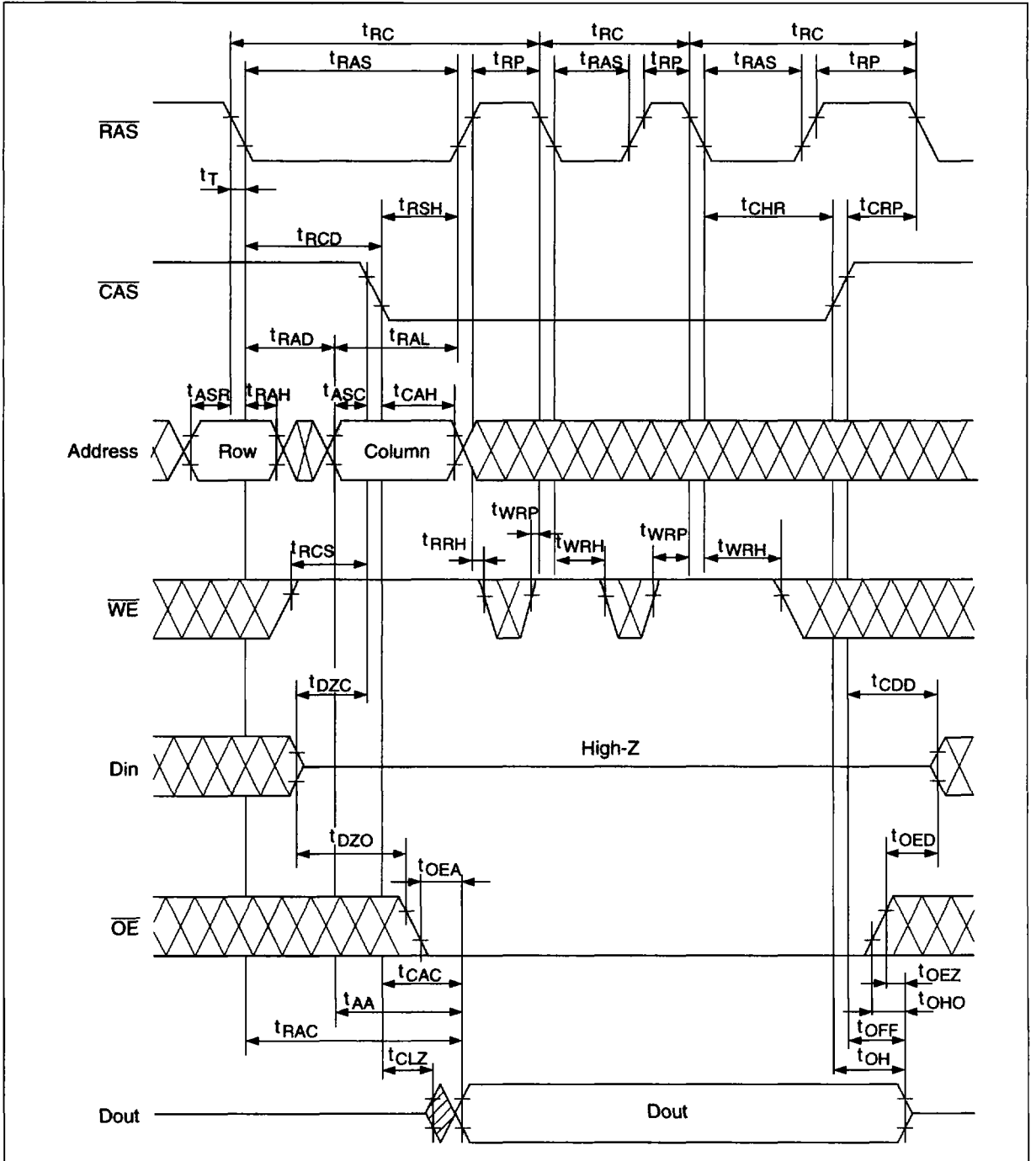


# HM51W17400B Series

## CAS-Before-RAS Refresh Cycle

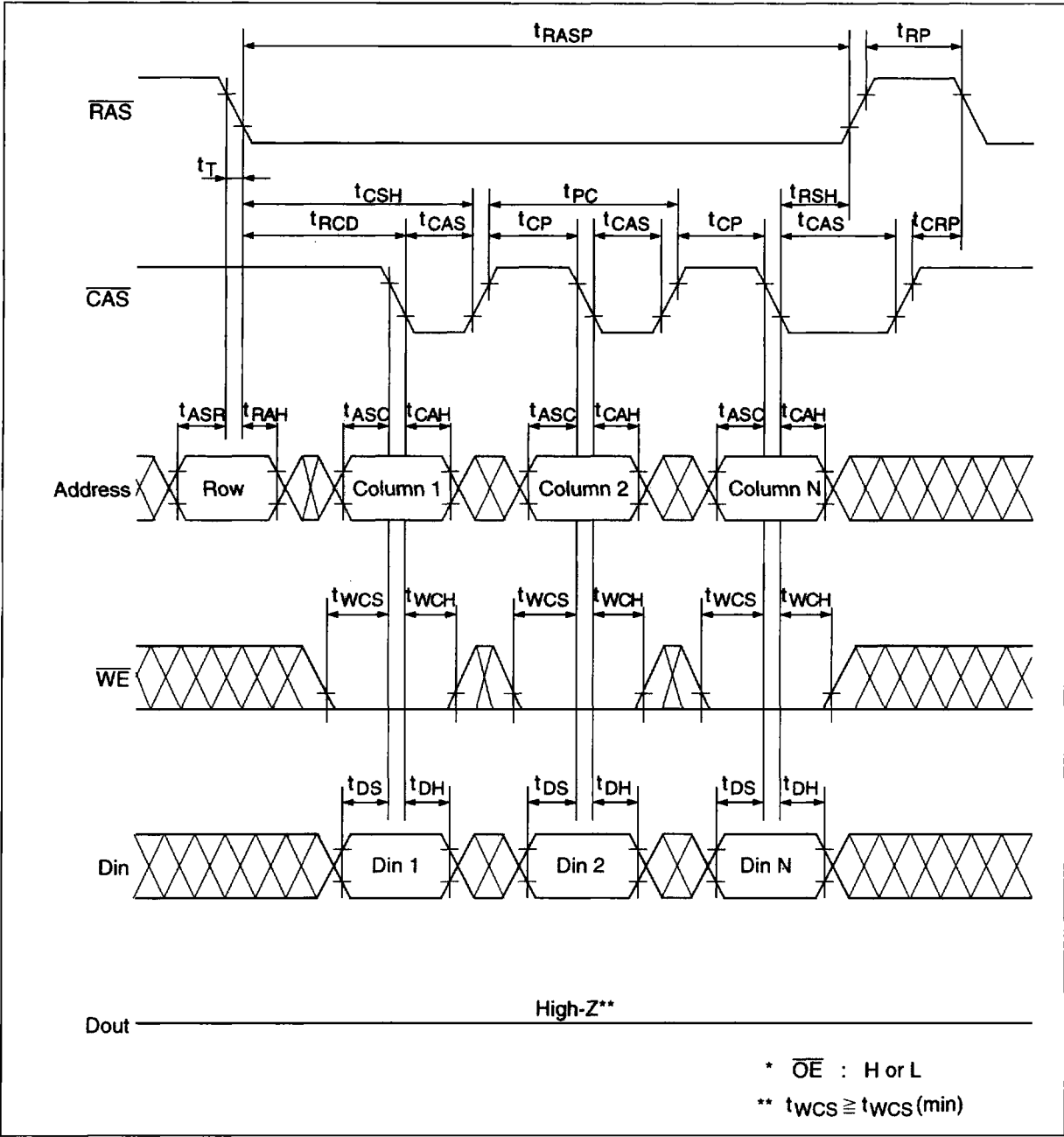


Hidden Refresh Cycle



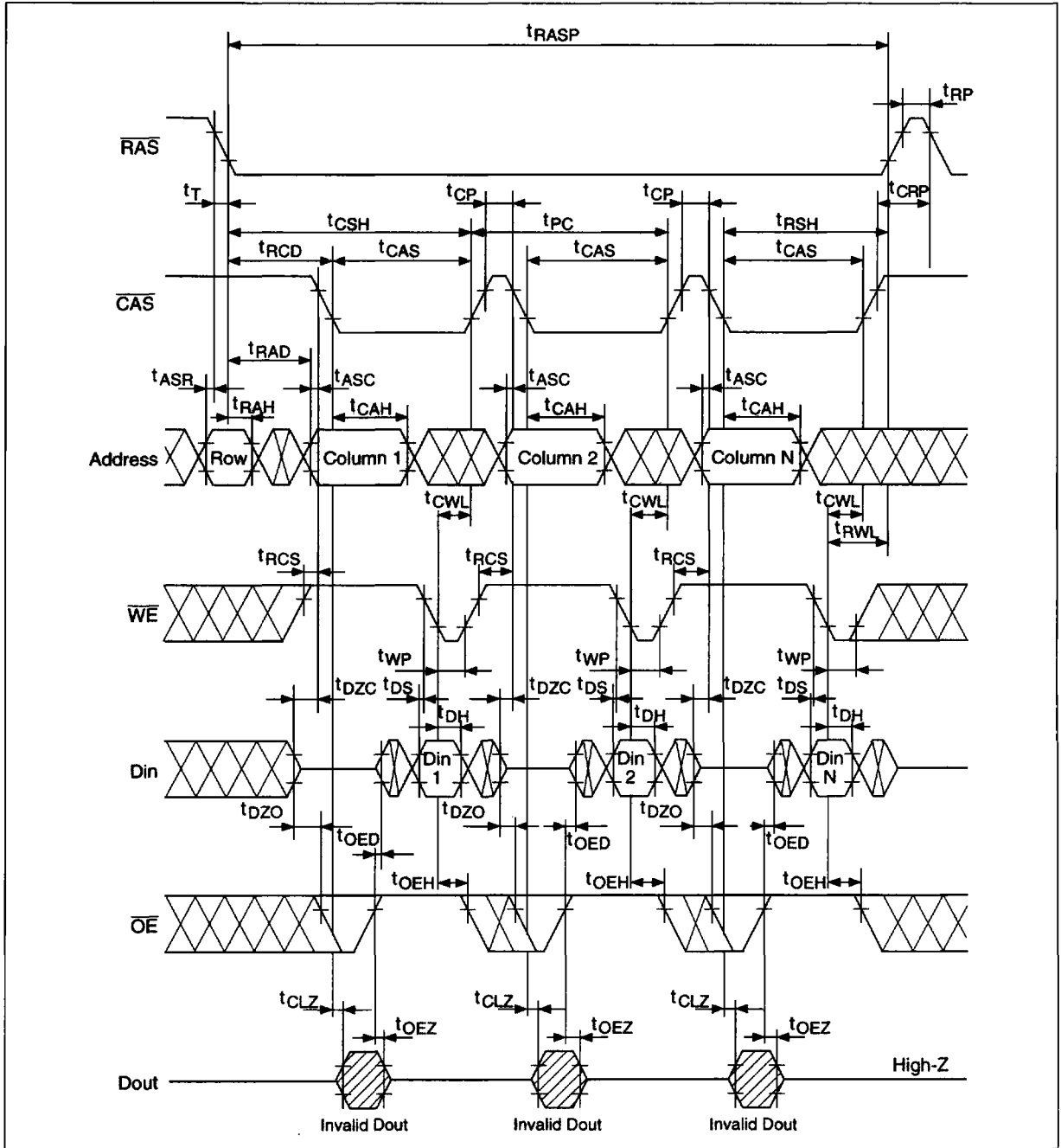


Fast Page Mode Early Write Cycle

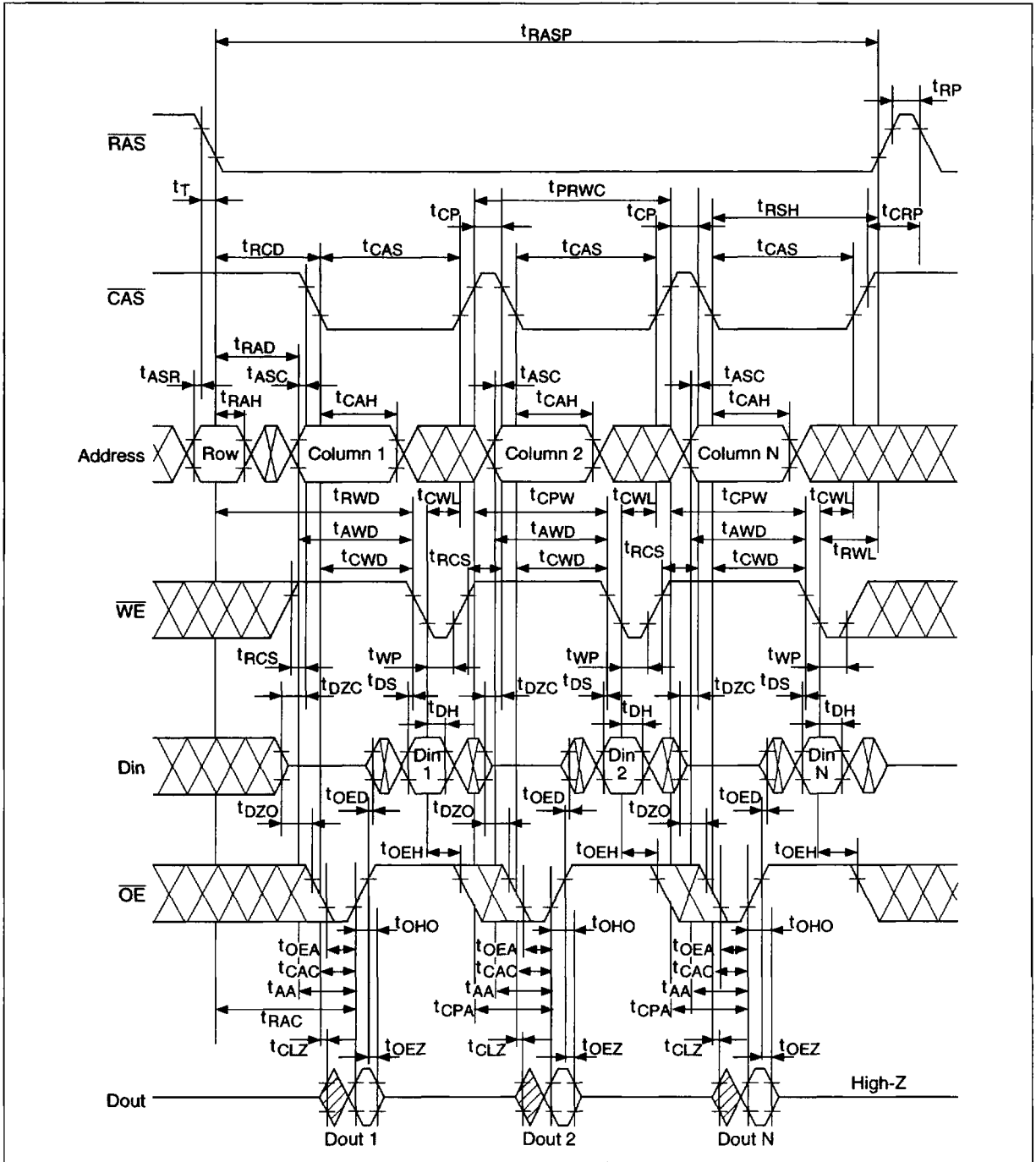


# HM51W17400B Series

## Fast Page Mode Delayed Write Cycle<sup>\*18</sup>

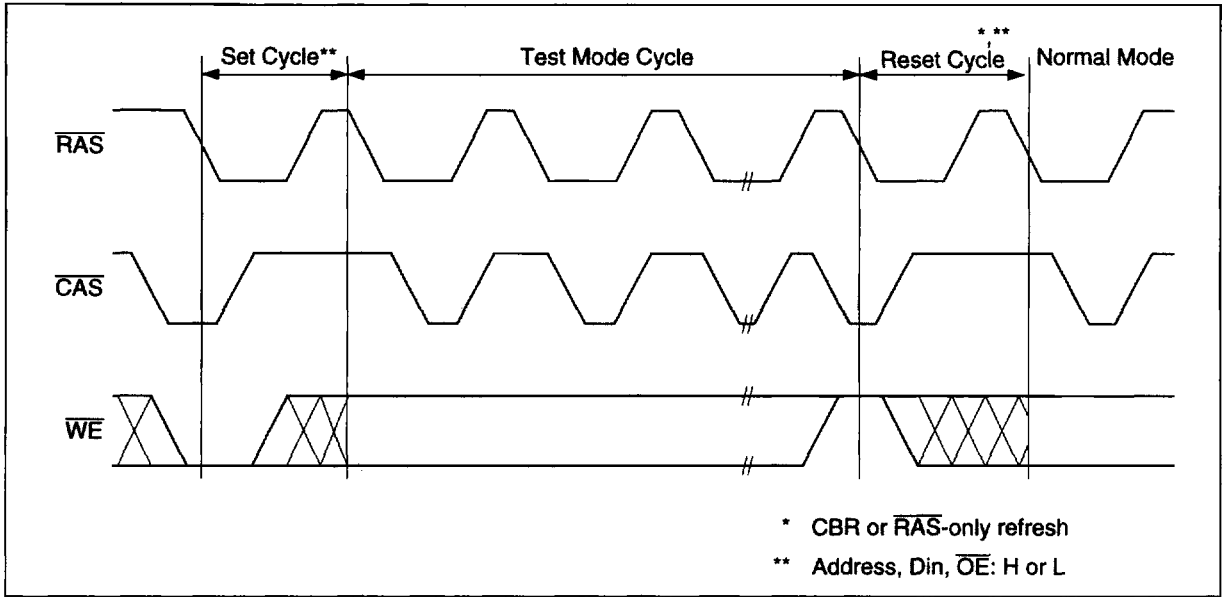


Fast Page Mode Read-Modify-Write Cycle\*18

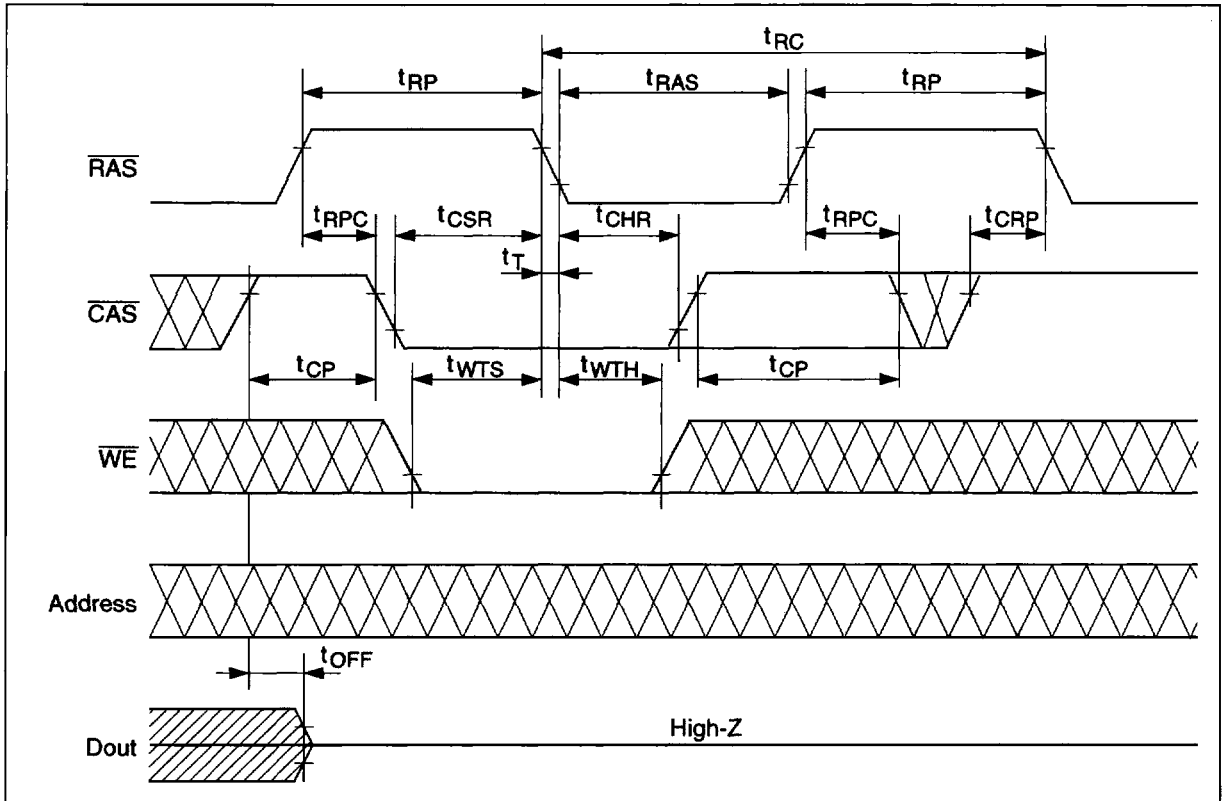


# HM51W17400B Series

## Test Mode Cycle \*19

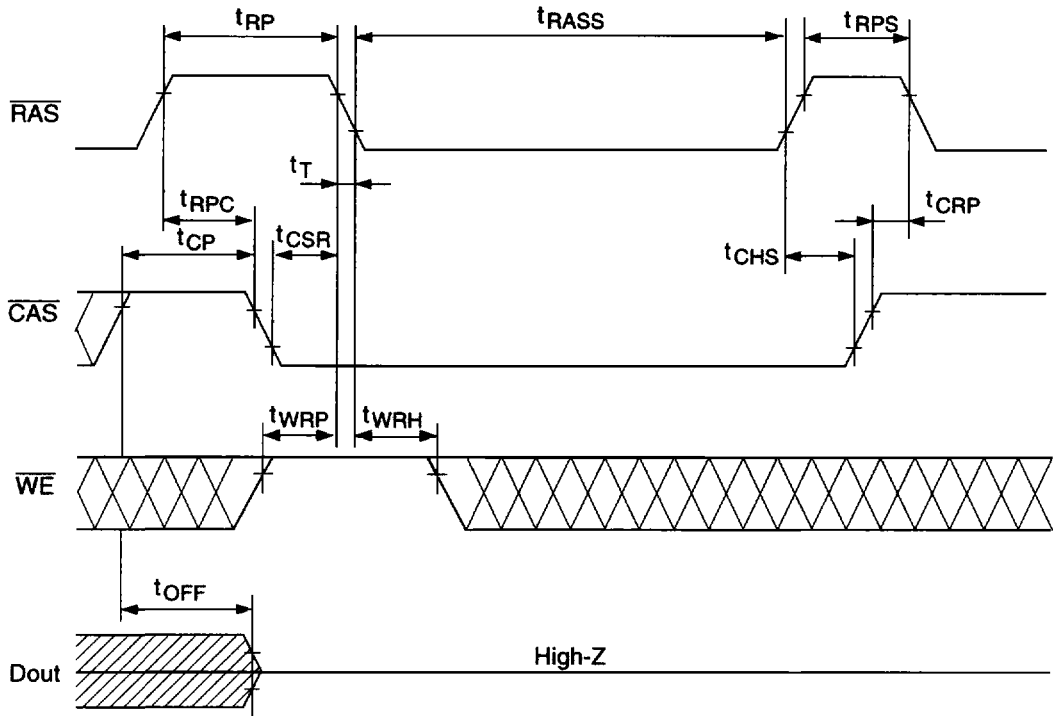


Test Mode Set Cycle



# HM51W17400B Series

## Self Refresh Cycle (L-version)



\* Address,  $\overline{\text{OE}}$  : H or L

The low self refresh current is achieved by introducing extremely long internal refresh cycle. Therefore some care needs to be taken on the refresh.

1. Please do not use  $t_{\text{RASS}}$  timing,  $10 \mu\text{s} \leq t_{\text{RASS}} \leq 100 \mu\text{s}$ . During this period, the device is in transition state from normal operation mode to self refresh mode. If  $t_{\text{RASS}} \geq 100 \mu\text{s}$ , then  $\overline{\text{RAS}}$  precharge time should use  $t_{\text{RPS}}$  instead of  $t_{\text{RP}}$ .
2. If you use distributed CBR refresh mode with  $15.6 \mu\text{s}$  interval in normal read/write cycle, CBR refresh should be executed within  $15.6 \mu\text{s}$  immediately after exiting from and before entering into self refresh mode.
3. If you use  $\overline{\text{RAS}}$  only refresh or CBR burst refresh mode in normal read/write cycle, 2048 cycles of distributed CBR refresh with  $15.6 \mu\text{s}$  interval should be executed within 32 ms immediately after exiting from and before entering into the self refresh mode.
4. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.