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SSI 32D535
Data Synchronizer/ 2, 7 RLL ENDEC with Write Precompensation

November 1991

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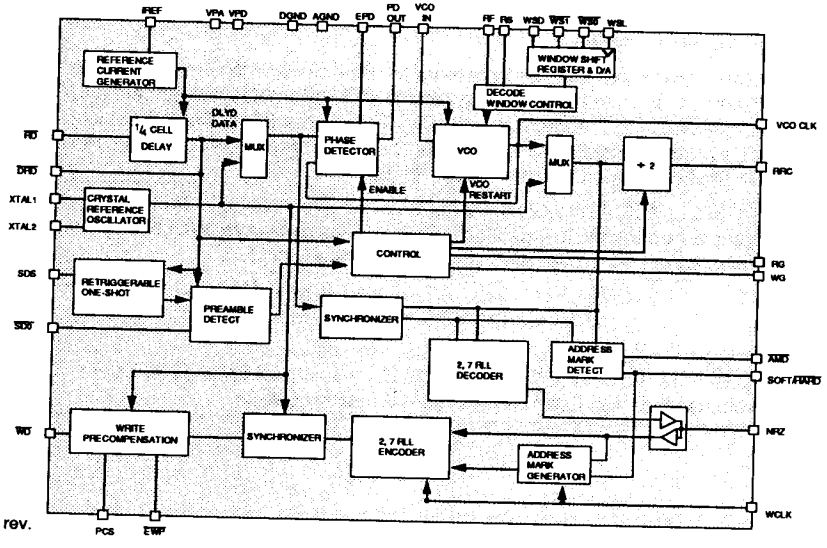
DESCRIPTION

The SSI 32D535 Data Separator provides data recovery, data encoding, and write precompensation for storage systems which employ a 2, 7 RLL encoding format. Data synchronization is performed with a fully integrated high performance PLL. A zero phase restart technique is used to minimize PLL acquisition time. The SSI 32D535 has been optimized for operation at a single data rate between 7.5 to 10 Mbit/s operation utilizing a crystal reference oscillator. The VCO frequency setting elements are incorporated within the SSI 32D535 for enhanced performance and reduced board space. Data rate is established with a single external programming resistor. The SSI 32D535 utilizes an advanced bipolar process technology which affords precise decode window control without requiring an accurate 1/4 cell delay or external devices. To enhance disk drive testability, decode window symmetry control is available through a digital µP port and/or two analog pins. This feature can facilitate defect mapping, automatic calibration, systematic error cancellation, window margin testing, and error recovery. The SSI 32D535 requires a single +5V power supply and is available in a 32-pin SOW, DIP & 28-pin PLCC package.

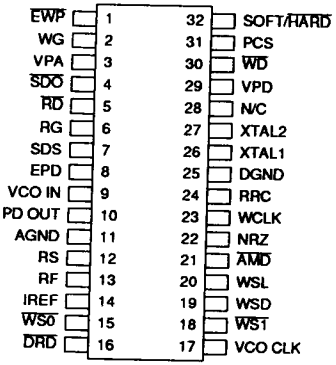
FEATURES

- **Data Synchronizer and 2, 7 RLL ENDEC**
- **Write Precompensation**
- **7.5 to 10 Mbit/s Programmed with a Single External Resistor or Current Source**
- **Optimized for Operation with the SSI 32C452A and AIC 010 Controllers**
- **ESDI compatible**
- **Programmable Decode Window Symmetry via a µP Port and/or Analog Pins**
- **Fast Acquisition Phase Locked Loop**
  - **Zero Phase Restart Technique**
- **Input Clock Circuitry Optimized for use with Crystal Controlled Reference Oscillator**
- **Hard/Soft Sector Operation**
- **+5V Operation**
- **32-Pin SOW & 28-Pin PLCC**

BLOCK DIAGRAM



PIN DIAGRAM



1191 - rev.

CAUTION: Use handling procedures necessary for a static sensitive component.

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PIN DESCRIPTION

INPUT PINS

NAME	TYPE	DESCRIPTION
$\overline{RD}$	I	READ DATA: Encoded Read Data from the disk drive read channel, active low.
RG	I	READ GATE: Selects the PLL reference input and initiates the PLL synchronization sequence. A high level selects the $\overline{RD}$ input and enables the Read Mode/Address Mark Detection sequences. A low level selects the crystal reference oscillator. Pin RG has an internal resistor pull-up.
WG	I	WRITE GATE: Enables the write mode. Pin WG has an internal resistor pull-up. If unused, tie pin low.
WSL	I	WINDOW SYMMETRY LATCH: Used to latch the input window symmetry control bits WSD, $\overline{WS0}$ and $\overline{WS1}$ into the internal DAC. An active high level latches the input bits. Pin WSL has an internal resistor pull-up. If unused, tie pin low.
WSD	I	WINDOW SYMMETRY DIRECTION: Controls the direction of the optional window symmetry shift. Pin WSD has an internal resistor pull-up.
$\overline{WS0}$	I	WINDOW SYMMETRY CONTROL BIT: A low level introduces a window shift of 1.5% TORC (Read Reference Clock Period) in the direction established by WSD. Pin $\overline{WS0}$ has an internal resistor pull-up. If unused, leave open or tie high.
$\overline{WS1}$	I	WINDOW SYMMETRY CONTROL BIT: A low level introduces a window shift of 6% TORC (Read Reference Clock Period) in the direction established by WSD. A low level at both $\overline{WS0}$ and $\overline{WS1}$ will produce the sum of the two window shifts. Pin $\overline{WS1}$ has an internal resistor pull-up. If unused, leave open or tie high.
SOFT/$\overline{HARD}$	I	SOFT/$\overline{HARD}$ SECTOR: Selects the address mark and the Preamble field patterns. A high level (Soft Sector) selects a 3T Preamble Field pattern and a non-violating 2, 7 address mark, N7V. A low level (Hard Sector) selects a 4T Preamble Field pattern and disables the address mark circuitry. Pin SOFT/$\overline{HARD}$ has an internal resistor pull-up.
WCLK	I	WRITE CLOCK: Write Clock input. Must be synchronous with the Write Data input on the NRZ Data Port. For small cable delays, WCLK may be connected directly to pin RRC (Read/Reference Clock).
EPD	I	ENABLE PHASE DETECTOR: A low level (Coast Mode) disables the phase detector and allows the VCO to coast. Pin EPD has an internal resistor pull up.
$\overline{EWP}$	I	ENABLE WRITE PRECOMPENSATION: A low level enables Write Precompensation. Pin $\overline{EWP}$ has an internal resistor pull-up.

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PIN DESCRIPTION (Continued)

OUTPUT PINS

NAME	TYPE	DESCRIPTION
$\overline{WD}$	O	WRITE DATA: Encoded write data output, active low.
RRC	O	READ/REFERENCE CLOCK: A multiplexed clock source used by the controller. In the read mode, this clock is the VCO frequency divided by two (1/TORC) and in the write mode it is the crystal reference frequency divided by two (1/TORO). No short clock pulses are generated during a mode change.
$\overline{AMD}$	O	ADDRESS MARK DETECT: In the soft sector Read Mode, a latched low level output indicates that an address mark has been detected. In non-Read modes $\overline{AMD}$ is configured as a high impedance output.
$\overline{SDO}$	O	SYNC DETECT OUTPUT: An active low output that indicates successful detection of the 3T Preamble sync field. THE $\overline{SDO}$ pin is not a TTL level signal.
VCO CLK	O	VCO CLK: An open emitter VCO clock test point. Two external resistors are required to utilize this output, they can be removed during normal operaton for reduced power dissipation.
$\overline{DRD}$	O	DELAYED READ DATA: Test point. The positive edges of this open emitter output signal indicate the data bit position. The positive edges of the $\overline{DRD}$ and the VCO CLK signals can be used to estimate window centering. The time jitter of $\overline{DRD}$'s positive edge is an indication of media bit shift. Two external resistors are required to perform this test, they can be removed during normal operation for reduced power dissipation.

BIDIRECTIONAL PINS

NRZ	I/O	NRZ DATA PORT: Read Data output when RG is high and Write Data input when WG is high. In the idle mode NRZ is in a high impedance state.

ANALOG PINS

IREF	I	TIMING PROGRAM PIN: The VCO center frequency and the 1/4 Cell Delay are a function of the current sourced into pin IREF. The current is set by an external resistor, RR, connected from IREF to VPA.
PCS	I	PRECOMP SET: Used to set the magnitude of the Write Precompensation time shift via an external capacitor, Cp to VPA and an external resistor, Rp to AGND.
XTAL1, XTAL2	I	CRYSTAL OSCILLATOR CONNECTIONS: The frequency must be at twice the data rate.
PD OUT	O	PHASE DETECTOR OUTPUT: Drives the Loop Filter input.
VCO IN	I	VCO CONTROL INPUT: Driven by the Loop Filter output.

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PIN DESCRIPTION (Continued)

OUTPUT PINS (Continued)

NAME	TYPE	DESCRIPTION
SDS	I	SYNC DETECT SET: Used to program the sync detect retriggerable one-shot timing with an external R-C network. Connect the capacitor, Cd, to VPA and the resistor, Rd, to AGND.
RF, RS	I	WINDOW SYMMETRY ADJUST PINS: Provides analog control over the decode window symmetry; typically used to null out any window symmetry offset. A resistor connected from either RF or RS to AGND will provide magnitude and direction control. They can be used in conjunction with the digital control port WSD, $\overline{WS0}$, $\overline{WS1}$.

POWER

DGND, AGND	I	DIGITAL AND ANALOG GROUND
VPA	I	ANALOG +5V
VPD	I	DIGITAL +5V

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OPERATION

The SSI 32D535 is designed to perform data recovery and data encoding in rotating memory systems which utilize a 2, 7 RLL encoding format. In the Read Mode the SSI 32D535 performs Data Synchronization, Sync Field Search and Detect, Address Mark Detect and Data Decoding. In the Write Mode, the SSI 32D535 converts NRZ data into the 2,7 RLL format described in Table 1, performs write precompensation, generates the Preamble Field, and inserts Address Marks as requested. The interface electronics and architecture of the SSI 32D535 have been optimized for use as a companion device to the SSI 32C452 or AIC 010 controllers.

The SSI 32D535 can operate with data rates ranging from 7.5 to 10 Mbit/s operation. This data rate is established by a single 1% external resistor, RR, connected from pin IREF to VPA. This resistor establishes a reference current which sets the VCO center frequency, the phase detector gain, and the 1/4 cell delay. The value of this resistor is given by:

$$RR = \frac{40.67}{DR} - 0.5\ (k\Omega)$$

where: DR = Data Rate in Mbit/s.

An internal crystal reference oscillator, operating at twice the data rate, generates the standby reference for the PLL. A series resonant crystal between XTAL1 and XTAL2 should be selected at twice the Data Rate.

The SSI 32D535 employs a Dual Mode Phase Detector; Harmonic in the Read Mode and Non-Harmonic in Write and Idle Modes. In the Read Mode the Harmonic Phase Detector updates the PLL with each occurrence of a DLYD DATA pulse. In the Write and Idle Modes the Non-Harmonic Phase Detector is continuously enabled, thus maintaining both phase and frequency lock. By acquiring both phase and frequency lock to the crystal reference oscillator and utilizing a zero phase restart technique, false lock to DLYD DATA is eliminated.

The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error. Figure 1 depicts the average output current as a function of the input phase error (relative to the VCO period).

The READ GATE (RG), and WRITE GATE (WG), inputs control the device mode as described in Table 2. RG is an asynchronous input and may be initiated or terminated at any position on the disk. WG is also an asynchronous input, but should not be terminated prior to the last output Write Data pulse.

READ OPERATION

The Data Synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the decode window. Read Gate, RG, initiates the PLL locking sequence and selects the PLL reference input; a high level (Read Mode) selects the $\overline{RD}$ input and a low level selects the crystal reference oscillator.

In the Read Mode the rising edge of DLYD DATA enables the Phase Detector while the falling edge is phase compared to the rising edge of the VCO. As depicted in Figure 2, DLYD DATA is a 1/4 cell wide (TVCO/2) pulse whose leading edge is defined by the leading edge of $\overline{RD}$. An accurate and symmetrical decode window is developed from the VCO clock. The decode window is generated from the falling edges of the VCO clock. By utilizing a fully integrated symmetrical VCO running at twice the data rate, the decode window is insured to be accurate and centered symmetrically about the falling edges of DLYD DATA. The accuracy of the 1/4 cell delay only affects the retrace angle of the phase detector and does not influence the accuracy of the decode window.

Shifting the symmetry of the VCO clock effectively shifts the relative position of the DLYD DATA pulse within the decode window. This powerful capability easily facilitates defect mappings, automatic calibration, window margin testing, error recovery, and systematic error cancellation. For enhanced disk drive testability and error recovery, decode window control is provided via a µP port (WSL, WSD, $\overline{WS0}$, $\overline{WS1}$) as described in Table 3. In applications not utilizing this feature, WSL must be connected to ground, while WSD, $\overline{WS0}$, and $\overline{WS1}$ must be left open.

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Window shifts in the range of ±1.5% to ±7.5% of TORC are easily programmed by latching the appropriate control word into the Window Shift Register with the WSL pin. Shifts in the positive or negative directions result in early or late decode windows respectively, as depicted in Figure 3. Additionally, for small systematic error cancellation, a resistor, R, connected from either RS (Early) or RF (Late) to ground will provide analog control over the decode window. The magnitude of this shift, TSA is determined by:

$$TSA = 0.125\ TORC\left(1 - \frac{680 + R}{1180 + R}\right)$$

where: R is in ohms

Pins RF and RS are intended to be used as a trim and should be restricted to ±1.5% window shifts. They can be used in conjunction with the digital control port.

The VCO CLK and $\overline{DRD}$ outputs can be used to estimate window centering and data bit shift. The rising edges of VCO CLK indicate the data detection window edges. The rising edge of $\overline{DRD}$ indicates the data bit position relative to the decode window. Two external resistors are required during such testing. A pull-up resistor of 130Ω should be connected to VPD, while a pull-down resistor of 200Ω should be connected to DGND. The resistors can be removed during normal operation to reduce power dissipation.

In Non-Read Modes, the PLL is locked to the crystal reference oscillator. This forces the VCO to run at a frequency which is very close to that required for tracking actual data and thus minimizes the associated frequency step during acquisition. When the reference input to the PLL is switched, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse, and the VCO clock divider is reset. By minimizing the phase alignment in this manner (phase error ≤ 0.5 rads), the acquisition time is substantially reduced.

The SSI 32D535 provides two sync modes for controlling the PLL locking sequence; Soft Sector and Hard Sector.

SOFT SECTOR MODE

The Soft Sector Mode activates the Preamble Search and Address Mark detection circuitry. As depicted in Figure 4, when RG transitions high, the counter is reset and the SSI 32D535 requires 10 high to low transitions (Preamble '1' bits) before switching the reference input to the PLL, 48 high to low transitions before switching the Read Reference Clock to the VCO clock divided by two and activating the Address Mark Detect circuitry; then it must detect the Address Mark prior to 80 high to low transitions in order to enter the Read Mode. This sequence repeats after 95 input '1' bits until the read mode is successfully entered or until RG is cancelled.

When RG transitions high, the following PLL locking sequence begins:

a) PREAMBLE SEARCH:

The 3T detect circuitry initiates the PLL locking sequence once it has detected 10 consecutive '100' bit groups from the 3T preamble field. The 3T detect timing is set by the sum of the 1/4 cell delay and the retriggerable one-shot delay. The 1/4 cell timing capacitor is included on-chip and its timing is externally set by resistor RR. The retriggerable one-shot timing is externally set by resistor Rd and capacitor Cd. The sum of their delays is set to 3.5 bit cell times. Therefore, a continuous stream of input pulses with a 3T bit cell time pulse rate keeps the one-shot reset, and a 4T or longer bit cell time input period allows the one-shot to time out producing a 4T detect pulse. The 4T detect pulse resets the Input Counter and the search is started over.

b) PLL ACQUISITION:

Once 10 consecutive '100' bit groups are detected, the reference input to the PLL is switched from the crystal reference oscillator to the DLYD DATA, the VCO is phase reset to the next DLYD DATA pulse, and PLL acquisition begins. When an additional 38 '100' bit groups are detected, the Read Reference Clock output (RRC) is switched to the VCO clock divided by 2, the 4T Detect circuitry is inhibited, and the Address Mark Detection circuitry is enabled. If a 4T detect pulse occurs before 48 Preamble '1' bits are detected, then the PLL is locked back to the crystal reference oscillator, the RRC output is switched to the crystal reference oscillator divided by 2, the

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Input Counter reset, and the sequence is restarted. No short duration glitches will occur at the RRC output during this switching.

c) **ADDRESS MARK DETECTION:**

The circuit searches for the occurrence of the $5EAx_{16}$ Address Mark. If an Address Mark is detected prior to the Input Counter reaching count 80, the correct phase of the RRC is ensured by resetting the n/2 divider, the $\overline{AMD}$ output is latched low, the PLL training sequence is terminated, and the Read Mode is entered allowing the data field to be read. If the Input Counter reaches count 80 before the Address Mark is detected, the PLL is locked back to the crystal reference oscillator, the RRC output is switched to the crystal reference oscillator divided by 2, and the PLL training sequence is restarted when the Input Counter reaches count 96. Figure 5 depicts the Address Mark detection sequence.

HARD SECTOR MODE

In the Hard Sector mode (SOFT/$\overline{HARD}$ = 0) the SSI 32D535 utilizes a 4T (1000) Preamble Field and disables the Preamble Search and Address Mark detection circuitry. It allows the PLL to be controlled directly by RG for Hard Sector format operation. With the absence of an Address Mark, the 4T Preamble Field is utilized to properly set the bit cell alignment boundaries for proper decoding.

When RG transitions high, as depicted in Figure 6, reference input to the PLL is switched from the crystal reference oscillator to DLYD DATA, the VCO is phase reset to the next DLYD DATA pulse, and the PLL acquisition begins. When 32 '1' Preamble bits are detected, the RRC output is switched to the VCO clock divided by 2, and the Read Mode is entered allowing the data field to be read.

In the Hard Sector mode, the NRZ output is inverted and will remain low until the data field is read, as shown in Figure 7. Since the Preamble Search circuitry is not utilized, the external one-shot timing components (Cd, Rd) are not required and the SDS pin can be left open.

WRITE OPERATION

In the Write Mode the SSI 32D535 converts NRZ data from the controller into 2, 7 RLL formatted data for storage onto the disk. The SSI 32D535 can operate with a soft or hard sectored disk drive. In the Soft Sector Mode, (SOFT/$\overline{HARD}$ = 1) the device generates a 3T Preamble Field and can insert a N7V Address Mark. The N7V Address Mark is a valid 2, 7 RLL pattern which is not contained in the code set. In the Hard Sector Mode, (SOFT/$\overline{HARD}$ = 0) the device generates a 4T Preamble Field and no Address Mark. Serial NRZ data is clocked into the SSI 32D535 and latched on defined cell boundaries. The NRZ input data must be synchronous with the rising edges of the WCLK input. The WCLK input is a feature provided for operation in an ESDI application to compensate for large cable delays. In a SCSI or ST506 operation, WCLK is connected directly to the RRC output.

Write precompensation circuitry is provided to compensate for media bit shift caused by intersymbol interference. The SSI 32D535 recognizes specific write data patterns and can add or subtract delays in the time position of write data bits to counteract the read back bit shift. The magnitude of the time shift, TC, is determined by an external R-C network on the PCS pin given by:

$$TC = 0.15\ (Rp)(Cp + Cs)$$

with $RP \geq 2.0\ k\Omega$, Cs = stray capacitance

When the ENABLE WRITE PRECOMP, $\overline{EWP}$, input is low the SSI 32D535 performs write precompensation according to the algorithm outlined in Table 4.

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SOFT SECTOR MODE

In the Soft Sector Mode, when WRITE GATE (WG), transitions high and the NRZ input is held low, the SSI 32D535 automatically generates the 3T (100) Preamble Field at the WRITE DATA ($\overline{WD}$), output. The 3T Preamble Field will continue to be generated until the first low to high transition on the NRZ line. As shown in Figure 8, the first low to high transition occurs with the second bit '1' of the 5_{16} (0101) in the $5EAx_{16}$ Address Mark generation pattern. To generate the Address Mark, the SSI 32D535 automatically changes the '1' in the eleventh position (see note 3) of the 2, 7 RLL encoded sequence, to a '0'. This generates a pattern of seven zeros followed by two zeros. This unique pattern satisfies the 2, 7 RLL constraints, but will never occur during a normal encoding sequence. The x_{16} of the $5EAx_{16}$ Address Mark generation pattern can be selected, a 'C_{16}' (1100) was utilized in this example.

HARD SECTOR MODE

In the Hard Sector Mode, when WG goes high and the NRZ input is held low, the SSI 32D535 automatically generates the 4T (1000) Preamble Field at the WRITE DATA, $\overline{WD}$, output. Note that in the Hard Sector mode, the NRZ input is inverted, therefore a constant low is equivalent to an '11 . . .' input which generates the 4T '1000 . . . ' Preamble Field. The 4T Preamble Field will be generated between the time WG goes high and the first low to high transition on the NRZ line. The 32D535 requires a minimum of 32 4T (1000) bit groups prior to the data field.

NRZ	2, 7 RLL
10	0100
11	1000
000	000100
010	100100
011	001000
0010	00100100
0011	00001000

TABLE 1: 2, 7 RLL Code Set

WG	RG	MODE
0	0	IDLE
0	1	READ
1	0	WRITE
1	1	ILLEGAL

TABLE 2: Mode Control

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Ts, NOMINAL WINDOW SHIFT	WSD	$\overline{WS1}$	$\overline{WS0}$
+TS3	0	0	0
+TS2	0	0	1
+TS1	0	1	0
0	0	1	1
-TS3	1	0	0
-TS2	1	0	1
-TS1	1	1	0
0	1	1	1

TABLE 3 : Decode Window Symmetry Control

ENCODED 2, 7 RLL DATA PATTERN							
BIT n - 3	BIT n - 2	BIT n - 1	BIT n	BIT n + 1	BIT n + 2	BIT n + 3	COMPENSATION BIT n
0	0	0	1	0	0	0	none
1	0	0	1	0	0	1	none
1	0	0	1	0	0	0	early
0	0	0	1	0	0	1	late

TABLE 4 : Write Precompensation Algorithm

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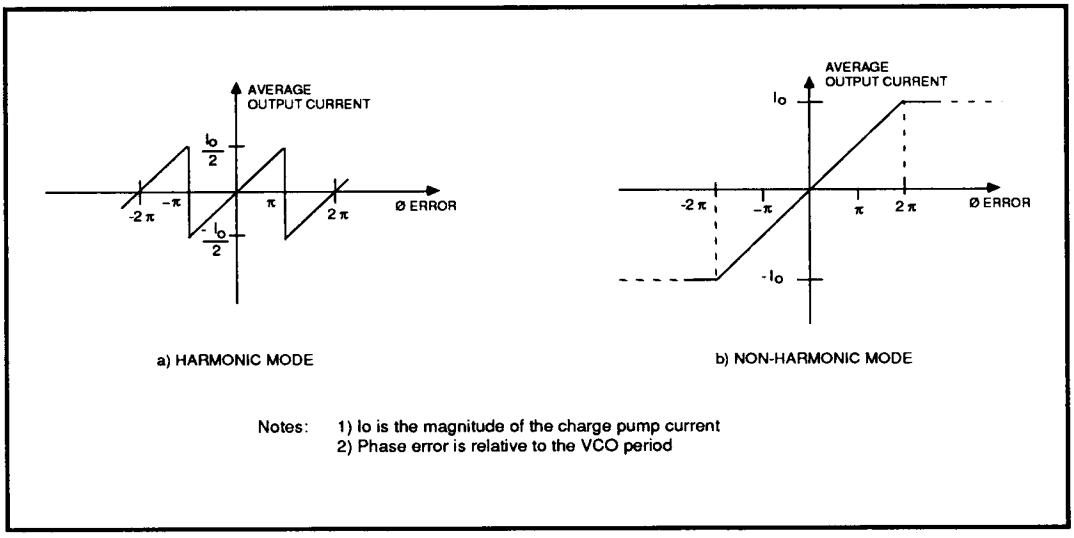

FIGURE 1: Phase Detector Transfer Function

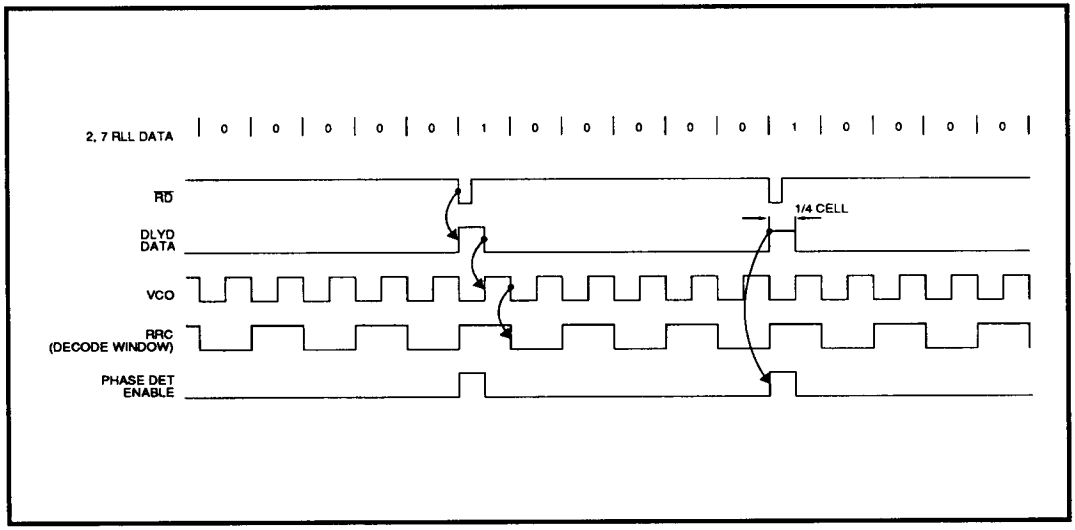

FIGURE 2: Data Synchronization Waveform Diagram

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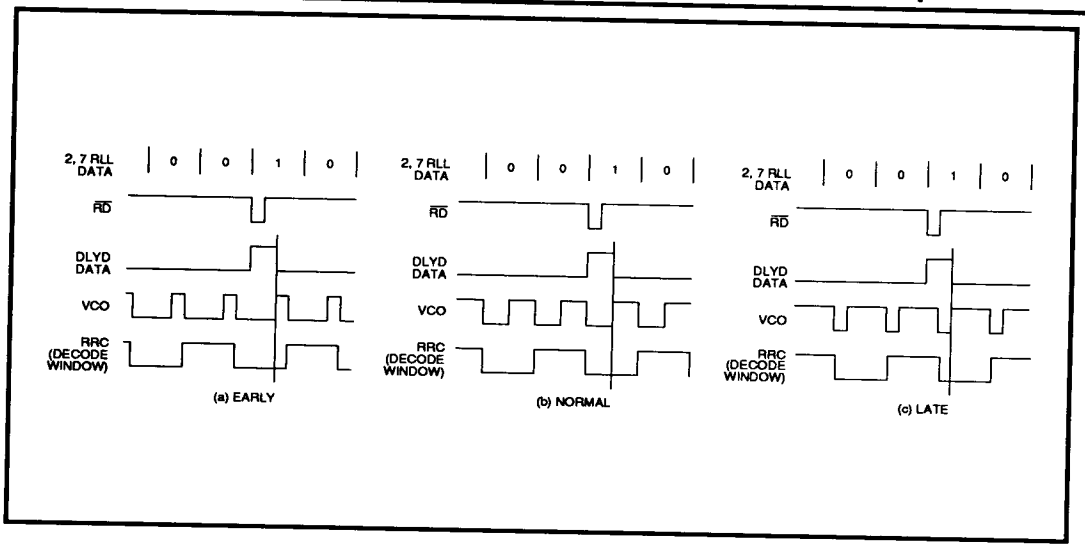

FIGURE 3: Decode Window

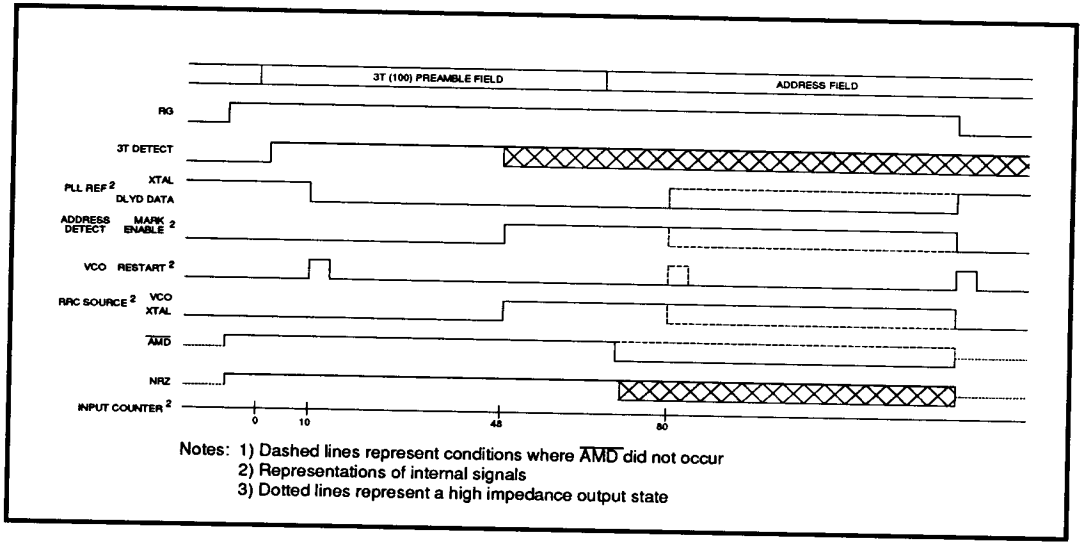

FIGURE 4: Soft Sector Mode Timing Diagram

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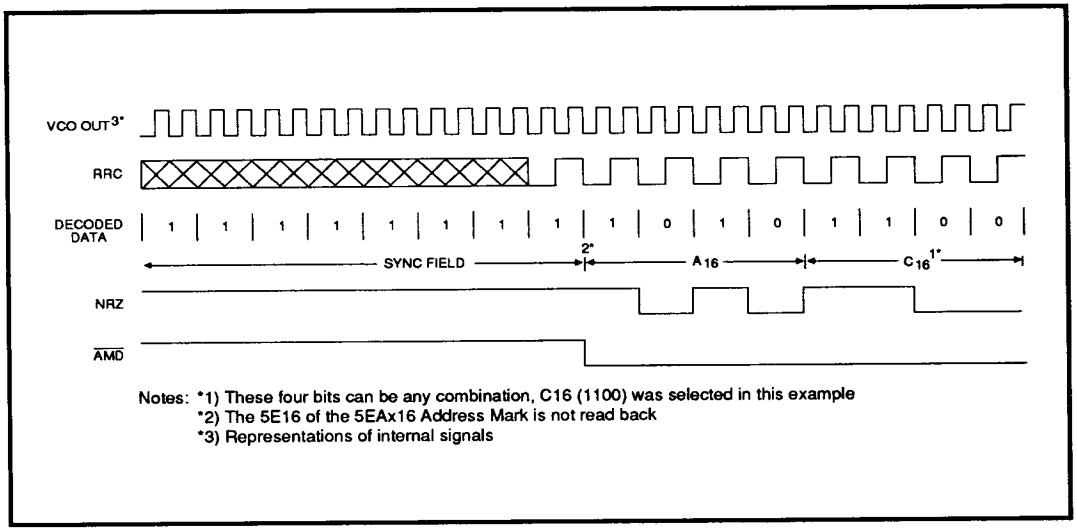
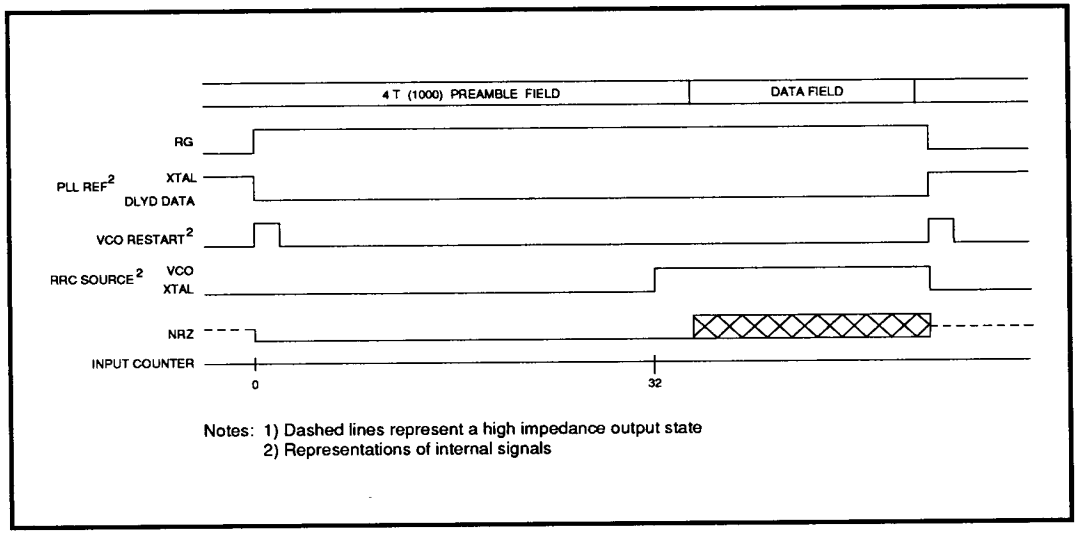


Notes: *1) These four bits can be any combination, C16 (1100) was selected in this example
*2) The 5E16 of the 5EAx16 Address Mark is not read back
*3) Representations of internal signals

FIGURE 5: Address Mark Detection and NRZ Output Waveform



Notes: 1) Dashed lines represent a high impedance output state
2) Representations of internal signals

FIGURE 6: Hard Sector Mode Timing Diagram

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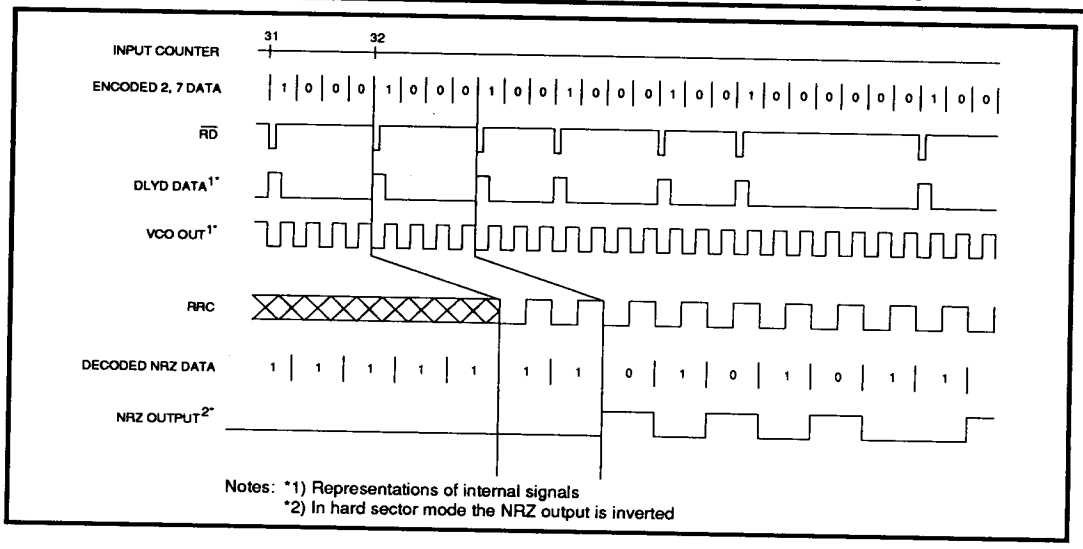

FIGURE 7: Hard Sector Mode Decode Timing

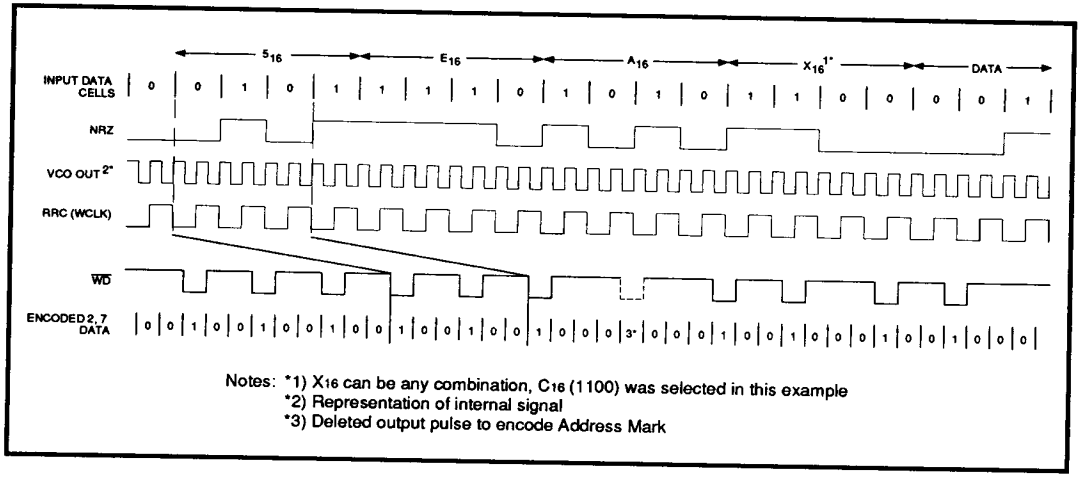

FIGURE 8: Write Address Mark Generation

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ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may permanently damage the device.

PARAMETER	RATINGS	UNIT
Storage Temperature	-65 to +150	° C
Ambient Operating Temperature, Ta	0 to +70	° C
Junction Operating Temperature, Tj	0 to +130	° C
Supply Voltage, VCC	-0.5 to 7	Vdc
Voltage Applied to Logic inputs	-0.5 to VCC +0.5	Vdc
Maximum Power Dissipation	950	mW

DC ELECTRICAL CHARACTERISTICS - unless otherwise specified, 4.75V < VCC < 5.25V, Ta = 0°C to 70°C, 7.5 MHz < 1/TORC < 10 MHz, 15 MHz < 1/TVCO < 20 MHz

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TTL Inputs:					
VIH, High Level Input Voltage		2.0			V
VIL, Low Level Input Voltage				0.8	V
IIH, High Level Input Current	VIH = 2.7V			20	µA
IIL, Low Level Input Current	VIL = 0.4V			-0.36	mA
TTL Outputs:					
VOH, High Level Output Voltage	IOH = -400 µA	2.4			V
VOL, Low Level Output Voltage	IOL = 4 mA			0.5	V
Test Point Outputs: $\overline{DRD}$, VCO CLK (See Figure 12)					
VOH, High Level Ouput Voltage	RL= 130Ω to VPD, 200Ω to DGND		VPD-1.0		V
VOL, Low Level Output Voltage	RL= 130Ω to VPD, 200Ω to DGND		VPD-1.75		V
ICC, Power Supply Current	All outputs open			180	mA

DYNAMIC CHARACTERISTICS AND TIMING

READ MODE (See Figure 9)

TRD, Read Data Pulse Width		20		TORC-40	ns
TFRD, Read Data Fall Time	2.0V to 0.8V, CL ≤ 15 pF			15	ns
TRRC, Read Clock Rise Time	0.8V to 2.0V, CL ≤ 15 pF			8	ns
TFRC, Read Clock Fall Time	2.0V to 0.8V, CL ≤ 15 pF			5	ns

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READ MODE (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TPNRZ, NRZ (out) Propagation Delay		-15		15	ns
TPAMD, $\overline{AMD}$ Propagation Delay		-15		15	ns
1/4 Cell + Retriggerable One-Shot Delay Stability	4.5V < VCC < 5.5V	-4		+4	%
1/4 Cell + Retriggerable One-Shot Delay*	TD = 6.14(RR +0.5) + 0.172 Rd (Cd +Cs)** RR = kΩ Rd = kΩ Cd = 68 pF to 100 pF	0.89 TD		1.11 TD	ns

* Excludes External Capacitor and Resistor Tolerances **Cs = Stray Capacitance

WRITE MODE (See Figure 10)

PARAMETER	CONDITIONS	MIN	MAX	UNIT
TWD, Write Data Pulse Width	CL ≤15 pF	(TOWC/2)-12-1.4TC	(TOWC/2) +12	ns
TFWD, Write Data Fall Time	2.0V to 0.8V, CL ≤ 15 pF		8	ns
TRWC Write Data Clock Rise Time	0.8V to 2.0V		10	ns
TFWC Write Data Clock Fall Time	2.0V to 0.8V		8	ns
TSNRZ, NRZ (in) Set Up Time		20		ns
THNRZ, NRZ (in) Hold Time		7		ns
TWDC Compensated Write Data Pulse Width	CL ≤ 15 pF	(TOWC/2)-2.4TC-12		ns
TE, TL Write Data Compensation Accuracy	TC = 0.15(Rp)(Cp + Cs) 2 kΩ ≤ Rp ≤ 3 kΩ, Cs = Stray Capacitance Cp = 15 pF to 36 pF	0.8 TC	1.2 TC	ns

DATA SYNCHRONIZATION

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TVCO VCO Center Frequency Period	VCO IN = 2.7V TO = 1.23E - 11(RR +500) VCC = 5.0V	0.8 TO		1.2 TO	sec

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DATA SYNCHRONIZATION (Cont.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VCO Frequency Dynamic Range		1.0V ≤ VCO IN ≤ VCC -0.6V VCC = 5.0V	±24		±40	%
KVCO	VCO Control Gain	ωo = 2π / TO 1.0V ≤ VCO IN ≤ VCC -0.6V	0.14 ωo		0.20 ωo	rad/s-V
KD	Phase Detector Gain	KD = 0.309 / (RR + 500) VCC = 5.0V	0.83 KD		1.17 KD	A/rad
*	KVCO x KD Product Accuracy		-28		+28	%
*	VCO Phase Restart Error			6		ns
	Decode Window Centering Accuracy				± (0.01 TORC + 2)	ns
	Decode Window		(TORC/2) -2			ns
TS1	Decode Window Time Shift Magnitude	TS1 = 0.015 TORC		TS1		sec
TS2	Decode Window Time Shift Magnitude	TS2 = 0.06 TORC		TS2		sec
TS3	Decode Window Time Shift Magnitude	TS3 = 0.075 TORC		TS3		sec
TSA	Decode Window Time Shift Magnitude	$TSA = 0.125\ TORC\left(1 - \frac{680 + R}{1180 + R}\right)$ with: R in ohms		TSA		sec

* Not directlly testable – Design Characteristics

CONTROL CHARACTERISTICS (See figure 11)

TSWS, $\overline{WS0}$, $\overline{WS1}$, WSD Set Up Time		50			ns
THWS, $\overline{WS0}$, $\overline{WS1}$, WSD Hold Time		0			ns
RG, WG, SOFT/$\overline{HARD}$ Time Delay				100	ns

REFERENCE CLOCK CHARACTERISTICS

TXPW, Crystal Input Pulse Width	Min. Negative Pulse Width	19.23			ns
(Reference Oscillator See Figure 10)	Min. Positive Pulse Width	16			ns

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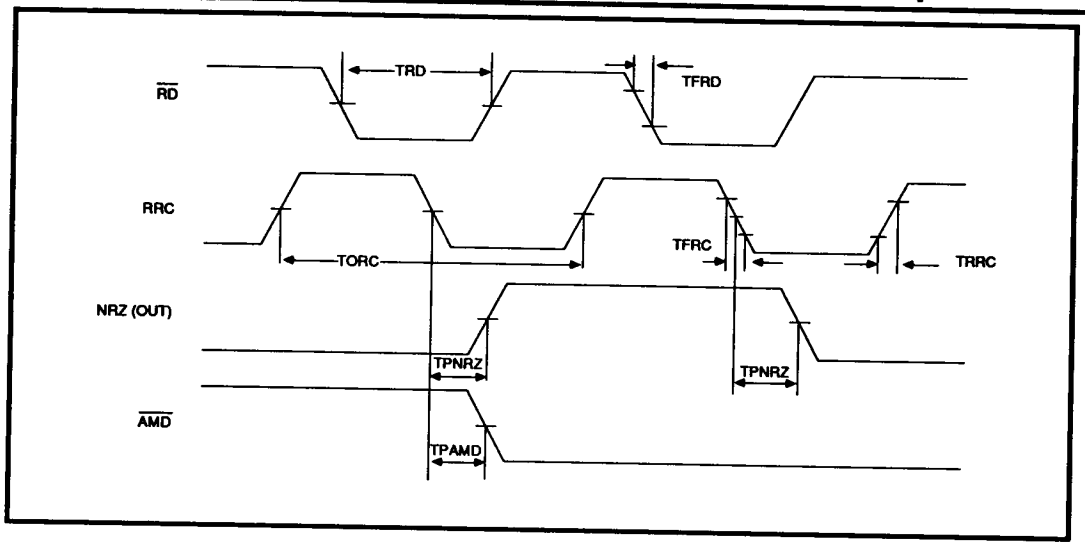

FIGURE 9: Read Timing

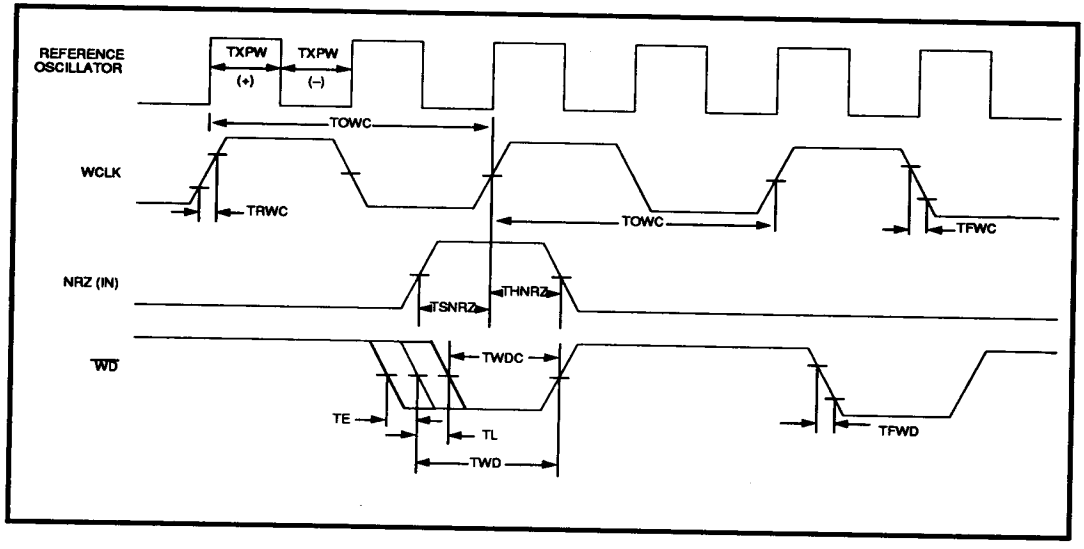

FIGURE 10: Write Timing

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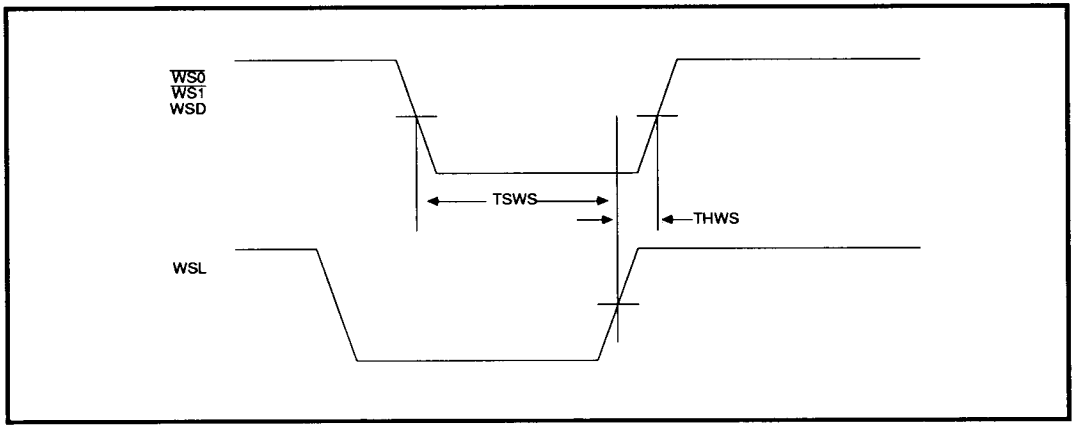

FIGURE 11: Control Timing

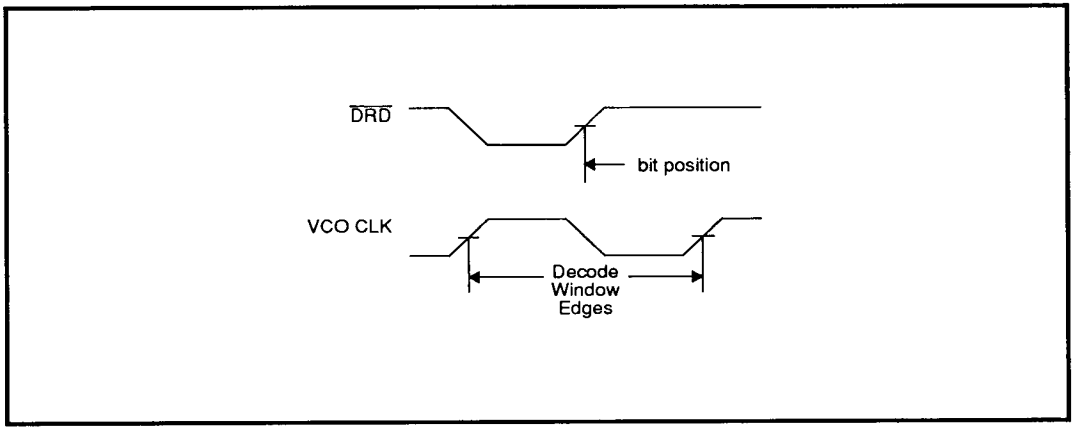

FIGURE 12: Test Point Timing

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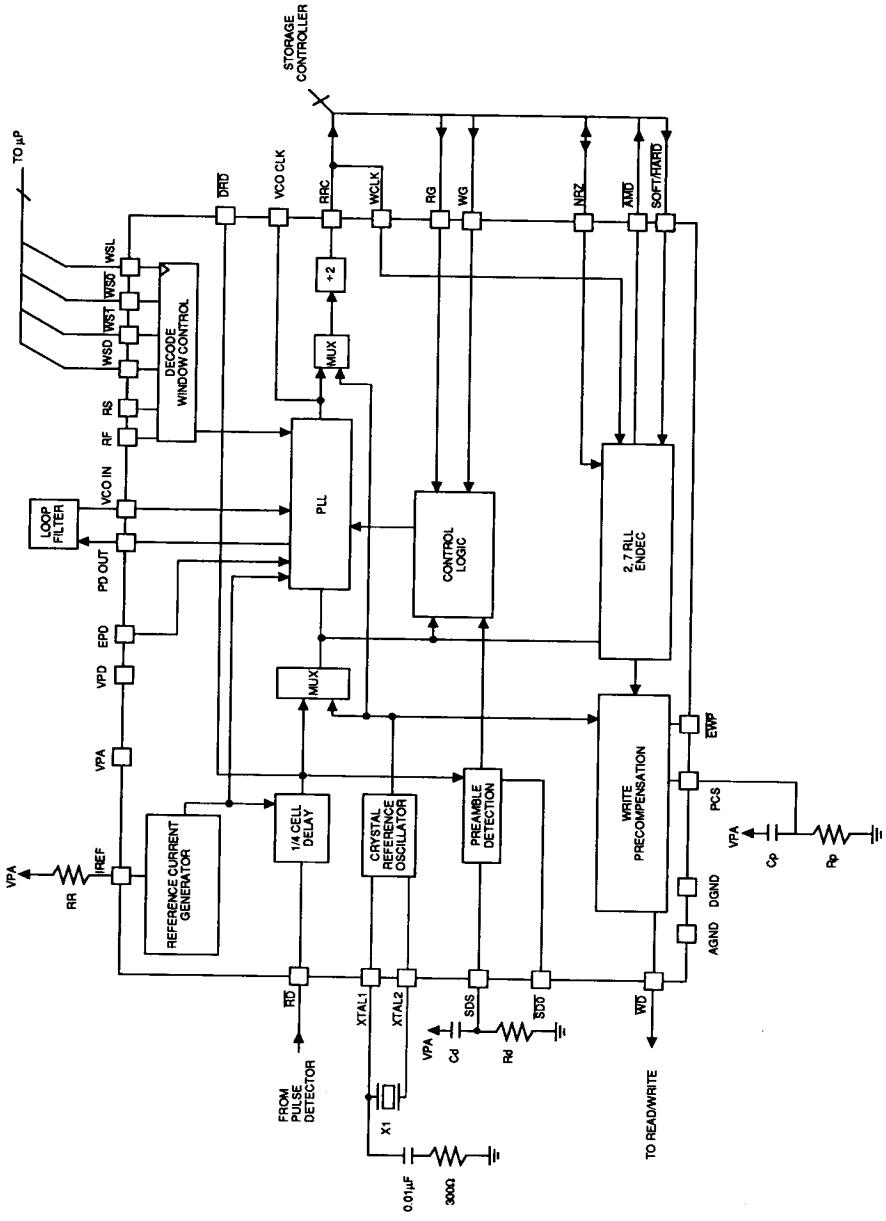

FIGURE 13: Typical SSI 32D535 Application

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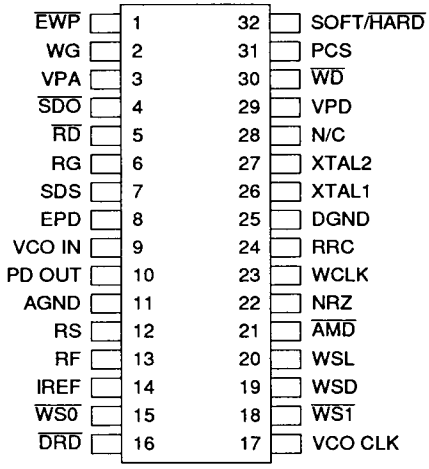
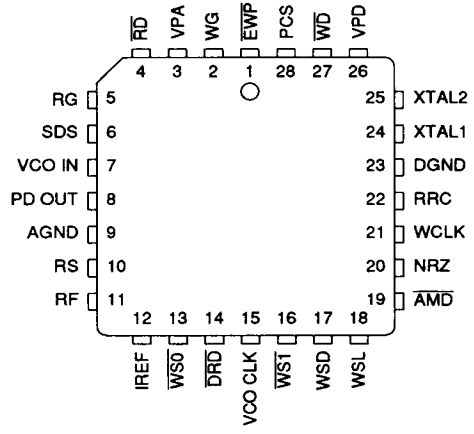
SSI 32D535
Data Synchronizer/ 2, 7 RLL ENDEC with Write Precompensation

PACKAGE PIN DESIGNATIONS

(Top View)



32-Lead SOW



28-Pin PLCC

Note: This package is bonded out for soft sector applications only. (SOFT/HARD) pin internally pulled up). SDO and EPD are not available in this package.

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32D535 32-Pin Small Outline - Wide	32D535 - CW	32D535 - CW
SSI 32D535 28-Pin PLCC	32D535 - CH	32D535 - CH

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