5. AC/DC Specification :

This section gives the AC and DC specification for R4762.

5.1. AC Specification :

Signal	T_{val}	T_{hold}	$T_{clk->Q}$
HOST BUS :			
SYSAD	2.0 - 3.5 ns	2.0 - 3.5 ns	12.15 - 6.03
SYSCMD	2.0 - 3.5 ns	2.0 - 3.5 ns	11.53 - 5.80
SYSADC	2.0 - 3.5 ns	2.0 - 3.5 ns	13.27 - 6.27
SYSCMDP	2.0 - 3.5 ns	2.0 - 3.5 ns	11.13 - 5.21
VALIDOUT	2.0 - 3.5 ns	2.0 - 3.5 ns	-
VALID_IN2nn	2.0 - 3.5 ns	2.0 - 3.5 ns	-
VALID_OUT2nn	2.0 - 3.5 ns	2.0 - 3.5 ns	11.36 - 5.80
BUSYnn	2.0 - 3.5 ns	2.0 - 3.5 ns	10.99 - 5.62
BUSREQnn	2.0 - 3.5 ns	2.0 - 3.5 ns	13.15 - 6.64
BUSACKnn	2.0 - 3.5 ns	2.0 - 3.5 ns	-
PCI BUS :	2.0 - 3.5 ns	2.0 - 3.5 ns	-
AD	7.0 ns	0 ns	11.0 - 6.5ns
CBEnn	7.0 ns	0 ns	11.0 - 6.5ns
FRAMEnn	7.0 ns	0 ns	11.0 - 6.5ns
DEVSELnn	7.0 ns	0 ns	11.0 - 6.5ns
IRDYnn	7.0 ns	0 ns	11.0 - 6.5ns
TRDYnn	7.0 ns	0 ns	11.0 - 6.5ns
STOPnn	7.0 ns	0 ns	11.0 - 6.5ns
PERRnn	7.0 ns	0 ns	11.0 - 6.5ns
SERRnn	7.0 ns	0 ns	11.0 - 6.5ns
PAR	7.0 ns	0 ns	11.0 - 6.5ns
IDSEL	7.0 ns	0 ns	-
LOCKnn	7.0 ns	0 ns	-
R4762_REQnn	7.0 ns	0 ns	11.0 - 6.5ns
R4762_GNTnn	7.0 ns	0 ns	11.0 - 6.5ns
REQ[4:0]	7.0 ns	0 ns	11.0 - 6.5ns
GNT[4:0]	7.0 ns	0 ns	11.0 - 6.5ns

5.2. DC Specification :

Signal	DC Drive Capability
SYSAD, SYSCMD, SYSCMDP, SYSADC	8 mA, CMOS 3-state Output
VALID_OUT2nn, BUSYnn	8mA, CMOS Output

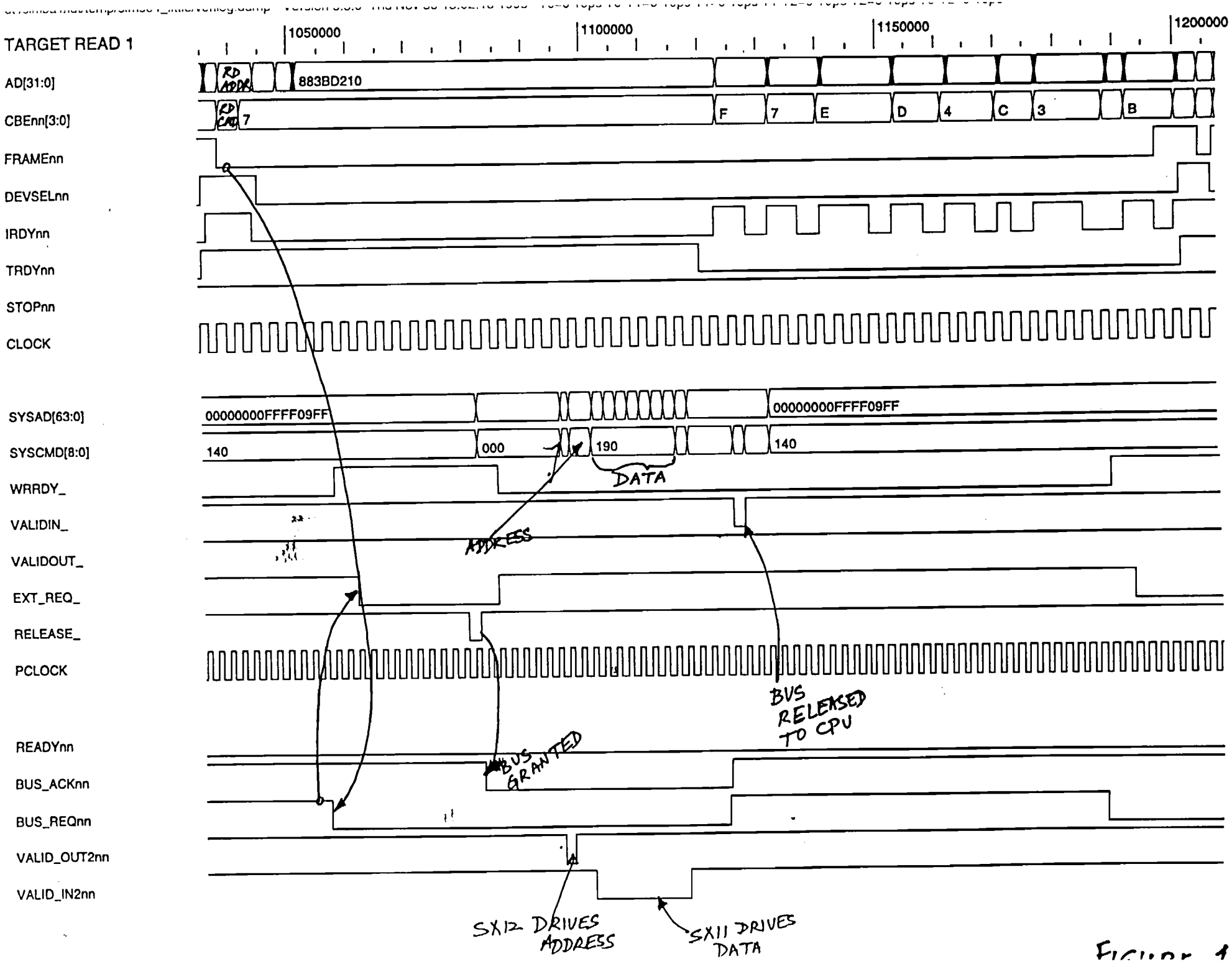
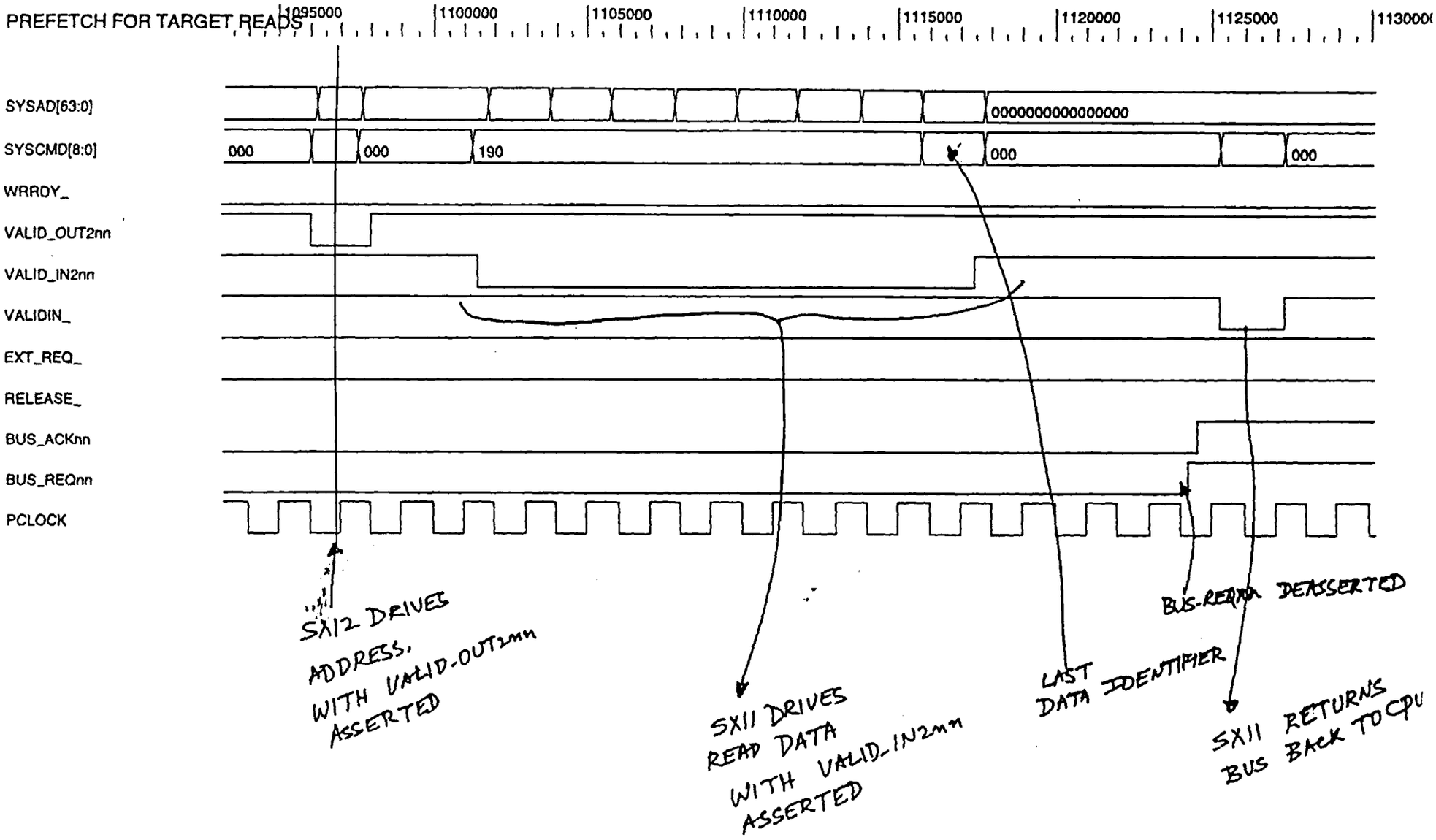
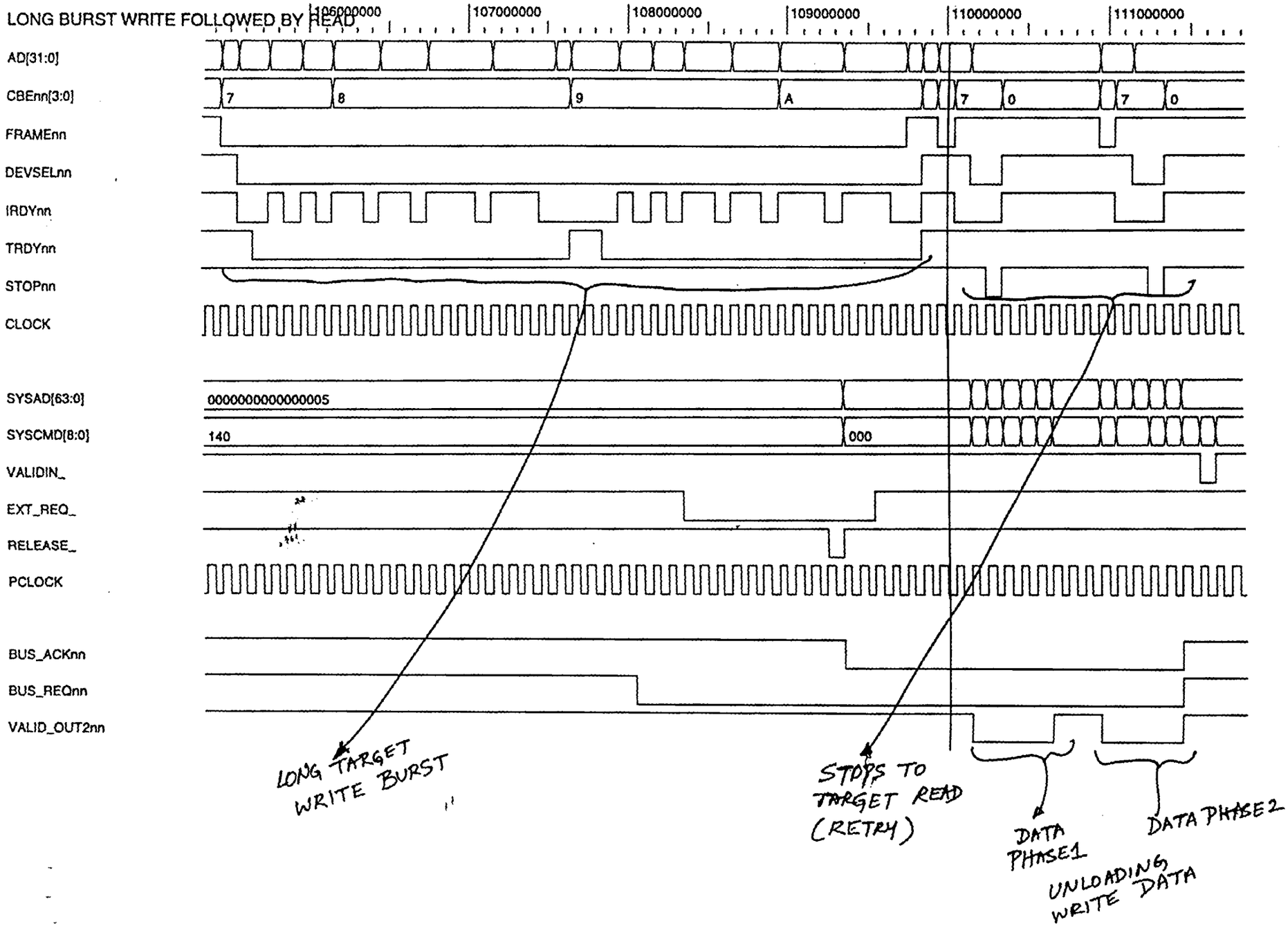

TARGET READ 1
1050000
1100000
1150000
1200000
AD[31:0]
RD ADDR
883BD210
CBEnn[3:0]
RD CMD
7
F
7
E
D
4
C
3
B
FRAMEnn
DEVSELnn
IRDYnn
TRDYnn
STOPnn
CLOCK
SYSAD[63:0]
00000000FFFF09FF
00000000FFFF09FF
SYSCMD[8:0]
140
000
190
140
DATA
WRRDY_
VALIDIN_
ADDRESS
VALIDOUT_
EXT_REQ_
RELEASE_
PCLOCK
BUS RELEASED TO CPU
READYnn
BUS_ACKnn
BUS GRANTED
BUS_REQnn
VALID_OUT2nn
VALID_IN2nn
SX12 DRIVES ADDRESS
SX11 DRIVES DATA

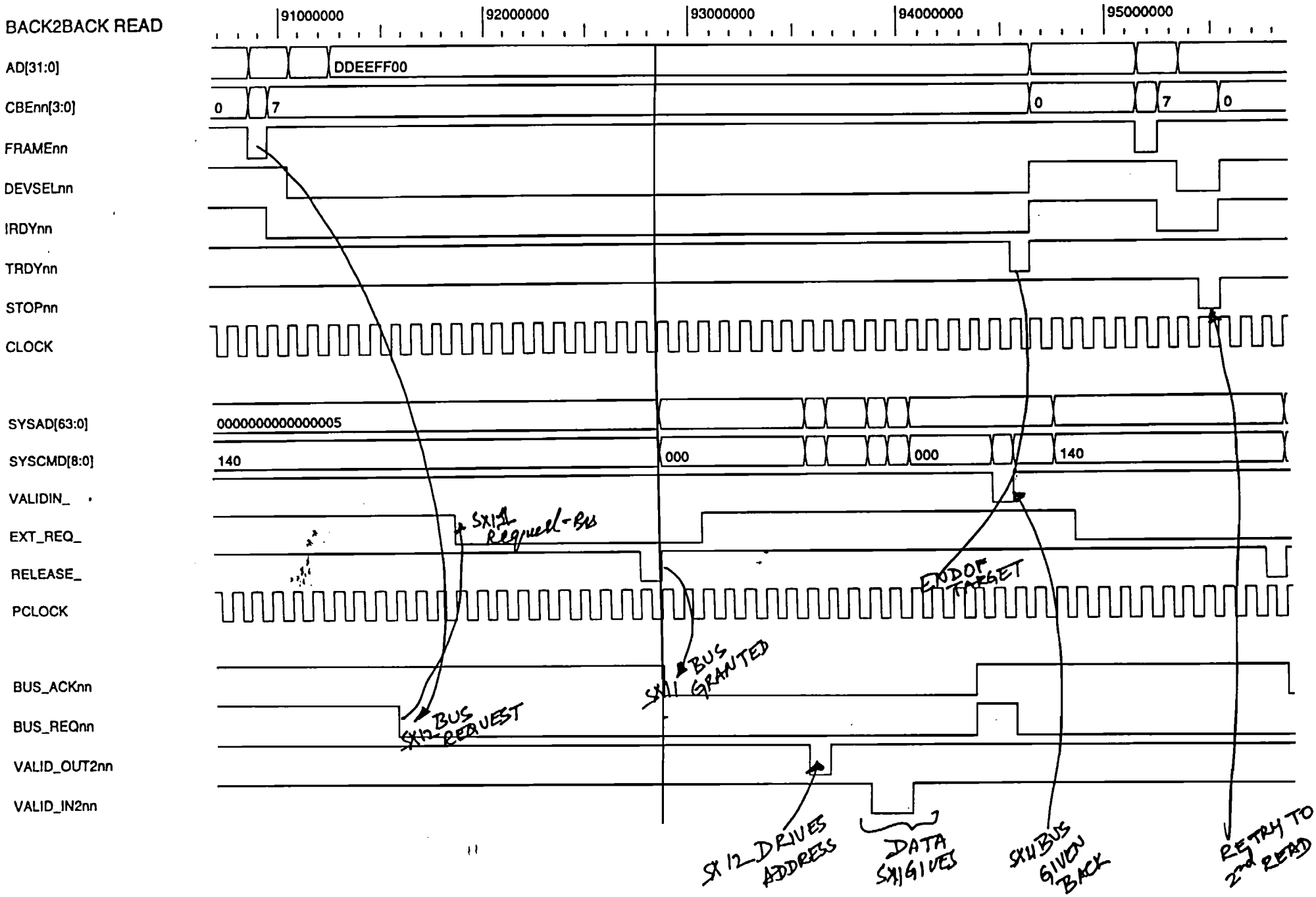
FIGURE 4

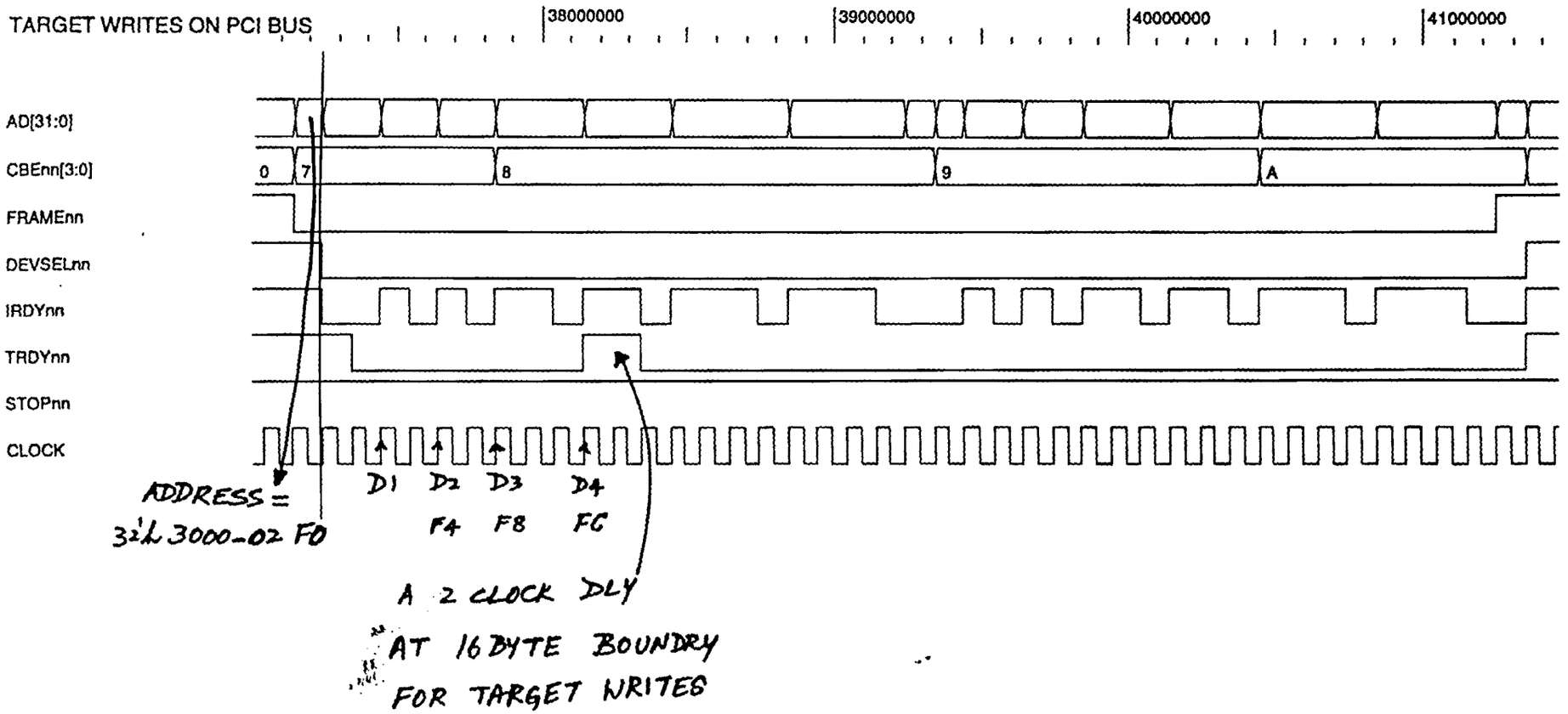
PREFETCH FOR TARGET READS

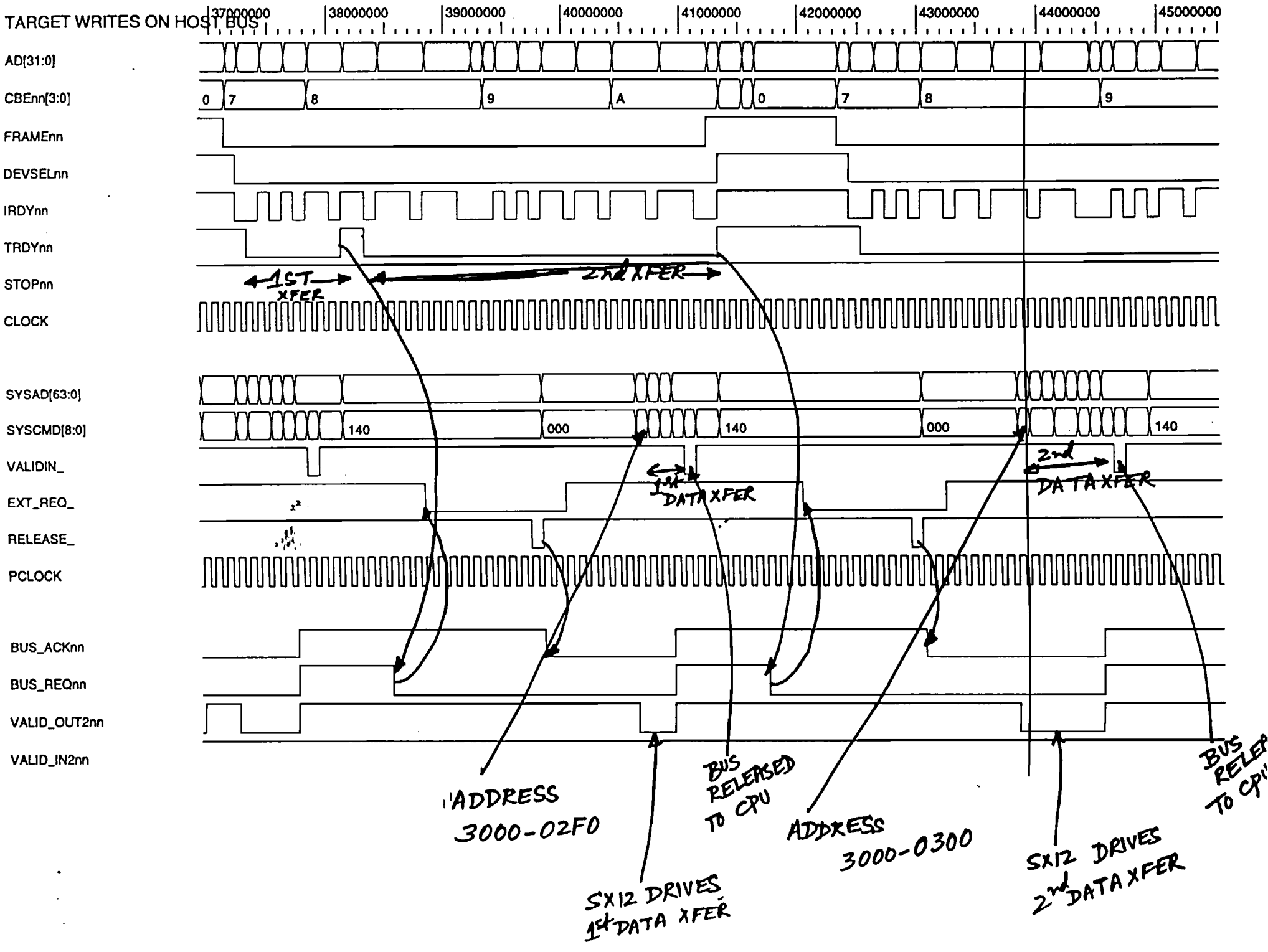


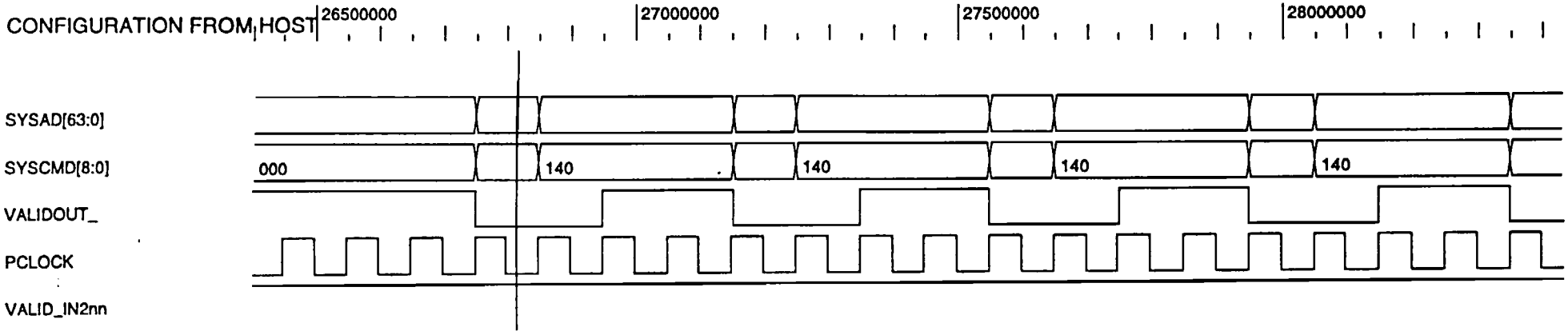
LONG BURST WRITE FOLLOWED BY READ




BACK2BACK READ
91000000
92000000
93000000
94000000
95000000
AD[31:0]
DDEEFF00
CBEnn[3:0]
0
7
0
7
0
FRAMEnn
DEVSELnn
IRDYnn
TRDYnn
STOPnn
CLOCK
SYSAD[63:0]
0000000000000005
SYSCMD[8:0]
140
000
000
140
VALIDIN_
EXT_REQ_
RELEASE_
PCLOCK
BUS_ACKnn
BUS_REQnn
VALID_OUT2nn
VALID_IN2nn
SX11 Request-Bus
SX12 BUS REQUEST
SX11 BUS GRANTED
END OF TARGET
SX12 DRIVES ADDRESS
DATA SX11 GIVES
SX11 BUS GIVEN BACK
RETRY TO 2nd READ

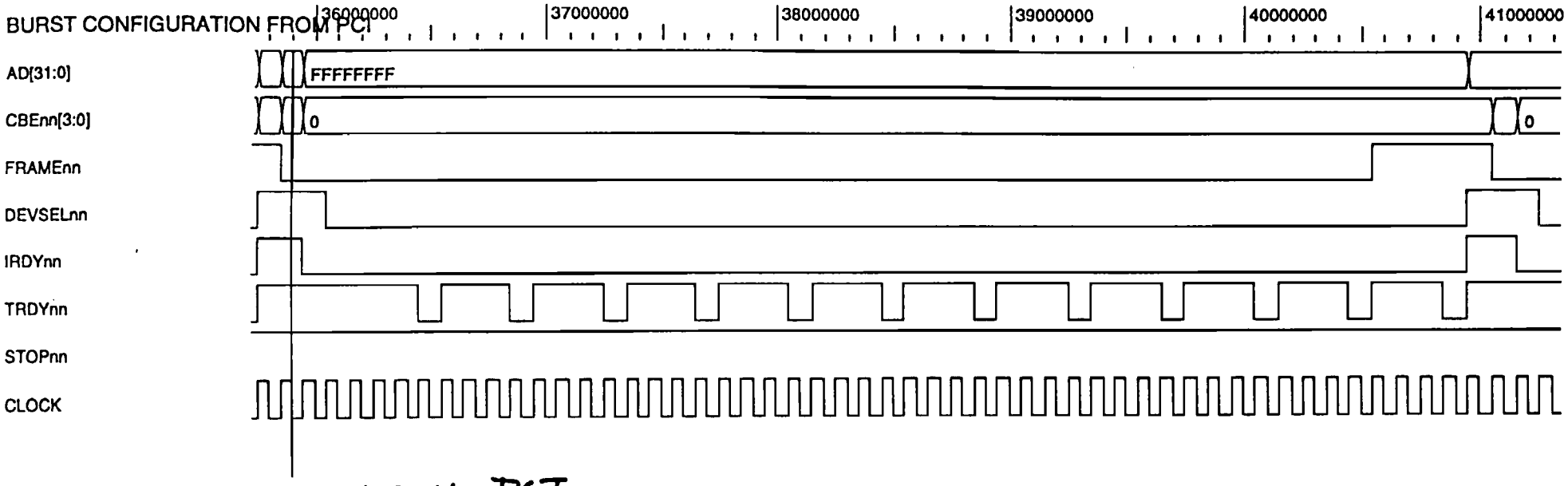

TARGET WRITES ON PCI BUS
38000000
39000000
40000000
41000000
AD[31:0]
CBEnn[3:0]
0
7
8
9
A
FRAMEnn
DEVSELnn
IRDYnn
TRDYnn
STOPnn
CLOCK
ADDRESS =
32'h 3000-02 F0
D1
D2
D3
D4
F4
F8
FC
A 2 CLOCK DLY
AT 16 BYTE BOUNDRY
FOR TARGET WRITES


TARGET WRITES ON HOST BUS
37000000
38000000
39000000
40000000
41000000
42000000
43000000
44000000
45000000
AD[31:0]
CBEnn[3:0]
0
7
8
9
A
0
7
8
9
FRAMEnn
DEVSELnn
IRDYnn
TRDYnn
STOPnn
CLOCK
1ST XFER
2nd XFER
SYSAD[63:0]
SYSCMD[8:0]
140
000
140
000
140
VALIDIN_
EXT_REQ_
RELEASE_
PCLOCK
1st DATA XFER
2nd DATA XFER
BUS_ACKnn
BUS_REQnn
VALID_OUT2nn
VALID_IN2nn
ADDRESS 3000-02F0
BUS RELEASED TO CPU
ADDRESS 3000-0300
SX12 DRIVES 1st DATA XFER
SX12 DRIVES 2nd DATA XFER
BUS RELEASED TO CPU



DOES NOT
SUPPORT BURST
WRITES

MUST CONFIGURE
EACH REGISTER
BY A SINGLE DWORD
WRITE



FROM PCI

BOTH CONFIGURATION DWORD

WRITES & CONFIGURATION

BURST WRITES