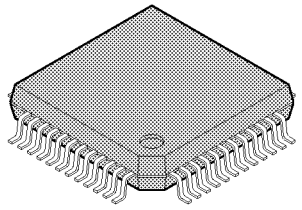
ASSP

FUJITSU

Single-Chip Demodulator for Digital Satellite Broadcasting

MB86660A



Package
- 48-pin plastic QFP
- FPT-48P-M15

Description

The MB86660A is a single-chip demodulator for digital satellite broadcasting receivers and is compliant with DVB-S and DSS. It features two A/D converters for I-input and Q-input, a QPSK demodulator and a forward-error correction (FEC) block, which is comprised of a Viterbi decoder, deinterleaver, Reed-Solomon decoder and descrambler.

Features

- DVB-S and DSS-compliant single-chip demodulator
- Operation rate up to 62 Mbps
- Integrated dual A/D converters for I-input and Q-input
  - Analog 1V p-p and up to 31 Msymbol/s input
- QPSK demodulator
  - Gray-coded QPSK demodulation with absolute mapping
  - On-chip multi-rate VCO (36 to 62 MHz operation)
  - Automatic carrier capture range = ±5 MHz
  - Half-Nyquist filters roll-off factor $\alpha = 0.35$
  - Automatic gain control (AGC): PWM output
- Viterbi decoder
  - Constraint length K = 7
  - Viterbi rate R = 1/2, 2/3, 3/4, 5/6, 7/8
- Reed-Solomon decoder: n = 204, k = 188
- Deinterleaver: depth I = 12
- Energy-dispersal removal: PRBS polynomial = $x^{15} + x^{14} + 1$
- C/N monitoring output via I²C interface
- I²C bus interface
- Power supply voltage: + 3.3V
- Package: QFP-48
- Process: 0.35µm CMOS

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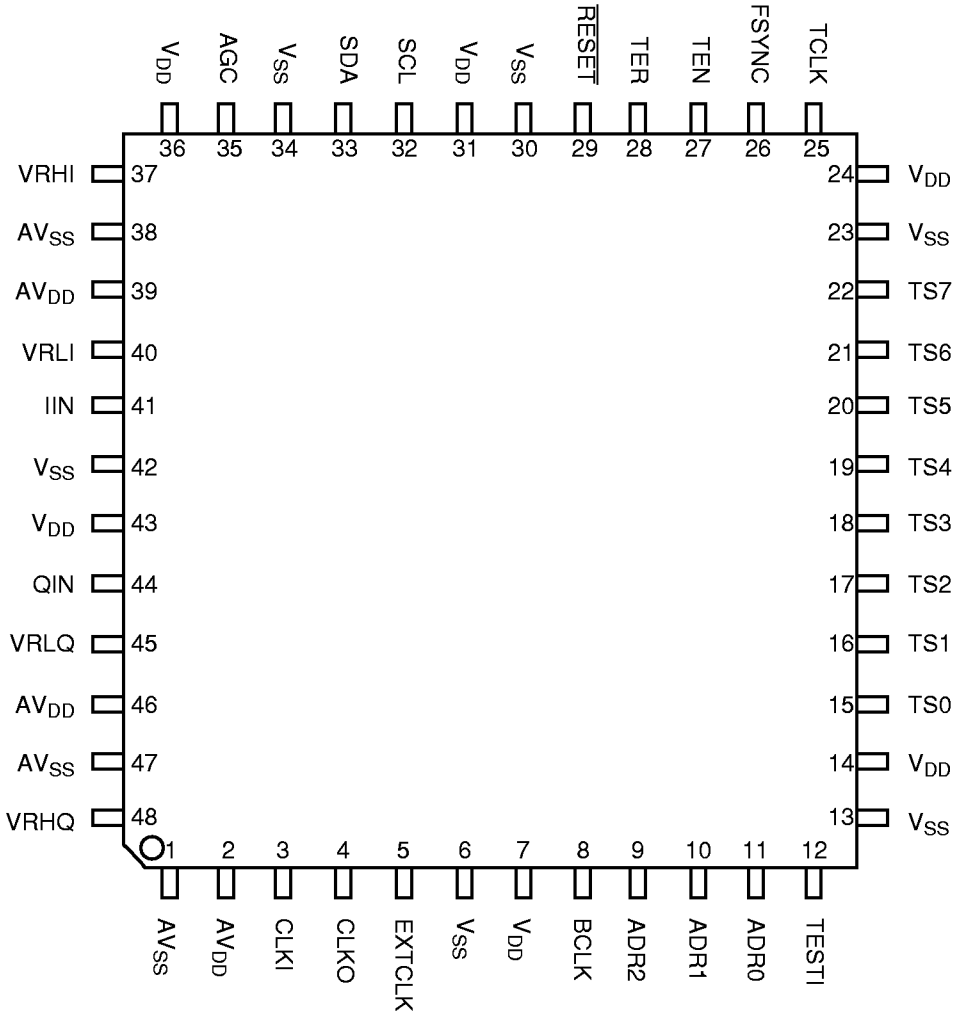
Pin Assignment

TOP VIEW



FPT-48P-M15

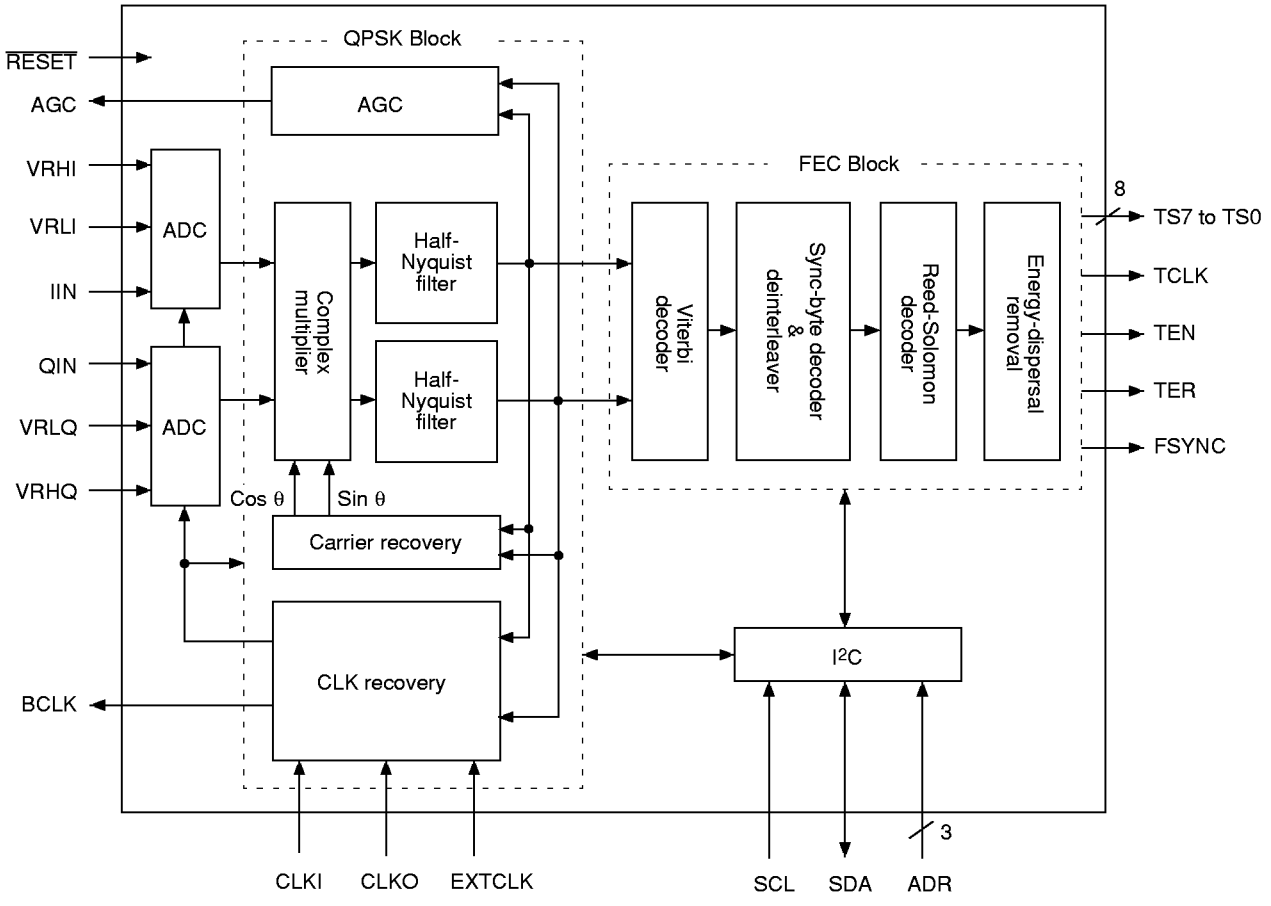
Pin Descriptions

Pin No.	Symbol	Pin Name	I/O	Function
41	IIN	QPSK analog I-input	I	**QPSK analog in-phase input:** Analog 1V p-p input. The maximum input rate is 31 Msymbol/s.
44	QIN	QPSK analog Q-input	I	**QPSK analog quadrature-phase input:** Analog 1V p-p input. The maximum input rate is 31 Msymbol/s.
37	VRHI	A/D high reference	I	**A/D high-reference input for IIN:** High-reference voltage input. The typical voltage is 1.4V.
40	VRLI	A/D low reference	I	**A/D low-reference input for IIN:** Low-reference voltage input. The typical voltage is 0V.
48	VRHQ	A/D high reference	I	**A/D high-reference input for QIN:** High-reference voltage input. The typical voltage is 1.4V.
45	VRLQ	A/D low reference	I	**A/D low-reference input for QIN:** Low-reference voltage input. The typical voltage is 0V.
35	AGC	AGC output	O	**AGC output:** PWM (Pulse Width Modulation) or 'H/L' level output. This output pin is fed to an external analog filter that controls an AGC amplifier of the tuner.
3 4	CLKI CLKO	Crystal oscillator input	I I/O	**Crystal oscillator input:** Connect a 27.0 MHz crystal oscillator between these pins. It is used to set the frequency of the internal multi-rate VCO. This crystal oscillator is not required when the EXTCLK pin inputs 27.0 MHz clock. When the crystal oscillator is not used, CLKI and CLKO must be 'L' and 'OPEN', respectively. When the crystal oscillator is used, EXTCLK must be set to 'L'.
5	EXTCLK	External clock input	I	**External clock input:** This pin inputs a 27.0 MHz clock to set the frequency of the internal multi-rate VCO. The crystal oscillator is not required when this pin is used. When this EXTCLK is not used, it must be set to 'L'.
22 to 15	TS7 to TS0	Transport packet data output	O	**Transport data output:** These pins are the transport stream packet data. The user can select the output mode, either from 8-bit parallel data or serial data output. When parallel output is selected, the user can select the MSB position to be TS7 or TS0. When serial output is selected, the user can select the output pin position, TS0 or TS7. All selections are done by setting an internal register.
25	TCLK	Transport packet clock output	O	**Transport clock output:** This pin is the transport stream packet clock for TS7 to TS0. The user can select the output mode that is parallel or serial clock, and can select the clock polarity. All selections are done by setting the appropriate internal register.
27	TEN	Transport packet enable	O	**Transport enable output:** This pin outputs 'H' when valid packet data is present, and outputs 'L' during other times, such as the parity bytes.
28	TER	Error indicator	O	**Error indicator output:** This pin outputs 'H' for a period of a packet that the Reed-Solomon decoder could not correct, and outputs 'L' for a period of a packet that it could correct.
26	FSYNC	Frame synchronous output	O	**Frame synchronous output:** This pin outputs 'H' when the frame is synchronized.
32	SCL	I^2C bus clock	I	**Serial clock input for I^2C bus**
33	SDA	I^2C bus data	I/O	**Serial data I/O for I^2C bus**
9 10 11	ADR2 ADR1 ADR0	I^2C bus address	I	**Address ID input for I^2C bus:** These are the lower 3-bit of I^2C bus address. The upper 4-bit is fixed with "0001".

Pin Descriptions (continued)

Pin No.	Symbol	Pin Name	I/O	Function
29	$\overline{RESET}$	Reset input	I	**Reset input:** The MB86660A is reset when this pin is 'L'. The LSI must be reset when the power is turned on. Refer to the "Power-on Reset" section for timing details.
8	BCLK	Bit clock output	O	**Bit clock output:** This pin can output a clock signal at twice the symbol rate, a clock signal at the symbol rate, or a packet start signal. All selections are done by setting an internal register. This pin outputs 'L' at the initial stage.
12	TESTI	Test pin	I	**Test pin:** This input test pin must be connected to 'L' for normal operation.
39, 46, 2	AV_{DD}	Analog V_{DD}	—	**Analog V_{DD}:** Analog V_{DD} for the internal A/Ds and VCO
38, 47, 1	AV_{SS}	Analog V_{SS}	—	**Analog V_{SS}:** Analog GND for the internal A/Ds and VCO
7, 14, 24, 31, 36, 43	V_{DD}	Digital V_{DD}	—	**Digital V_{DD}**
6, 13, 23, 30, 34, 42	V_{SS}	Digital V_{SS}	—	**Digital V_{SS}**

Block Diagram



Absolute Maximum Ratings (See WARNING)

Parameter	Symbol	Rating		Unit
		Min.	Max.	
Power supply voltage	V_{DD}, AV_{DD}	–0.5	+4.0	V
Input voltage	V_I	–0.5	V_{DD} + 0.5	V
Output voltage	V_O	–0.5	V_{DD} + 0.5	V
Storage temperature	T_{ST}	–55	+125	°C

WARNING: Semiconductor devices can be permanently damaged by the application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions (See WARNING)

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Power supply voltage	V_{DD}, AV_{DD}	3.0	3.3	3.6	V
High-level input voltage	V_{IH}	$V_{DD} \times 0.65$	—	V_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	—	$V_{DD} \times 0.25$	V
Operating temperature	Ta		0 to +70		°C

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their Fujitsu representative beforehand.

Electrical Characteristics

DC Characteristics

(V_{DD} = +3.3 ± 0.3 V, Ta = 0 to +70°C unless otherwise specified)

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.*1	Max.	
Logic input						
Input high voltage	V_{IH}	—	$V_{DD} \times 0.65$	—	$V_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	–0.3	—	$V_{DD} \times 0.25$	V
I²C bus input (SDA and SCL)						
Input high voltage	V_{IH}	—	3.0	—	5.5	V
Input low voltage	V_{IL}	—	–0.5	—	1.5	V
A/D input (VRHI, VRHQ, VRLI, VRLQ, IIN and QIN)						
Input reference high voltage (for VRHI and VRHQ)	V_{RH}	—	$V_{RL} + 1.0$	1.4	V_{DD}	V
Input reference low voltage (for VRLI and VRLQ)	V_{RL}	—	0	0	$V_{RH} - 1.0$	V
Differential reference voltage	V_{RW}	$V_{RH} - V_{RL}$	1.0	1.4	2.5	V
Reference input resistance	R_{RW}	V_{RH} to V_{RL}	—	5	—	kΩ
Analog input voltage (for IIN and QIN)	V_i	—	V_{RL}	—	V_{RH}	V
Analog input capacitance (for IIN and QIN)	C_{in}	—	—	15	—	pF
Logic output						
Output high voltage	V_{OH}	I_{OH} = –4 mA	$V_{DD} - 0.5$	—	—	V
Output low voltage	V_{OL}	I_{OL} = 4 mA	—	—	0.4	V
I²C bus output (SDA)						
Output low voltage	V_{OL}	I_{OL} = 3 mA	—	—	0.4	V
Power supply current (V_{DD} and AV_{DD})						
Average power supply current	I_{DD}	IIN, QIN = 31 Mbaud/s V_{DD} = 3.6 V	—	300	T.B.D.	mA

*1 Typical values assume that V_{DD} = +3.3 V and Ta = +25°C.

Register Table

Register Map

< I^2C address: | 0 | 0 | 0 | 1 | ADR2 | ADR1 | ADR0 | >

Register Address	Access	Register Name	(MSB) Bit Function Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00000000 (0)	R/W	MODE-1	MOD7 (0)	Reserved (0)	MOD5 (0)	MOD4 (0)	MOD3 (0)	MOD2 (0)	MOD1 (0)	MOD0 (0)
00000001 (1)	R/W	MODE-2	Reserved (0)	Reserved (0)	Reserved (0)	BCLK1 (0)	BCLK0 (0)	ER_EN (1)	RS_EN (1)	DI_EN (1)
00000010 (2)	R/W	AGC	Reserved (0)	AGCP (0)	AGCM (0)	AGC4 (1)	AGC3 (0)	AGC2 (0)	AGC1 (0)	AGC0 (0)
00000011 (3)	R/W	VCO	VCO7 (0)	VCO6 (0)	VCO5 (0)	VCO4 (1)	VCO3 (0)	VCO2 (1)	VCO1 (1)	VCO0 (0)
00000100 (4)	R/W	Viterbi VCO expansion	LVCO (0)	0	0	VIR4 (0)	VIR3 (0)	VIR2 (1)	VIR1 (0)	VIR0 (0)
00000101 (5)	R/W	Frame synchronization	SYT3 (1)	SYT2 (1)	SYT1 (1)	SYT0 (1)	SYA3 (0)	SYA2 (0)	SYA1 (1)	SYA0 (0)
00000110 (6)	R/W	Carrier recovery loop filter coefficient	CA_SW (1)	CA_β2 (0)	CA_β1 (1)	CA_β0 (0)	0	CA_α2 (0)	CA_α1 (0)	CA_α0 (1)
00000111 (7)	R/W	Clock recovery loop filter coefficient	0	CL_β2 (0)	CL_β1 (1)	CL_β0 (1)	0	CL_α2 (0)	CL_α1 (1)	CL_α0 (0)
00001000 (8)	W	RESET	X (0)	X (0)	X (0)	X (0)	X (0)	X (0)	QP_RST (0)	LSI_RST (0)
00001001 (9)	R	Status	X	X	X	STA4	STA3	STA2	STA1	STA0
00001010 (10)	R	AFC	AFC7	AFC6	AFC5	AFC4	AFC3	AFC2	AFC1	AFC0
00001011 (11)	R	C/N	CN7	CN6	CN5	CN4	CN3	CN2	CN1	CN0
00001100 (12)	—	Reserved	X	X	X	X	X	X	X	X
00010000 (16)	—	Reserved	X	X	X	X	X	X	X	X
00010001 (17)	R/W	Start carrier coefficient	X (0)	CAS_β2 (0)	CAS_β1 (1)	CAS_β0 (1)	X (0)	CAS_α2 (0)	CAS_α1 (1)	CAS_α0 (1)
00010010 (18)	R	Unused	1	1	1	1	1	1	1	1
00010011 (19)	R/W	AGC coefficient	X (0)	AGC_β2 (0)	AGC_β1 (0)	AGC_β0 (0)	X (0)	AGC_α2 (0)	AGC_α1 (1)	AGC_α0 (1)

Note: X: Don't care
(0) or (1): Default value

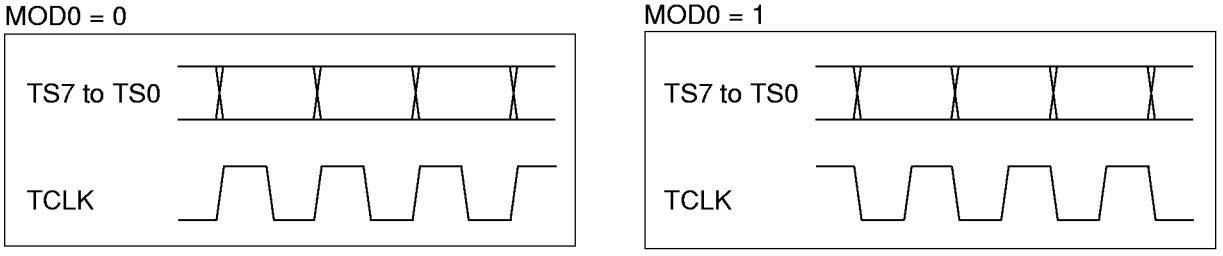
Functional Description

MODE-1

- The user can select the output polarity of TCLK, the output mode of TS7 to TS0, and so on by setting the register.
- Register value: I²C address = 0001ADR [2:0]. Register address = 00000000(2).

Bit Name	Function	Bit Value	Operation
MOD0	TCLK polarity	0 (default)	TS7 to TS0 are latched at the falling edge of the TCLK.
		1	TS7 to TS0 are latched at the rising edge of the TCLK.
MOD1	Error indicator	0 (default)	The error indicator flag of the transport stream packet is set to 'H' when the Reed-Solomon decoder cannot correct the error.
		1	The error indicator flag of the transport stream packet is not changed.
MOD2	Output mode of TS7 to TS0	0 (default)	Parallel output
		1	Serial output. Unused TS bits output 'L'.
MOD3	Output order of TS7 to TS0	0 (default)	TS7 is MSB when parallel. TS0 outputs when in serial mode.
		1	TS0 is MSB when parallel. TS7 outputs when in serial mode.
MOD4	FSYNC output mode	0 (default)	FSYNC outputs the frame synchronous signal.
		1	FSYNC outputs the Viterbi synchronous signal.
MOD5	Frame sync-mode	0 (default)	'B8(h)' of the frame sync-byte value is changed to '47(h)'.
		1	'B8(h)' of the frame sync-byte value is not changed.
bit6	Reserved	0	Don't change
MOD7	Data reverse switch	0 (default)	Normal operation
		1	Received data is reversed in LSI.

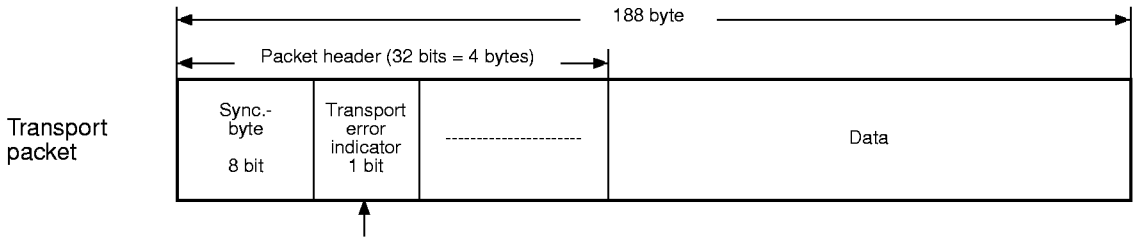
[MOD0 function]



MODE-1 (continued)

[MOD1 function]

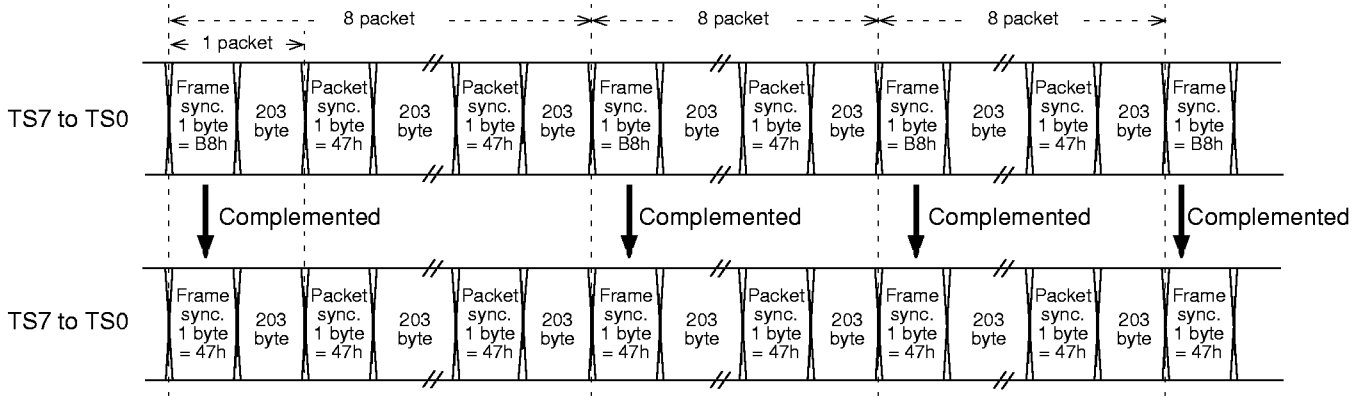
The structure of the transport packet



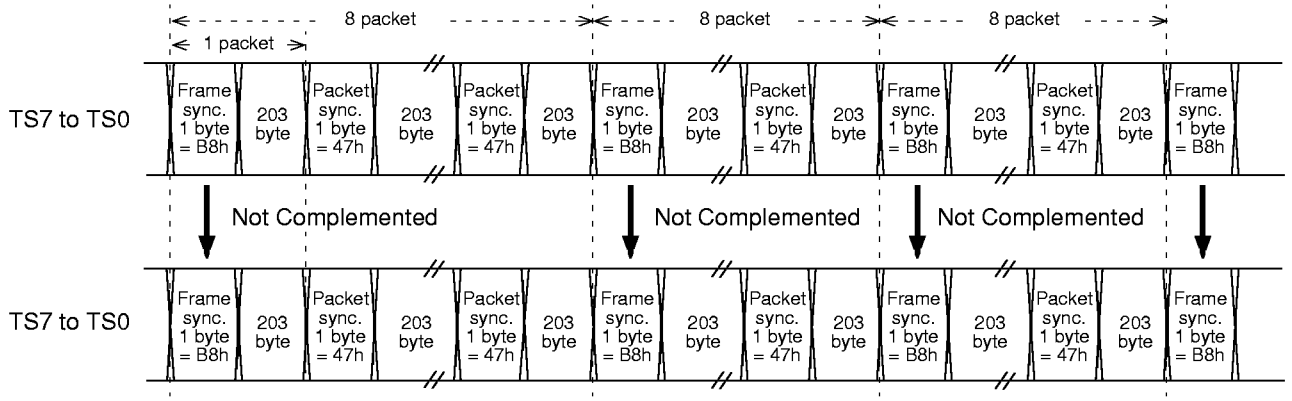
MOD1 = 0: This bit is set to 'H' when the Reed-Solomon decoder cannot correct the error.
MOD1 = 1: This bit is not changed.

[MOD5 function]

MOD5 = 0



MOD5 = 1



MODE-2

- Deinterleaver, Reed-Solomon and Energy dispersal removal functions may be bypassed by setting this register.
- Register value: I²C address = 0001ADR [2:0]. Register address = $00000001_{(2)} = 1_{(10)}$.

Bit Name	Function	Bit Value	Operation
DI_EN	Deinterleaver enable	0	Deinterleaver is bypassed.
		1 (default)	Normal operation. Deinterleaving is performed.
RS_EN	Reed-Solomon enable	0	Read-Solomon decoder is bypassed.
		1 (default)	Normal operation. Reed-Solomon decoding is performed.
ER_EN	Energy dispersal removal enable	0	Energy dispersal removal is not performed.
		1 (default)	Normal operation. Energy dispersal removal is performed.

- BCLK output may be changed by setting the register.
- Register value: I²C address = 0001ADR [2:0]. Register address = $00000001_{(2)} = 1_{(10)}$.

Bit Name	Function	Bit Value	Operation
BCLK [1:0]	BCLK output select	00 (default)	'L' level output
		01	Packet start signal output
		10	Clock signal with frequency = twice the symbol rate
		11	Clock signal with frequency = symbol rate

- Bit 5 to bit 7 should not be changed.
- Register value: I²C address = 0001ADR [2:0]. Register address = $00000001_{(2)} = 1_{(10)}$

Bit Name	Function	Bit Value	Operation
Bit 5	Reserved	0 (default)	Don't change.
Bit 6		0 (default)	Don't change.
Bit 7		0 (default)	Don't change.

Status

- The user can monitor the internal status by reading the status register.
- Register value: I²C address = 0001ADR [2:0]. Register address = $00001001_{(2)} = 9_{(10)}$, Read only.

Bit Name	Function	Bit Value	Operation
STA0	Frame synchronization	0	Shows Frame is not in synchronization.
		1	Shows Frame is in synchronization.
STA1	Viterbi decode synchronization	0	Shows the Viterbi decoder is not in synchronization.
		1	Shows the Viterbi decoder is in synchronization.
STA [4:2]	Viterbi rate detection	000	Shows the Viterbi decoder is not in synchronization.
		001	Shows the Viterbi rate is 1/2.
		010	Shows the Viterbi rate is 2/3.
		011	Shows the Viterbi rate is 3/4.
		100	Shows the Viterbi rate is 5/6.
		101	Shows the Viterbi rate is 7/8.

A/D Converter

- I and Q analog input data are automatically sampled by the internal clock.

Nyquist Filter

- Digital half-Nyquist filtering is performed for the I and Q input signal. The roll-off factor is 0.35.

AGC

- The amplitude of I and Q input data is compared with the reference value AGC [4:0] set by the user. The compared result is output to the AGC pin in PWM (Pulse Width Modulation) form or 'H/L' level. It adjusts the amplifier gain of the tuner via an external analog filter.
- The pulse width of the PWM output is changed at 1/(2Fs) × n (µs) step (n= 0 to 255, Fs: symbol rate (Msymbol/s)). The frequency is Fs/128 (MHz).
- The pulse width of the 'H/L' level output is changed at minimum 4/Fs (µs) step (Fs: symbol rate (Msymbol/s)). The frequency is maximum Fs/8 (MHz). As the response is faster than PWM, it is useful if quick response is required.
- The reference value AGC [4:0] and the AGC output polarity are programmable.
- Register value: I²C address = 0001ADR [2:0]. Register address = $00000010_{(2)} = 2_{(10)}$.

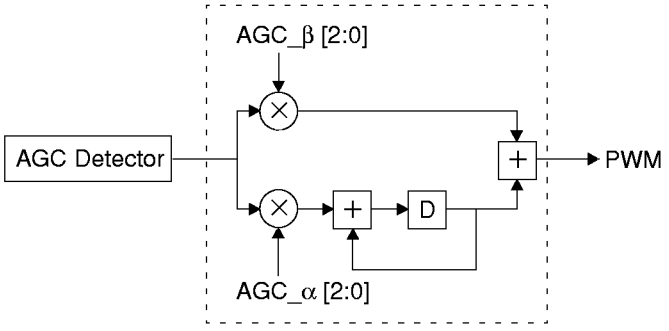
Bit Name	Function	Bit Value	Operation
AGC [4:0]	Reference value for AGC	00000 to 10000 (default) to 11111	Minimum reference value The amplifier gain of the tuner is adjusted to equal the reference value. Maximum reference value
AGCM	AGC output mode	0 (default)	PWM output
		1	'H/L' level output
AGCP	AGC output polarity	0 (default)	When AGC [4:0] > Amplitude of I and Q input data: If AGCM = 0 (PWM output), it repeatedly outputs pulses with 'H' period longer than 'L' period. If AGCM = 1 ('H/L' level output), it outputs 'H'. When AGC [4:0] < Amplitude of I and Q input data: If AGCM = 0 (PWM output), it repeatedly outputs pulses with 'L' period longer than 'H' period. If AGCM = 1 ('H/L' level output), it outputs 'L'.
		1	When AGC [4:0] > Amplitude of I and Q input data: If AGCM = 0 (PWM output), it repeatedly outputs pulses with 'L' period longer than 'H' period. If AGCM = 1 ('H/L' level output), it outputs 'L'. When AGC [4:0] < Amplitude of I and Q input data: If AGCM = 0 (PWM output), it repeatedly outputs pulses with 'H' period longer than 'L' period. If AGCM = 1 ('H/L' level output), it outputs 'H'.
Bit 7	Reserved	0 (default)	Do not set this bit.

AGC (continued)

- Some external AGC-loop configuration in user systems may need to adjust the filter value using the following register.
- Register value: I²C address = 0001ADR [2:0]. Register address = $00010011_{(2)} = 19_{(10)}$.

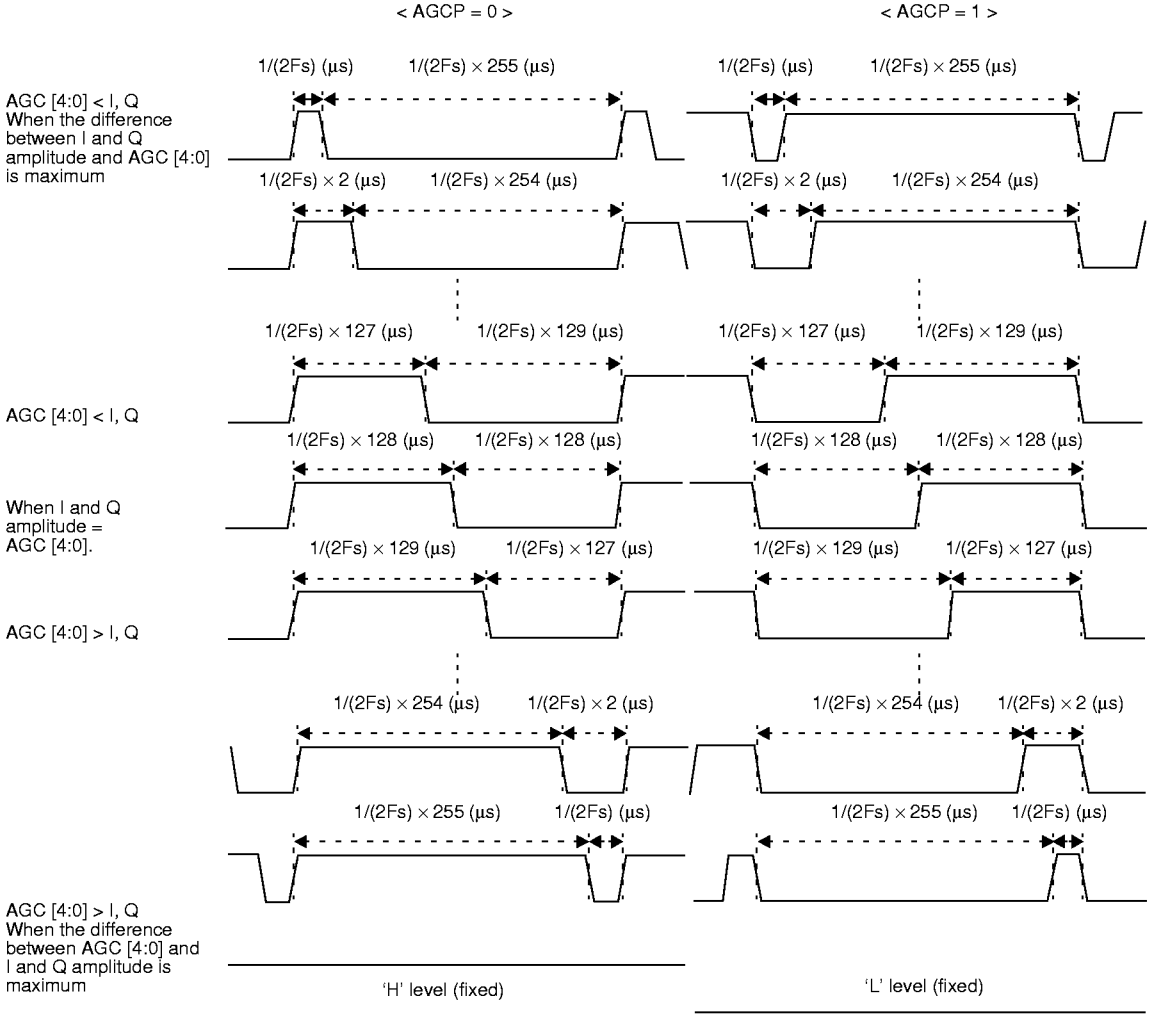
Bit Name	Function	Bit Value	Operation
AGC_α [2:0]	α-Coefficiency of AGC loop-filter	000	$\alpha = 2^0 (= 1)$
		001	$\alpha = 2^1 (= 2)$
		010	$\alpha = 2^2 (= 4)$
		011 (default)	$\alpha = 2^3 (= 8)$
		100	$\alpha = 2^4 (= 16)$
		101	$\alpha = 2^5 (= 32)$
		110	$\alpha = 2^6 (= 64)$
		111	—
AGC_β [2:0]	β-Coefficiency of AGC loop-filter	000 (default)	$\beta = 0$
		001	$\beta = 2^1 (= 2)$
		010	$\beta = 2^2 (= 4)$
		011	$\beta = 2^3 (= 8)$
		100	$\beta = 2^4 (= 16)$
		101	$\beta = 2^5 (= 32)$
		110	$\beta = 2^6 (= 64)$
		111	$\beta = 2^7 (= 128)$

Block Diagram of AGC:



AGC (continued)

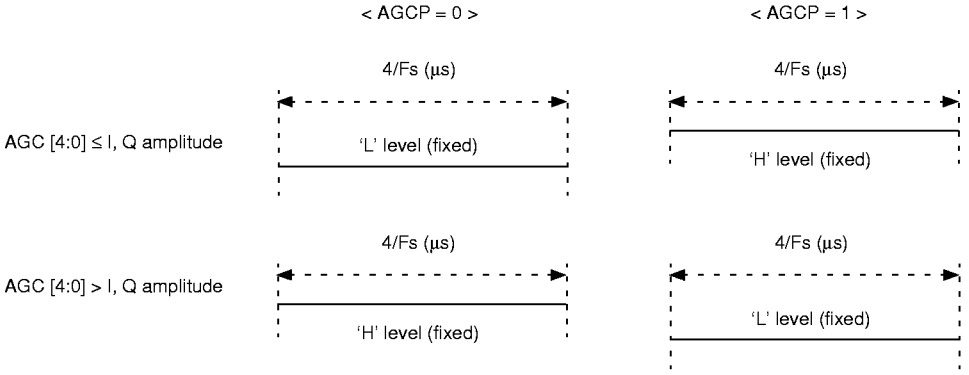
PWM AGC output waveform: The pulse width is changed at 1/(2Fs) × n (µs) step (n = 0 to 255, Fs: symbol rate (Msymbol/s). The frequency is Fs/128 (MHz).



Fs: symbol rate (Msymbol/s)

AGC (continued)

'H/L' level AGC output waveform: The pulse is changed at minimum 4/Fs (μs) step (Fs: symbol rate). The frequency is Fs/8 (MHz).



Fs: symbol rate (Msymbol/s)

Carrier Recovery

- The difference between the actual and expected carrier frequency is automatically recovered up to ± 5 MHz in the LSI.
- The loop filter coefficient for the carrier recovery operates with CAS_α [2:0] and CAS_β [2:0] at first and then automatically switches to CA_α [2:0] and CA_β [2:0] after the lock-up. However, when CA_SW is "0", the filter coefficient always operates with CA_α [2:0] and CA_β [2:0].
- The loop filter is variable.
- Register value: I²C address = 0001ADR [2:0].

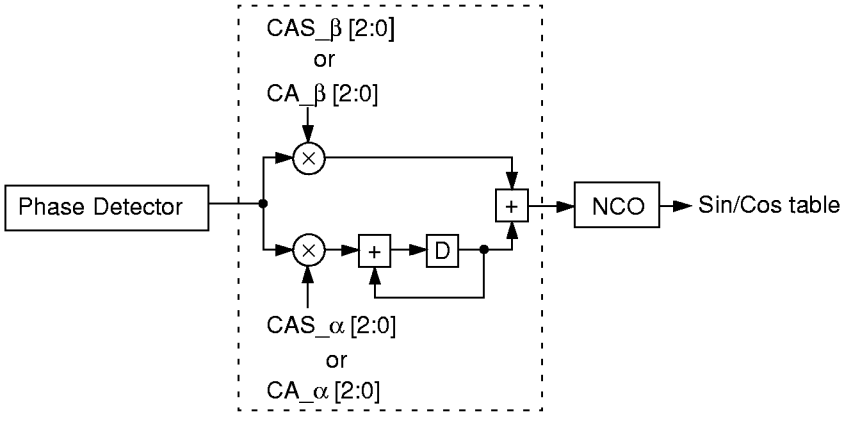
< Register address = 00010001(2) = 17(10) > .

Bit Name	Function	Bit Value	Operation
CAS_α [2:0]	α-factor for the loop filter at first	000	$\alpha = 2^1$ (=2)
		001	$\alpha = 2^2$ (=4)
		010	$\alpha = 2^3$ (=8)
		011 (default)	$\alpha = 2^4$ (=16)
		100	$\alpha = 2^5$ (=32)
		101 to 111	$\alpha = 2^6$ (=64)
CAS_β [2:0]	β-factor for the loop filter at first	000	$\beta = 2^8$ (=256)
		001	$\beta = 2^9$ (=512)
		010	$\beta = 2^{10}$ (=1024)
		011 (default)	$\beta = 2^{11}$ (=2048)
		100	$\beta = 2^{12}$ (=4096)
		101 to 111	$\beta = 2^{13}$ (=8192)

< Register address = 00000110(2) = 6(10) > .

Bit Name	Function	Bit Value	Operation
CA_α [2:0]	α-factor for the loop filter after lock-up	000	$\alpha = 2^1$ (=2)
		001 (default)	$\alpha = 2^2$ (=4)
		010	$\alpha = 2^3$ (=8)
		011	$\alpha = 2^4$ (=16)
		100	$\alpha = 2^5$ (=32)
		101 to 111	$\alpha = 2^6$ (=64)
CA_β [2:0]	β-factor for the loop filter after lock-up	000	$\beta = 2^8$ (=256)
		001	$\beta = 2^9$ (=512)
		010 (default)	$\beta = 2^{10}$ (=1024)
		011	$\beta = 2^{11}$ (=2048)
		100	$\beta = 2^{12}$ (=4096)
		101	$\beta = 2^{13}$ (=8192)
CA_SW	Loop filter SW	0	Auto SW: off
		1(default)	Auto SW: on

Carrier Recovery Block Diagram:



AFC

- The user can monitor the difference between the actual recovered carrier frequency and the nominal local oscillator frequency in the tuner.
- The different frequency of the tuner may be calculated by reading the AFC register:

  Δf (kHz) = (128 – AFC[7:0]) × 82.474 × (n/42.192) (n: Receiving bit rate (Mbps))

  Ex.1: When AFC[7:0] = 01111100 and Receiving bit rate n = 40 (Mbps),
  $AFC_{(DEC)} = 2^2 + 2^3 + 2^4 + 2^5 + 2^6 = 124$
  Δf = 312.8 (kHz) → shows the local oscillator frequency in the tuner is 312.8 kHz higher.

  Ex.2: When AFC[7:0] = 10000101 and Receiving bit rate n = 60 (Mbps),
  $AFC_{(DEC)} = 2^0 + 2^2 + 2^7 = 133$
  Δf = –586.4 (kHz) → shows the local oscillator frequency in the tuner is 586.4 kHz lower.

- Register value: I²C address = 0001ADR [2:0], Register address = 00001010 (2), Read only

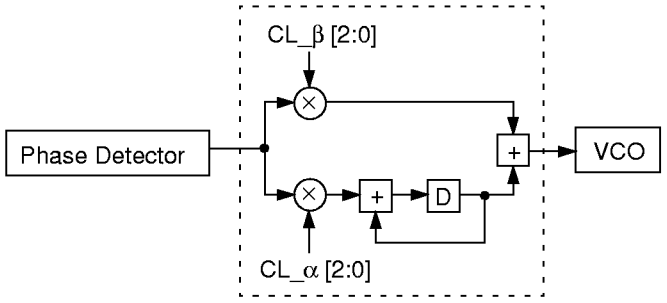
Bit Name	Function	Bit Value	Operation
AFC [7:0]	The difference of the carrier frequency	00000000	Shows the local oscillator frequency in the tuner is very high.
		00000001 to 01111111	
		10000000	Shows the local oscillator frequency in the tuner is almost correct.
		10000001 to 11111110	
		11111111	Shows the local oscillator frequency in the tuner is very low.

Clock Recovery

- The clock synchronized to the baseband data is automatically recovered in the LSI. The internal VCO must be set to the required frequency in advance. Refer to Section 10 for setting the internal VCO frequency.
- The Loop filter is variable.
- Register value: I²C address = 0001ADR [2:0]. Register address = $00000111_{(2)} = 7_{(10)}$.

Bit Name	Function	Bit Value	Operation
CL_α [2:0]	α-factor for the clock recovery loop filter	000	$\alpha = 2^9$ (=512)
		001	$\alpha = 2^{10}$ (=1024)
		010 (default)	$\alpha = 2^{11}$ (=2048)
		011	$\alpha = 2^{12}$ (=4096)
		100	$\alpha = 2^{13}$ (=8192)
		101	$\alpha = 2^{14}$ (=16384)
		110, 111	Prohibited
CL_β [2:0]	β-factor for the clock recovery loop filter	000	$\beta = 2^{17}$ (=131072)
		001	$\beta = 2^{18}$ (=262144)
		010	$\beta = 2^{19}$ (=524288)
		011 (default)	$\beta = 2^{20}$ (=1048576)
		100	$\beta = 2^{21}$ (=2097152)
		101	$\beta = 2^{22}$ (=4194304)
		110, 111	Prohibited

Clock Recovery Block Diagram:



VCO

- The internal VCO frequency must be set to two times the received data symbol rate. Because the frequency resolution is 0.1 MHz, it should be set to the nearest step.
  Exp.: When the received data symbol rate is 21.096 Msym/s, set 42.2 MHz as 21.096 Msym/s x2 = 42.192 MHz.
- Register value: I²C adress = 0001ADR [2:0]. Register address = $00000011_{(2)} = 3_{(10)}$ & $00000100_{(2)} = 4_{(10)}$.

Bit Name	Function	Bit Value	Operation	
			LVCO Register = '0'	LVCO Register = '1'
VCO [7:0]	VCO frequency (0.1 MHz step)	00000000	Internal VCO is set to 40.0 MHz.	
		00000001	Internal VCO is set to 40.1 MHz.	
		to	↓	
		00000110	Internal VCO is set to 40.6 MHz.	
		to	↓	
		00010110	Internal VCO is set to 42.2 MHz. (Initial value)	
		to	↓	
		01000100	Internal VCO is set to 46.8 MHz.	
		to	↓	
		01110100	Internal VCO is set to 51.6 MHz.	
		to	↓	
		10010110	Internal VCO is set to 55.0 MHz.	
		to	↓	
		10100010	Internal VCO is set to 56.2 MHz.	
		to	↓	
		11001000	Internal VCO is set to 60.0 MHz.	
		to	↓	
		11011000	Internal VCO is set to 61.6 MHz.	Set to 36.0 MHz
		to	↓	↓
		11100000	Internal VCO is set to 62.4 MHz.	Set to 36.8 MHz
		to	↓	↓
		11111110	Internal VCO is set to 65.4 MHz.	Set to 39.8 MHz
		11111111	Internal VCO is set to 65.5 MHz.	Set to 39.9 MHz

Reset

- The whole block of LSI or QPSK-block only is reset when LSI_RST or QP_RST bit is set to '1'.
- Register value: I²C address = 0001ADR [2:0]. Register address = $00001000_{(2)} = 8_{(10)}$.

Bit Name	Function	Bit Value	Operation
LSI_RST	LSI software reset	1	The whole LSI (including QPSK block, FEC block and I²C interface) is reset when LSI_RST bit is set to '1'.
QP_RST	QPSK block software reset	1	QPSK block only is reset when QP_RST bit is set to '1'.

Viterbi Decoder

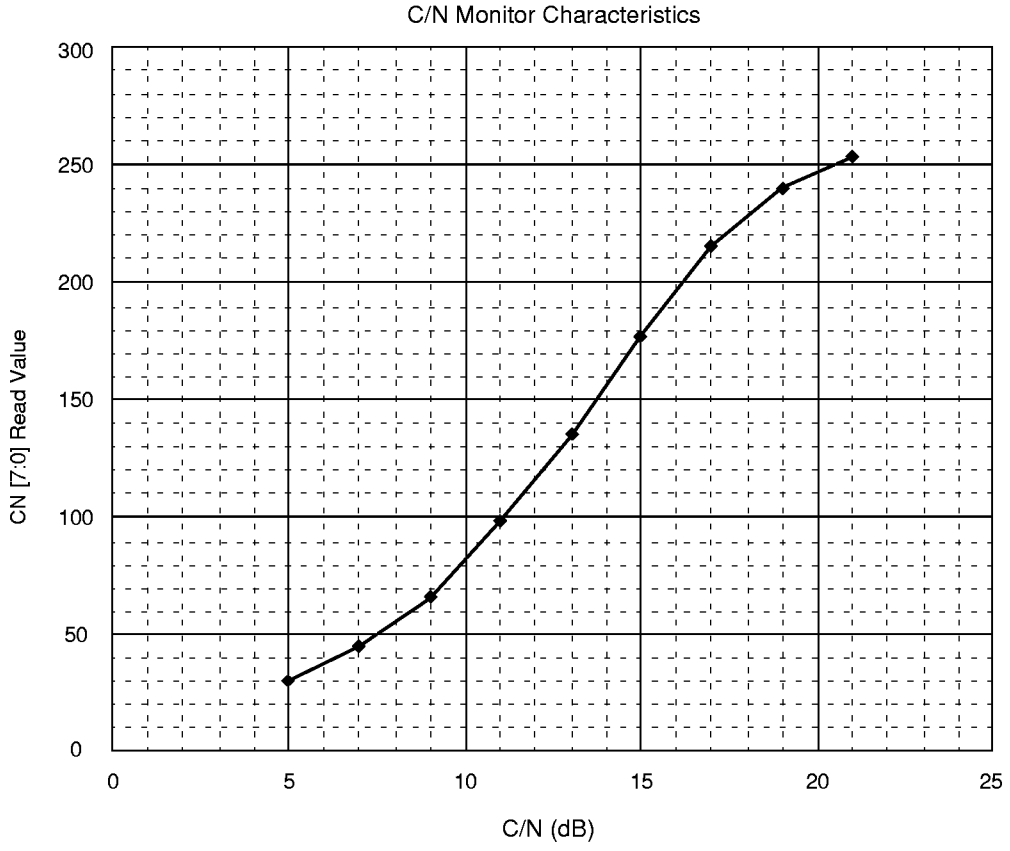
- Constraint length K = 7.
- Optionally, some Viterbi rates may be selected from R = 1/2, 2/3, 3/4, 5/6 and 7/8.
- The receiving Viterbi rate is automatically detected from the selected Viterbi rates. The time it takes to detect the actual rate is proportional to the number of selected rates, so it is recommended to select one rate if the rate is known beforehand.
- The detected Viterbi rate is written to the STA [4:2] register (refer to the section on Status, page 13).
- Register value: I²C address = 0001ADR [2:0], Register address = $00000100_{(2)} = 4_{(10)}$.

Bit Name	Function	Bit Value	Operation
VIR0	R = 1/2 setting	0 (default)	Viterbi rate detection is not performed for R = 1/2.
		1	Viterbi rate detection is performed for R = 1/2.
VIR1	R = 2/3 setting	0 (default)	Viterbi rate detection is not performed for R = 2/3.
		1	Viterbi rate detection is performed for R = 2/3.
VIR2	R = 3/4 setting	0	Viterbi rate detection is not performed for R = 3/4.
		1 (default)	Viterbi rate detection is performed for R = 3/4.
VIR3	R = 5/6 setting	0 (default)	Viterbi rate detection is not performed for R = 5/6.
		1	Viterbi rate detection is performed for R = 5/6.
VIR4	R = 7/8 setting	0 (default)	Viterbi rate detection is not performed for R = 7/8.
		1	Viterbi rate detection is performed for R = 7/8.

C/N Monitor

- The approximate C/N value of the input signal is monitored.
- The monitored C/N value depends on the evaluation environment, LSI mounting conditions, and so on in the user application system. Therefore, the value must be carefully checked. The typical characteristic curve is shown below.
- Register value: I²C address = 0001ADR [2:0]. Register address = $00001011_{(2)} = 11_{(10)}$, Read only.

Bit Name	Function	Bit Value	Operation
CN [7:0]	C/N monitor	00000000	Shows that the error of the receiving data is large.
		to	
		11111111	Shows that the error of the receiving data is small.



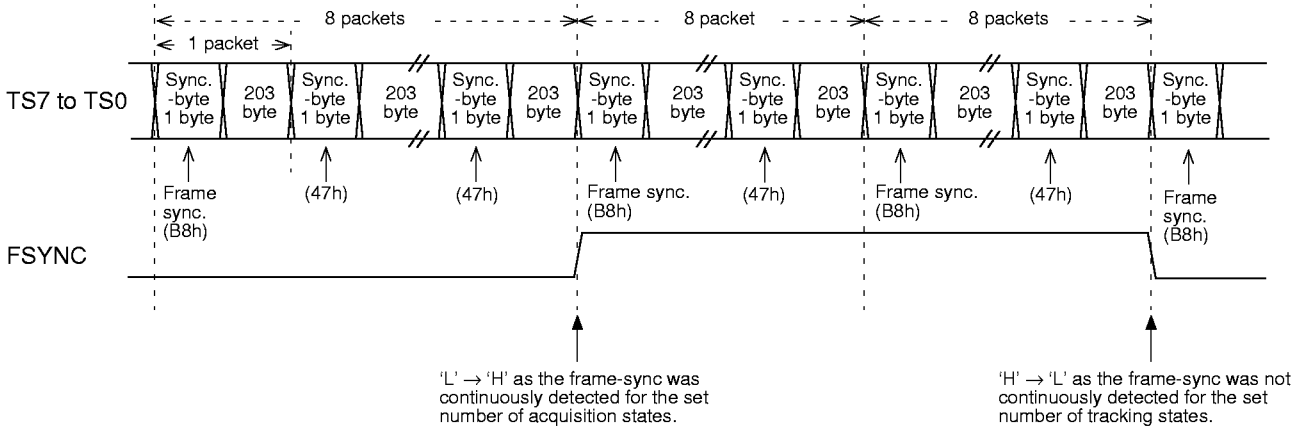
Note: CN [7:0] Read Value is translated to decimal value.

Frame Synchronization

- The frame synchronization signal (B8h) at the start of 8 packets is detected. The number of states for acquisition and tracking is programmable.
- The LSI is considered to lock if the synchronization signal is continuously detected for the set number of acquisition states, and then FSYNC is changed to 'H' when ((MOD4 (Register address: 00000000) = '0')). After lock, the LSI is considered to be out of lock if the synchronization signal would not be continuously detected for the set number of tracking states, and then FSYNC is changing to 'L'.
- Register value: I²C address = 0001ADR [2:0]. Register address = $00000101_{(2)} = 5_{(10)}$.

Bit Name	Function	Bit Value	Operation
SYA [3:0]	Number of acquisition states	0000,0001, 0010 (default) to 1111	The LSI is considered to lock if the synchronization signal is continuously detected two times. to The LSI is considered to lock if the synchronization signal is continuously detected fifteen times.
SYT [3:0]	Number of tracking states	0000 to 0010 to 1111 (default)	The LSI is considered not to lock if the synchronization signal would not be continuously detected two times. to The LSI is considered not to lock if the synchronization signal would not be continuously detected fifteen times.

Timing



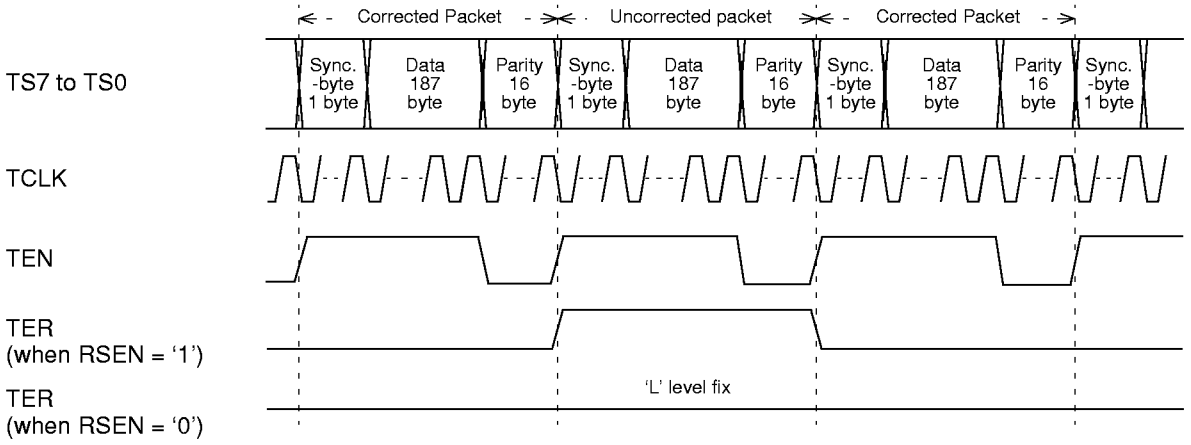
Deinterleaver

- The deinterleaving depth I = 12 on byte-stream.
- When DI_EN (Register address = 00000001) = '0', deinterleaving is not performed. When DI_EN = '1', deinterleaving is performed.

Reed-Solomon Decoder

- n = 204, k = 188, t = 8
  Code Generator Polynomial: $g(x) = (x + \lambda^0)(x + \lambda^1)(x + \lambda^2) \cdots (x + \lambda^{15})$
  Field Generator Polynomial: $p(x) = x^8 + x^4 + x^3 + x^2 + 1$
- If the total errors are less than 8 bytes for the 204-byte block, all errors can be corrected. If the total errors are more than 9 bytes, all errors are not corrected. The TER outputs 'L' for a packet that all errors were corrected. The TER outputs 'H' for a packet that the errors were not corrected.
- To distinguish the parity bytes of Reed-Solomon, the TEN outputs 'H' for a period of the valid data, and then outputs 'L' for a period of the parity bytes.
- When RS_EN (Register address: 00000001) = '0', Reed-Solomon decoding is not performed and all errors are not corrected. TEN operates normally, but TER outputs 'L'.
  When RS_EN = '1', Reed-Solomon decoding is performed.

Timing

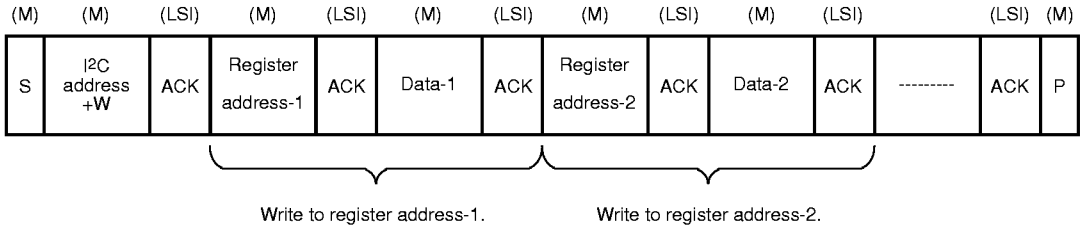


Energy Dispersal Removal

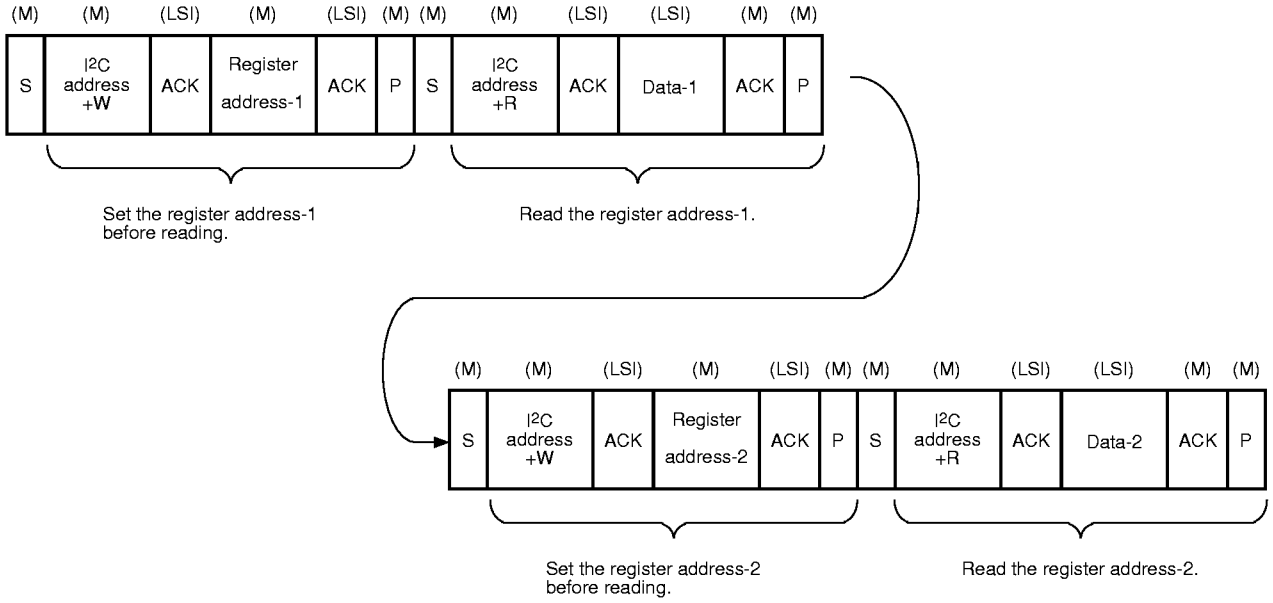
- When ER_EN (Register address: 00000001) = '0', Energy dispersal removal is not performed.
  When ER_EN = '1', Energy dispersal removal is performed.
- Pseudo-Random Binary Sequence (PRBS) Polynomial: $x^{15} + x^{14} + 1$
  The polynomial is initialized into the sequence '100101010000000' every eight packets.

I²C Bus

- Write protocol

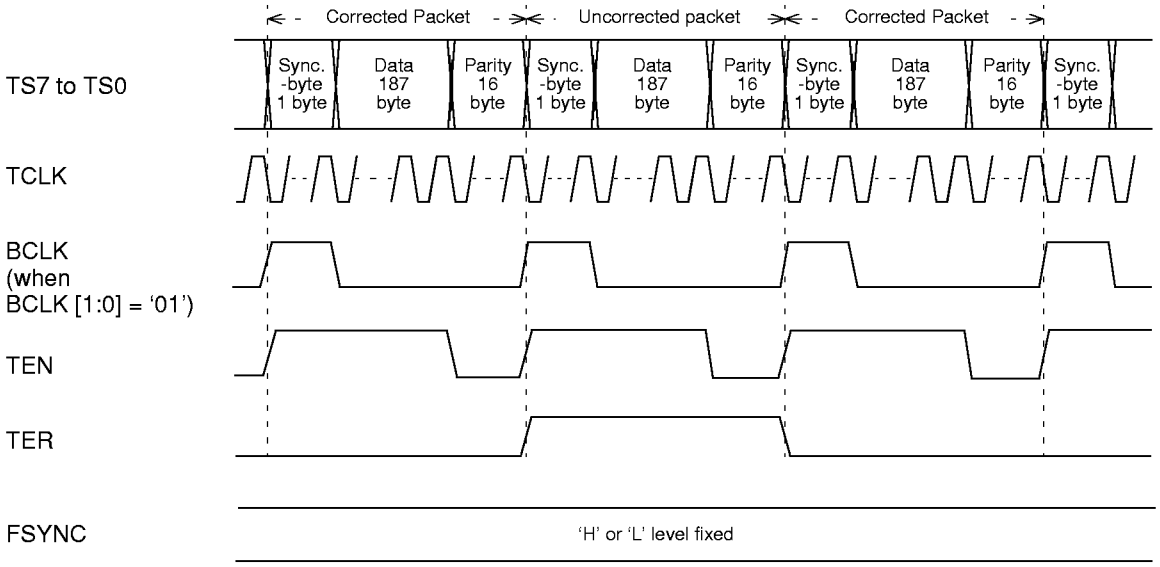


- Read protocol



Notes: S: Start condition
I²C address (7bit): 0001 (ADR2) (ADR1) (ADR0)
ADR [2:0]: User setting
R/W (1bit): 0 = write, 1 = read
Data-n (8bit): Data of register address-n
ACK: Acknowledge
P: Stop condition
(M) : Output from I²C master
(LSI): Output from MB86660A

Output Signal Timing

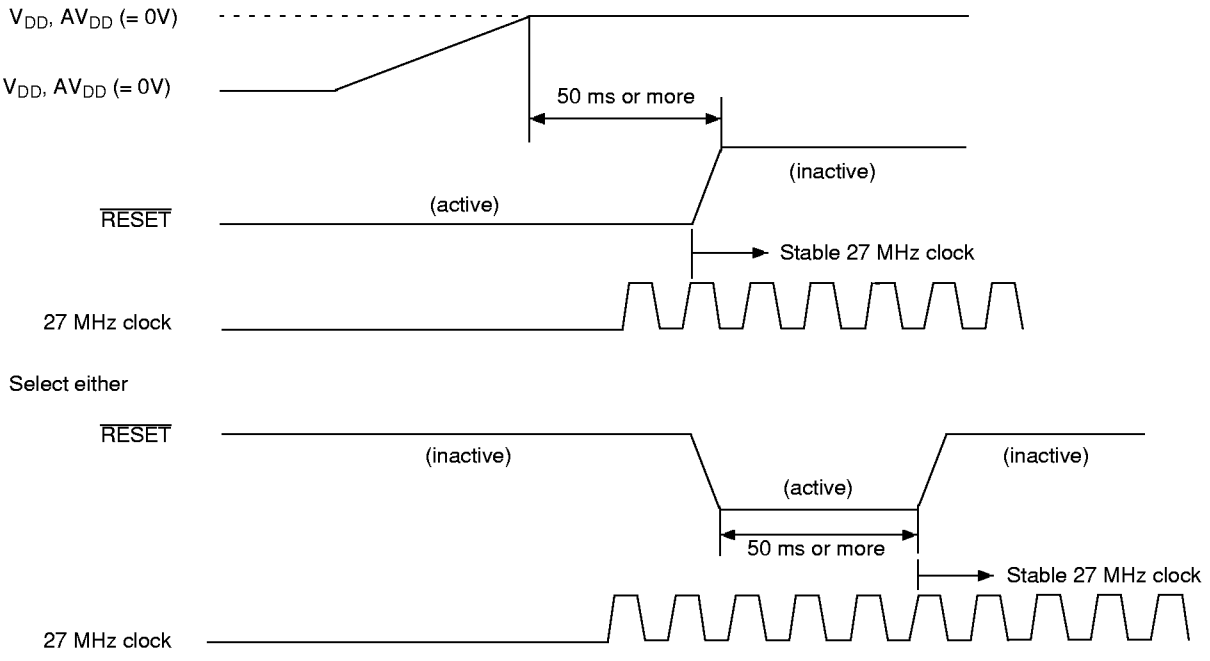


Note: TCLK polarity may be changed by setting the register.

Power-On Reset

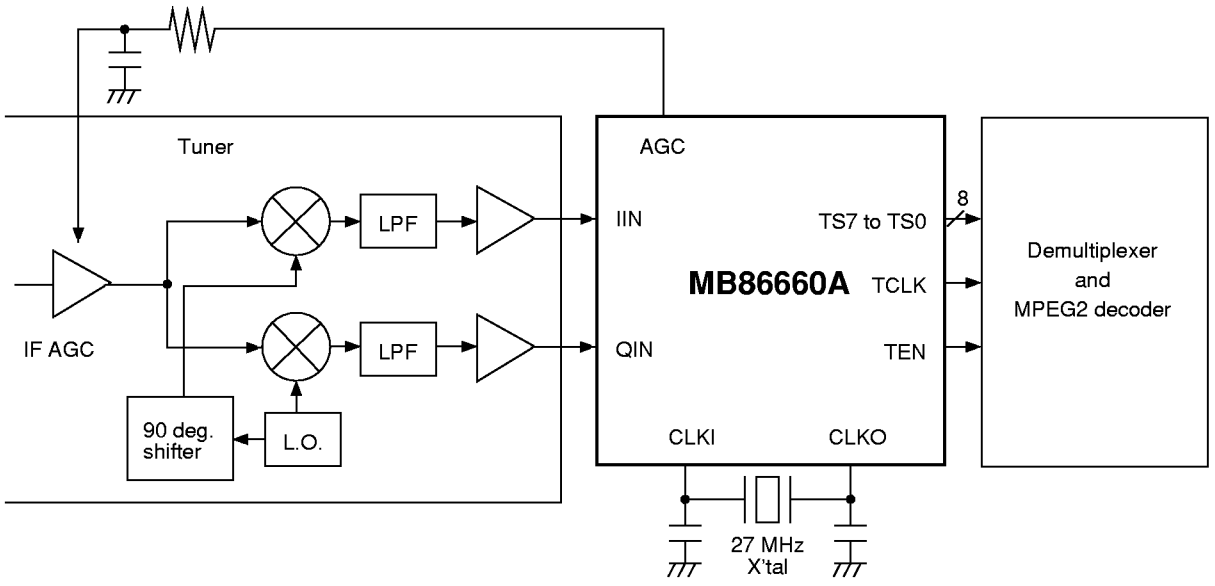
The MB86660A must be reset via the $\overline{\text{RESET}}$ pin when the power is turned on.

- Apply a reset signal to the LSI at power-on, then remove the reset 50 ms after the V_{DD} and AV_{DD} have reached 3.3V or have input a reset pulse width of 50 ms after they reached 3.3V. Note that the 27.0 MHz clock by the crystal oscillator or the external clock of EXTCLK must be stable before the reset is removed. (See the diagram below.)

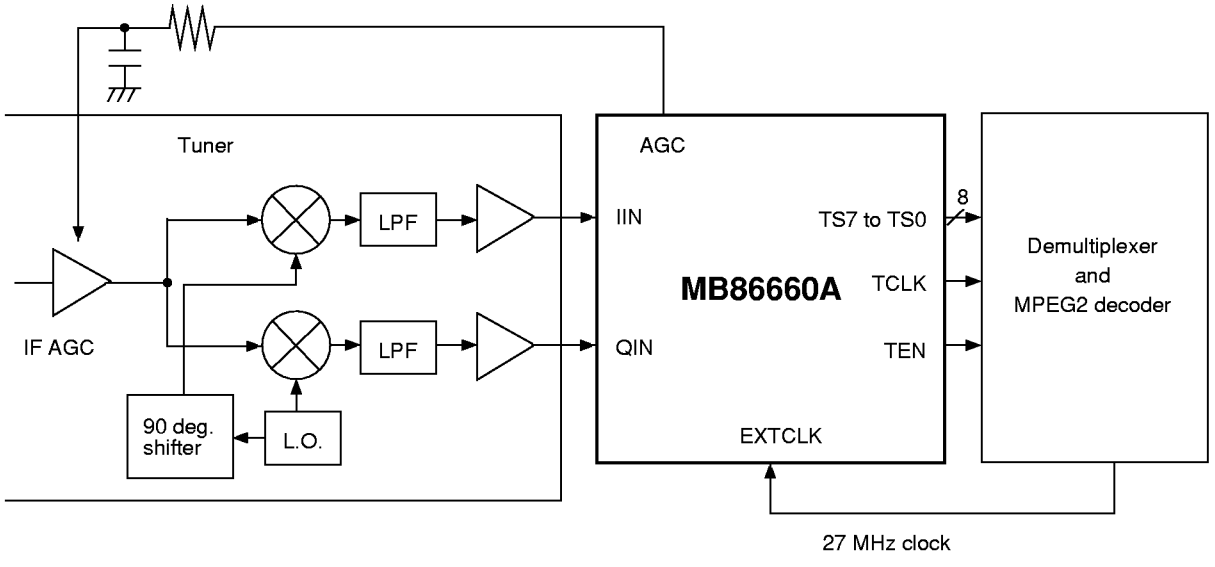


Application Example

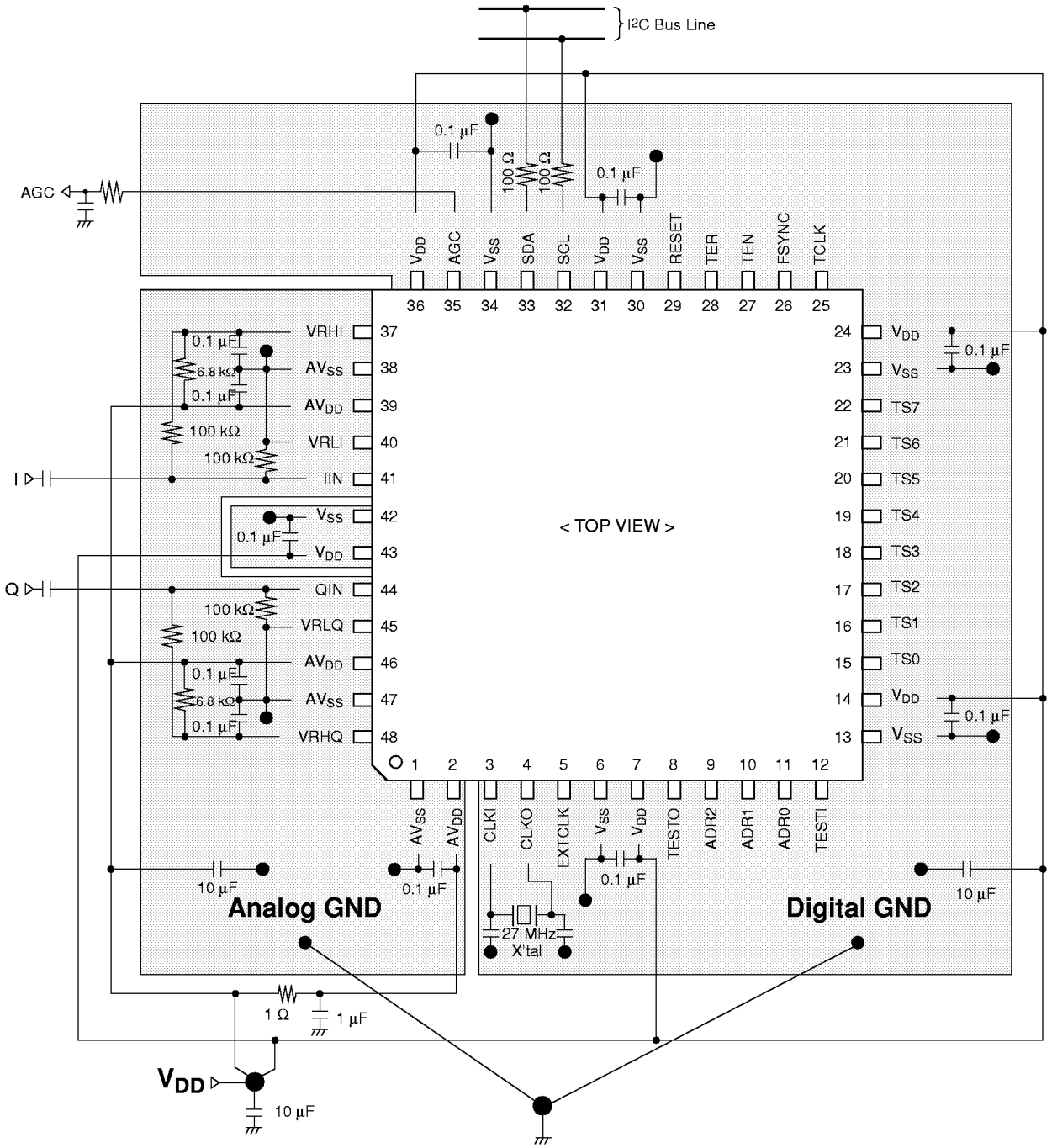
- When a 27 MHz crystal oscillator is used



- When a 27 MHz external clock is used.



Peripheral Circuit Example



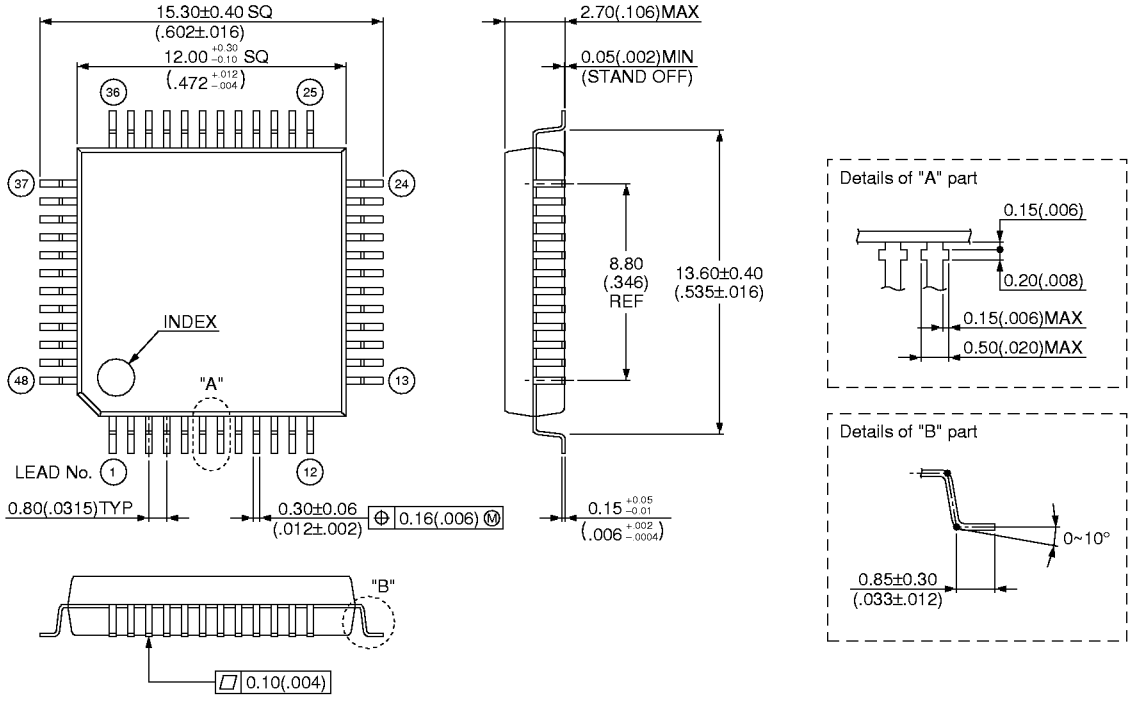
Notes: 1. The analog and digital power supplies should be separated and each GND pattern should be sufficiently wide. Connect the bypass capacitors with good high-frequency characteristics for $V_{DD} - V_{SS}$ and $AV_{DD} - AV_{SS}$. Connect the analog and digital power supply pattern at a point such as the illustration above.

2. Connect the bypass capacitors with good high-frequency characteristics between the analog GND 'AV_{SS}' and VRHI, VRLI, VRHQ and VRLQ which are the reference voltages of the A/Ds. It is very important to stabilize the reference voltages for the A/D. Furthermore, it is recommended to connect a large value of about 10 µF to AV_{SS}.

3. Use a board with 4 layers or more.

Package Dimensions

48-pin plastic QFP
(FPT-48P-M15)



Dimensions in mm (inches)

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