VITESSE

VSC8175
Datasheet

9.953 Gbps to 11.1 Gbps SONET/SDH 16:1 Multiplexer with Clock Generator

FEATURES

- 16:1 SONET/SDH Mux with Clock Generator
- Input FIFO to Simplify Parallel Interface Timing
- Continuous Tuning Operation at 9.953Gb/s to 11.1Gb/s Rates
- LVDS Parallel Data Inputs
- 622MHz to 694MHz Data Clock Input
- Data Polarity Invert
- Bit-Order Swap
- Loss of Lock Detection
- Loss of REFCK Detection
- 622MHz to 694MHz Ref Clock Input
- Divide-by-16 or -64 Clock Output
- 2.1 Watt Typical Power
- +3.3V Single Supply
- Integrated PLL-Based Clock Generator
- Meets SONET OC-192 and SDH STM-64 Jitter Generation Requirements
- Full Compliance with the OIF99.102 Standard
- Even/Odd Parity Checking
- High-Speed Clock Output

GENERAL DESCRIPTION

The VSC8175 consists of a 16:1 multiplexer and a clock generator for use in SONET STS-192/SDH STM-64 systems. Two versions of the device are available: the VSC8175-01 and the VSC8175-02. The 16:1 multiplexer accepts 16 parallel low-voltage, differential swing (LVDS) inputs (D[0:15]±) and (PARITY±) at a data rate of 622.08Mb/s to 669.31Mb/s for VSC8175-01 (622.08Mb/s to 693.75Mb/s for VSC8175-02). This parallel data stream is then serialized into a 9.953Gb/s to 10.709Gb/s output (DOUT±) for VSC8175-01 (9.953Gb/s to 11.1Gb/s output (DOUT±) for VSC8175-02). The clock generator creates the 9.953GHz to 10.709GHz clock signal used to retime the transmitted serialized data for VSC8175-01 (9.953GHz to 11.1GHz for VSC8175-02). The clock generator requires a 622.08MHz to 669.31MHz LVPECL reference clock input (REFCK±) for VSC8175-01 (622.08MHz to 693.75MHz for VSC8175-02). To ease timing constraints on the parallel interface, a 16-bit wide by 8-bit deep FIFO is included. A high-speed clock output (COUT±) is provided that is synchronized to the high-speed serial data output. A divide-by-16 or divide-by-64 LVDS clock output (CK16_64±) is available for use as a clock input to the data source of the parallel inputs (D[0:15]±) and (PARITY±).

Additional features include parity checking of a parity bit (PARITY±) that is clocked in with the 16-bit parallel data, Bit-Order Swap (BITORDER) and Data Polarity Invert (DINVERT). To assist in monitoring device operation, a Loss of Lock (LOLN) alarm and internal temperature diode are included. The VSC8175-01 and VSC8175-02 are packaged in a 90-ball Taped Ball Grid Array (TBGA). The VSC8175-01 and VSC8175-02 have a minimum high-speed clock (COUT±) output specification of 500mV, and clock to data skew (t_{CKQ}) of ±10ps.

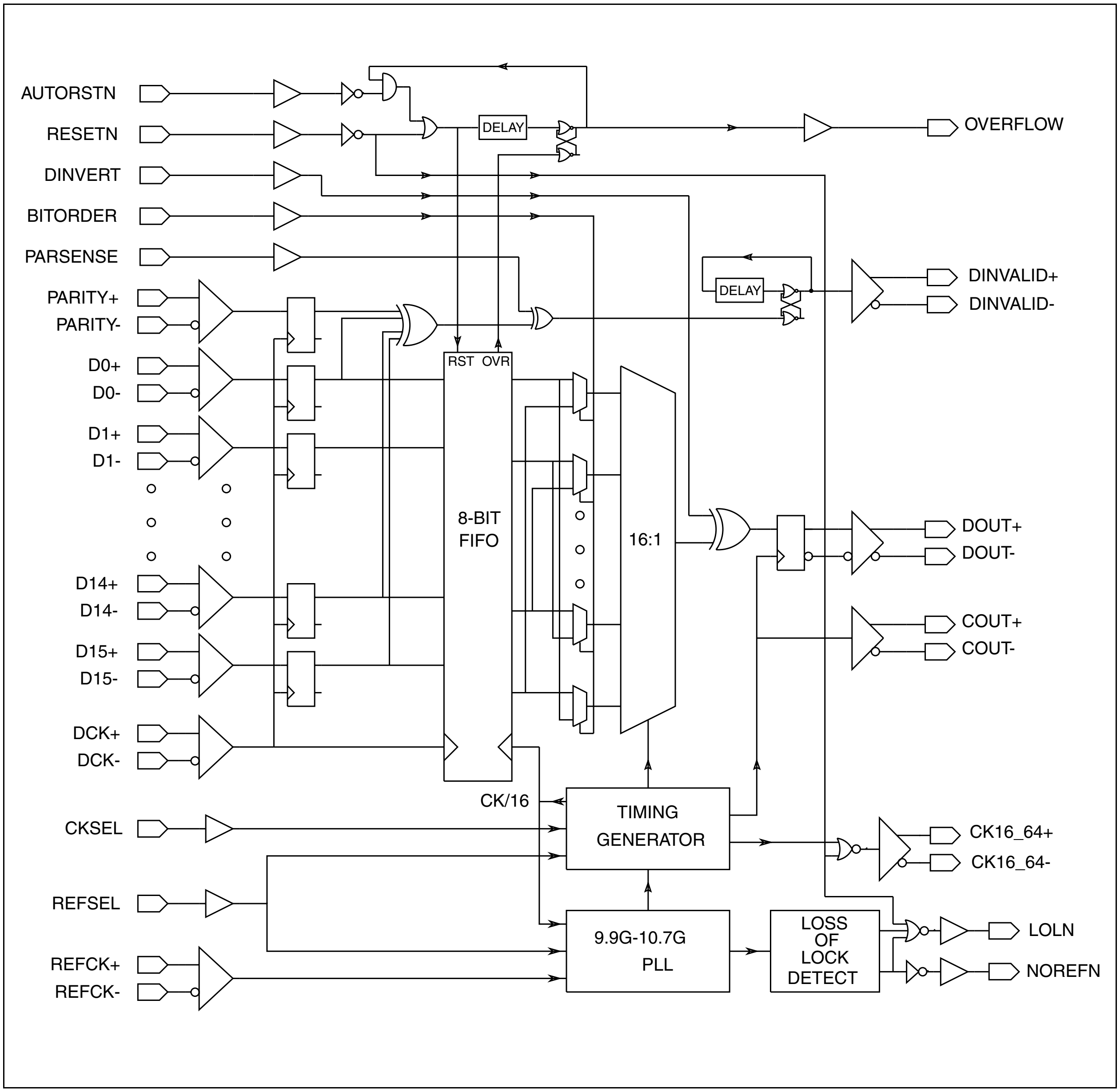


Figure 1. VSC8175 Block Diagram

REVISION HISTORY

This section describes the changes that were implemented in this document. The changes are listed by revision, starting with the most current publication.

Revision 4.3

Revision 4.3 of this datasheet was published in September 2006. The following is a summary of the changes implemented in the datasheet:

- The VSC8175UT-02 device was added along with its data rates and clock frequencies throughout the datasheet. For more information, see "Ordering Information" on page 22.
- All references of the VSC8175UT device were removed.

Revision 4.2

Revision 4.2 of this datasheet was published in May 2004. In revision 4.2 of the document, the modified high-speed clock output was updated in the general description and ordering information.

Revision 4.1

Revision 4.1 of this datasheet was published in May 2004. The following is a summary of the changes implemented in the datasheet:

- The minimum value was updated for the COUT peak-to-peak output swing parameter (VSC8175-01).
- Thermal specifications were added for the VSC8175UT and VSC8175UT-01 device.

Revision 4.0

Revision 4.0 of this datasheet was published in February 2003. This was the first production-level publication of the document.

FUNCTIONAL DESCRIPTION

Low-Speed LVDS Interfaces

The 16 parallel inputs (D[0:15]±), parity bit (PARITY±), and parallel data clock input (DCK±) comprise the VSC8175 low-speed inputs. The VSC8175 is optimized to accept parallel inputs that conform to the LVDS input standard. The reference clock output (CK16_64±), and parity check result (DINVALID±) are also LVDS compatible.

The LVDS I/O has a small differential voltage swing which allows high-speed and low noise with low power dissipation. The output driver has a targeted 50Ω source impedance and the input receiver has a differential 100Ω termination resistor between true and complement on the chip. The LVDS receivers have an internal biasing network, which allows the LVDS inputs to be AC-coupled. A 0.1µF SMT capacitor is recommended for AC-coupling. Figure 2 shows the typical LVDS I/O configuration.

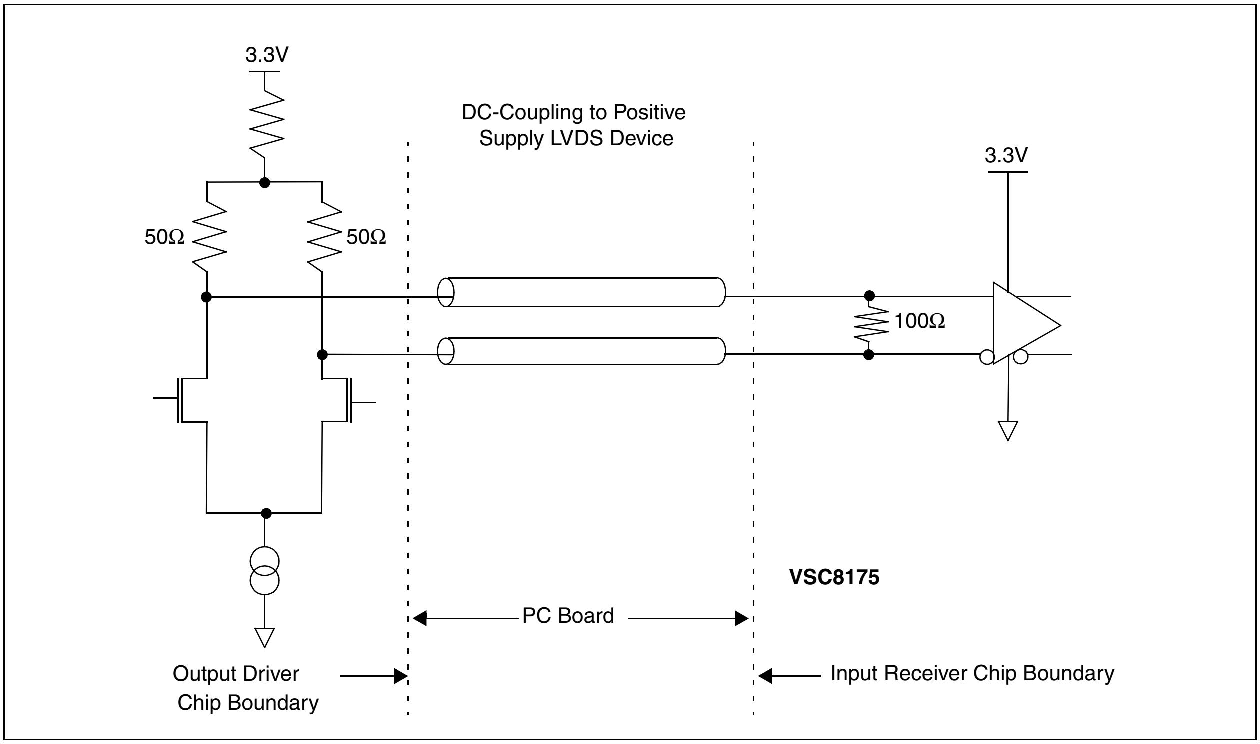


Figure 2. Typical LVDS Compatible Driver/Receiver Interface

REFCK Input Receiver

The REFCK input receiver diagram is depicted in Figure 3 on page 5. The REFCK receiver is LVPECL compatible with DC levels shown in Table 9 on page 14. The on-chip termination is 100Ω between true and complement. An internal bias generator, nominally set at +0.6 • V_{CC}, is provided for AC-coupling. An internal termination tap (REFTERM) is provided to allow adjustment of the input common-mode voltage. It is good practice to put a capacitor between REFTERM and V_{CC} or V_{EE}. Single-ended REFCK operation is possible; however, best jitter performance is obtained by using a differential REFCK. For single-ended operation, REFTERM and REFCK should be shorted together and a clean AC ground provided.

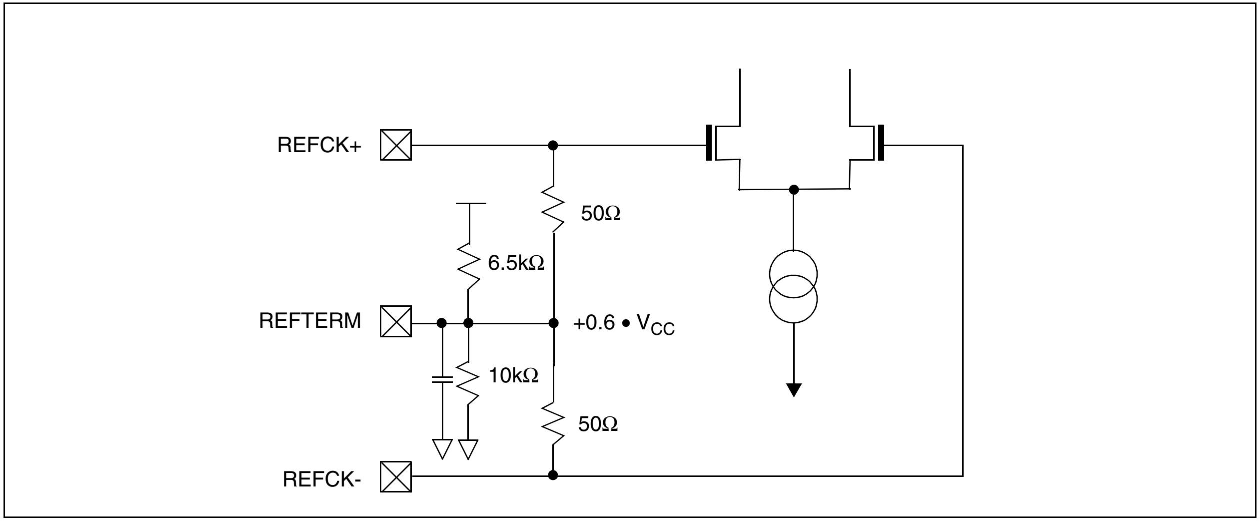


Figure 3. REFCK Input Receiver

FIFO Reset

The 16-bit parallel data is clocked into a 16-bit wide, 8-bit deep FIFO that allows synchronization of the parallel data to the Mux. The data is clocked into the FIFO by the parallel input data clock (DCK±). The RESETN pin (active LOW with an internal pull-up resistor) acts as a reset to the FIFO restoring the FIFO to a position that allows for the maximum amount of skew between DCK± and the internally-generated clock. The VSC8175 contains a FIFO overflow (OVERFLOW) output indication (active HIGH). This alarm output is triggered when the FIFO reaches one word less than the elastic limit for overflow or underflow. There is an auto-reset enable input pin (AUTORSTN), which is active LOW with internal pull-up resistor. If AUTORSTN is LOW, the overflow condition will generate an automatic RESETN signal to reset the FIFO. If AUTORSTN is HIGH, the overflow condition will not generate an automatic FIFO reset and it the responsibility of the user to reset the FIFO using the RESETN pin. In the event of a FIFO reset, some data will be lost. The RESETN, AUTORSTN inputs, and the OVERFLOW output are LVTTL compatible. See Table 1 for Reset FIFO Truth Table.

Table 1. Reset FIFO Truth Table

AUTORSTN	RESETN	Action
0	0	External Reset of FIFO
0	1	Automatic Internally Generated Reset of FIFO
1	0	External Reset of FIFO
1	1	No Reset of FIFO

Reset Function

The chip reset pin (RESETN) performs a chip initialization for predictable start-up conditions. While RESETN is in the active state (active LOW), the FIFO is recentered, CK16_64± is inhibited to a LOW state, and the LOLN pin is in the LOW state, indicating LOL. Once the RESETN condition is no longer active, the lock function reverts back to normal operation.

High-Speed Data Output

For normal bit order (BITORDER = LOW), the high-speed data (DOUT±) is multiplexed in the sequence D0 to D15, with D0 transmitted first. The high-speed data output driver consists of a differential pair designed to drive a 50Ω transmission line. The output driver is source terminated on the die, 50Ω to V_{CC}, minimizing any reflections (see Figure 4). The output may be either DC-coupled or AC-coupled. If AC-coupling is used, the value of the coupling capacitor needs to be sufficiently large to transmit the full spectrum of the data. It is recommended that 0.1µF be used for the coupling capacitor. If used single-ended, the complementary output must be terminated equally.

High-Speed Clock Output

The high-speed clock (COUT±) output is intended to clock a RZ laser driver module (see Table 8 on page 13 for output swing). The clock output is always on and expected to maintain a given phase relationship with respect to the high-speed data (see Table 5 on page 11). The high-speed clock output driver consists of a differential pair designed to drive a 50Ω transmission line. The output driver is source terminated on the die, 50Ω to V_{CC}, minimizing any reflections (see Figure 4). If used single-ended, the complementary output must be terminated equally.

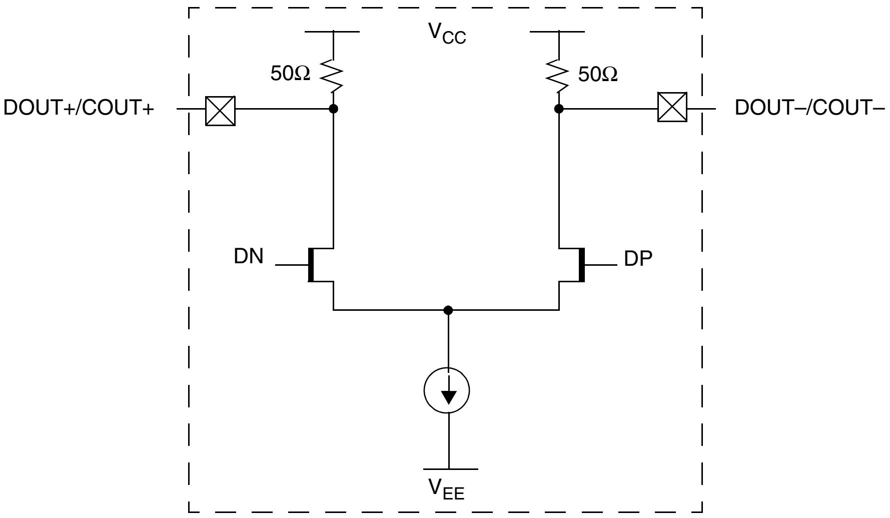


Figure 4. High-Speed Data and Clock Output Driver (COUT±, DOUT±)

Clock Generator

A Phase-Locked Loop (PLL) on the die generates the 9.953GHz to 11.1GHz transmit clock from the externally provided REFCK± input. The PLL uses a loop filter on the die, however, external loop filter capacitors may be used to improve jitter peaking specification (see Table 6 on page 12). The 622.08MHz to 693.75MHz REFCK± should be high quality. Noise on the REFCK± below the loop bandwidth of the PLL will pass through the PLL and appear as jitter on the output. Preconditioning of the REFCK± signal with a VCXO may be required to avoid passing REFCK± jitter to the output. Such a condition would create an output from the VSC8175, which has the REFCK± noise jitter in addition to the intrinsic jitter from the VSC8175 itself.

Parity

Systems employing internal parity are supported by the VSC8175. A parity check is performed between the PARITY± input and the 16 data bits (D[0:15]±). Even parity is expected. In other words, the DINVALID+ output is the XOR of all 16 parallel data+ bits and the PARITY+ input. If the XOR gate fails to confirm even parity, the DINVALID± output will be asserted. If a parity error is detected, the DINVALID± will be asserted. The parity sense pin (PARSENSE) inverts the sense of the parity check:

$$\text{DINVALID+} = (\text{PARSENSE}) \text{ XOR } (\text{PARITY+}) \text{ XOR } (\text{D[0:15]+}) \qquad \textbf{(EQ 1)}$$

10GbE and Forward Error Correction Rate Support

To support 10 Gigabit Ethernet (10GbE), G.975 and G.709 Forward Error Correction (FEC) requirements, the VSC8175-01 will operate at serial data rates of 9.953Gb/s to 10.709Gb/s with parallel input streams of 622Mb/s to 670Mb/s. The VSC8175-02 operates at serial data rates of 9.953Gb/s to 11.1Gb/s with parallel input streams of 622Mb/s to 694Mb/s.

Bit-Order Swap and Data Invert

The BITORDER and DINVERT functions are provided to allow compatibility with framer ASICs having reversed pin ordering. With BITORDER LOW, D0 is the MSB and is the first bit clocked out. Forcing BITORDER HIGH reverses the parallel data pin number ordering such that D15 is the MSB and is clocked out first (see Table 2). DINVERT is LOW for normal data input polarity. Forcing DINVERT HIGH reverses the serial output data true and complement states. Both BITORDER and DINVERT are LVTTL compatible and have internal pull-down resistors.

Table 2. BITORDER and DINVERT Selection

Control Pin	Logic State	Action
BITORDER	0	D0 = MSB and is the first bit out
BITORDER	1	D15 = MSB and is the first bit out
DINVERT	0	Normal Polarity
DINVERT	1	Reverse Polarity

Loss of Lock Detection

The LOLN pin is a status of the Phase-Locked Loop (PLL) condition. LOLN HIGH indicates the PLL is locked to the reference clock. The LOW state indicates a LOL condition with the PLL. LOLN is a LVTTL-compatible output.

No Reference Clock Detection

The NOREFN pin indicates the status of the REFCK condition. When the REFCK± is not detected, the NOREFN output will go LOW within 100ns (typical). Once a REFCK± is detected again, NOREFN will return to HIGH. NOREFN is a LVTTL-compatible output.

The NOREFN indicator is internally logically OR'd into the LOLN indicator. If reference clock stops toggling for any reason, the LOLN alarm will be activated, as well as the NOREF alarm. If the reference clock is detected again, LOLN and NOREF will return inactive, assuming there is not a true LOL condition at that time.

Internal Temperature Resistor

An analog output (TEMPA, TEMPC) from an internal temperature resistor, is also provided for measurement of junction temperature. The temperature monitoring resistor is a metal resistor with a nominal resistance of approximately 18Ω and a temperature coefficient of approximately 0.4%/°C. This resistance will have part-to-part variation, therefore, if accurate temperature sensing is required, each part will need to be individually calibrated. In general, this resistance should fall within 10Ω to 30Ω of normal bounds.

To begin calibration, the VSC8175 must be powered off, including any input signals, such that there will be no power dissipation inside the part to create a thermal gradient. Force the device to various known temperatures and measure the resistance of the part as a function of temperature. Be sure to let the part soak before taking a reading to ensure all thermal transients have settled out. Once this calibration curve has been established, the temperature can be measured under powered-up conditions.

Reference Select Input

The reference clock is a LVPECL input receiver providing a reference for the internal Clock Multiplication Unit (CMU). The DC levels for this receiver are listed in Table 9 on page 14. The CMU requires the following clock frequencies selectable by the REFSEL pin;

- For VSC8175-01, 622.08MHz to 669.31MHz.
- For VSC8175-02, 622.08MHZ to 693.75 MHz.

The REFSEL pin defaults HIGH to 622MHz using an internal pull-up resistor. REFSEL must be LOW in order to use a 155.52MHz reference clock.

NOTE: *SONET jitter generation is not guaranteed with 155.52MHz reference clock operation. For SONET jitter compliance, use a 622MHz to 669.31MHz reference clock. The CMU supports FEC rates up to the industry-standard G.709, 10.709Gb/s rate.*

PLL Output and CKSEL

In order to aid in downstream timing, a clock derived from the PLL is provided. This output is LVDS compatible. The clock output rate is either a divide-by-16 or a divide-by-64 of the internal PLL, depending on the mode selected by the CKSEL pin. The CKSEL pin is not a TTL-compatible input and must be either floated, tied to V_{CC}, or tied to V_{EE}. Table 3 shows the resultant CK16_64± clock output frequency, depending on the conditions stated. When CKSEL is floated (not connected), the CK16_64± pin equals the internal PLL frequency divide-by-64 if REFSEL = 0, and divide-by-16 if REFSEL = 1. When CKSEL is tied to V_{CC}, it always equals the internal PLL divide-by-16 frequency. When CKSEL is tied to V_{EE}, it always equals the internal PLL divide-by-64 frequency.

Table 3. CK16_64 and CKSEL Function

REFSEL	Reference Clock Input (VSC8175-01)	Reference Clock Input (VSC8175-02)	CKSEL	CK16_64± (VSC8175-01)	CK16_64± (VSC8175-02)
0	155.52MHz to 167.34MHz	155.52MHz to 173.4375MHz	Float (No Connect)	155.52MHz to 167.34MHz	155.52MHz to 173.4375MHz
1	622.08MHz to 669.31MHz	622.08MHz to 693.75MHz		622.08MHz to 669.31MHz	622.08MHz to 693.75MHz
0	155.52MHz to 167.34MHz	155.52MHz to 173.4375MHz	V_{CC}	622.08MHz to 669.31MHz	155.52MHz to 173.4375MHz
1	622.08MHz to 669.31MHz	622.08MHz to 693.75MHz		622.08MHz to 669.31MHz	622.08MHz to 693.75MHz

Table 3. CK16_64 and CKSEL Function (continued)

REFSEL	Reference Clock Input (VSC8175-01)	Reference Clock Input (VSC8175-02)	CKSEL	CK16_64± (VSC8175-01)	CK16_64± (VSC8175-02)
0	155.52MHz to 167.34MHz	155.52MHz to 173.4375MHz	V_{EE}(1)	155.52MHz to 167.34MHz	155.52MHz to 173.4375MHz
1	622.08MHz to 669.31MHz	622.08MHz to 693.75MHz		155.52MHz to 167.34MHz	622.08MHz to 693.75MHz

1. When divide-by-64 Reference Clock mode (CKSEL = V_{EE}) is selected, SONET jitter compliance cannot be met.

Power Supplies

Decoupling of the +3.3V power supply is a critical element in maintaining the proper operation of the VSC8175. It is recommended that the V_{CC} power supply be decoupled using a 0.1µF and 0.01µF capacitor placed in parallel on each V_{CC} power supply pin as close to the package as possible. If room permits, a 0.001µF capacitor should also be placed in parallel with the 0.1µF and 0.01µF capacitors mentioned above. Recommended capacitors are low-inductance ceramic SMT X7R devices. For the 0.1µF capacitor, a 0603 package should be used. The 0.01µF and 0.001µF capacitors can be either 0603 or 0402 packages.

For low-frequency decoupling, many 47µF tantalum low-inductance SMT capacitors should be spread over the board's main +3.3V power supply and placed close to the C-L-C pi filter.

SPECIFICATIONS

AC Characteristics

Over Recommended Operating Conditions.

Table 4. Low-Speed Inputs/Outputs

Symbol	Parameter	Min	Typ	Max	Unit	Condition
t_{DCREF}	REFCK± Duty Cycle	40		60	%	
t_R, t_F	REFCK± Rise and Fall Time	100		400	ps	REFCK = 622MHz to 694MHz
t_{ER}	REFCK Edge Rate	1.25			V/ns	REFCK = divide-by-16
CK_{DC}	CK16_64± Duty Cycle	45		55	%	
t_{OR}, t_{OF}	CK16_64± Rise and Fall Time			250	ps	V_{CC} = +3.3V See Figure 7.
t_{DINV}	DINVALID± Pulse Width	100			ns	
t_R, t_F	DINVALID± Rise and Fall Time			400	ps	
t_{IR}, t_{IF}	D[0:15]± Rise and Fall Time	100		250	ps	
t_{DCDCK}	DCK± Duty Cycle	40		60	%	See Figure 5.
t_{DSU}	D[0:15]± Setup Time Before the Rising Edge of DCK+	250			ps	See Figure 5.
t_{DH}	D[0:15]± Hold Time After the Rising Edge of DCK+	250			ps	See Figure 5.
F_{OVF}	FIFO Overflow HIGH Pulse Width	100	300		ns	Characterized, but not tested.

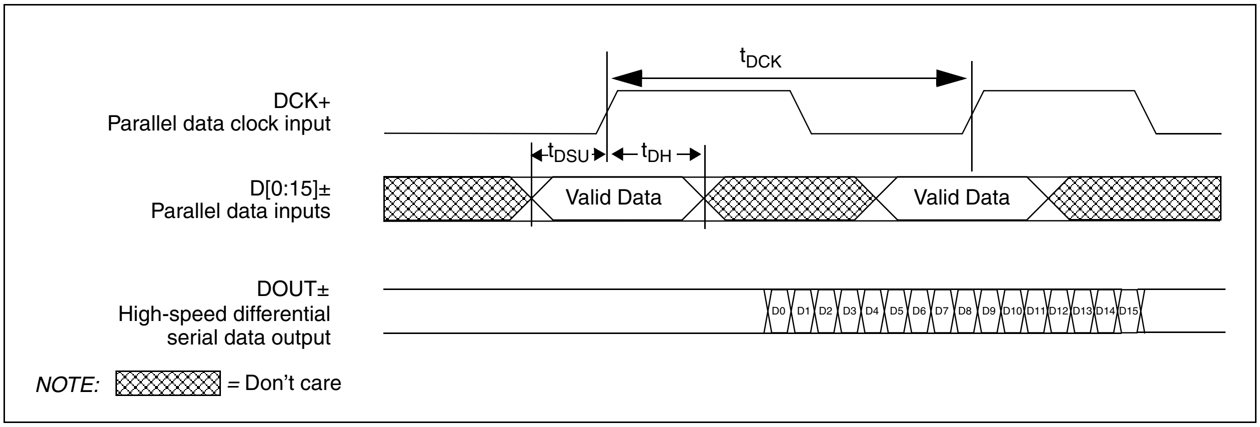


Figure 5. Low-Speed Input Timing Waveforms

Table 5. High-Speed Outputs

Symbol	Parameter	Min	Typ	Max	Unit	Condition
t_R, t_F	DOUT±, COUT± Rise and Fall Time		25	35	ps	20% to 80% into 50Ω load. See Figure 7.
DC_{COUT}	COUT± Duty Cycle	40		60	%	
t_{CKQ}	DATA Time With Respect to Rising COUT± Edge	–10		+10	ps	Measured at COUT frequency of 11.1GHz. Reference clock = 693.75MHz. See Figure 6.
S_{22}	Output Return Loss, 0GHz to 5GHz			–15	dB	Characterized, but not tested.
S_{22}	Output Return Loss, 5GHz to 8GHz			–10	dB	Characterized, but not tested.

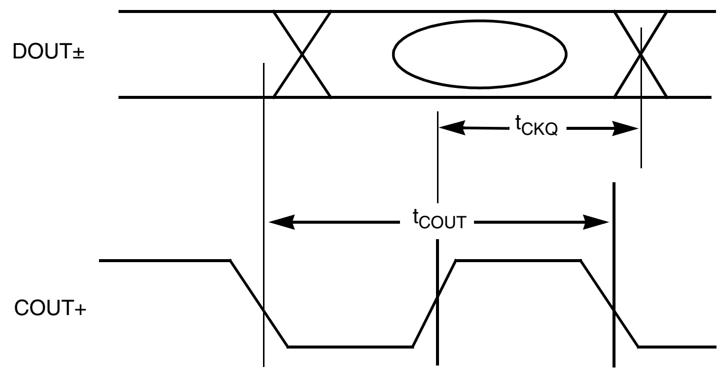


Figure 6. Output Data Eye

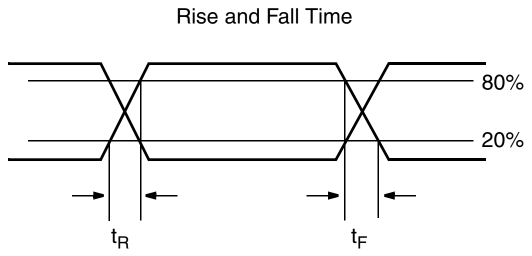


Figure 7. Parametric Measurement Information

Table 6. Clock Multiplier Performance

Symbol	Parameter	Min	Typ	Max	Unit	Condition
f_{REFCK}	REFCK Frequency (VSC8175-01)	622.08		669.31	MHz	See Table 3
f_{REFCK}	REFCK Frequency (VSC8175-01)	155.52		167.34	MHz	See Table 3
f_{REFCK}	REFCK Frequency (VSC8175-02)	622.08		693.75	MHz	See Table 3
f_{REFCK}	REFCK Frequency (VSC8175-02)	155.52		173.4375	MHz	See Table 3
J_{GD}	DOUT± Jitter Generation, Peak-to-Peak			0.09	UI	50kHz to 80MHz, soldered down, f = 10GHz, 2^{31}–1 PRBS, 625MHz reference clock.(1)
J_{GC}	COUT± Jitter Generation, Peak-to-Peak			0.09	UI	50kHz to 80MHz, soldered down, f = 10GHz, 2^{31}–1 PRBS, 625MHz reference clock.(1)
L_{BW}	Loop Bandwidth	2		8	MHz	Characterized, but not tested.
J_P	Jitter Peaking			0.1	dB	Requires external filter capacitor. Characterized, but not tested.

1. *Specification is after compensating for test equipment jitter and measurement techniques.*

Table 7. Loss of Lock and No Reference

Symbol	Parameter	Min	Typ	Max	Unit	Condition
$LOLN_{ST}$	LOLN Set Time	0.5		100	µs	Guaranteed, but not tested. REFCK frequency error of less than 10,000ppm.
$LOLN_{CR}$	LOLN Clear Time	125		250	µs	Guaranteed, but not tested. REFCK frequency error of less than 10,000ppm.
NRF_{ST}	NOREFN Set Time		100		ns	Guaranteed, but not tested.

DC Characteristics

Over Recommended Operating Conditions.

Table 8. High-Speed Outputs

Symbol	Parameter	Min	Typ	Max	Unit	Condition
ΔV_{SWING}	DOUT± Peak-to-Peak Output Swing	600		1200	mV_{p-p}	AC-coupled with 0.1μF capacitor into a 50Ω load. One side of differential signal. See Figure 8.
ΔV_{SWING}	COUT± Peak-to-Peak Output Swing	500		1200	mV_{p-p}	AC-coupled with 0.1μF capacitor into a 50Ω load. One side of differential signal. See Figure 8.
V_{OH}	Voltage Output HIGH	$V_{CC} - 200$		V_{CC}	mV	
V_{OL}	Voltage Output LOW			$V_{OH} - \Delta V_{SWING}$	mV	

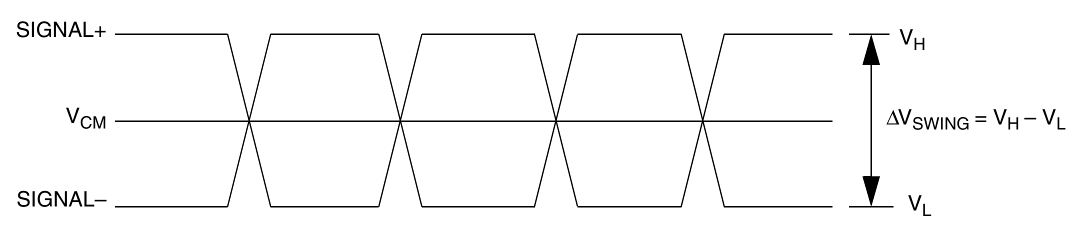


Figure 8. Differential Signal

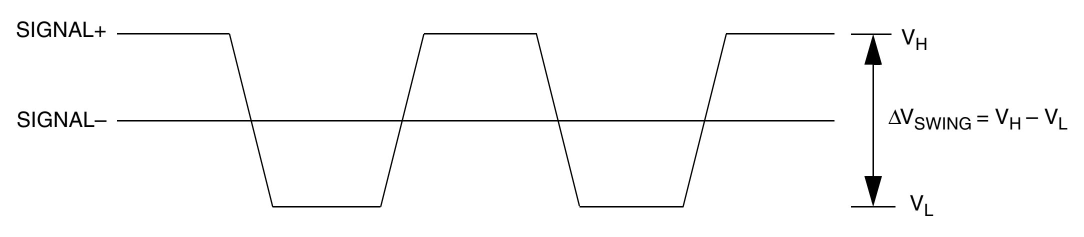


Figure 9. Single-Ended Signal

Table 9. Low-Speed Inputs/Outputs

Symbol	Parameter	Min	Typ	Max	Unit	Condition
LVDS Inputs						
ΔV_{DIFF}	Absolute Voltage Differential Peak-to-Peak Swing	100			mV_{p-p}	Terminated 100Ω between true and complement. One side of differential signal. See Figure 8.
V_I	Input Voltage Range	0.3		2.4	V	
V_{IDIFF}	Input Differential Offset	18	25		mV	
R_{IN}	Input Resistance Between Differential LVDS Input Pads	80	100	120	Ω	
REFCK Inputs						
ΔV_{REFCK}	REFCK Input Voltage	150		1000	mV_{p-p}	One side of differential signal, REFCK = 622MHz to 694MHz. See Figure 8.
		300		1000	mV_{p-p}	Single-ended peak-to-peak, REFCK = 622MHz to 694MHz. See Figure 9.
$V_{REFTERM}$	REFTERM Voltage		$0.6 \bullet V_{CC}$		mV	
V_{IH}	REFCK Input HIGH			$V_{CC} - 700$	mV	
V_{IL}	REFCK Input LOW	$V_{CC} - 2000$			mV	
LVTTL Inputs						
V_{IH}	Voltage Input HIGH	2.0			V	
V_{IL}	Voltage Input LOW			0.8	V	
I_{IH}	Current Input HIGH			+500	µA	$V_{IH} = V_{CC}$
I_{IL}	Current Input LOW			–500	µA	$V_{IL} = 0V$
CKSEL Inputs						
V_{IH}	Voltage Input HIGH	2.8			V	Guaranteed, but not tested.
V_{IF}	Voltage Input Float	$V_{CC}/2 - 0.3$		$V_{CC}/2 + 0.3$	V	Guaranteed, but not tested.
V_{IL}	Voltage Input LOW			0.5	V	Guaranteed, but not tested.
LVDS Outputs						
V_{ODIFF}	Voltage Output Differential	250		600	mV_{p-p}	One side of differential signal. See Figure 8.
V_{OH}	Voltage Output HIGH			1675	mV	
V_{OL}	Voltage Output LOW	925			mV	
R_O	Output Impedance	40		140	Ω	Guaranteed but not tested.
LVTTL Outputs						
V_{OH}	Voltage Output HIGH	2.4			V	$I_{OH} = 1mA$

Table 9. Low-Speed Inputs/Outputs (continued)

Symbol	Parameter	Min	Typ	Max	Unit	Condition
V_{OL}	Voltage Output LOW			0.4	V	$I_{OL} = –1mA$

Table 10. Power Dissipation

Symbol	Parameter	Min	Typ	Max	Unit	Condition
I_{CC}	Supply Current		622	765	mA	Outputs unloaded
P_D	Power Dissipation		2.05	2.65	W	Outputs unloaded

Table 11. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Power Supply Voltage	3.135	3.3	3.465	V
T_C	Case Temperature Range Under Bias	0		+85	°C

Table 12. Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage	–0.5		+3.8	V
	DC Input Voltage (Differential inputs)	–0.5		V_{CC} +0.5	V
	Output Current (Differential outputs)	–50		+50	mA
T_C	Case Temperature Under Bias	–55		+125	°C
T_S	Storage Temperature	–65		+150	°C
V_{ESD}	ESD (Human Body Model)				
	High-Speed Outputs, C2PN			200	V
	All Other I/O			500	V

Stresses listed under Absolute Maximum Ratings may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE

This device can be damaged by ESD. Vitesse recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

PACKAGE INFORMATION

Heat sink up and cavity-down package. Heat sink should be either tied to V_{EE} or electrically floated.

Figure 10. Pin Diagram for 90-Ball TBGA (UT)

Table 13. Pin Identification for 90-Ball TBGA (UT)

Ball Site	Signal	I/O	Level	Description
A14	REFCK–	I	LVPECL	Reference clock, complement. See Table 3.
A13	VCC	Pwr	+3.3V	Most positive supply
A12	COUT+	O	CML	High-speed clock, true
A10	COUT–	O	CML	High-speed clock, complement
A9	VCC	Pwr	+3.3V	Most positive supply
A8	DOUT+	O	CML	High-speed data output, true
A6	DOUT–	O	CML	High-speed data output, complement
A5	VCC	Pwr	+3.3V	Most positive supply
A4	AUTORSTN	I	LVTTL	Auto FIFO reset enable: LOW = enable auto FIFO reset on overflow HIGH = disable auto FIFO reset (internal 30kΩ pull-up resistor to V_{CC})
A3	VCC	Pwr	+3.3V	Most positive supply
A2	TEMPA	O	Analog	Temperature resistor
A1	TEMPC	O	Analog	Temperature resistor
B14	REFCK+	I	LVPECL	Reference clock, true. See Table 3.
B13	VEE	Pwr	GND	Most negative supply
B12	NC			No connect(1)
B9	VEE	Pwr	GND	Most negative supply
B6	NC			No connect(1)
B5	VEE	Pwr	GND	Most negative supply
B4	OVERFLOW	O	LVTTL	FIFO overflow indication, active HIGH
B3	NC			No connect(1)
B2	VEE	Pwr	GND	Most negative supply
B1	VEE	Pwr	GND	Most negative supply
C14	VCC	Pwr	+3.3V	Most positive supply
C13	REFTERM	I	Analog	Termination for REFCK input receiver
C2	VCC	Pwr	+3.3V	Most positive supply
C1	NC			No connect(1)
D14	C2P–	I	Analog	External loop filter #1 capacitor, complement
D13	C2P+	I	Analog	External loop filter #1 capacitor, true
D2	PARSENSE	I	LVTTL	Parity polarity sense (internal 30kΩ pull-down resistor to V_{EE})
D1	NOREFN	O	LVTTL	No reference clock detected, active LOW
E14	C2N–	I	Analog	External loop filter #2 capacitor, complement
E13	C2N+	I	Analog	External loop filter #2 capacitor, true
E2	VCC	Pwr	+3.3V	Most positive supply
E1	DINVERT	I	LVTTL	Data invert (HIGH inverts input data polarity, internal 30kΩ pull-down resistor to V_{EE})
F14	VCC	Pwr	+3.3V	Most positive supply
F13	RESETN	I	LVTTL	Reset active LOW (internal 30kΩ pull-up resistor to V_{CC})

Table 13. Pin Identification for 90-Ball TBGA (UT) (continued)

Ball Site	Signal	I/O	Level	Description
F2	BITORDER	I	LVTTL	Bit-order swap: LOW = D0 is MSB and first out HIGH = D15 is MSB and first out (internal 30kΩ pull-down resistor to V_{EE})
F1	REFSEL	I	LVTTL	Reference clock select: LOW = 155.52MHz to 173.4375MHz HIGH = 622.08MHz to 693.75MHz (internal 30kΩ pull-up resistor to V_{CC})
G14	CK16_64–	O	LVDS	PLL output clock, complement
G13	VEE	Pwr	GND	Most negative supply
G2	DINVALID+	O	LVDS	Parity output status, true
G1	DINVALID–	O	LVDS	Parity output status, complement
H14	CK16_64+	O	LVDS	PLL output clock, true
H13	CKSEL	I	3-Level	CK16_64 mode select (V_{EE}, $V_{CC,}$ or float) (internal 30kΩ pull up resistor to V_{CC}; internal 30kΩ pull-down resistor to V_{EE}). See Table 3.
H2	VEE	Pwr	GND	Most negative supply
H1	VCC	Pwr	+3.3V	Most positive supply
J14	VCC	Pwr	+3.3V	Most positive supply
J13	LOLN	O	LVTTL	Loss of PLL lock indication, active LOW
J2	PARITY–	I	LVDS	Low-speed parity input, complement
J1	PARITY+	I	LVDS	Low-speed parity input, true
K14	D15–	I	LVDS	Low-speed data input, complement
K13	D15+	I	LVDS	Low-speed data input, true
K2	D0–	I	LVDS	Low-speed data input, complement
K1	D0+	I	LVDS	Low-speed data input, true
L14	D14–	I	LVDS	Low-speed data input, complement
L13	D14+	I	LVDS	Low-speed data input, true
L2	D1–	I	LVDS	Low-speed data input, complement
L1	D1+	I	LVDS	Low-speed data input, true
M14	D13–	I	LVDS	Low-speed data input, complement
M13	D13+	I	LVDS	Low-speed data input, true
M2	D2–	I	LVDS	Low-speed data input, complement
M1	D2+	I	LVDS	Low-speed data input, true
N14	D12–	I	LVDS	Low-speed data input, complement
N13	VEE	Pwr	GND	Most negative supply
N12	D11–	I	LVDS	Low-speed data input, complement
N11	D10–	I	LVDS	Low-speed data input, complement
N10	D9–	I	LVDS	Low-speed data input, complement
N9	D8–	I	LVDS	Low-speed data input, complement
N8	VCC	Pwr	+3.3V	Most positive supply
N7	VEE	Pwr	GND	Most negative supply

Table 13. Pin Identification for 90-Ball TBGA (UT) (continued)

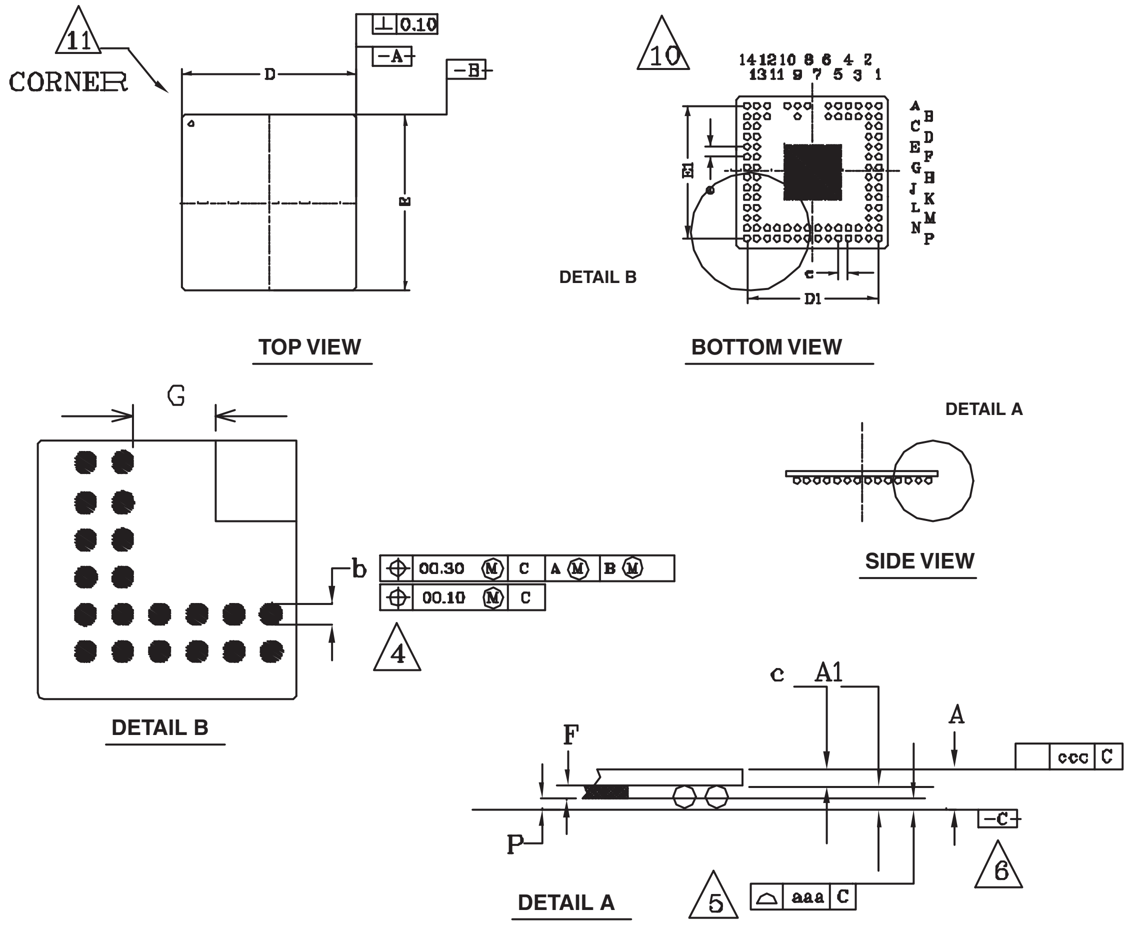
Ball Site	Signal	I/O	Level	Description
N6	D7+	I	LVDS	Low-speed data input, true
N5	D6+	I	LVDS	Low-speed data input, true
N4	D5+	I	LVDS	Low-speed data input, true
N3	D4+	I	LVDS	Low-speed data input, true
N2	VEE	Pwr	GND	Most negative supply
N1	D3+	I	LVDS	Low-speed data input, true
P14	D12+	I	LVDS	Low-speed data input, true
P13	VCC	Pwr	+3.3V	Most positive supply
P12	D11+	I	LVDS	Low-speed data input, true
P11	D10+	I	LVDS	Low-speed data input, true
P10	D9+	I	LVDS	Low-speed data input, true
P9	D8+	I	LVDS	Low-speed data input, true
P8	DCK–	I	LVDS	Clock low-speed data, complement
P7	DCK+	I	LVDS	Clock low-speed data, true
P6	D7–	I	LVDS	Low-speed data input, complement
P5	D6–	I	LVDS	Low-speed data input, complement
P4	D5–	I	LVDS	Low-speed data input, complement
P3	D4–	I	LVDS	Low-speed data input, complement
P2	VCC	Pwr	+3.3V	Most positive supply
P1	D3–	I	LVDS	Low-speed data input, complement

[1] *No connect (NC) pins must be left unconnected or floating. Connecting any of these pins to either the positive or negative power supply rails can cause improper operation or failure of the device; or in extreme cases, cause damage to the device.*

Table 14. Power Supply Summary for 90-Ball TBGA (UT)

Ball Site	Power	Level	Description
A3, A5, A9, A13, C2, C14, E2, F14, H1, J14, N8, P2, P13	V_{CC}	+3.3V	Most positive supply
B1, B2, B5, B9, B13, G13, H2, N2, N7, N13	V_{EE}	GND	Most negative supply

All supplies that reference the same voltage may be connected to the same power supply plane. Appropriate power supply noise suppression should be applied to optimize the performance of the device.



DIMENSIONAL REFERENCES			
REF.	MIN.	TYP.	MAX.
A	1.25	1.40	1.55
A1	0.45	0.5	0.55
D	14.80	15.00	15.20
D1	13.00 (BSC)		
E	14.80	15.00	15.20
E1	13.00 (BSC)		
b	0.54	0.64	0.74
c	0.80	0.90	1.00
M	14		
N	90		
aaa			0.25
ccc			0.25
e	1.00 TYP.		
P	0.15		
G	0.35		
F			0.40

NOTES:

1. All dimensions are in millimeters.
2. “e” represent the basic solder ball grid pitch.
3. “M” represents the basic solder ball matrix size, and symbol “N” is the maximum allowable number of balls after depopulating.
4. “b” is measured at the maximum solder ball diameter parallel to primary datum -C- .
5. Dimension”aaa” is measured parallel to primary datum -C- .
6. Primary datum - C- and seating plane are defined by the spherical crowns of the solder balls.
7. Package surface shall be black oxide.
8. Cavity depth varies with die thickness.
9. Substrate material base is copper.
10. Bilateral tolerance zone is applied to each side of package body.
11. 45 deg. 0.35MM chamfer corners and white dot for Pin 1 identification.
12. “G” is measured at the edge of encapsulant to the inner edge of ball pad.
13. Dimension "F" is measured for max encapsulation height.
14. Dimensioning and tolerancing per ASME Y14.5M-1994.

Figure 11. Package Drawing for 90-Ball TBGA (UT)

Thermal Specifications

Thermal specifications for this device are based on the JEDEC standard EIA/JESD51-2 and have been modeled using a four-layer test board with two signal layers, a power plane, and a ground plane (2s2p PCB). For more information, see the JEDEC standard.

Table 15. Thermal Resistances

Part Number	θ_{JC}	θ_{JA} (°C/W) vs. Airflow (ft/min)		
		0	**100**	**200**
VSC8175UT-01	4	28	24.5	22.3
VSC8175UT-02	4	28	24.5	22.3

To achieve results similar to the modeled thermal resistance measurements, the guidelines for board design described in the JEDEC standard EIA/JESD51 series must be applied. For information about specific applications, see the following:

EIA/JESD51-5, *Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms*

EIA/JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*

EIA/JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

EIA/JESD51-10, *Test Boards for Through-Hole Perimeter Leaded Package Thermal Measurements*

EIA/JESD51-11, *Test Boards for Through-Hole Area Array Leaded Package Thermal Measurements*

Moisture Sensitivity

This device is rated moisture sensitivity level 3 or better as specified in JEDEC standard IPC/JEDEC J-STD-020B. For more information, see the JEDEC standard.

ORDERING INFORMATION

VSC8175 SONET/SDH 16:1 Multiplexer with Clock Generator

Part Number	Description
VSC8175UT-01	90-Ball TBGA, 15mm x15mm x 1.4mm Body, 9.953Gb/s to 10.709Gb/s Operation High-Speed Output Clock Amplitude: 500mV minimum Clock to Data Skew (t_{CKQ}): ±10ps Temperature Range Under Bias: 0°C case to +85°C case
VSC8175UT-02	90-Ball TBGA, 15mm x15mm x 1.4mm Body, 9.953Gb/s to 11.1Gb/s Operation High-Speed Output Clock Amplitude: 500mV minimum Clock to Data Skew (t_{CKQ}): ±10ps Temperature Range Under Bias: 0°C case to +85°C case

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