29C70

ATM Adaptation Layer Controller for AAL 3/4 and AAL5

Description

The 29C70 ATM Adaptation Layer Controller for AAL3/4 and 5 implements CCITT recommentation I.363. The AAL3/4 and AAL5 are used for data transmission over an ATM Network. The 29C70 is designed to interface to ATM Network with the maximum speed of 155 MBit/s. The device integrates a transmitter, receiver and a DMA controller to interface with external message memory. The maximum data transfer rate to message memory is 800 MBit/s. The DMA controller has 24-Bit address bus and it is capable of addressing 16 MBytes of message memory. A general control unit provides a full chip control with a microprocessor interface. The microprocessor has a separate 16-Bit data and 11-Bit address bus to communicate with the 29C70. This bus is dedicated for programming the device and controlling the status of the operations. The transmitter and receiver are connected to an external ATM LAYER controller with a 8-bit (8-Bit in, 8-Bit out in parallel) data bus in order to decrease the clock speed on the ATM interface. The device provides also errors metering and internal loop capabilities for testing purposes. The 29C70 has a maximum system clock speed of 25 MHz.

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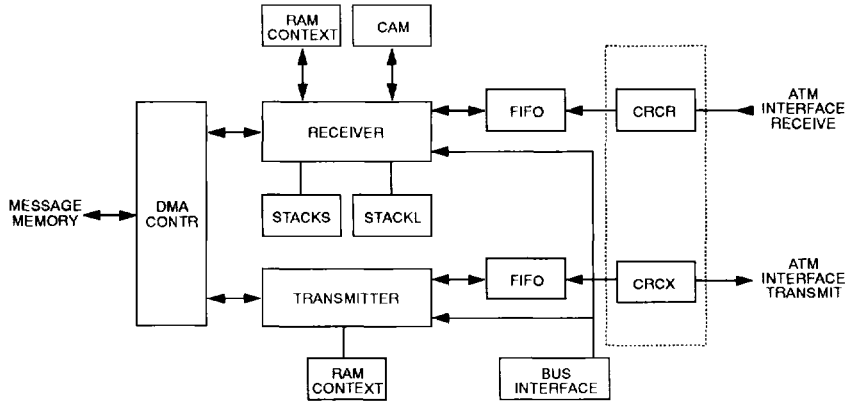
Features

- Asynchronous transfer mode (ATM) adaptation layer controller for AAL3/4 and AAL5
- Integrates receiver, transmitter, DMA controller and control unit
- Performs segmentation and reassembly (SAR), and part of the convergence sub-layer control (CS)
- Full duplex operation for 64 receive and transmit messages simultaneously
- Transmit multiplexing capability. 4 channels within a VC and 16 VCs in parallel
- 8-Bit parallel interface to ATM layer controller
- 32-Bit data and 24-bit address bus to message memory
- 16-Bit data and 11-bit address bus to local microprocessor for register programming and status information
- 155 Mbit/s ATM network connection and 800 Mbit/s message memory connection
- Internal loop capability for testing and errors metering
- 25 MHz system clock
- PQFP 208 package

Functional Block Diagram



Functional Description

Receiver

The Receiver is designed to be connected to an external ATM LAYER INTERFACE UNIT with an 8-Bit data bus, an associated data clock, an ATM CELL SYNC Strobe, an Additional translated VPI/VCI information (VX), and AAL number on a 6-bit bus. The 29C70 has a programmable AAL number so that up to 24 AAL controllers can be connected on the same ATM LAYER Bus.

The Receiver can support up to 64 messages simultaneously for 64 different VPI/VCI/MID. The 29C70 processes the VPI/VCI information which is translated by the ATM LAYER Interface Unit on a 6-Bit words called VX.

An internal associative memory is used to create a new context (new message) fetch an existing context (on going message) or to kill a context (end of message or error). The contexts are stored internally on the chip. This dynamic handling of the context allows to support more than 64 virtual connetions. The Receiver also implements a 4 cells FIFO as an elastic store.

The Receiver transfers the messages to the external message memory through the internal DMA controller. The DMA controller description table is stored internally on the context RAM which is located on the chip. Additionally, 2 stacks, 32 descriptor pointers each, is also provided. The first Stack is for small messages and the second Stack for large messages. The local microprocessor is responsible of maintaining enough free descriptor pointers in each stack. Each time when a new message is starting (BOM, SSM) a new descriptor pointer is fecthed from one of the stacks. Each time when the message is ended (EOM, SSM) a complete status is assembled in a queue on the external message memory by the DMA Controller and it can be red by a HOST or a local microprocessor. Additionally an interrupt is generated for 1 or 15 messages to local microprocessor.

The receiver handles the SAR and CS layers according to CCITT recommentation I.363. It detects errors such as CRC, Tempo, Overflow and Sequencing. The CPCS-PDU shall be checked by the processor (CPI, BETAG, lenght for AAL3/4, CPCS Trailer, CPI, lenght for AAL5).

Transmitter

The Transmitter is connected to the external ATM LAYER INTERFACE Unit with an 8-Bit data bus, an associated data clock, an ATM CELL Sync strobe, an multiplex output for an request to send through the ATM Layer Interface, a 6 bit input control bus to indicate which AAL controller is authorized to transmit a cell. Up to 24 AAL controllers can be connected to the same ATM Layer Interface.

The Transmitter supports 64 channels with 16 VC and same level 4 multiplexed or/and chained channels per VC. The Transmitter controls the throughput (cell/second) selectively on each VC (n × 64 kBit/s). Each active channel within a VC transmits a cells under controlled circular mechanism. The Transmitter has a 4 cells FIFO as an elastic store.

For each channel a context is maintained internally, including a DMA descriptor. The Transmitter reads the messages from the message memory through the internal DMA controller.

Each time when a message is finished (EOM, SSM) an interrupt is generated to the local microprocessor and the context is free. There is no status written to the message memory. The Transmitter handles the SAR and CS layers according to CCITT recommentation I.363. The ATM cell header is initiliazed by the local microprocessor (VCI/VPI/MID). The AAL controller processes the segment type by sequencing and CRC.

The CPCS is prepared by the processor (CPI, Btag, BAsize, AL, Etag, PAD, Lenght for AAL3/4, CPCS-UU, CPI, PAD, Lenght for AAL5).

DMA

The DMA Controller is located on the chip. It reads and writes 32-Bit words for the Transmitter and Receiver. It has 24-Bit address bus to the Message Memory. The DMA Controller controls the bus handshake signals with the Message Memory Bus Arbiter. The Message Memory bus is synchronous and it is assumed to use the System Clock. Wait States can be inserted to the bus cycles using the DATA ACK input. The DMA Controller also supports burst mode access to the Message Memory. This access is activated with the LOCK output.

Control Logic

The Control Unit is connected to the 16-Bit data bus and 11-Bit address bus. This unit is responsible of controlling all internal and external operations and synchronizing them together. The Control Unit has a separate bus for the local microprocessor. The Control

Unit also maintains the status information in its registers and interrupts the local microprocessor when it is needed to take the control of the operation. All the internal registers in this Unit are memory mapped.

Registers

The Registers can be divided in 3 different main groups. These are Status Registers, Command Registers and Address Registers. The Status Registers are used by the local CPU to determine the status of the process and to make needed actions in terms of free descriptors, error handling and causes of different interrupts. The Command Registers are used to determine different masks, context and they also store some statistic information. The Address Registers are used by the DMA controller for different channels which are active. All registers are memory mapped. The total number of registers is 70.

Test Support

The 29C70 offers also a JTAG test and extra register locations to determine the status of the process and to keep statistic on the number of cells transmitted/received or lost in transmission. These extra bits are targeted to be used for software debugging and application monitoring.

Pin Description

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Message Buffer Interface

Pin	Type	Description
DMAREQ	O	DMA request to message memory arbiter
DMAGT	I	DMA grant from message memory arbiter
DMALOCK	O	DMA lock request to exercise burst transfer
DMAACK	I	DMA cycle acknowledge from message memory
DMARW	O	DMA read (high), DMA write (low)
DMAD (31 : 0)	I/O	DMA data bus (31 : MSB, 0 : LSB)
DMAAD (23 : 0)	O	DMA address bus (23 : MSB, 0 : LSB)
CELLBOM	O	BOM, SSM information
CKTEMPO	I	Timer to receive house keeping (garbage kits)

Microprocessor Interface

Pin	Type	Description
MPUCS	I	Microprocessor chip select (active low)
MPURW	I	Read (high), Write (low)
MPURDY	O	Ready (active low, wait state inserted while low)
MPUINT	O	Interrupt request
MPUD (15 : 0)	I/O	PMU data bus (15 : MSB, 0 : LSB)
MPUAD (9 : 0)	I	PMU address bus (9 : MSB, 0 : LSB)

ATM Layer Interface

Receiver

Pin	Type	Description
ATMDR (7 : 0)	I	Receive ATM data (7 : MSB, 0 : LSB)
ATMRCLK	I	ATM receive clock
ATMRSYN	I	ATM receive sync strobe
ATMRNB (7 : 0)	I	ATM receive AAL number and VX for next cell (7 : MSB, 0 : LSB)

Transmitter

Pin	Type	Description
ATMXD (7 : 0)	I	Transmit ATM data (7 : MSB, 0 : LSB)
ATMXCLK	I	ATM transmit clock
ATMXSYN	I	ATM transmit sync strobe
ATMXREQS	O	AAL number transmitted serially for request to send
ATMXNAAL (5 : 0)	O	AAL number authorized to transmit on next cell (5 : MSB, 0 : LSB

Other

Pin	Type	Description
SCLK	I	System clock 25 MHz
RESET	I	Reset active low
JTAG		Reserved for JTAG (4)
TEST		Reserved for Test
VCC		Positive power supply
VSS		Negative power supply

Registers and Memory Mapping

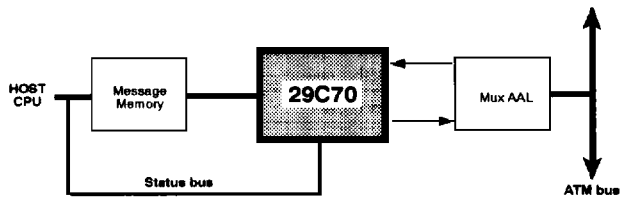
Address	CPU Access	Registers and Memories	Name
0 - 1FF	Read/Write	Transmit context memory	
200	Read	Interrupt register	IT
201	Read	Status register	STATUS
202	Read	Command and mask interrupt register	CMDE
203	Read/Write	AAL number register	NUMAAL
204	Read/Write	Soft reset register	RESET
205-214	Read/Write	Price (0) to Price (15) registers	PRICE (n)
215-224	Read/Write	Inc (0) to Inc (15) registers	INC (n)
225-228	Read	ESP (0) to ESP (3) state registers	ESP (n)
229-22C	Write	ESP (0) to ESP (3) set state registers	SESP (n)
22D-230	Write	ESP (0) to ESP (3) reset state registers	RESP (n)
231	Write	FIFO of large buffer address	LFIFO_H
232	Write	FIFO of large buffer address	LFIFO_L
233	Write	FIFO of small buffer address	SFIFO_H
234	Write	FIFO of small buffer address	SFIFO_L
235	Read/Write	Address of status context for buffer queue	SCTX_AD_H
236	Read/Write	Address of status context for buffer queue	SCTX_AD_L
237	Read/Write	Buffer size for status context queue	SIZ_SCTX
238	Read/Write	Context address to process in buffer queue	SCTX_RD_H
239	Read/Write	Context address to process in buffer queue	SCTX_RD_L
23A	Write	Free acknowledge for buffer in queue	ACK_FREE_RD
23B	Read/Write	Max size of small buffer register	MAX_SMALL
23C	Read/Write	Max size of small buffer register	MAX_LARGE
23D	Read/Write	Size level of small buffer register	SIZ_LEVEL
23E	Read/Write	Command register of reception - temporatisation	R_TEMPO
23F	Read/Write	Command register of reception - synchronization lost	LOSSTEMPO
240	Read/Write	Main clock request register	REQXINC
241	Read/Write	Main clock request register	REQXPRICE_H
242	Read/Write	Main clock request register	REQXPRICE_L
243	Read/Write	Statistic register BOM with context	BOMwCTX
244	Read/Write	Statistic register COM without context	COMsCTX
245	Read/Write	Statistic register CAM full	CV65
246	Read/Write	Statistic register cell FIFO receive full	FIFOR_FULL
247	no access	Reserved	WRIT_CTX
260-2DF	Read/Write	CAM memory	
300-6FF	Read/Write	Receive context memory	

29C70

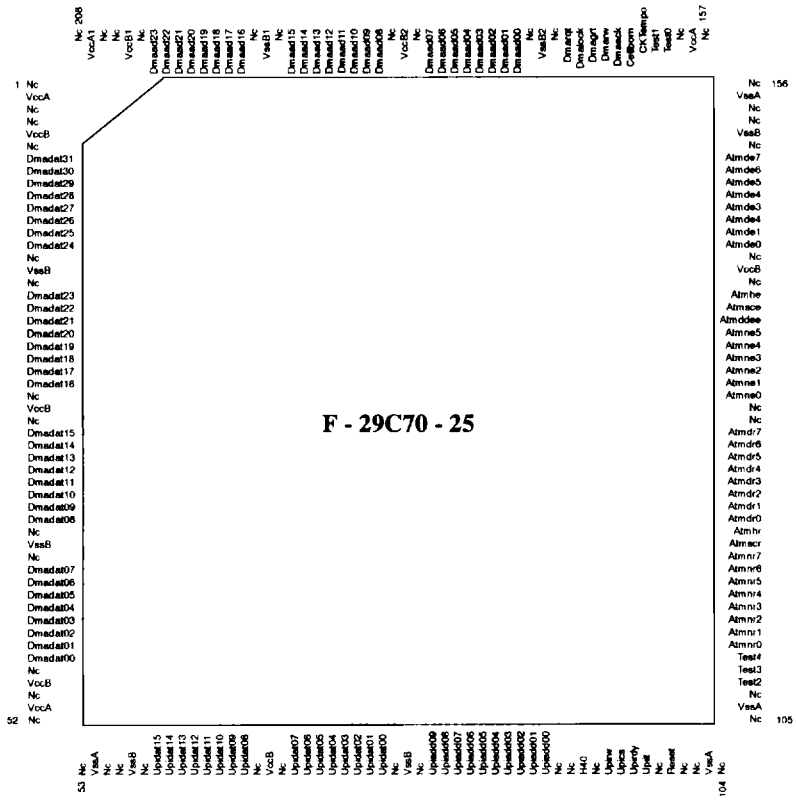
Applications

- ATM Inter Working Devices (Routers, DSUS)
- ATM LANs
- LAN to ATM Bridges
- ATM Multiplexers
- Workstation to ATM Interfaces

Application Diagram



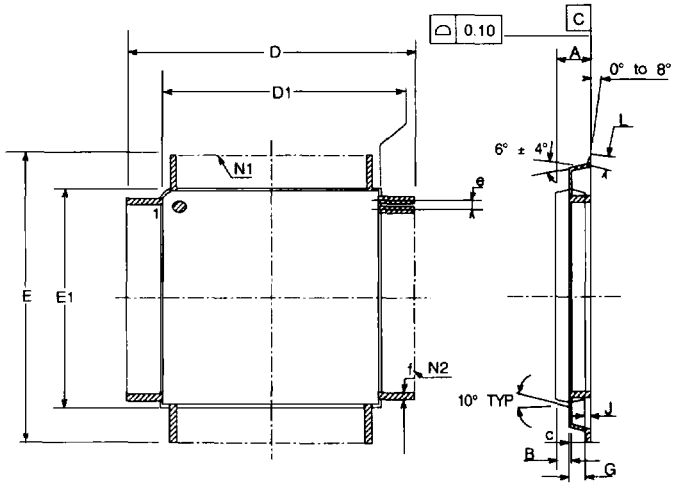
Pinout



Top View of 208 pins PQFP Square Gull Wing Package

Note : Final marking information may change.

Mechanical Outline



	MM		INCH	
	Min	Max	Min	Max
A	3.64	3.94	.143	.155
B	1.57	1.77	.062	.070
c	0.13	0.20	0.005	0.008
D	31.75	31.95	1.250	1.258
D1	27.95	28.05	1.100	1.104
e	0.500 TYP		.0197 TYP	
E	31.75	31.95	1.250	1.258
E1	27.95	28.05	1.100	1.104
f	0.22	0.35	.009	.014
G	1.57	1.77	.062	.070
J	0.305 TYP		.012 TYP	
L	0.70	0.90	.028	.035
N1/N2	52/52		52/52	