

Dual-Range High-Speed Analog-to-Digital Converter 12-Bit, 8 Msps

The THC1200 is a complete 12-bit 8 Msps (Mega-samples-per-second) analog-to-digital converter that includes all the circuitry required to digitize signals within a DC to 35MHz band. The THC1200 features two user-selectable input voltage ranges which give the A/D converter a large dynamic range. With its two-step architecture, the THC1200 achieves a very high conversion rate and superior performance. The device contains a wideband input amplifier, a precision track/hold, analog-to-digital quantizer, voltage reference, precision timing generator and registered three-state TTL output drivers.

The THC1200 offers significant advantages over previous converter boards in space efficiency, ease of use, power dissipation, DC and AC performance, reliability and flexibility.

Designed to meet demanding requirements, the THC1200 is housed in a 46-pin hermetically sealed dual-in-line package. Specified performance is guaranteed over the industrial (-25 to 85°C case) and extended (-55 to 125°C case) temperature ranges. Military-grade parts are in compliance with MIL-STD-883 and are manufactured in facilities certified and qualified to MIL-STD-1772.

Features

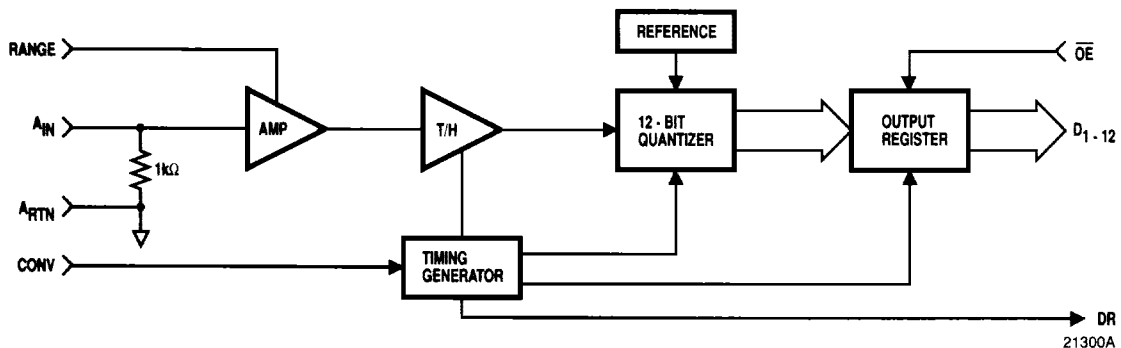
- Conversion Rate DC To 8 Msps
- Two User-Selectable Input Voltage Ranges
- Analog Input Ranges: ± 2.5 and ± 0.167 Volts
- Input Signal Bandwidth >30MHz
- No Missing Codes, Guaranteed
- SNR = 62dB At 8 Msps With 2.5MHz Input, Guaranteed
- TTL-Compatible Input And Three-State Outputs
- 46-Pin Metal DIP
- Evaluation Board (THC1200E1C) Available

Applications

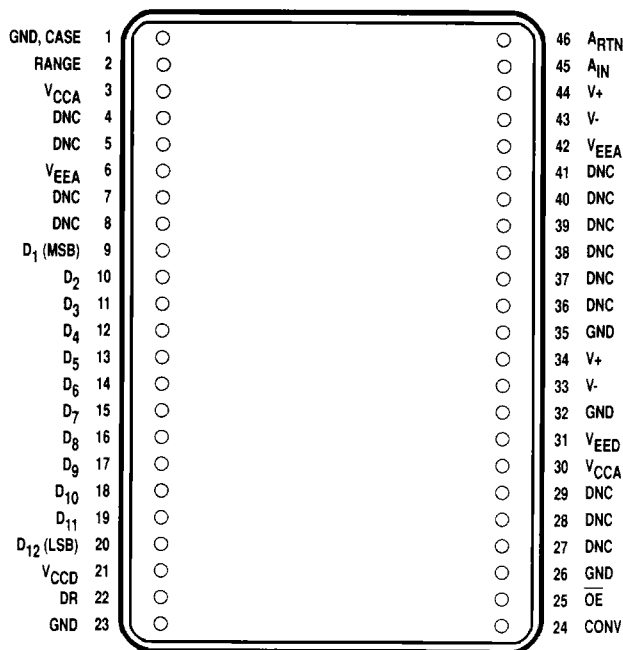
- Radar
- Data Acquisition Systems
- Digital Oscilloscopes
- Medical Imaging
- Communications
- CCD Digitization
- Transient Recorders
- Forward-Looking InfraRed Systems
- Focal Plane Arrays



Functional Block Diagram



Pin Assignments



46-Pin Metal DIP, S3 Package

21301A

Functional Description

General Information

The THC1200 is a complete 12-bit 8 Msps A/D converter that features a wideband input amplifier, precision track/hold, voltage reference, timing circuitry and a three-state digital output register all housed in a 46-pin hermetic DIP. Input voltage ranges of ± 2.5 and ± 0.167 Volts are selectable by way of a single TTL-compatible input. The THC1200 employs a two-step analog-to-digital converter architecture and proprietary components to achieve a 8 Msps conversion rate and superior performance. The THC1200 is guaranteed to meet all specifications without additional adjustment or calibration. Additional information on applying the THC1200 is found in TRW *Application Note TP-45, "Designing with the THC1200 A/D Converter Family."*

Three-state TTL-compatible outputs permit the THC1200 to drive a shared data bus directly. Data emerges from the THC1200 synchronously with respect to CONV. The digital output corresponding to the sample of the analog input

signal is valid after the rising edge CONV. The THC1200 provides a 12-bit two's-complement digital output as indicated in the *Output Coding Table*.

Power and Ground

The THC1200 requires four standard power supplies for operation: $V_{CCA} = V_{CCD} = +5V$, $V_{EEA} = V_{EED} = -5.2V$, $V_+ = +15V$, and $V_- = -15V$. Linear regulated power supplies are preferred over switching power supplies for optimum performance. All power supply inputs to the THC1200 should be properly decoupled.

Separate analog and digital grounds are maintained within the the THC1200, but no distinction is made at the package pins. For optimum converter performance, all ground pins should be connected to a common solid ground plane. Wire-wrap breadboarding techniques are not recommended for use with this high-speed high-precision analog-to-digital converters. TRW LSI Products Inc. *Application Note TP-45, "Designing with the THC1200 A/D Converter Family"* is recommended for additional information on using the THC1200.

Analog Input and Analog Input Return

The two input voltage ranges of the THC1200 are: -2.500 to $+2.500$ Volts and $+0.167$ to -0.167 Volts. This results in a Least Significant Bit weight of 80 microvolts in the smaller range, giving the THC1200 an overall dynamic range of nearly 96dB. A $1k\Omega$ thin-film resistor is connected between A_{IN} and $ARTN$ and is provided for termination of analog input signals

$ARTN$ is the internal ground reference point for internal analog circuitry and voltage references within the THC1200. In normal operation $ARTN$ should be connected to signal ground where the analog input signal connection is in close proximity to the THC1200. $ARTN$ should also be connected to power supply ground.

RANGE

The RANGE input selects which of the two analog input voltage ranges the THC1200 is to use. When LOW, the input range of the THC1200 is 5.0 Volts peak- to-peak, centered around zero Volts. When RANGE is HIGH, the analog input voltage range is 0.333 Volts peak-to-peak, centered around zero Volts.

CONV

Each rising edge of the CONV signal initiates conversion (*See Timing Diagram*). The THC1200 operates independently of the duty cycle of CONV as long as t_{PWH} and t_{PWL} limitations are not exceeded.

CONV clock jitter, t_{CJ} , must be minimized in order to optimize performance. Time errors in sampling a high slew

rate (large $\Delta V/\Delta T$) signal appear as voltage errors in the conversion. The high-speed and precision of the THC1200 may reveal system timing errors (jitter) that would not be apparent with lower resolution converters (see *TP-45*).

Data Outputs and Output Enable

The 12 TTL-compatible data outputs (D_1 – D_{12}) provide two's-complement data as shown in the *Output Coding Table*. The output data becomes valid t_D after the rising edge of CONV, and remains valid until t_{H0} after the next rising edge of CONV. D_{12} is the least significant bit.

The output drivers become disabled (high-impedance) within t_{DIS} after the asynchronous input \overline{OE} is switched HIGH. The outputs are enabled within t_{ENA} after \overline{OE} is switched LOW.

Data Ready

A Data Ready output is provided which may be used to control the registering of data from the THC1200 into storage devices following in the data path. DR is generated within the THC1200 by inverting the CONV signal. As long as the user operates the THC1200 within the t_{PWH} and t_{PWL} limits on CONV, the rising edge of DR will occur when output data is valid and therefore can be used as the clock input to positive edge-triggered storage devices.

Do Not Connect

DNC pins are used in factory calibration and must remain unconnected.



Package Interconnections

Name	Function	Value	Package Pins
VCCA	Positive Analog Supply	+5.0V	3, 30
VCCD	Positive Digital Supply	+5.0V	21
VEEA	Negative Analog Supply	-5.2V	6, 42
VEED	Negative Digital Supply	-5.2V	31
V+	Positive Supply	+15V	34, 44
V-	Negative Supply	-15V	33, 43
GND	Ground	0.0V	1, 23, 26, 32, 35
CONV	Convert Input	TTL	24
AIN	Analog Input	see text	45
ARTN	Analog Input Return	0.0V	46
RANGE	Range Control Input	TTL	2
D ₁ (MSB)	Most Significant Bit	TTL	9
D ₂		TTL	10
D ₃		TTL	11
D ₄		TTL	12
D ₅		TTL	13
D ₆		TTL	14
D ₇		TTL	15
D ₈		TTL	16
D ₉		TTL	17
D ₁₀		TTL	18
D ₁₁		TTL	19
D ₁₂ (LSB)	Least Significant Bit	TTL	20
DR	Data Ready Output	TTL	22
OE	Output Enable Control	TTL	25
DNC	Do Not Connect	Open	4, 5, 7, 8, 27, 28, 29, 36, 37, 38, 39, 40, 41

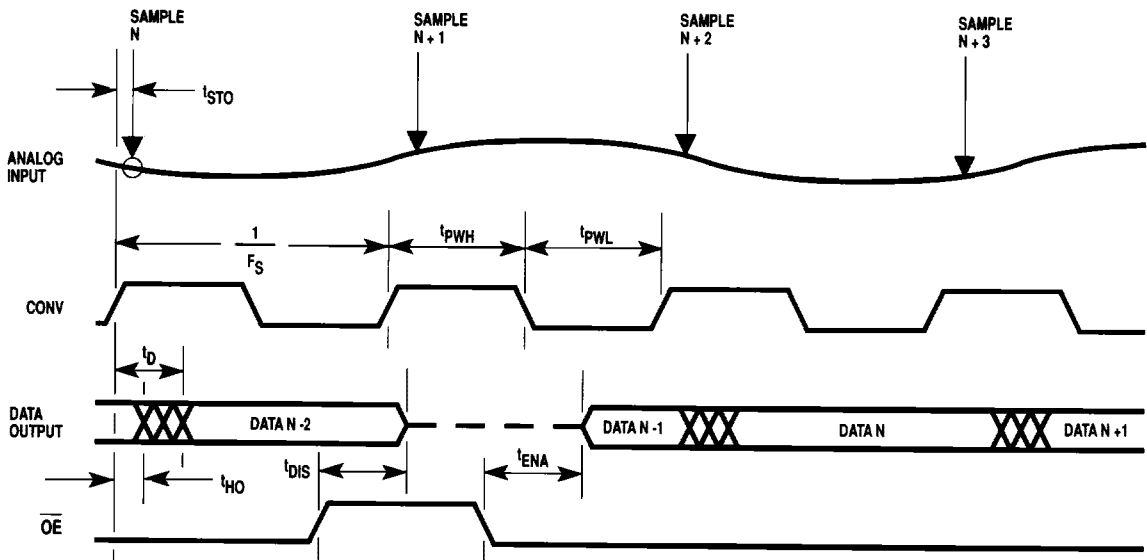
Output Coding Table

Input Voltage (Code Midpoints)		Digital Outputs	
RANGE = LOW	RANGE = HIGH	MSB	LSB
+2.5000	+0.16700	1000	0000 0000
+2.4988	+0.16692	1000	0000 0001
+2.4975	+0.16684	1000	0000 0010
•	•	•	•
•	•	•	•
•	•	•	•
+0.0024	+0.00016	1111	1111 1110
+0.0012	+0.00008	1111	1111 1111
0.0000	0.00000	0000	0000 0000
-0.0012	-0.00008	0000	0000 0001
-0.0024	-0.00016	0000	0000 0010
•	•	•	•
•	•	•	•
•	•	•	•
-2.4963	-0.16676	0111	1111 1101
-2.4975	-0.16684	0111	1111 1110
-2.4988	-0.16692	0111	1111 1111

- Notes: 1. For RANGE = HIGH, 1 LSB Step size = $0.330 / 4095 = 80.6\mu\text{V}$.
 2. For RANGE = LOW, 1 LSB Step size = $5.000 / 4095 = 1.22\text{mV}$.

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Figure 1. Timing Diagram



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Figure 2. Simplified Analog Input Equivalent Circuit

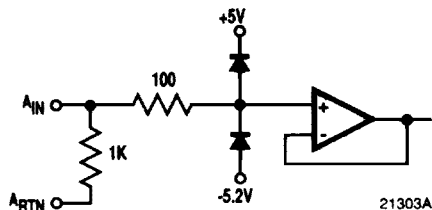
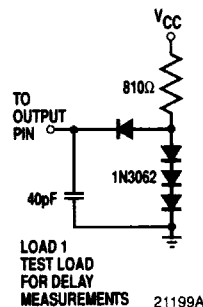


Figure 3. Standard TTL Test Load



Absolute maximum ratings (beyond which the device may be damaged)¹

Supply Voltages

V _{CC}	-0.5 to +7.0V
V _{EE}	-7.0 to +0.5V
V ₊	-0.5 to +18.0V
V ₋	-18.0 to +0.5V

Input Voltages

A _{IN}	+8.0 to -8.0
CONV, \overline{OE}	-0.5V to V _{CC}

Outputs

Digital Outputs, Applied Voltage ²	-0.5V to V _{CC}
Digital Outputs, Applied Current ³	100mA
Short-Circuit Duration (Single Output to Ground)	1 sec

Temperature

Operating, Case	-65 to +130°C
Lead, Soldering (10 seconds)	+300°C
Storage	-60 to +150°C

Notes: 1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Device performance and reliability are guaranteed only if the Operating Conditions are not exceeded.

2. Applied voltage must be current limited to specified range.

3. Forcing voltage must be limited to specified range.

Operating conditions

Parameter		Min	Nom	Max	Units
VCC	Positive Supply Voltage	4.7	5.0	5.3	V
VEE	Negative Supply Voltage	-4.89	-5.2	-5.51	V
V+	Positive Supply Voltage	14.4	15.0	15.6	V
V-	Negative Supply Voltage	-14.4	-15.0	-15.6	V
tPWH	CONV Pulse Width HIGH	45			ns
tPWL	CONV Pulse Width LOW	25			ns
fS	Conversion Rate	0		8	msps
tCJ	CONV Clock Jitter			10	psRMS
VIL	Input Voltage, Logic LOW			0.7	V
VIH	Input Voltage, Logic HIGH	2.0			V
A _{IN}	Analog Input Range, RANGE = LOW	-2.50		+2.50	V
A _{IN}	Analog Input Range, RANGE = HIGH	-0.167		+0.167	V
T _C	Case Temperature, B-grade	-25		85	°C
T _C	Case Temperature, V-grade	-55		125	°C



Electrical characteristics within specified operating conditions

Parameter	Conditions	Typ	Temperature Range				Units
			Industrial		Military		
			Min	Max	Min	Max	
I _{CC} Total +5V Power Supply Current ¹		485		600		600	mA
I _{EE} Total -5.2V Power Supply Current ¹		-315		-640		-640	mA
I ₊ Total V ₊ Power Supply Current ¹		150		400		400	mA
I ₋ Total V ₋ Power Supply Current ¹		-180		-400		-400	mA
P _D Total Power Dissipation ²		9.45		13.7		13.7	W
I _{IH} Input Current, Logic HIGH	V _{IH} = 2.4V			150		150	μA
I _{IL} Input Current, Logic LOW	V _{IL} = 0.5V			-3.2		-3.2	mA
V _{OH} Output Voltage, Logic HIGH	I _{OH} = 160μA		2.4		2.4		V
V _{OL} Output Voltage, Logic LOW	I _{OL} = -3.2mA			0.5		0.5	V
I _{OZH} Output Leakage Current, Logic HIGH	\overline{OE} = HIGH, V _{OH} = 2.4V			±50		±50	μA
I _{OZL} Output Leakage Current, Logic LOW	\overline{OE} = HIGH, V _{OL} = 0.7V			±50		±50	μA
I _{OS} Short Circuit Current	1 second Max., one pin shorted to ground		-30	-100	-30	-100	mA
R _{IN} Analog Input Resistance	A _{RTN} connected to GND	1000	950	1050	950	1050	Ω
C _{IN} Input Capacitance	All Inputs			20		20	pF
V _{FP1} Full-Scale Positive Input	A _{IN} at 1/2 LSB above most positive transition, RANGE = LOW	2.50	2.45	2.55	2.45	2.55	V
V _{FN1} Full-Scale Negative Input	A _{IN} at 1/2 LSB below most negative transition, RANGE = LOW	-2.50	-2.45	-2.55	-2.45	-2.55	V
V _{FP2} Full-Scale Positive Input	A _{IN} at 1/2 LSB above most positive transition, RANGE = HIGH	0.167	0.157	0.177	0.157	0.177	V
V _{FN2} Full-Scale Negative Input	A _{IN} at 1/2 LSB below most negative transition, RANGE = HIGH	-0.167	-0.157	-0.177	-0.157	-0.177	V

Notes: 1. Typical values are the statistical average of actual measurements taken over the Operating Temperature Range.

2. Typical value is calculated from typical power supply currents and maximum power supply voltages over the Operating Temperature Range. Maximum values are calculated from measured maximum currents and maximum voltages over the Operating Temperature Range.

Switching characteristics within specified operating conditions

Parameter	Conditions	Typ	Temperature Range				Units
			Industrial		Military		
			Min	Max	Min	Max	
f _S Maximum Conversion Rate			8		8		MSPS
t _{STO} Sampling Time Offset	RANGE = LOW		-2.0	4.0	-2.0	4.0	ns
t _{STO} Sampling Time Offset	RANGE = HIGH		-11.0	-17.0	-11.0	-17.0	ns
t _D Data Output Delay Time	C _{LOAD} = 50pF Max			50		50	ns
t _{HO} Data Output Hold Time	C _{LOAD} = 50pF Max		5		5		ns
t _{ENA} Output Enable Time	C _{LOAD} = 50pF Max			40		40	ns
t _{DIS} Output Disable Time	C _{LOAD} = 50pF Max			100		100	ns
t _G Gain switch settling time				1		1	μs
t _{QR1} Overload Recovery Time	V _{IN} = 2x Full-Scale			140		140	ns
t _{QR1} Overload Recovery Time	V _{IN} = ±8V			4		4	μs



Thermal Characteristics

Parameter	Conditions	Typ	Units
delta T _{JC} Junction-to-Case Temperature Rise	Worst-Case Power Dissipation	20	°C
theta _{CA} Case-to-Ambient Thermal Resistance	in Still Air	10	°C/W
	with 500 LFPM Airflow	6	°C/W

System Performance Characteristics

Parameter	Conditions	Typ	Temperature Range				Units
			Industrial		Military		
			Min	Max	Min	Max	
ELI Integral Linearity Error	Independent based			±4.0		±4.0	LSB
ELD Differential Linearity Error	$f_S = 8 \text{ Msps}$, $f_{IN} = 2.5 \text{ MHz}$	±0.6		±1.8		±1.8	LSB
SNR Signal-to-Noise Ratio	$f_S = 8 \text{ Msps}$, $f_{IN} = 2.5 \text{ MHz}$		59		59		dB
	V_{IN} is 1dB below Full-Scale RANGE = HIGH						
	$f_S = 8 \text{ Msps}$, $f_{IN} = 2.5 \text{ MHz}$		62		62		dB
	V_{IN} is 1dB below Full-scale RANGE = LOW						
SFDR Spurious Free Dynamic Range	$f_S = 8 \text{ Msps}$, $f_{IN} = 2.5 \text{ MHz}$		65		65		dB
	V_{IN} is 1dB below Full-Scale RANGE = HIGH						
	$f_S = 8 \text{ Msps}$, $f_{IN} = 2.5 \text{ MHz}$		62		62		dB
	V_{IN} is 1dB below Full-Scale RANGE = LOW						
IMD Intermodulation Distortion	$f_S = 8 \text{ Msps}$, $f_{IN1} = 2.4 \text{ MHz}$		62		62		dB
	$f_{IN2} = 2.45 \text{ MHz}$, each input signal is 7dB below Full-Scale						
BW -3dB Analog Bandwidth	$V_{IN} = 0.330 \text{ Volts p-p}$, RANGE = HIGH		8		8		MHz
	$V_{IN} = 5 \text{ Volts p-p}$, RANGE = LOW		25		25		MHz
EAP Aperture Jitter		±40					ps
SC Spurious Codes				0		0	codes
MC Missing Codes				0		0	codes
EG Gain Error				±1.5		±1.5	%FS
VOS1 Offset Error	A_{IN} at Mid-Scale code transition, RANGE = HIGH			±5		±5	%FS
VOS2 Offset Error	A_{IN} at Mid-Scale code transition, RANGE = LOW			±2.2		±2.2	%FS
PSR1 Power Supply Rejection	V_+ , V_-			0.05		0.05	%FS/%V
PSR2 Power Supply Rejection	V_{CC} , V_{EE}			0.025		0.025	%FS/%V

Definitions

SNR (Signal-to-Noise Ratio)

The ratio, expressed in decibels, of the RMS level of the output signal to the RMS level of the in-band noise. This noise is measured with the signal present and excludes harmonic distortion products.

HD (Harmonic Distortion)

The ratio, expressed in decibels, of the second harmonic of the output fundamental to the RMS level of the output fundamental.

SINAD (Signal-to-Noise and Distortion)

The ratio, expressed in decibels, of the RMS level of the output signal to the RMS sum of both the in-band noise and the RMS sum of the first 10 harmonics of the output fundamental.

IMD (Intermodulation Distortion)

The ratio, expressed in decibels, of the largest output frequency spur to either of the two equal-level output fundamentals.

t_{TR} (Transient Response Time)

The time required to begin returning accurate data after a full scale input voltage step whose initial and final voltages are within the analog input range. t_{TR} is an analog domain parameter and excludes pipeline latency.

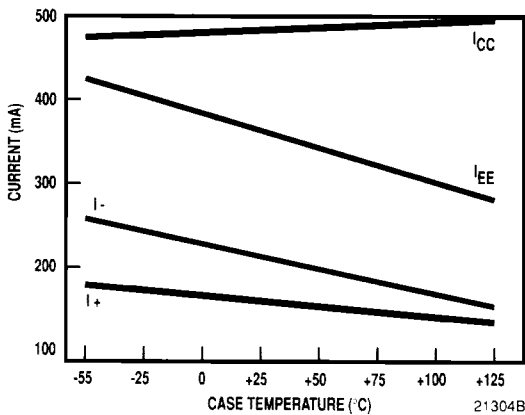
t_{OR} (Overload Recovery Time)

The time required to begin producing accurate data after the input voltage returns to the allowable range, following an excursion to 200% of either full-scale limit. t_{OR} is an analog domain parameter and excludes pipeline latency.



Typical Performance Curves

Power Supply Current vs Temperature



Dynamic Performance vs. Input Frequency

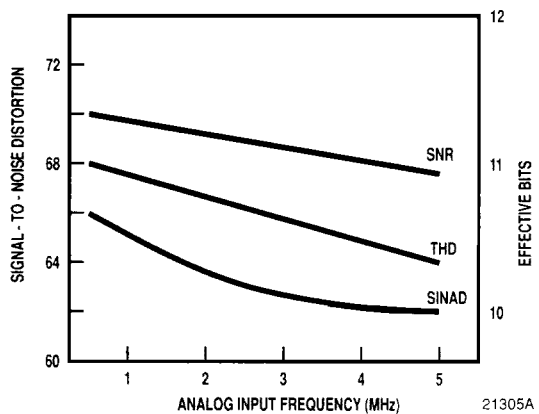
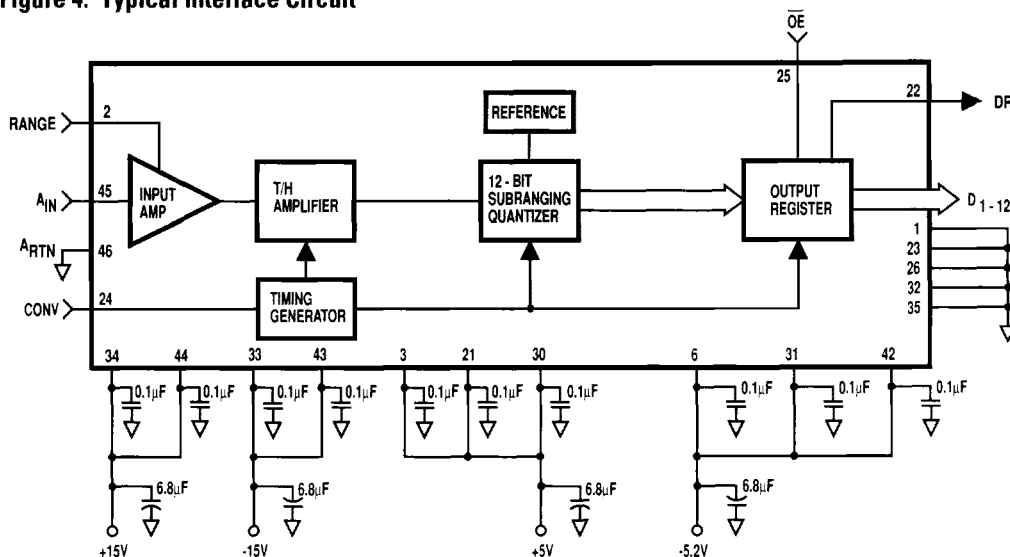


Figure 4. Typical Interface Circuit



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Evaluation Board

The THC1200E1C is a Eurocard-style printed circuit board designed to aid in the evaluation of the THC1200 A/D converter. The board dimensions are 100mm x 160mm with a standard 64-pin double-row DIN male connector installed. A complementary 64-pin double-row DIN female connector is included with the board.

The board employs only two conducting sides. Most of the circuit interconnections are on the bottom of the board while the top is mostly solid ground plane. SMA connectors are installed on the board to facilitate analog I/O and clocks. The circuitry on the board includes all power supply decoupling required for the THC1200, and a TDC1012 12-bit D/A converter which may be used in evaluating certain parameters of the THC1200. Additional information on applying the THC1200 is found in TRW Application Note *TP-45, "Designing with the THC1200 A/D Converter Family"*.

The THC1200E1C board has been designed to be used, not only for the THC1200, but also for the THC1201 and THC1202 A/D converters. Therefore, the board has interconnect patterns for some circuitry that is not used by the THC1200. Jumpers J1, J6 and FT will be installed while all others are not.

The board is calibrated and tested at the factory and is supplied complete with THC1200 and TDC1012 installed.

Power and Ground

Four power supply voltages are required for the operation of the THC1200E1C: $V_{CC} = +5V$, $V_{EE} = -5.2V$, $V_+ = +15V$ and $V_- = -15V$. All power inputs are decoupled to a single solid ground plane, GND. All GND pins of the board are connected to the ground plane and it is recommended that all GND pins be used.

A/D Converter Inputs

The clock to the THC1200, CONV, is normally brought onto the board by way of an SMA connector labeled "CONV" near pin 24 of the THC1200. A location for a terminating resistor, R20 is available on the board for terminating cables. CONV may be brought onto the board through the edge-connector pin B2 by installing jumper J9. The DIP switch enables control of \overline{OE} and RANGE which are both pulled HIGH when the switches are open.

The analog signal input to the THC1200, A_{IN} is normally brought onto the board by way of an SMA connector labeled " A_{IN} " near pin 45 of the THC1200. A resistor network, R13 through R16, is included on the board for terminating and attenuating the signal in user-determined impedances and losses.

A/D Converter Data Outputs and D/A Converter Data Inputs

The 12 data outputs of the THC1200 are brought to edge-conductor pins B9 through B21 (excluding B18). These pins are located directly across the edge-conductor from the 12 data inputs of the TDC1012 D/A converter to simplify connection of A/D outputs to D/A inputs.

D/A Converter Inputs

The clock to the TDC1012, CLK, is normally brought onto the board through an SMA connector labeled "CLK" near pin 16 of the TDC1012. A location for a terminating resistor, R6 is provided for clock cable termination. The clock input to the TDC1012 is also brought to the edge-conductor pin B24.

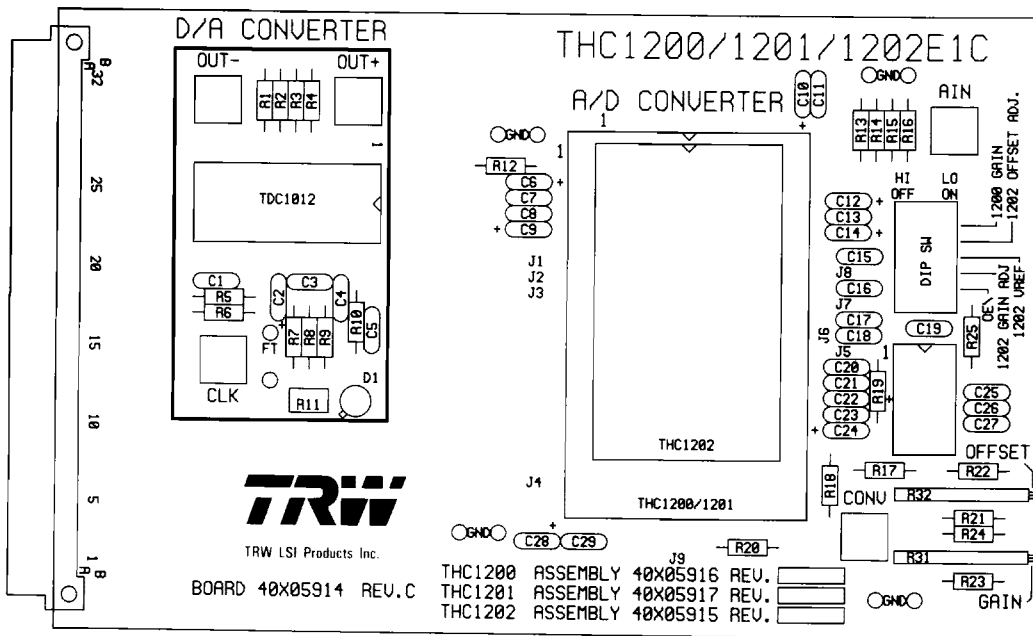
D/A converter outputs are brought to SMA connectors labeled OUT+ and OUT- as well as edge-conductor pins B28 and B27. Load resistors of 51.1Ω are provided on the board to facilitate 50Ω cable connection to the board.

Potentiometer R11 is used to adjust the reference voltage to the TDC1012. This voltage is adjusted to -1.0 V as part of the factory test and calibration procedure.

Removing the jumper in the location labeled "FT" will put the TDC1012 into feedthru (unlocked) mode. This eliminates the requirement for a D/A clock signal, but will degrade the fidelity of the TDC1012 reconstruction.

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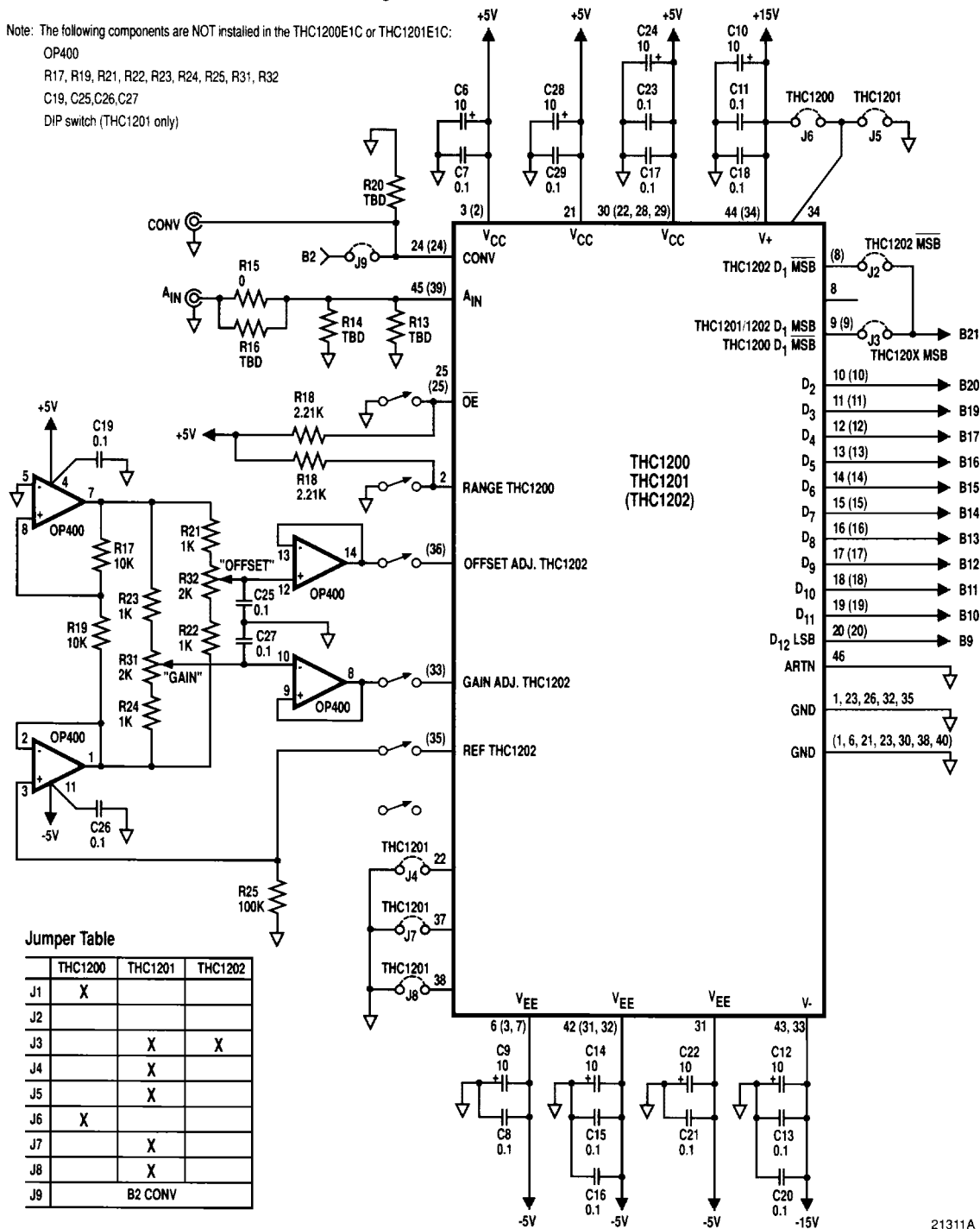
THC1200E1C silkscreen layout



THC1200E1C A/D Converter Schematic Diagram

Note: The following components are NOT installed in the THC1200E1C or THC1201E1C:

- OP400
- R17, R19, R21, R22, R23, R24, R25, R31, R32
- C19, C25, C26, C27
- DIP switch (THC1201 only)



Jumper Table

	THC1200	THC1201	THC1202
J1	X		
J2			
J3		X	X
J4		X	
J5		X	
J6	X		
J7		X	
J8		X	
J9	B2 CONV		

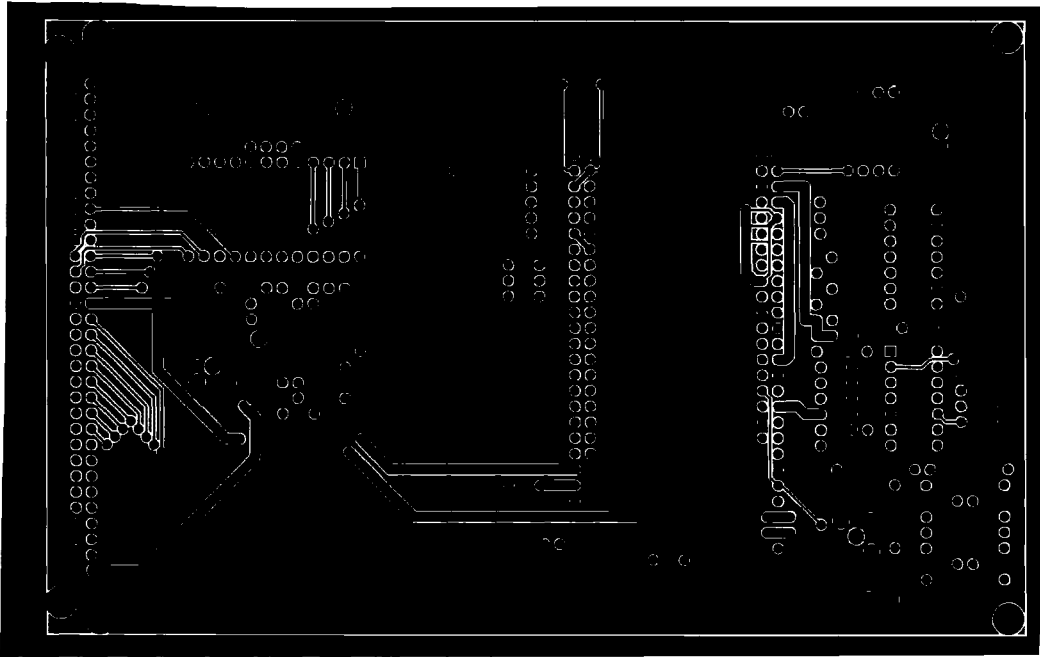
Evaluation Board Pin Assignments

GND	A32	B32	V- (-15V)
GND	A31	B31	V+ (+15V)
GND	A30	B30	N/C
GND	A29	B29	N/C
GND	A28	B28	D/A OUT+
GND	A27	B27	D/A OUT-
GND	A26	B26	N/C
GND	A25	B25	N/C
GND	A24	B24	D/A CLK
GND	A23	B23	N/C
GND	A22	B22	N/C
D/A D ₁ MSB	A21	B21	A/D D ₁ MSB
D/A D ₂	A20	B20	A/D D ₂
D/A D ₃	A19	B19	A/D D ₃
GND	A18	B18	V _{CC} (+5V)
D/A D ₄	A17	B17	A/D D ₄
D/A D ₅	A16	B16	A/D D ₅
D/A D ₆	A15	B15	A/D D ₆
D/A D ₇	A14	B14	A/D D ₇
D/A D ₈	A13	B13	A/D D ₈
D/A D ₉	A12	B12	A/D D ₉
D/A D ₁₀	A11	B11	A/D D ₁₀
D/A D ₁₁	A10	B10	A/D D ₁₁
D/A D ₁₂ LSB	A9	B9	A/D D ₁₂ LSB
N/C	A8	B8	N/C
N/C	A7	B7	N/C
N/C	A6	B6	N/C
N/C	A5	B5	N/C
GND	A4	B4	N/C
GND	A3	B3	N/C
GND	A2	B2	A/D CONV
GND	A1	B1	V _{EE} (-5.2V)

Mating Connectors for THC1200E1C

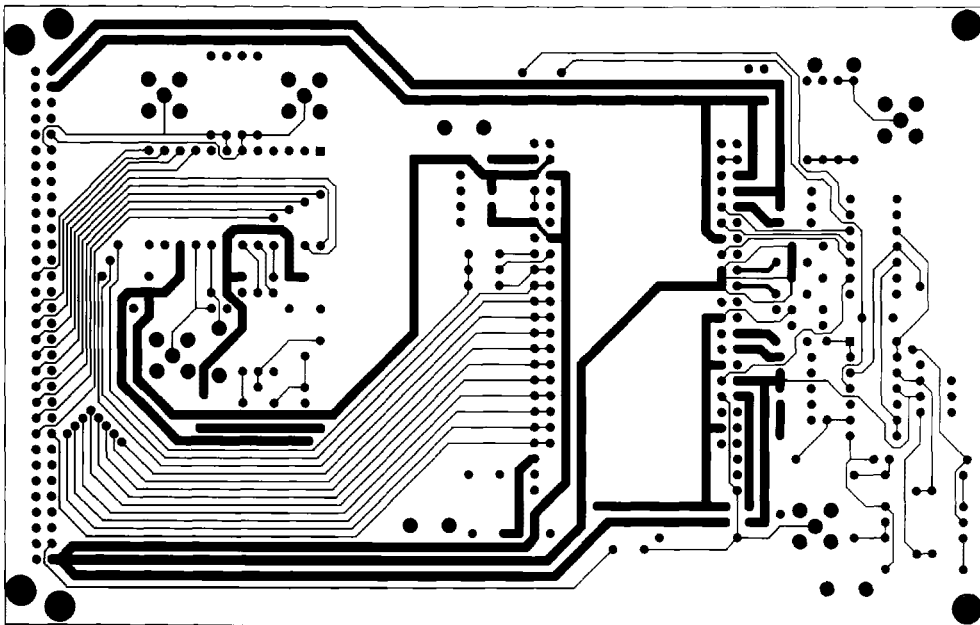
AMP	532507-2	Wire-wrap
AMP	532507-1	Solder tail
Robinson-Nugent	RNE-64BS-W-TG30	Wire-wrap
Robinson-Nugent	RNE-64BS-S-TG30	Solder tail
Souriau	8609-264-6115-7550E1	Wire-wrap
Souriau	8609-264-6114-7550E1	Solder tail
Souriau	8609-264-6813-7550E1	Solder tail, right-angle bend

THC1200E1C Component Side Layout



A

THC1200E1C Circuit Side Layout



Ordering Information

Product Number	Temperature Range	Screening	Package	Marking
THC1200S3B	IND, T _C = -25 to 85°C	Industrial	46 Pin Hermetic Metal DIP	THC1200S3B
THC1200S3V	EXT, T _C = -55 to 125°C	MIL-STD-883	46 Pin Hermetic Metal DIP	THC1200S3V
THC1200E1C	STD, T _A = 0 to 70°C	—	Eurocard PC Board	THC1200E1C

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