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April 1st, 2010
Renesas Electronics Corporation

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CMOS LSI FOR 12 lines \times 24 columns CHARACTER DISPLAY ON SCREEN

μ PD6451A is the CMOS LSI for on-screen character display that can be used in combination with a micro-computer to display time, channel numbers, and chapter numbers on the screen.

Use of this LSI for the video camera and VTR allows recording of video signals with the time and date.

The display character format is 12 \times 18 dots. Because there is no space between characters, this LSI enables display of a combination of two or more characters, kanji characters, and graphs.

Both μ PD6451ACX-001 and μ PD6451AGT-101 display the same characters. μ PD6451AGT-301 displays characters differ from μ PD6451ACX-001, μ PD6451AGT-101. μ PD6451ACX-001 is enclosed in a 18-pin DIP (Dual In-line Package), while μ PD6451AGT-101 and μ PD6451AGT-301 are enclosed in a 20-pin SOP (Small Out-line Package).

FEATURES

- Number of characters displayed : 12 lines \times 24 columns
- Number of character types : 112
- Character size : Any one of 1H, 2H, 3H, and 4H per dot can be selected.
- Character color : Any one of 8 colors can be selected for each character.
- Background : One of No Background, Black fringe, Square Background, or Solid Background can be selected for each image. (For Square Background and Solid Background, any one of eight colors can be selectable.)
- Dot matrix : 12-by-18 dot pattern with no space between characters.
- Blink : Selectable at 1:1, 3:1, or 1:3.
- Mask pulse (Code Option) : To be output in vertical direction for each line.
- Progressive scan TV mode (Switching by Command) : Switching of the vertical-scan lines counter adapts to a system in which one field contains 525 scan lines.
- Blanking signal output : 1 blanking signal output (V_{BLK}) or 3 blanking signal output (R_{BLK} , G_{BLK} , B_{BLK}) are selectable by mask code option.
- Interface with microprocessor : 8-bit serial input format
- Power supply : +5 V single power supply
- Construction : Low-power-consumption CMOS

ORDERING INFORMATION

PART NUMBER	PACKAGE	QUALITY GRADE
μ PD6451ACX-001	18-pin plastic DIP (300 mil)	standard
μ PD6451AGT-101	20-pin plastic SOP (375 mil)	standard
μ PD6451AGT-301	20-pin plastic SOP (375 mil)	standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

The block diagram illustrates the VLSI architecture of the TMS320C25 DSP. It shows the internal components and their interconnections. Key components include:

- Input/Output:** DATA, CLK, STB, BUSY, CKOUT, OSCIN, OSCOUT, LOSC, COSCIN, COSCOUT, HSYNC, VSYNC, HOLD, VMON, VR, VG, VB, VBLK.
- Control and Timing:** Instruction decoder, F0, Write address counter, Horizontal address counter, Vertical address counter, Horizontal position counter, Vertical position counter, Horizontal size counter, Vertical size counter, Synchronous protection circuit, Oscillation circuit, OSCOUT, LOSC, COSCIN, COSCOUT, HSYNC, VSYNC, HOLD.
- Data Path:** Data input shift register, Character size register, Horizontal address register, Horizontal position counter, Horizontal size counter, Data selector, Video RAM (Character data, Color data, Blink data), Character generator ROM, Output controller.
- Registers:** Background control data register, Display control data register, Horizontal address register, Vertical address register.

The diagram shows the flow of data and control signals between these components, highlighting the parallel processing capabilities of the DSP.

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Supply Voltage	$V_{DD}-V_{SS}$	7.0	V
Input Voltage	V_{IN}	$V_{DD} + 0.3 > V_{IN} > V_{SS} - 0.3$	V
Output Voltage	V_{OUT}	$V_{DD} + 0.3 > V_{OUT} > V_{SS} - 0.3$	V
Operating Temperature	T_{opt}	-20 to +75	$^\circ\text{C}$
Storage Temperature	T_{stg}	-40 to +125	$^\circ\text{C}$
Output Current	I_O	± 5	mA

RECOMMENDED OPERATING RANGE

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	$V_{DD} - V_{SS}$	4.5	5.0	5.5	V
Oscillation Frequency	f_{osc}	4.5		7.0 (12) ^{Note}	MHz

Note: The parenthesized value in the double-speed mode.

ELECTRICAL CHARACTERISTICS

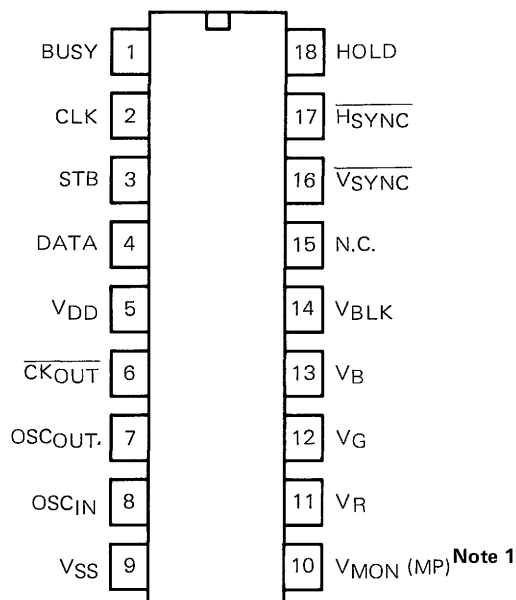
($T_a = 25^\circ\text{C}$, $V_{DD} = 5.0\text{ V}$, $V_{SS} = 0\text{ V}$, $L_{osc} = 39/56\ \mu\text{H}$, $C_{osc\ OUT} = 30\text{ pF}$, $C_{osc\ IN} = 5\text{ to }30\text{ pF}$)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Supply Voltage	$V_{DD} - V_{SS}$	4.5	5.0	5.5	V	
Current Consumption	I_{DD}			10	mA	
Control Input High Level Voltage	V_{IH}	2.4			V	
Control Input Low level Voltage	V_{IL}			0.8	V	
Synchronous Signal Input High level Voltage	V_{IH}	2.4			V	
Synchronous Signal Input Low level Voltage	V_{IL}			0.8	V	
Signal Output High level Voltage	V_{OH}	4.5			V	$I_{OH} = -1.0\text{ mA}$
Signal Output Low level Voltage	V_{OL}			0.5	V	$I_{OL} = 1.0\text{ mA}$
Clock Output High level Voltage	V_{OH}	4.5			V	$I_{OH} = -0.5\text{ mA}$
Clock Output Low level Voltage	V_{OL}			0.5	V	$I_{OL} = 0.5\text{ mA}$
Hold Signal Input High level Voltage	V_{HHOLD}	4.5			V	
Hold Signal Input Low level Voltage	V_{LHOLD}			2.5	V	

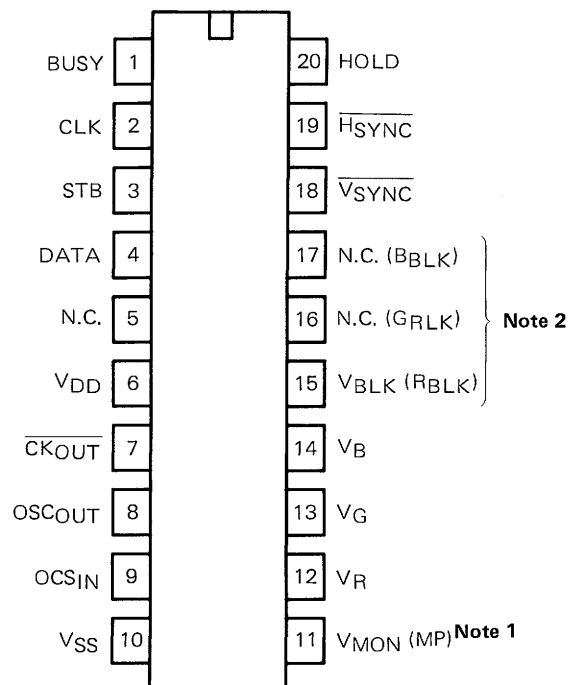
Note Control input DATA, CLK, STB
Synchronous signal input $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$
Signal output V_R , V_G , V_B , V_{BLK} , V_{MON} , BUSY
Clock output $\overline{\text{CKOUT}}$
Hold signal input HOLD

CONNECTION DIAGRAM (Top View)

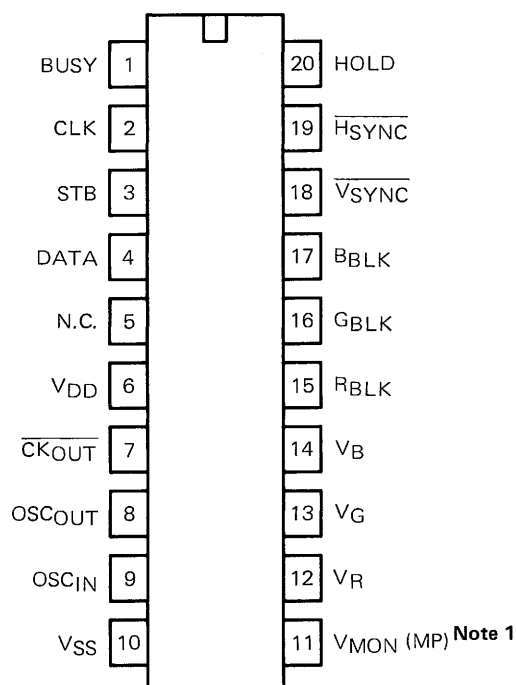
(1) μPD6451ACX-001



(2) μPD6451AGT-101



(3) μPD6451AGT-301



Note 1: Pin 10 (μPD6451ACX) or 11 (μPD6451AGT) within parentheses is the mask code option to be used as the mask pulse. However, μPD6451ACX-001, μPD6451AGT-101, μPD6451AGT-301 do not use the mask pulse, so pin 10 or 11 is used as monitor output VMON.

2: When 3 blanking signal output is selected by mask code option.

PIN DESCRIPTION

SYMBOL	PIN NAME	FUNCTION
V _{DD}	Power supply terminal	This terminal supplies +5 V power.
V _{SS}	Grounding terminal	This is connected to the system GND.
DATA	Serial data input terminal	This terminal inputs control data. It reads data synchronizing with the clock input to the CLK terminal.
CLK	Clock input terminal	This terminal inputs the clock for reading data. At the rise of this clock, the data input to the DATA terminal is read.
STB	Strobe input terminal	This terminal inputs the strobe pulse after input of serial data. The 8-bit data is read at the rise of the strobe pulse input to the STB terminal. If the 8-bit data is a character, the data address is incremented by 1 at the fall of the strobe pulse.
OSC _{IN} OSC _{OUT}	Oscillation terminals	These terminals are connected to the oscillation capacitor or coil.
H _{SYNC}	Horizontal synchronous signal input terminal	This terminal inputs the horizontal synchronizing signal. The oscillator oscillates when this signal is high, synchronizing with the rise of the signal. Be sure to input the horizontal synchronizing signal when it is active low.
V _{SYNC}	Vertical synchronizing signal input terminal	This terminal inputs the vertical synchronizing signal. Be sure to input this signal when it is active low.
V _R V _G V _B	Character signal output terminals	These terminals output the character data corresponding to R, G, and B.
V _{BLK}	Blanking signal output terminal	This terminal outputs the blanking signal to cut the video signal.
R _{BLK} G _{BLK} B _{BLK}	Blanking signal output terminal	These terminals output the blanking signal correspond to the character signal (V _R , V _G , V _B).
CK _{OUT}	Clock output terminal	This is the inverted output of OSC OUT. To connect another type of on-screen IC in parallel, be sure to connect this terminal to OSCIN of the IC.
HOLD	Hold terminal	Oscillation stops when this signal is low. At this time, the signals output from V _R , V _G , V _B , and V _{BLK} all become low. (Be sure to normally set this signal high.)
BUSY	Data input enable terminal	Output terminal to notify the microcomputer that data is enabled or disabled for input. Data can be input at a low level.
V _{MON} Note	Character signal output monitor terminal	If any of character signal outputs V _R , V _G , and V _B is High, the high-level signal is output.

Note:

The mask code option enables this terminal to be used as the mask pulse output terminal.

However, μ PD6451ACX-001, μ PD6451AGT-101, μ PD6451AGT-301 does not use the mask pulse, so pin 10 or 11 is used as monitor output V_{MON}.

Command Format

All the control commands are in 8-bit serial input format.

Each control command is executed when a strobe pulse is input after 8-bit data has been input.

Before starting the program, be sure to input the format reset command ("FR = 1", set by the format selection command) to release the test mode.

μ PD6451ACX-xxx/6451AGT-xxx Command List

Content	F ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Display character data	0	0	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀
Color blink data for each character	0	1	0	0	0	Blink	R	G	B
Character display line address	0	1	0	0	1	AR ₃	AR ₂	AR ₁	AR ₀
Character display column address	0	1	0	1	AC ₄	AC ₃	AC ₂	AC ₁	AC ₀
Background specification	0	1	1	0	BS ₄	BS ₃	R _b	G _b	B _b
Blink, oscillation, Display ON/OFF	0	1	1	1	0	D ₀	BL ₂	BL ₁	OSC
Fringing Control	0	1	1	1	1	0	0	Eg ₁	Eg ₂
Format selection	X	1	1	1	1	1	1	F ₀	FR
Display position vertical address, Double-speed selector	1	0	1	V _D	V ₄	V ₃	V ₂	V ₁	V ₀
Display position horizontal address	1	1	1	0	H ₄	H ₃	H ₂	H ₁	H ₀
Character size specification Note	1	1	0	S ₅	S ₄	AR ₃	AR ₂	AR ₁	AR ₀
Test mode setting	1	1	1	1	0	T ₃	T ₂	T ₁	T ₀

Note:

Change of a command by using a mask pulse (mask code option).

If the mask code option allows pin 10 (6451ACX) or 11 (6451AGT) to be used as the mask pulse output terminal (MP), the character size specification command is changed as follows and used as the mask pulse selection command. (The number of selectable character sizes is changed from 4 to 2.)

Content	F ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Character size/mask pulse	1	1	0	MP	S ₄	AR ₃	AR ₂	AR ₁	AR ₀

Format Selection/Reset (Test Mode Releasing)

The μ PD6451A commands consist of 9 bits, but the shift registers for serial interfacing with external units consist of 8 bits. Therefore, instructions are divided into two banks. One of these banks is selected by one bit of the format selection command.

Bank-0 commands ($F_0 = 0$)

- Display character data
- Color/blink data for each character
- Character display line address
- Character display column address
- Background specification
- Blink, Oscillation control, Display ON/OFF
- Fringing control

Bank-1 commands ($F_0 = 1$)

- Vertical display position address, Double-speed selector
- Horizontal display position address
- Character size specification

Format Reset (Test Mode Releasing)

When bit 1 (FR) of the format reset command is set to "1", the test command mode is released to reset the contents of the following command. A normal command cannot be accepted in the test command mode. Therefore, be sure to release the test command mode by resetting the format before starting the program.

Command to Be Reset

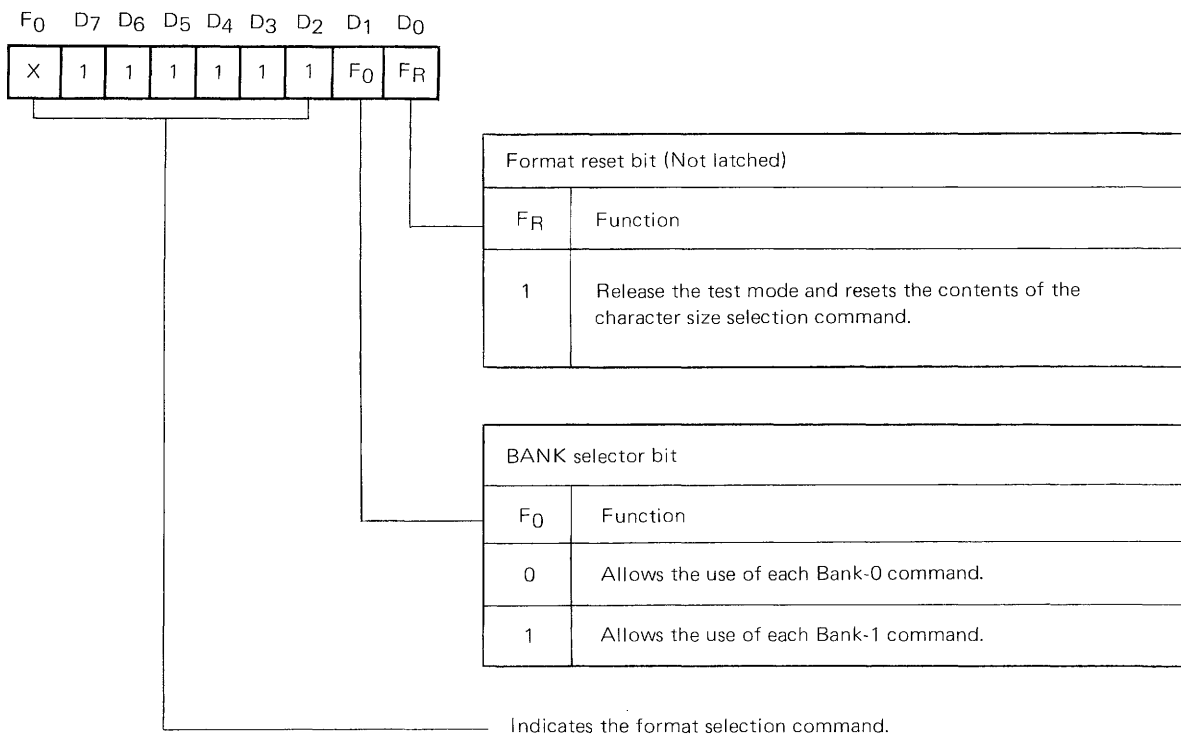
The contents of all the line size registers (AR_{0-3}) are set to $(S_5, S_4) = (0, 0)$.

[All the lines are specified in the minimum size.]

If the mask option allows pin 10 (μ PD6451ACX) or pin 11 (μ PD6451AGT) to be used as the mask pulse output terminal, the contents of all the line size registers (AR_{0-3}) are set to " $(S_4) = (0)$ " to disable the mask pulse output from any line. (MP) = (0).

To release the test command mode without resetting the above command, use the test command mode release instruction ($F_0, D_7, D_6, D_5, D_4, D_3, D_2, D_1, D_0$) = (1, 1, 1, 1, 0, 0, 0, 0, 0).

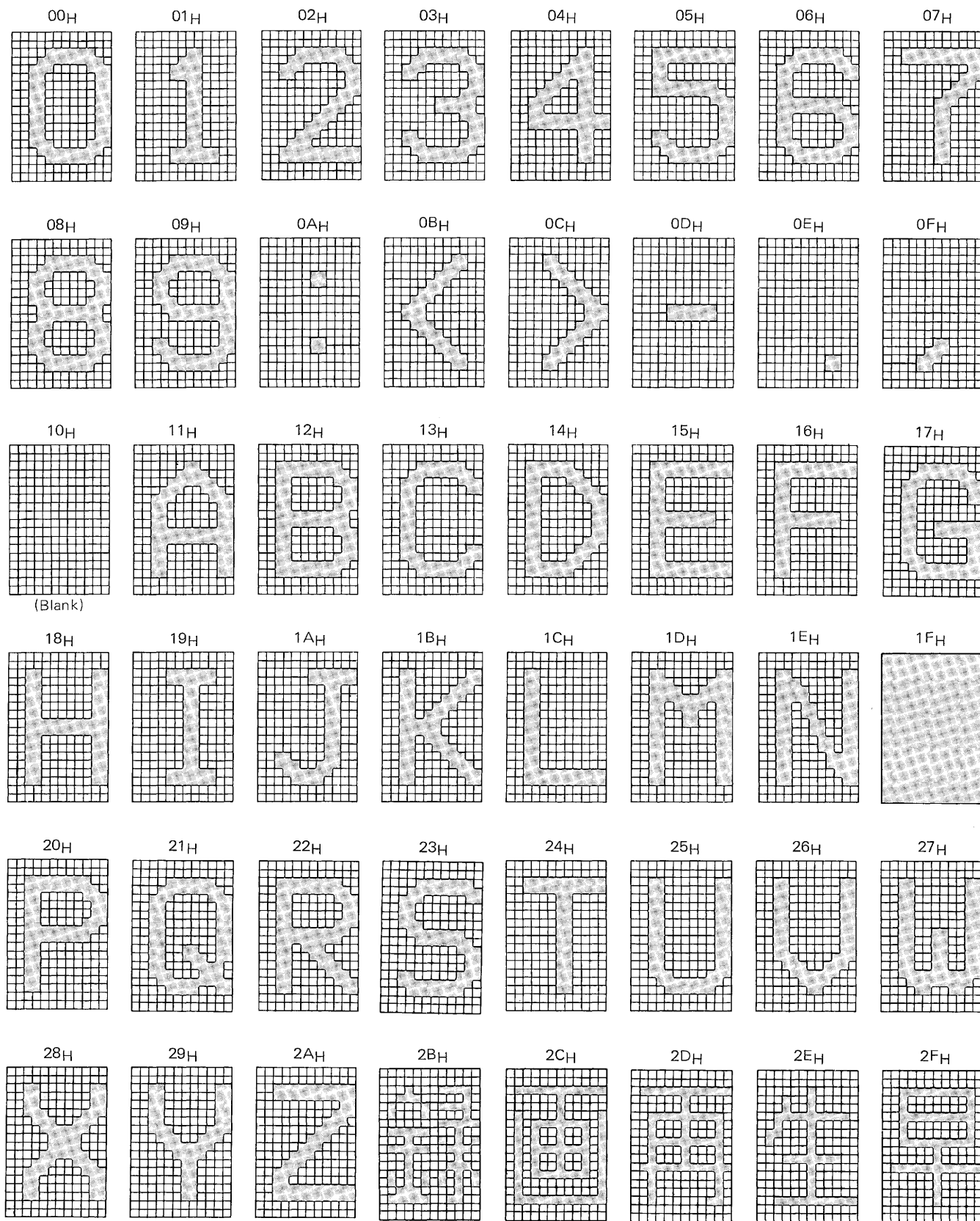
Format Selection Command

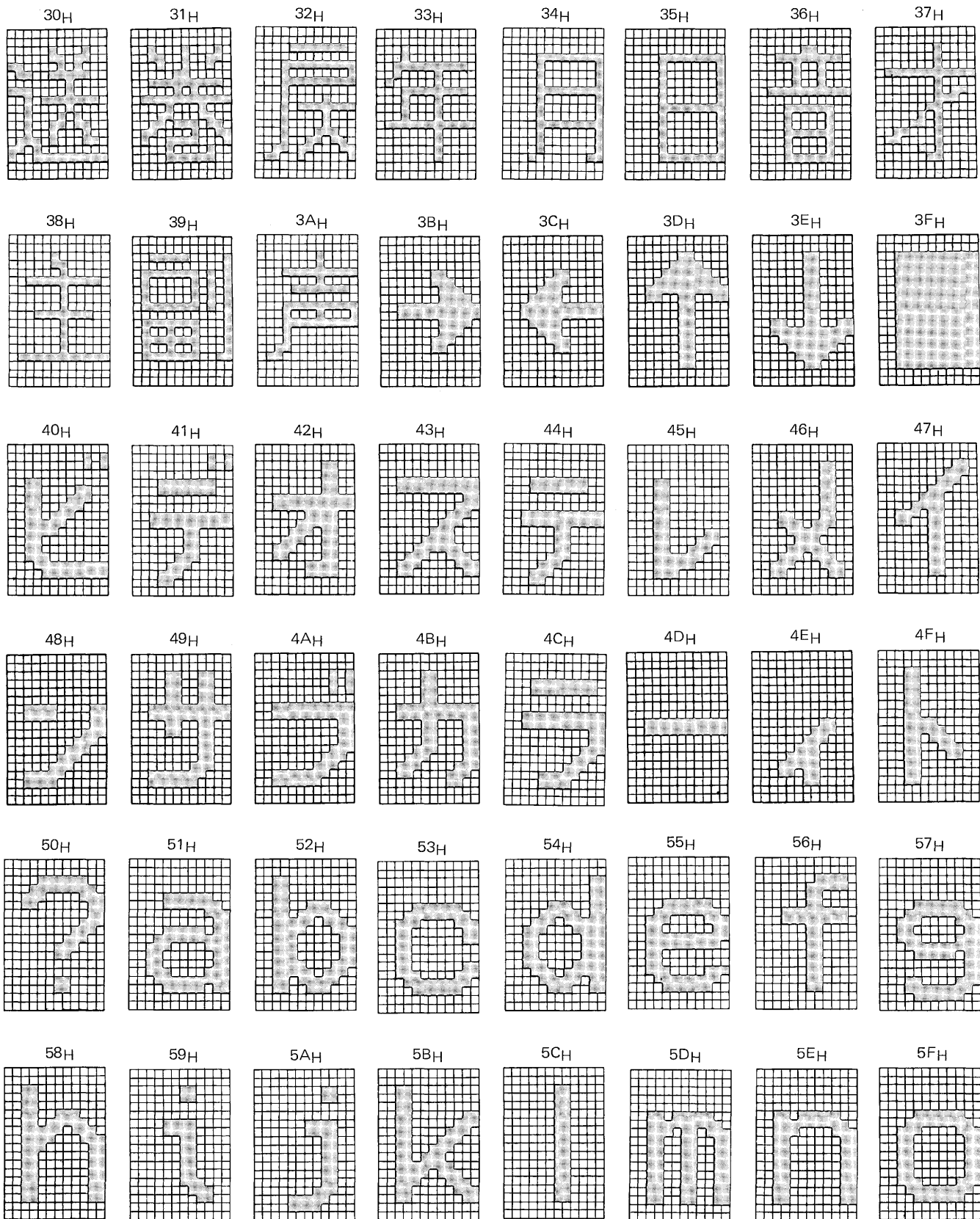


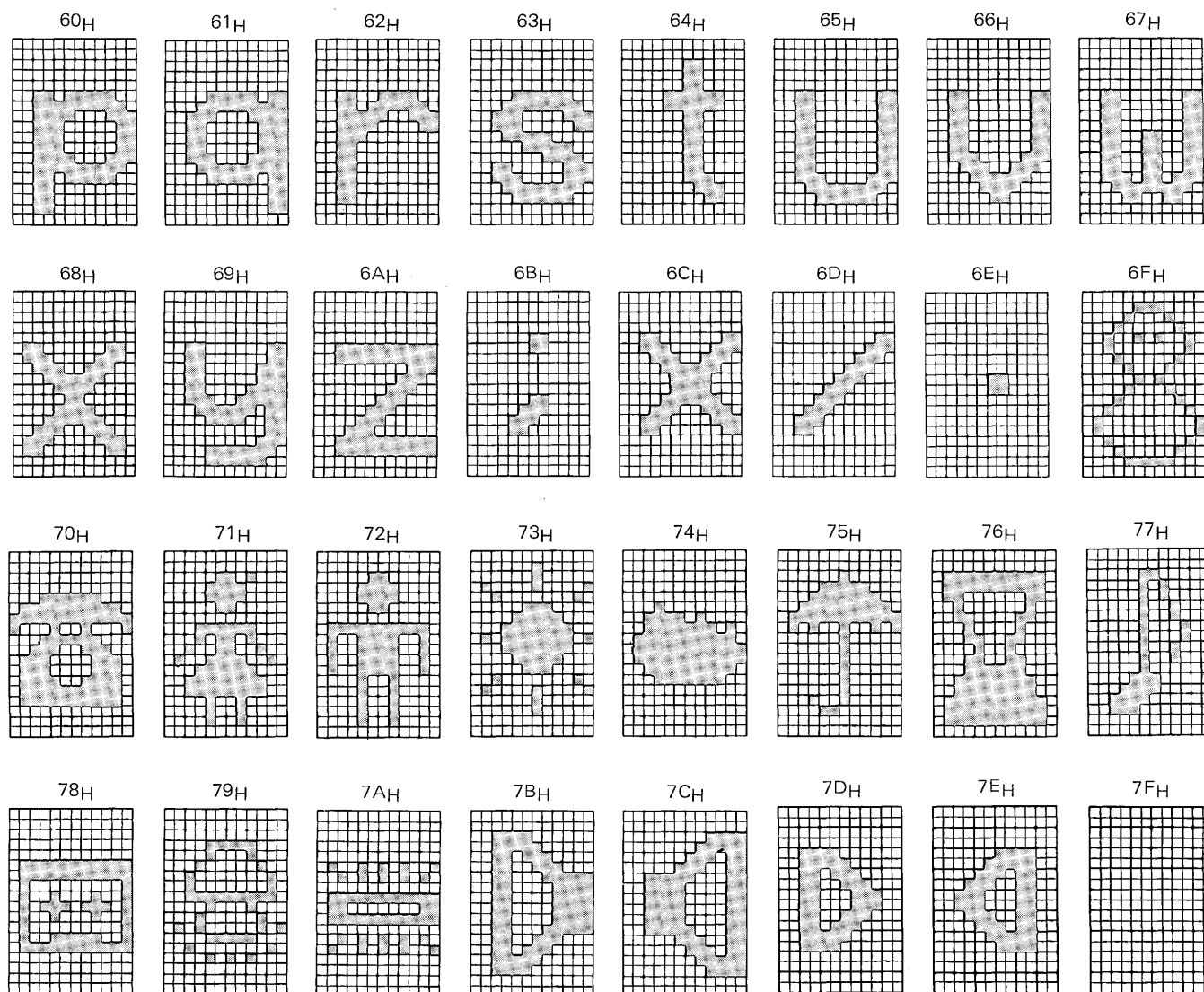
μPD6451ACX-001, μPD6451AGT-101, μPD6451AGT-301 Character Pattern

As shown in the following, μPD6451ACX-001, μPD6451AGT-101, μPD6451AGT-301 enables display of 128 character generator ROM patterns. The 128 character generator ROM patterns can be changed by the mask code option. However, character code "7FH" is fixed to the display OFF code so that no character pattern can be input to this code.

μPD6451CX-001 and μPD6451AGT-101 have the same character patterns in the character generator ROM though their packages are different. μPD6451AGT-101 and μPD6451AGT-301 have the same package though their character patterns are different.

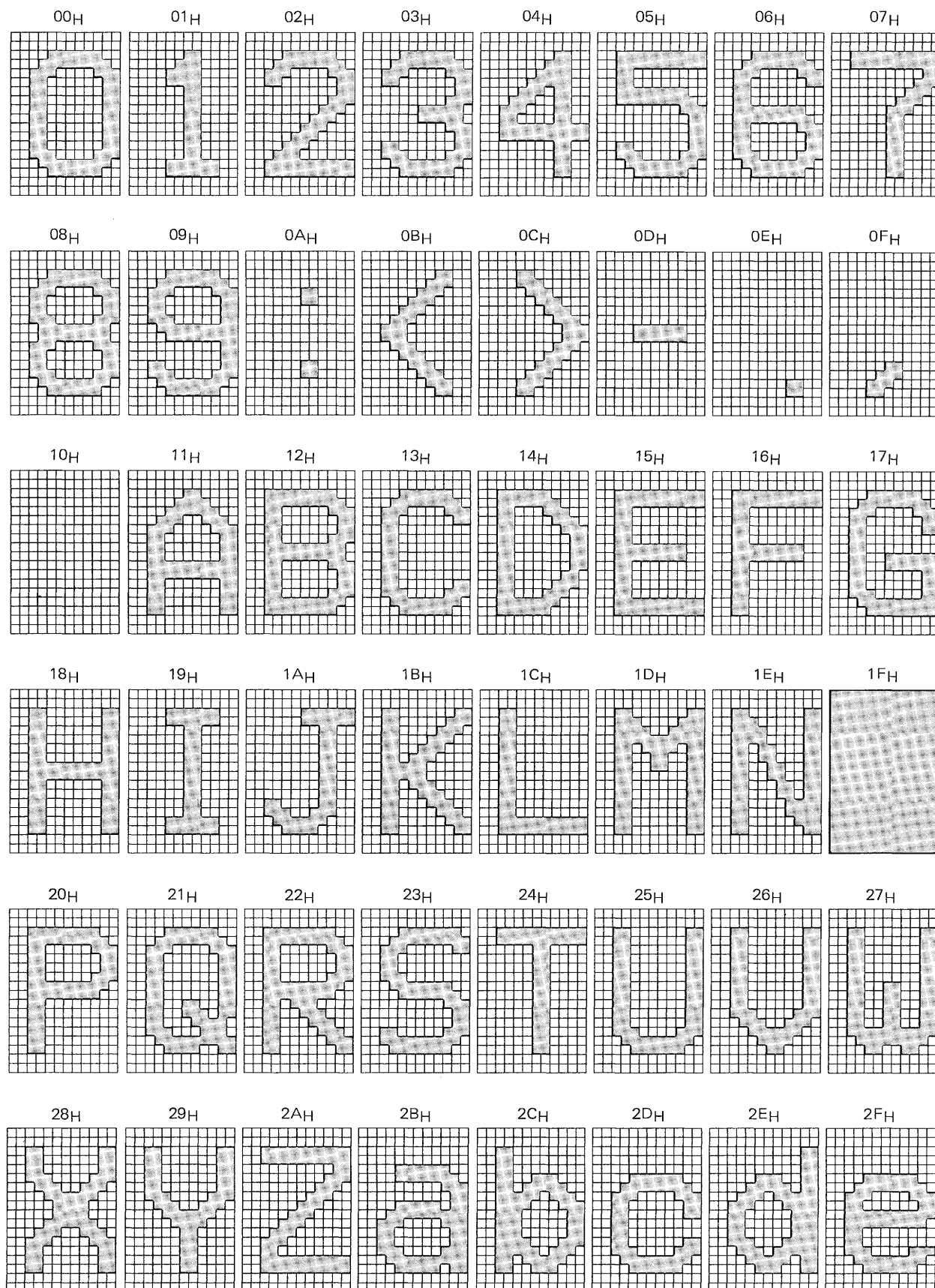
μ PD6451ACX-001, μ PD6451AGT-101 Character Patterns

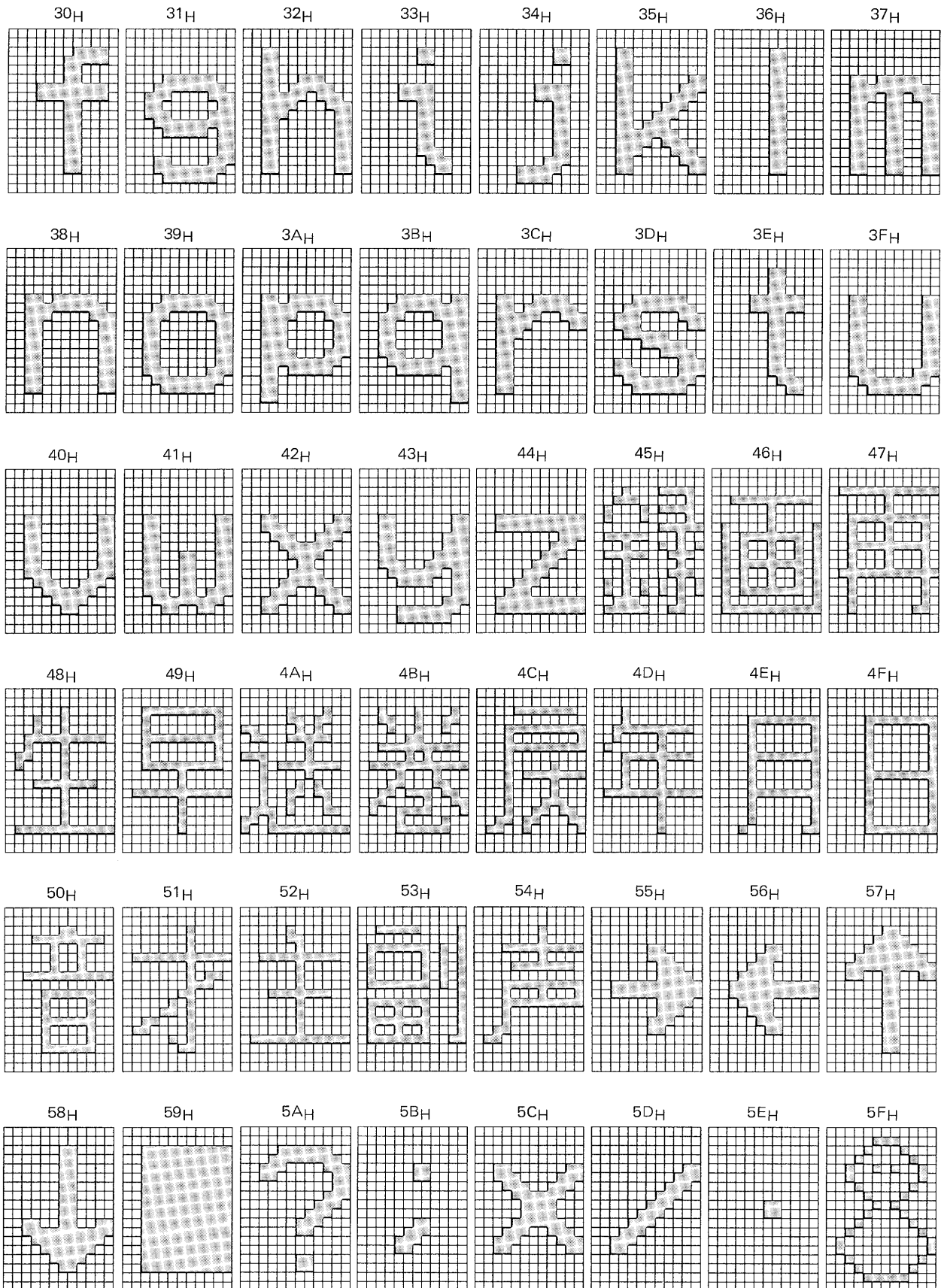


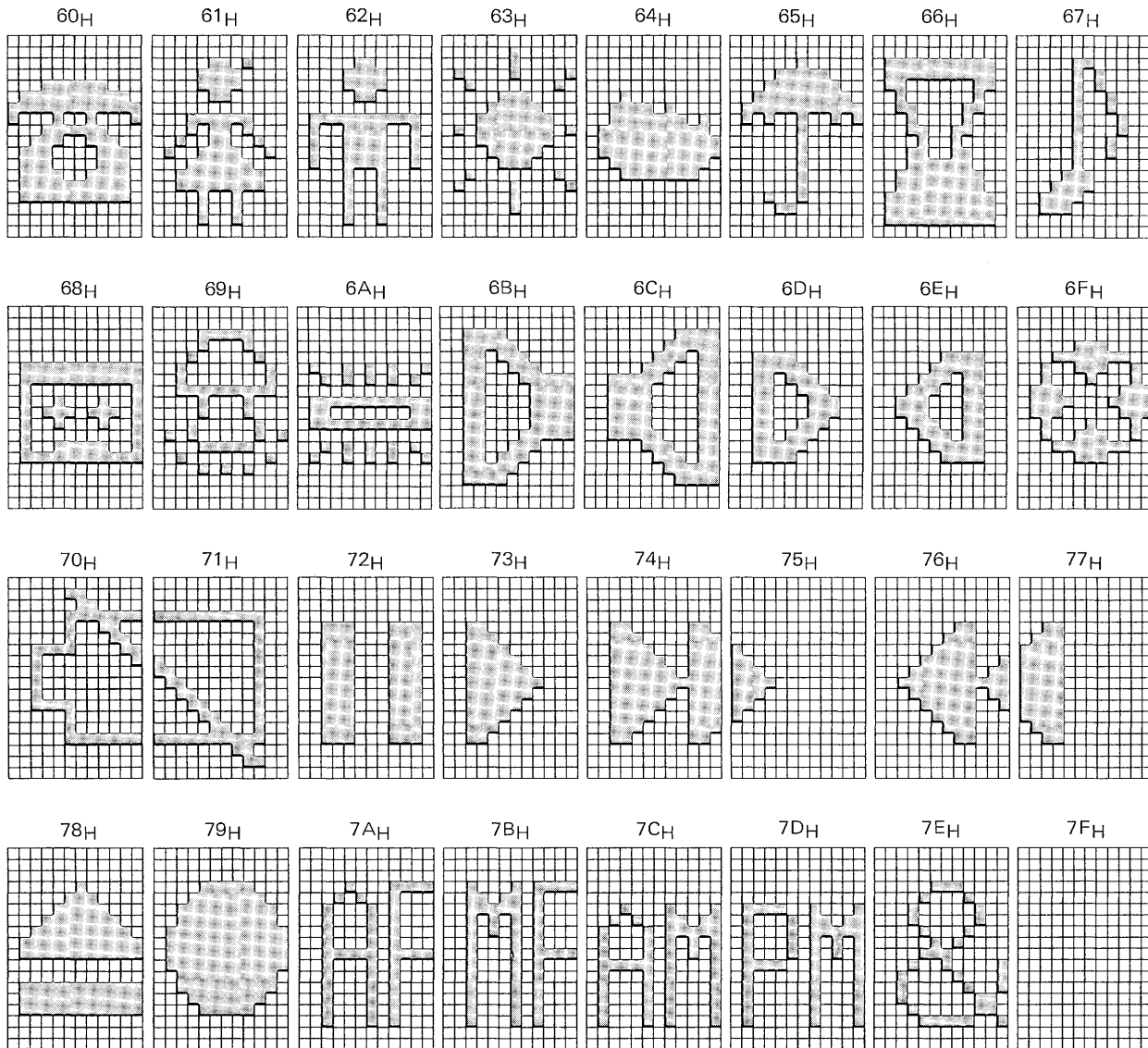


Display off data
(No character pattern
can be entered)

μPD6451AGT-301 Character Patterns







Display off data
(No character pattern
can be entered)

Character Display

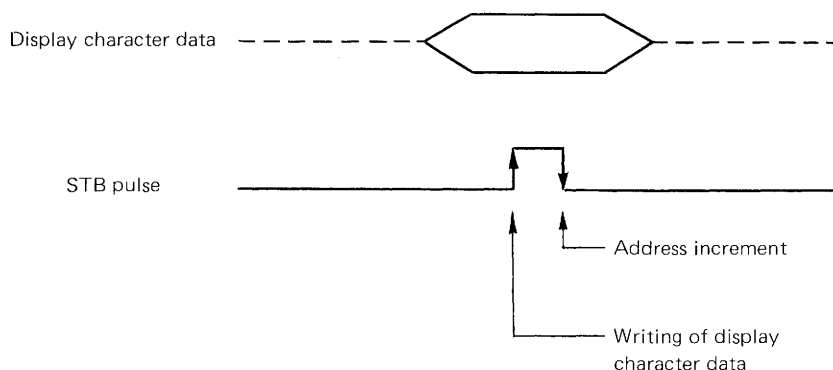
The number of characters displayed is 12 lines x 24 columns; that is, 288 as shown below:

AC4, AC3, AC2, AC1, AC0		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
AR3 AR2 AR1 AR0	0000																
	0001																
	0010																
	0011																
	0100																
	0101																
	0110																
	0111																
	1000																
	1001																
	1010																
	1011																

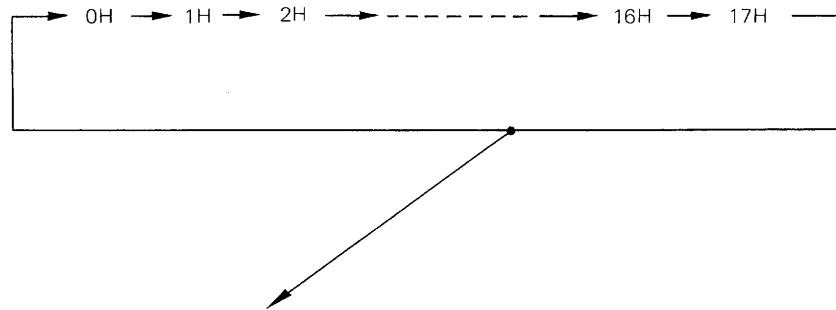
Writing of Display Character Data and Color/Blink Data for Each Character

The write address for data can be directly set in the address counter by the character display line address command and the character display column address command.

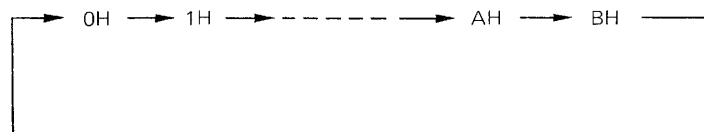
After the write address is set, the color/blink data for each character is input by the color/blink data command. The color or blink data for each character is saved in the internal register. Then, the display character data is input by the display character data command. At the rise of the STB pulse (to be input at completion of execution of the display character data command), the color/blink data and the display character data, which are saved in the internal register, are written to the video RAM. The write address is incremented as shown below at the fall of the STB pulse when the display character data is input. To write display character data continuously without changing the color/blink data for each character, just input the display character command.



Column address counter AC₄, AC₃, AC₂, AC₁, AC₀

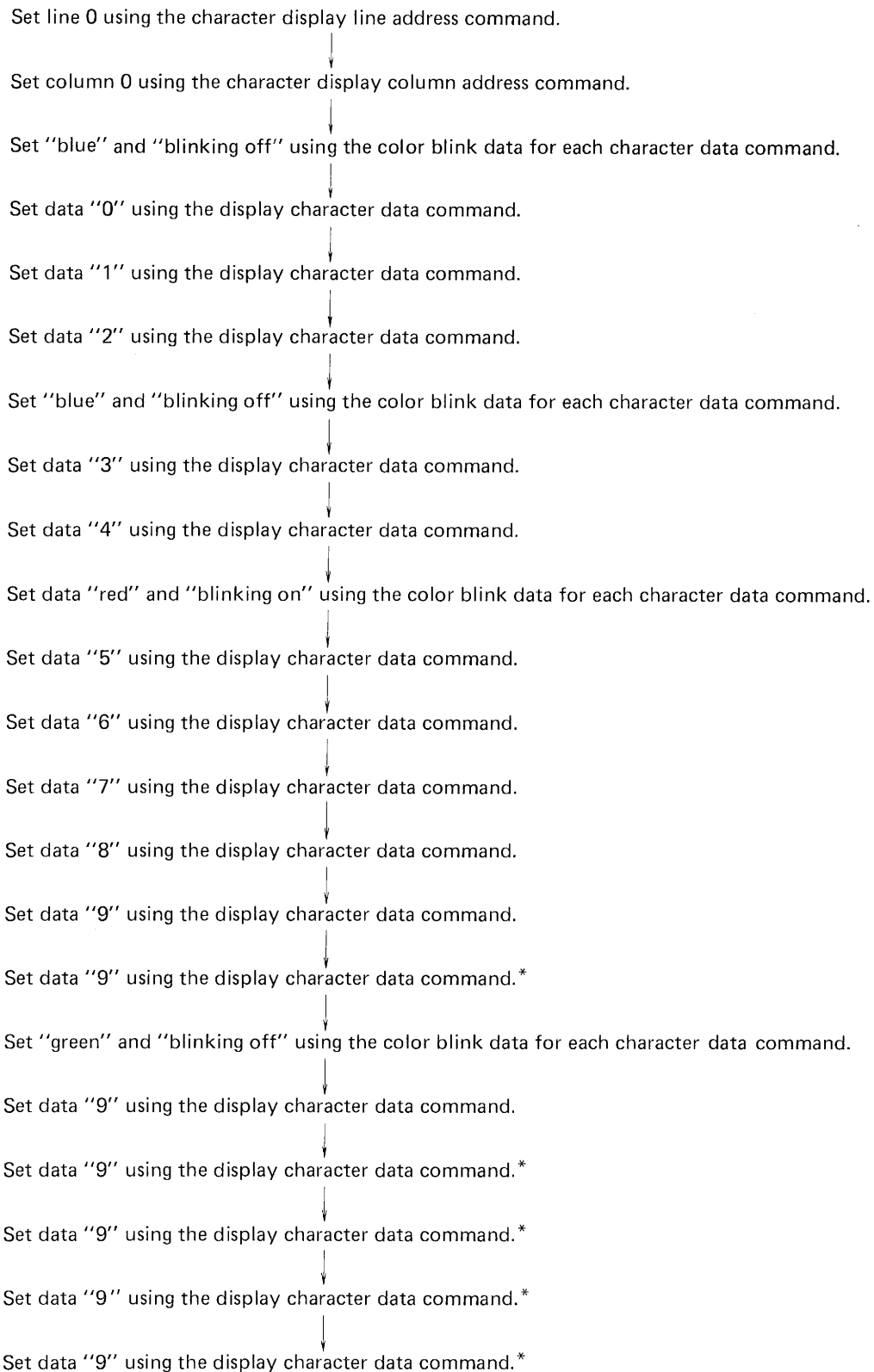


Line address counters AR₃, AR₂, AR₁, AR₀



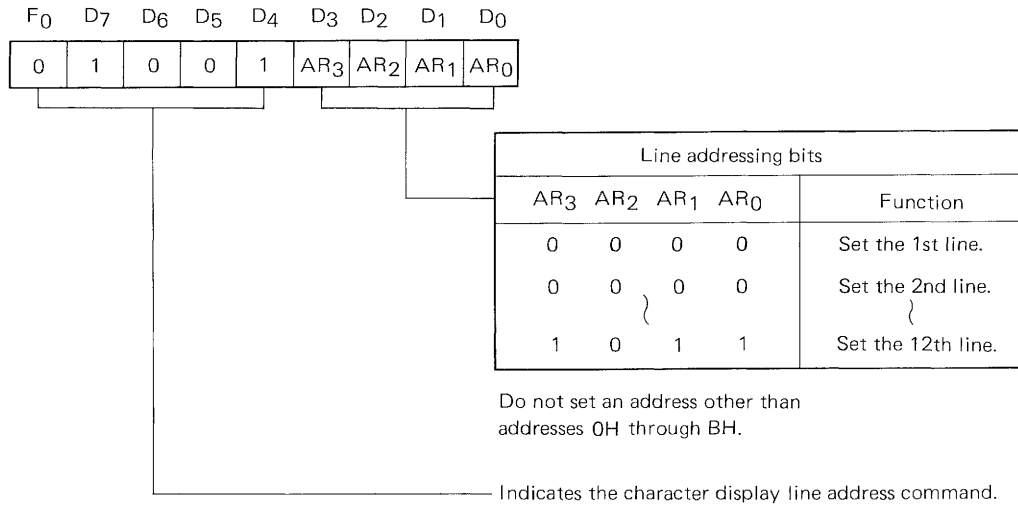
Example: Writing of the following data in lines/columns from line 0/column 0 to line 0/column F

Character color	Blue	Blue	Blue	Blue	Blue	Red	Red	Red	Red	Red	Red	Green	Green	Green	Green	Green
Character blinking	OFF	OFF	OFF	ON	ON	ON	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF	OFF
Display character	0	1	2	3	4	5	6	7	8	9	9	9	9	9	9	9

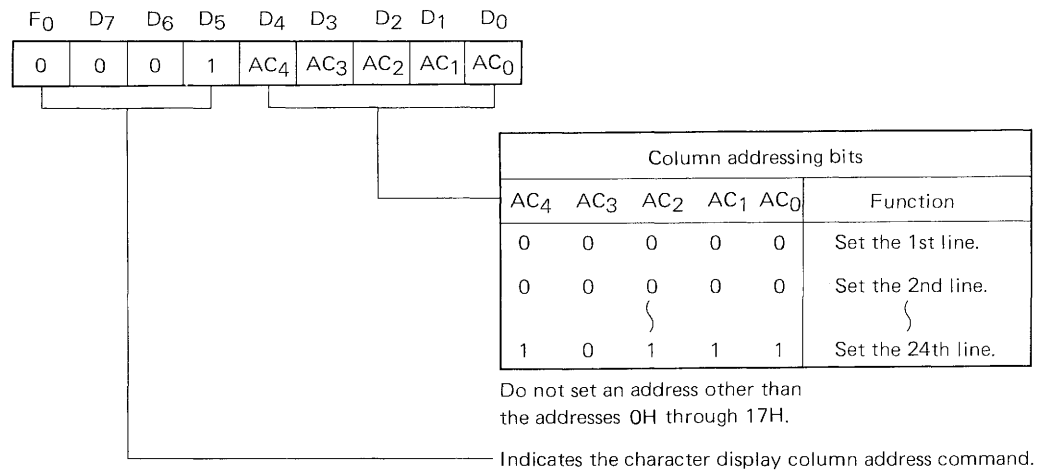


*Data can be set by only sending the STB signal without sending 8-bit serial data.

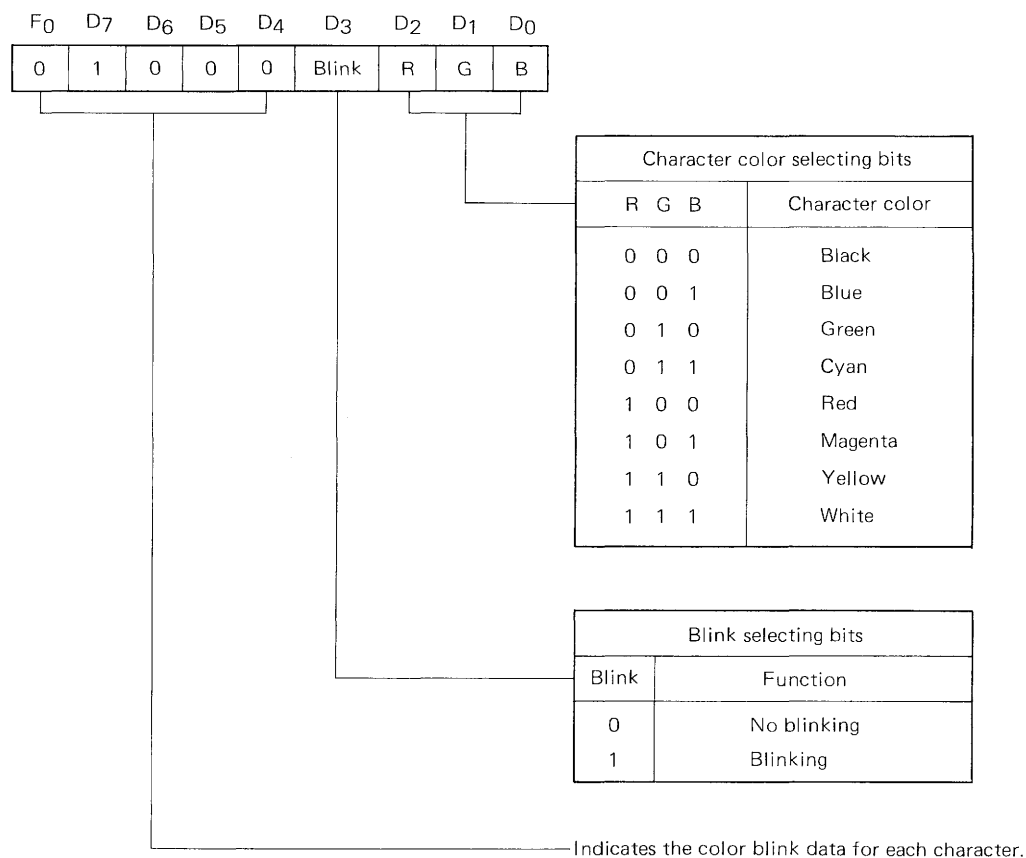
Character Display Line Address Command



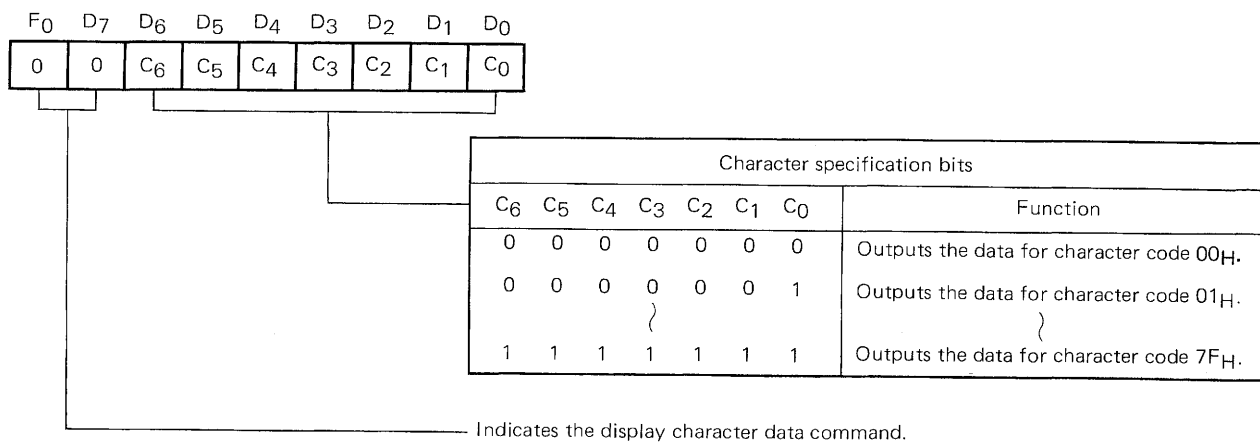
Character Display Column Address Command



Color Blink Data for Each Character Command



Display Character Data Command



Oscillation Control

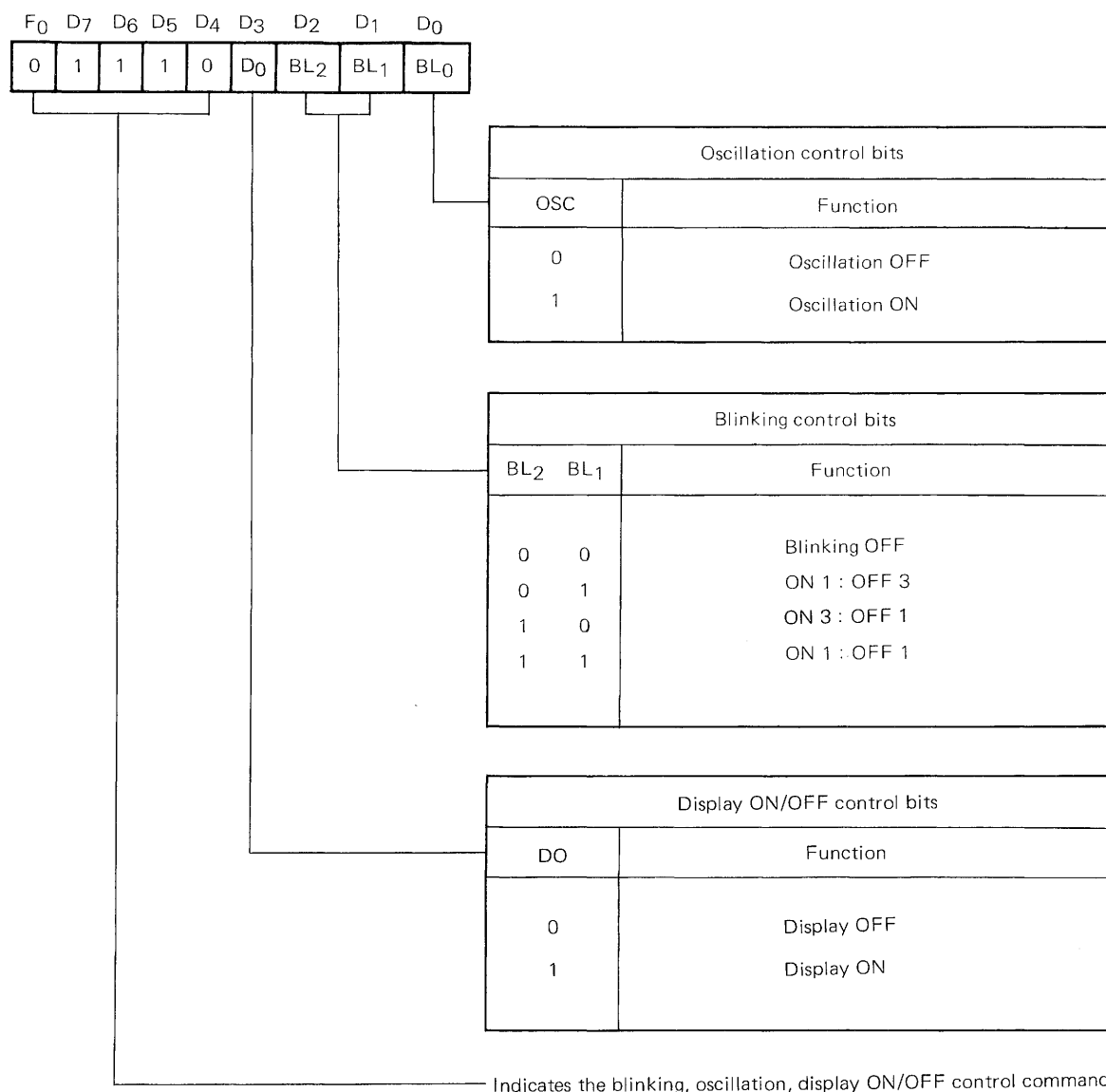
This IC allow oscillation to be turned ON/OFF with the blinking/oscillation control command so that it can stop oscillation during the period for displaying no character in order to save power. However, the character output remains executable even after oscillation has been stopped. Therefore, use the display control command in conjunction with this command. And the VRAM cannot be overwritten while oscillation is off.

Note: When display is ON, the oscillation synchronizes $\overline{\text{HSYNC}}$, so the oscillation is stopping at the low level term of $\overline{\text{HSYNC}}$. When display is OFF, the oscillation keeps on irrespective of $\overline{\text{HSYNC}}$.

Character Blinking

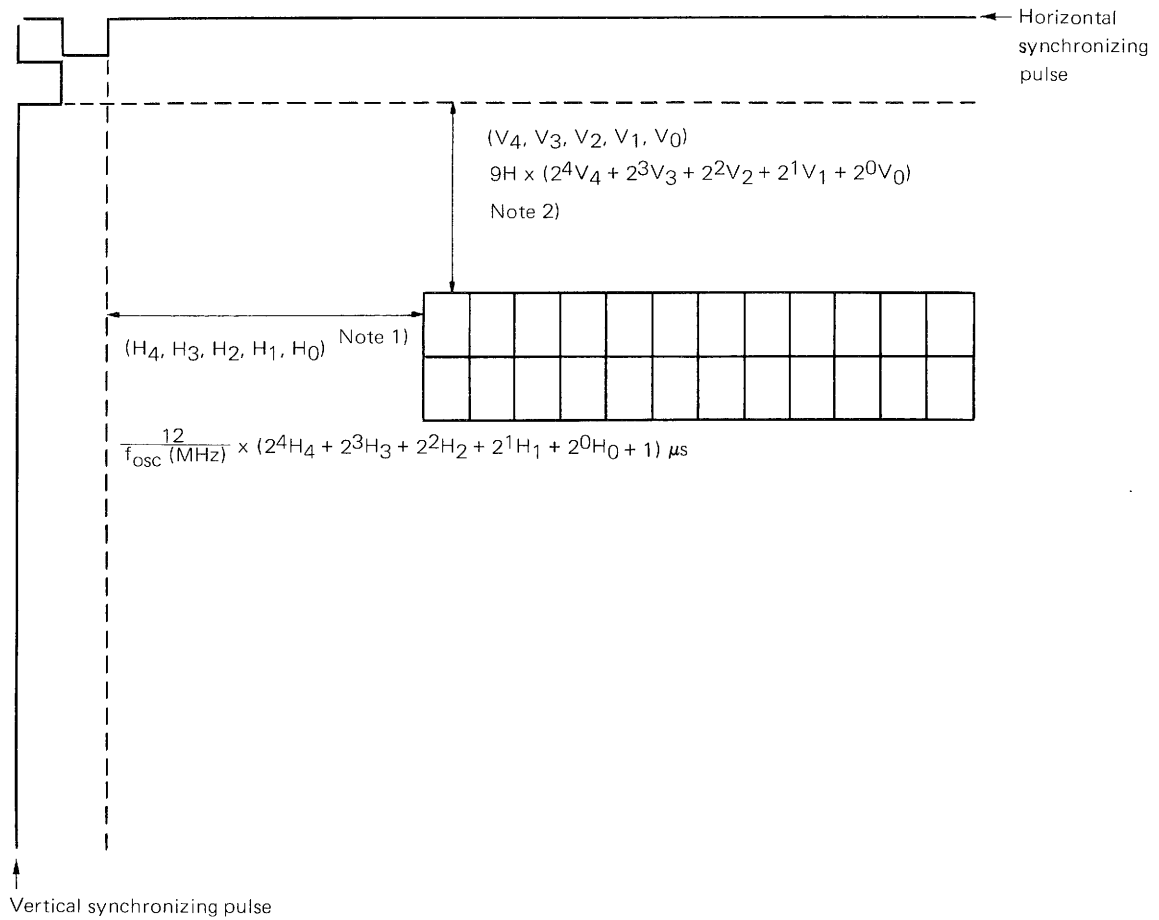
This IC allow character-by-character blinking with the blinking/oscillation control command. Use the color blink data for each character command to specify the character or characters to be blinked. Select a blinking ratio of 1:1, 1:3, or 3:1. (A blinking cycle of approximately one second is equivalent to 64 times the vertical cycle.)

Blinking, Oscillation, Display ON/OFF Control Command



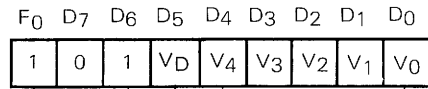
Character Display Address

The character display start address can be determined, as shown below, according to the values specified by the display position vertical address Progressive selector command ($F_0, D_7, D_6, D_5, D_4, D_3, D_2, D_1, D_0$) = (1, 0, 1, $V_D, V_4, V_3, V_2, V_1, V_0$) and the display position horizontal address command ($F_0, D_7, D_6, D_5, D_4, D_3, D_2, D_1, D_0$) = (1, 1, 1, 0, H_4, H_3, H_2, H_1, H_0):



Note 1: 9H is changed to 18H when the progressive scan TV mode is selected by the progressive selector command.

Display Position Vertical Address Command

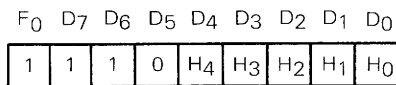


Vertical address assignment bits					
V ₄	V ₃	V ₂	V ₁	V ₀	Start address
0	0	0	0	0	From the trailing edge of the vertical synchronizing pulse Note) 9 x 0H
0	0	0	0	1	From the trailing edge of the vertical synchronizing pulse 9 x 1H
1	1	1	1	1	From the trailing edge of the vertical synchronizing pulse 9 x 31H

Progressive scan selector bit	
V _D	Function
0	Normal TV
1	Progressive scan TV

Indicates the command for display position vertical address and double-speed switching.

Display Position Horizontal Address Command



Horizontal address assignment bits					
H ₄	H ₃	H ₂	H ₁	H ₀	Start address
0	0	0	0	0	From the trailing edge of the horizontal synchronizing pulse $12/f_{\text{osc}}(\text{MHz}) \times 1 \text{ } [\mu\text{s}]$
0	0	0	0	1	From the trailing edge of the horizontal synchronizing pulse $12/f_{\text{osc}}(\text{MHz}) \times 2 \text{ } [\mu\text{s}]$
1	1	1	1	1	From the trailing edge of the horizontal synchronizing pulse $12/f_{\text{osc}}(\text{MHz}) \times 32 \text{ } [\mu\text{s}]$

Indicates the display position horizontal address command.

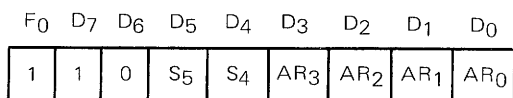
Note: 9H is changed to 18H when the progressive scan TV mode is selected by the progressive selector command.

Character Size Specification

As the character size, one dot 1H, 2H, 3H, or 4H can be selected for each line. Use the character size specification command to specify lines and their character sizes.

If, however, the mask pulse function is selected by the mask option, only two character sizes (one-dot 2H and 4H) can be selected. (See the section for the mask pulse.)

Character Size Specification Command



Line address selection bits				Function
AR3	AR2	AR1	AR0	
0	0	0	0	Select the 1st line.
0	0	0	1	Select the 2nd line.
}				}
1	0	1	1	Select the 12th line.

Do not set an address other than addresses 0H through BH.

Character size specification bits		Character dot size	
S5	S4		
0	0	Vertical 1H	Horizontal t_{dot}
0	1	2H	$2 \cdot t_{\text{dot}}$
1	0	3H	$3 \cdot t_{\text{dot}}$
1	1	4H	$4 \cdot t_{\text{dot}}$

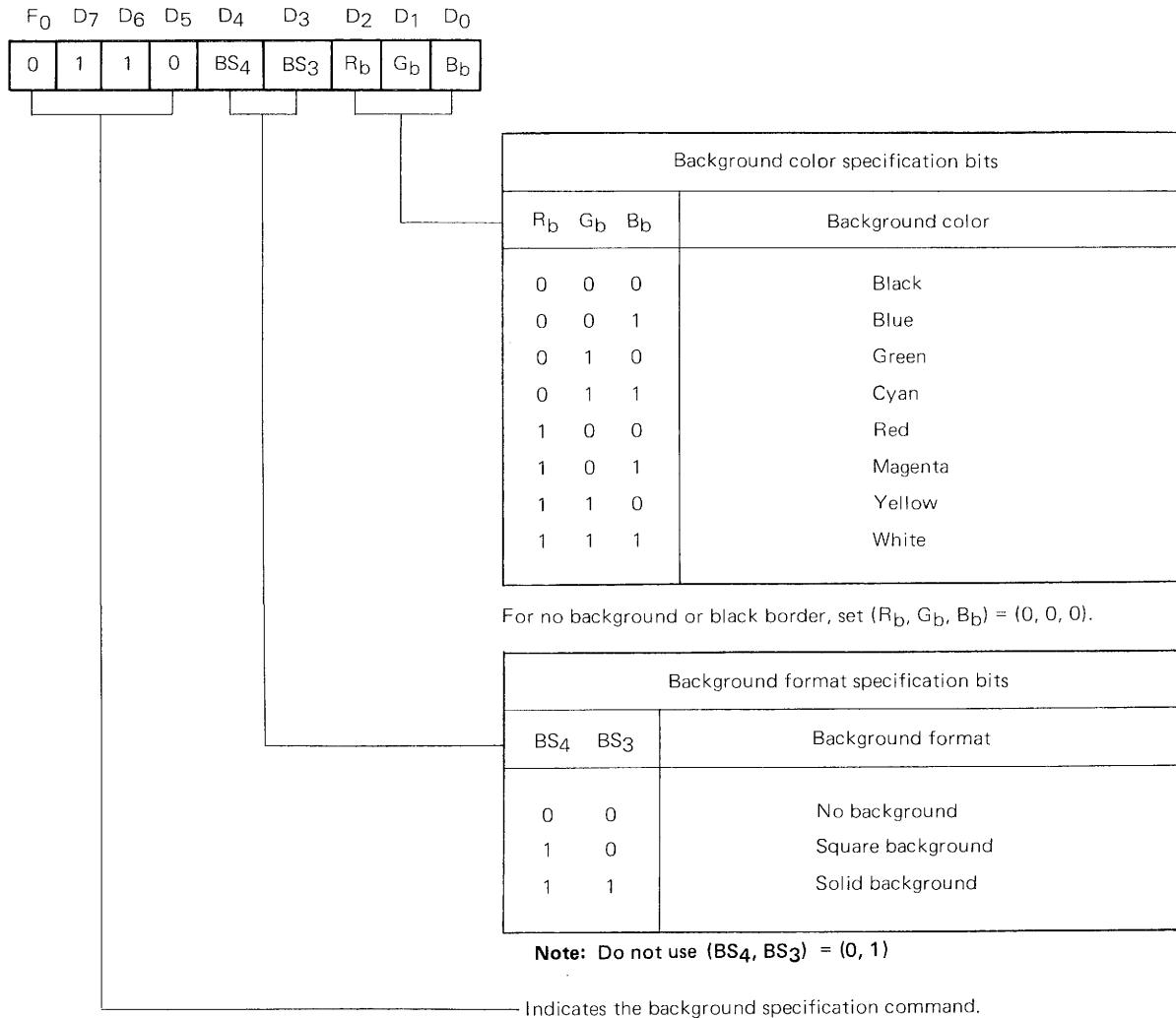
$$t_{\text{dot}} = \frac{1}{f_{\text{osc}}(\text{MHz})} \mu\text{s}$$

Indicates the character size specification command.

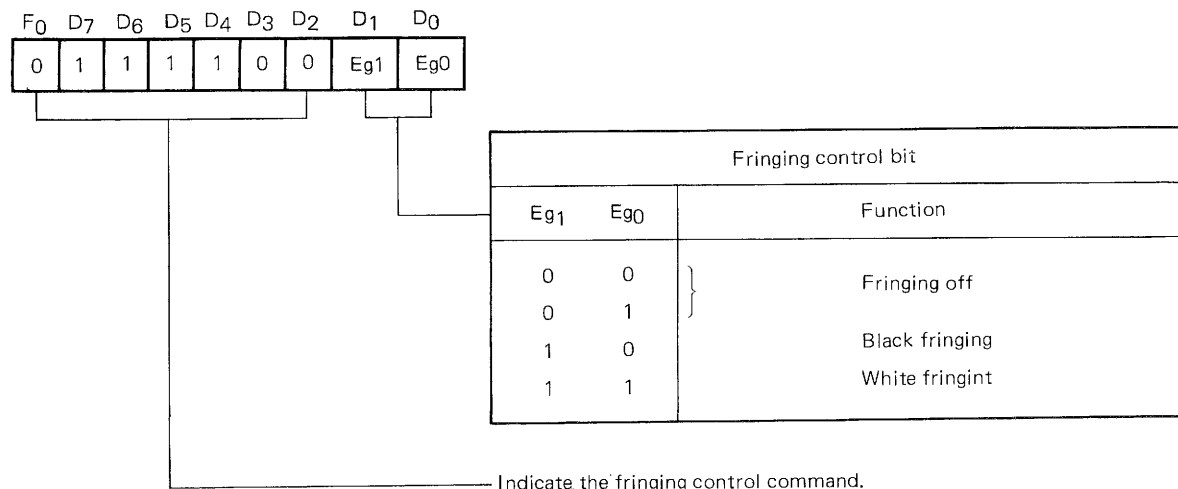
Background Specification

The background type and color can be specified for each image using the background specification command. The background types available are: no background, black fringe, square background, and solid background. The background colors available are: black, blue, green, cyan, red, magenta, yellow, and white.

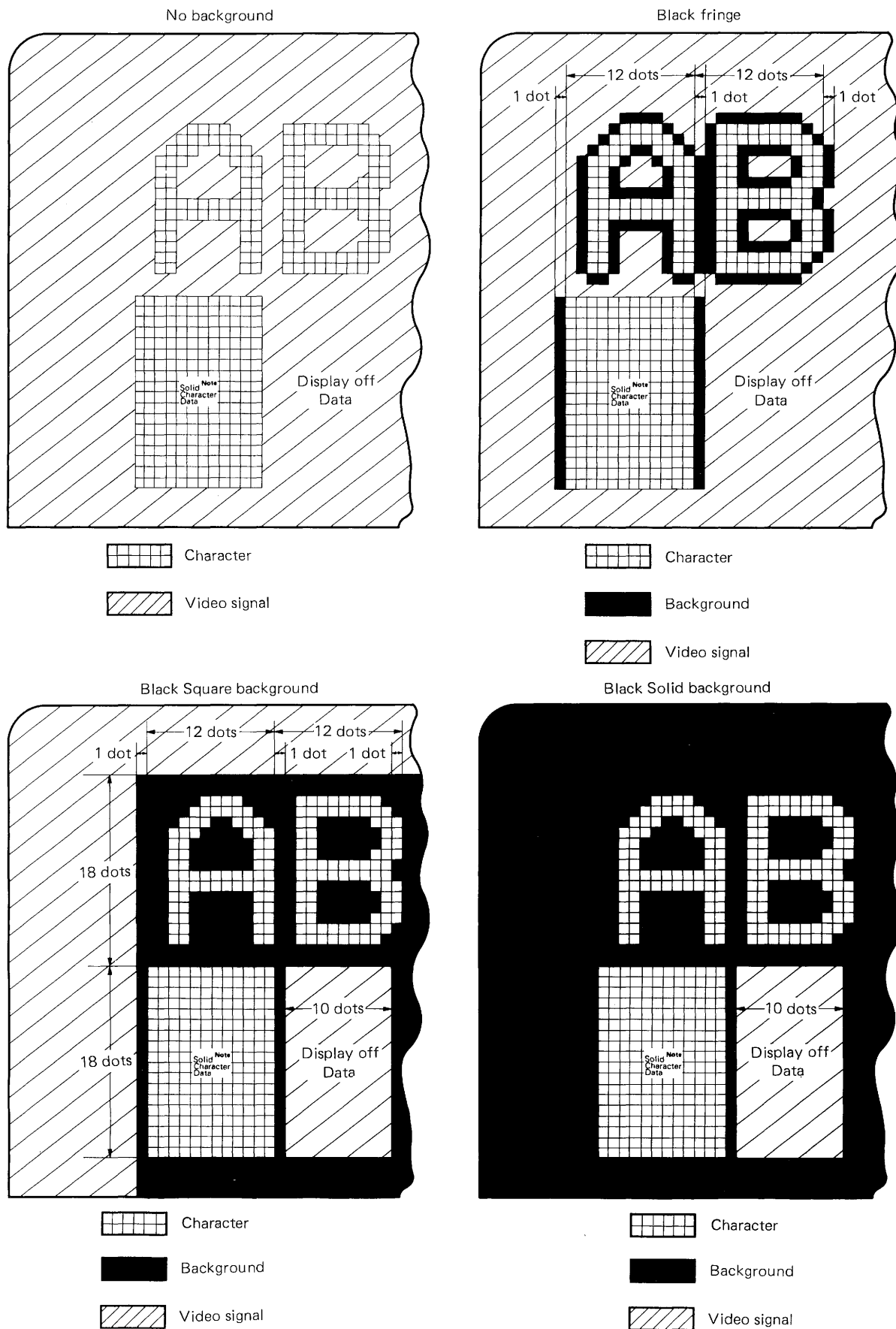
Background Specification Command



Fringing Control Command



Display in Various Background Modes



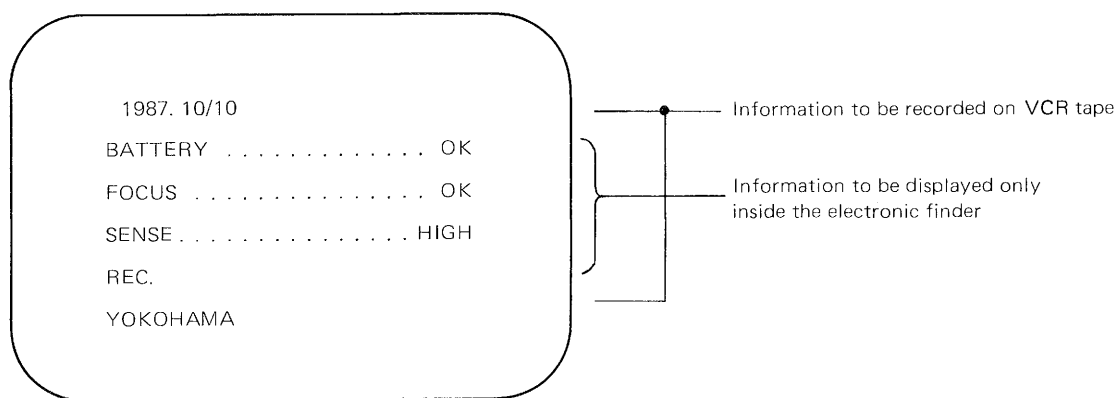
Note: The solid character data means the data of character code 1FH (standard type of NEC).

Write Control

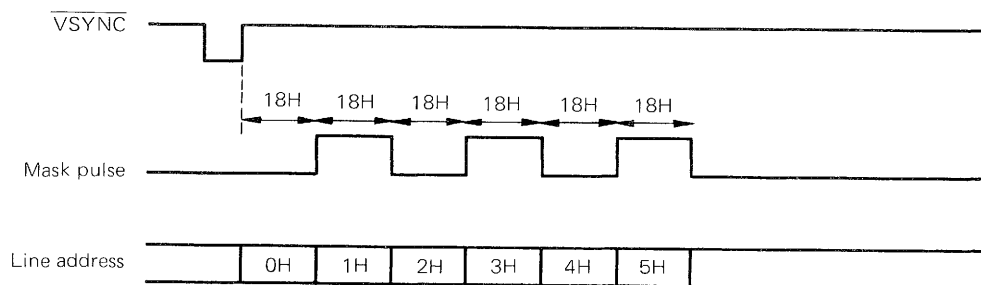
Data to be displayed is synchronized with the dot clock whether or not characters are being displayed on the screen according to the display on/off command. While the displayed data is being written, the BUSY terminal (terminal 1) becomes high to direct the microcomputer to stop sending data, to prevent the next data from being sent to the external source.

Mask Pulse Function (Mask Code Option)

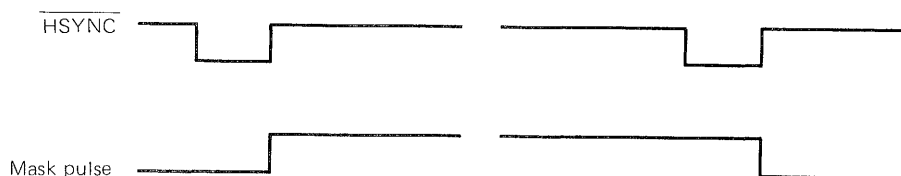
When used in a VCR camera, the on-screen ICs provide two types of information; information to be recorded on VCR tape, such as the date and title, and information to be displayed only inside the electronic view finder, such as the battery, focus, sensitivity, and mode. For proper use of these two types of information, the mask option allows the V_{MON} terminal to be used as the character-by-character signal output terminal.



Example: The mask pulse is to be output to line addresses 1H, 3H, and 5H with vertical address 0H and a character size of 1H/dot.

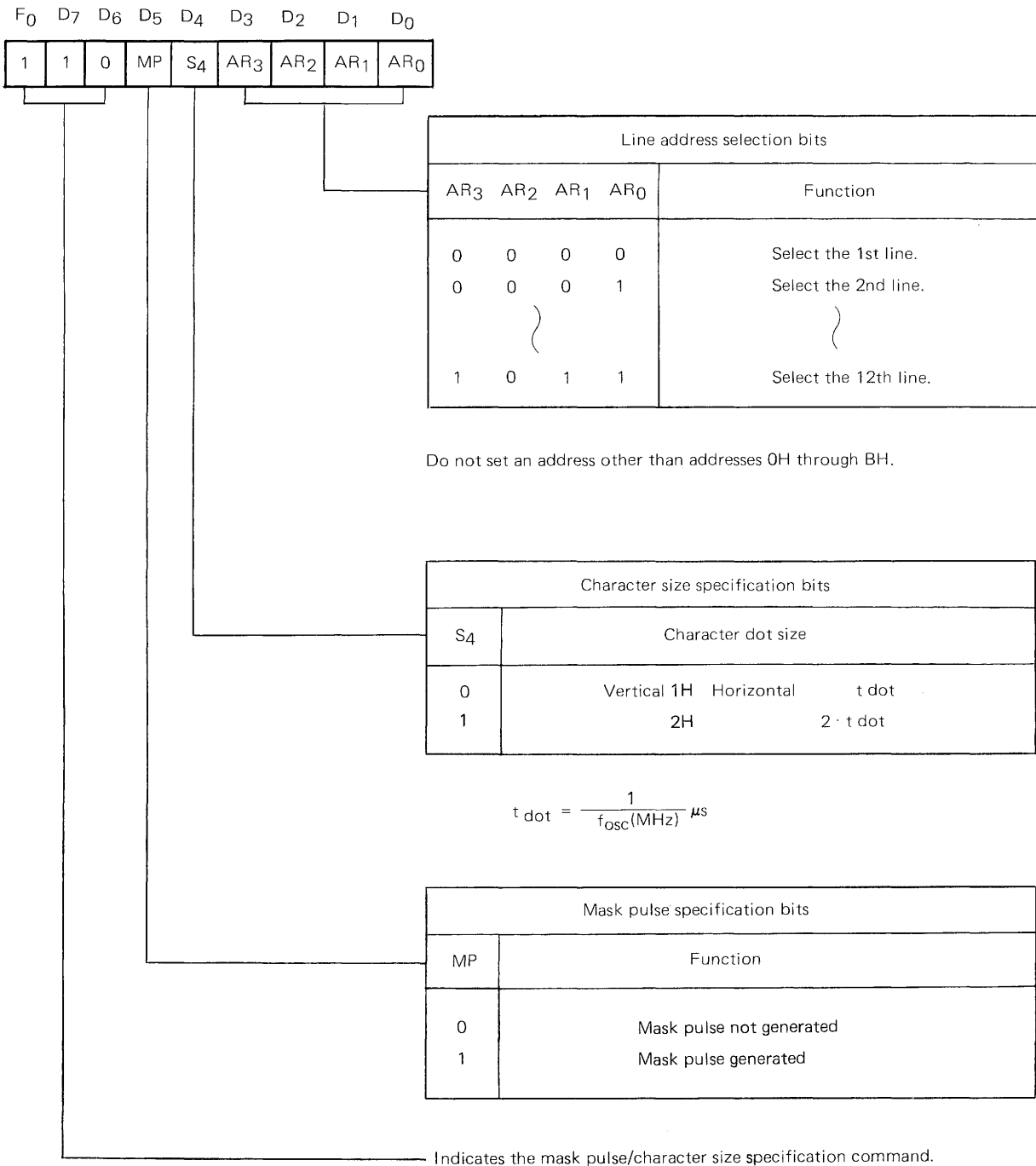


The leading and trailing edges of the mask pulse are synchronized with the trailing edge of HSYNC.



Mask Pulse/Character Size Specification Command

(Available only when the mask pulse function is selected by the mask code option.)



$$t_{dot} = \frac{1}{f_{osc}(\text{MHz})} \mu s$$

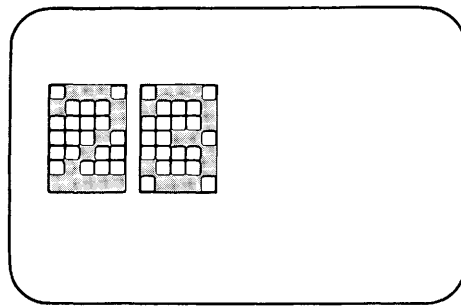
Note: The mask pulse is not used for μPD6451ACX-001, μPD6451AGT-101 and μPD6451AGT-01; therefore, this command cannot be used.

Double-Speed Scan TV Application (Mask Code Option)

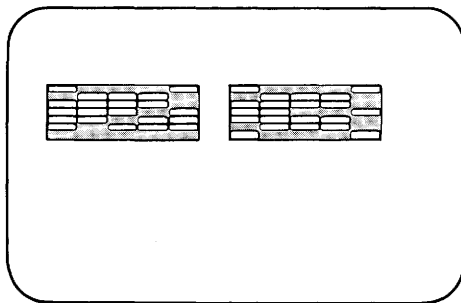
In general, if on-screen ICs are used in a television set with a progressive scanning function, the number of scan lines per field (twice the conventional number) and the time required for horizontal scan (half of the conventional time) are different from those for the conventional NTSC and PAL TV systems.

Character output is doubled in width, halved in height, and halved in time lag with respect to the vertical synchronizing pulse. The character width can be adjusted according to oscillation frequency (but the maximum permissive value of f_{osc} is 7.0 MHz in the case of progressive scan TV it is 10.0 MHz), but neither the character height nor the vertical position can be changed because they are automatically determined by the number of horizontal lines.

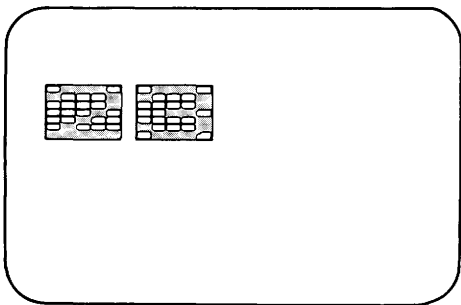
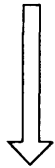
The μ PD6451A is therefore designed so that the character height and vertical position can be changed by inserting a single stage of 1/2-cycle dividers in the vertical address counter section using a mask code option. This, however, involves the following changes to the display-position vertical address assignment command and the character size specification command.



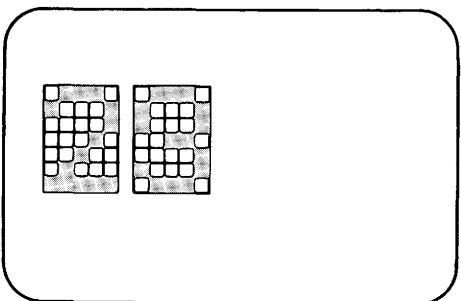
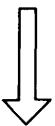
When an on-screen IC is used in a system with one field equivalent to 262.5 H (or 312.5 H).



When an on-screen IC is used directly in a system with one field equivalent to 525 H (or 625 H).



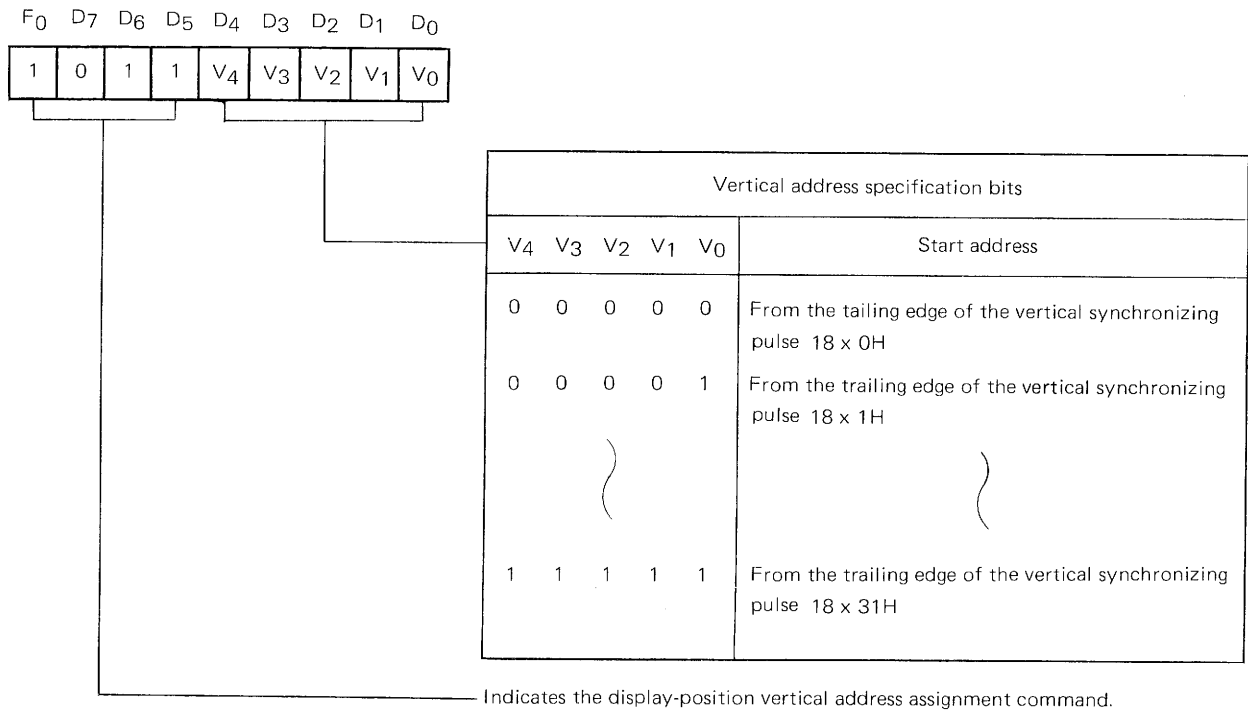
When an on-screen IC with its oscillation frequency doubled is used in a system with one field equivalent to 525 H (or 625 H).



When μ PD6451ACX/AGT is used in a system applying the double-speed scanning TV mode with a mask option.

Display-Position Vertical Address Assignment Command

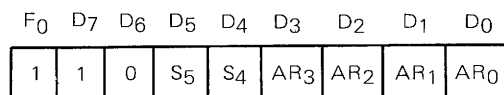
(Available only when the system is set in a progressive scanning TV mode by mounting a mask code option)



Note: Neither the μPD6451ACX-001, μPD6451AGT-101 nor μPD6451AGT-301 are optional in the double-speed scanning TV mode.

Character Size Specification Command

(Available only when the system is set in progressive scanning TV mode)



Line address selection bits				Function
AR ₃	AR ₂	AR ₁	AR ₀	
0	0	0	0	Select the 1st line.
0	0	0	1	Select the 2nd line.
<div> <div></div> <div></div> </div>				<div> <div></div> <div></div> </div>
1	0	1	1	Select the 12th line.

Do not set an address other than addresses 0H through BH.

Character size specification bits		Character dot size
S ₅	S ₄	
0	0	Vertical 2H Horizontal, t dot
0	1	4H 2 · t dot
1	0	6H 3 · t dot
1	1	8H 4 · t dot

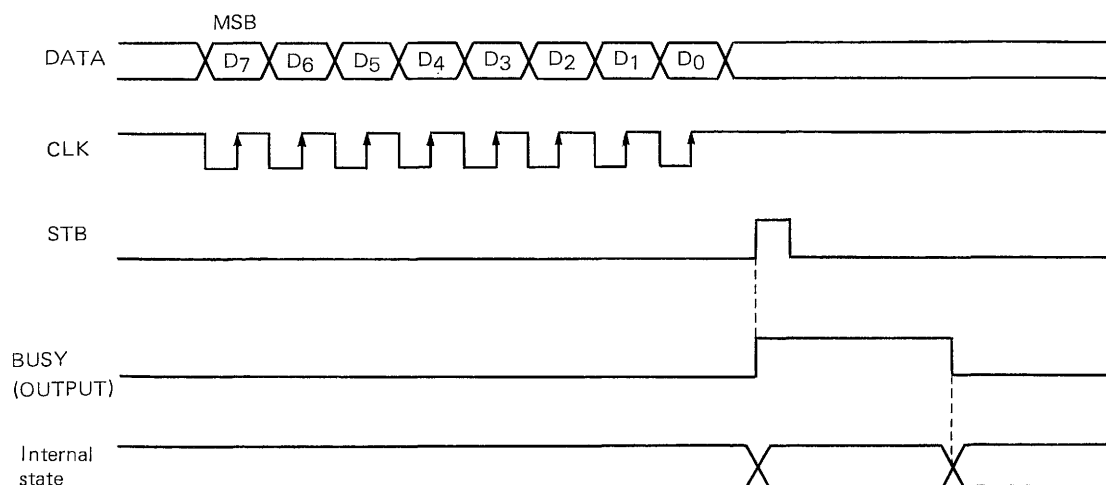
$$t_{\text{dot}} = \frac{1}{f_{\text{osc}}(\text{MHz})} = \mu\text{s}$$

Indicates the character size specification command.

RECOMMENDED CONDITIONS FOR OPERATION TIMING

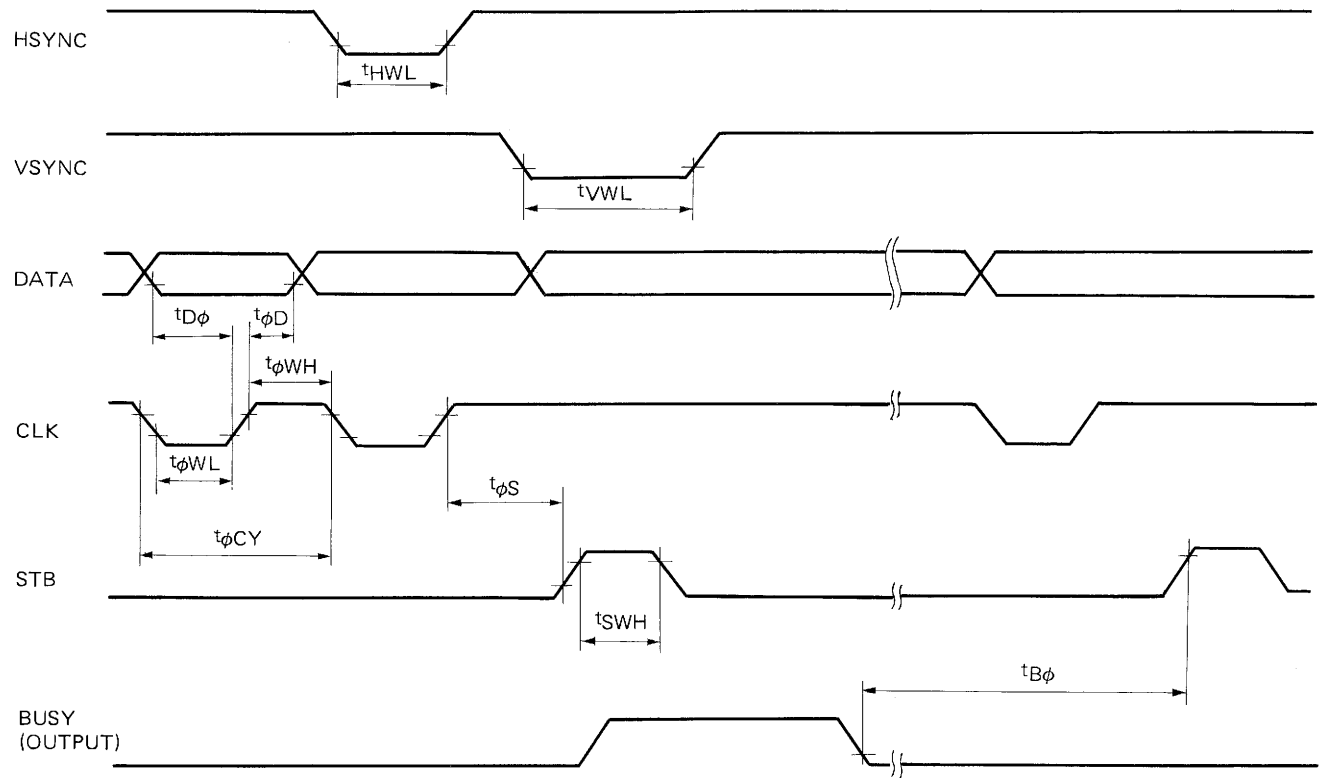
(T_a = 25 °C, V_{DD} – V_{SS} = 5.0 V)

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Minimum setup time	t _{Dφ}		200			ns
Minimum hold time	t _{φD}		200			ns
Minimum clock width at low level	t _{φWL}		700			ns
Minimum clock width at high level	t _{φWH}		700			ns
Minimum clock-to-strobe time	t _{φS}		400			ns
Minimum strobe width at high level	t _{SWH}		1			μs
Clock cycle	t _{φCY}		1.6			μs
Minimum Busy-to-strobe time	t _{Bφ}	During display OFF	100			ns
Minimum $\overline{\text{VSYNC}}$ width at low level	t _{VWL}		4			μs
Minimum $\overline{\text{HSYNC}}$ width at high level	t _{HWL}		4			μs

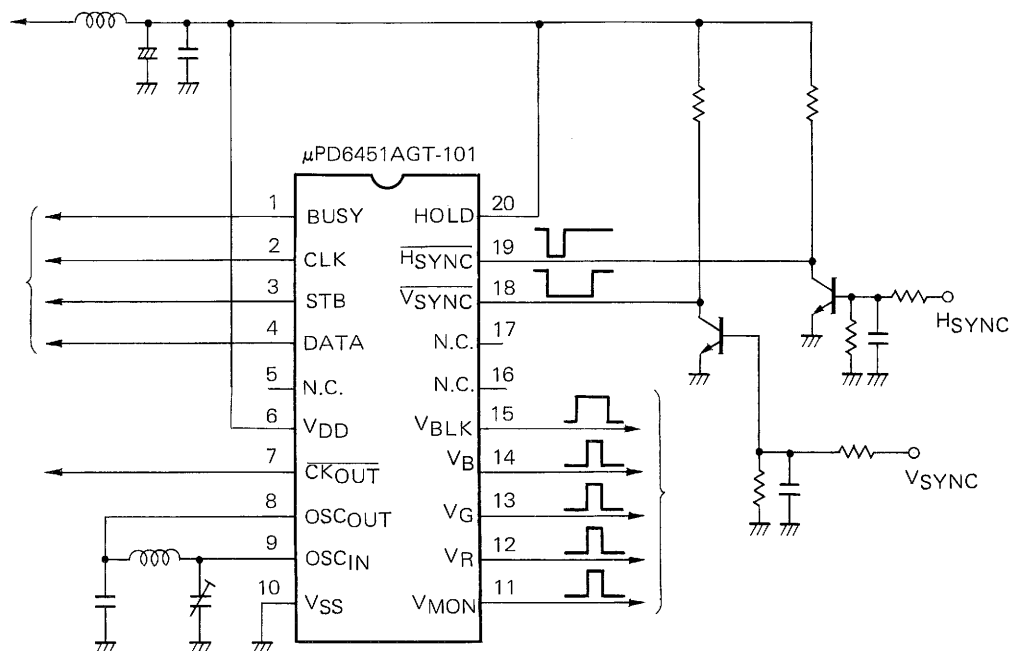
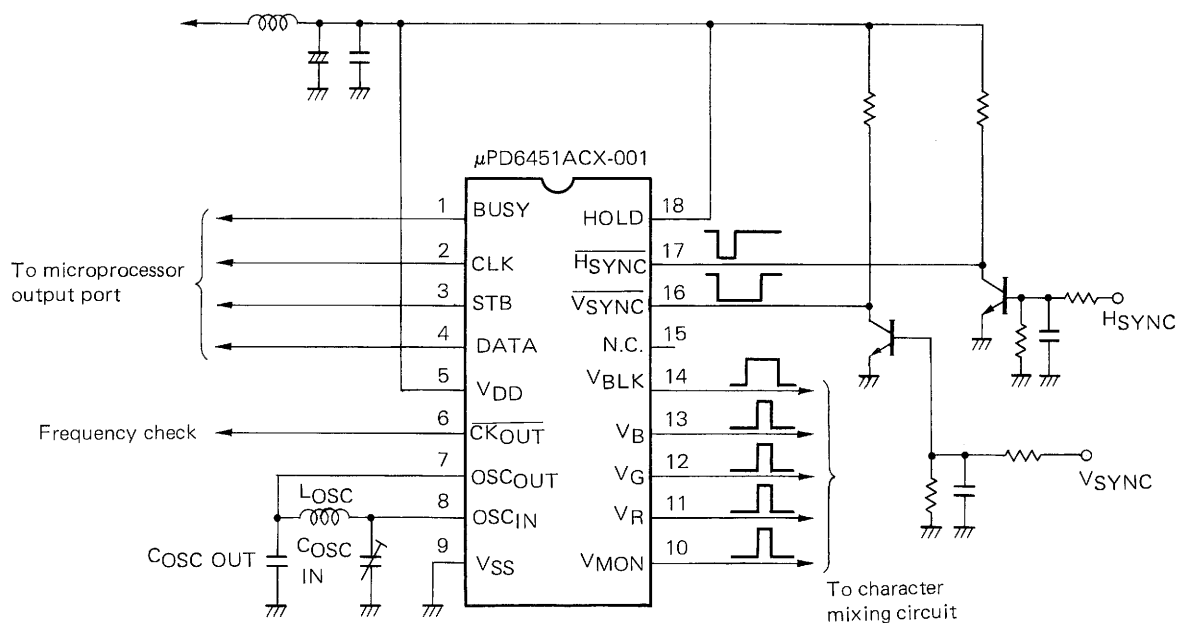


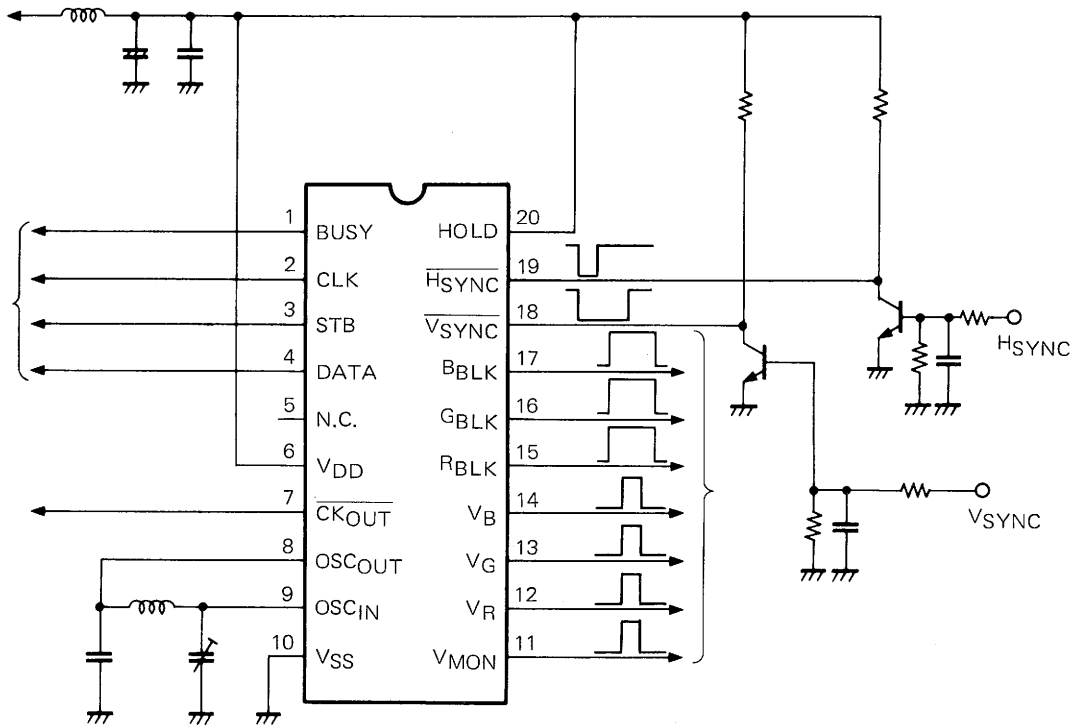
For format data, the BUSY signal goes low after the internal state is completely established. It also goes low when writing data into the VRAM is finished.

When writing data into the VRAM extends to the horizontal flyback time, the BUSY signal lasts longer than usual. (This is because oscillation is off and data cannot be written into the VRAM during the horizontal flyback time.)



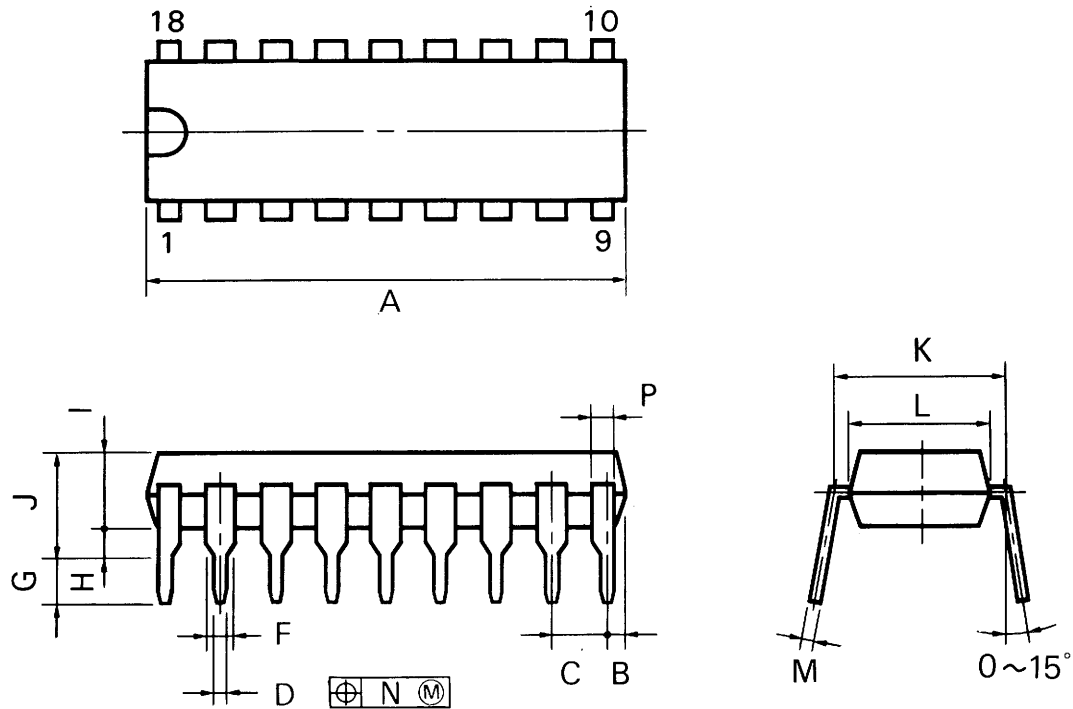
APPLICATION CIRCUIT CONFIGURATION





μ PD6451ACX-001

18-pin plastic DIP (300 mil)



P18C-100-300B

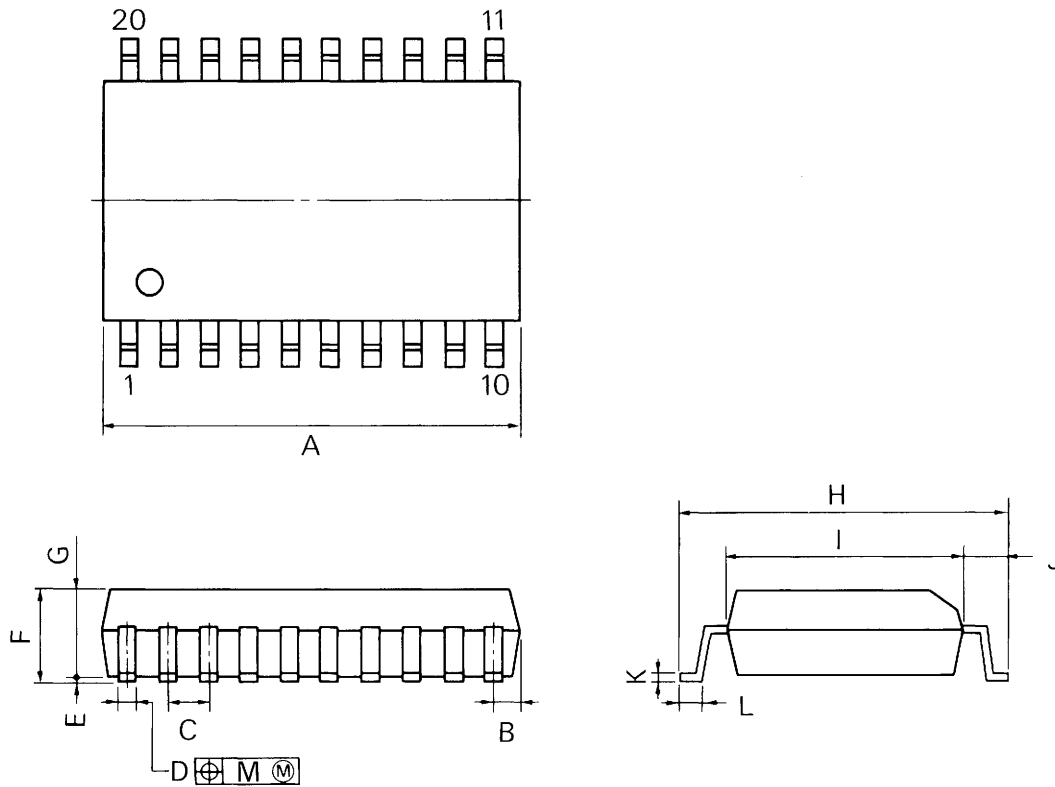
NOTES

- 1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	22.86 MAX.	0.900 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	0.50 ± 0.10	0.020 $\begin{smallmatrix} +0.004 \\ -0.005 \end{smallmatrix}$
F	1.2 MIN.	0.047 MIN.
G	3.2 ± 0.3	0.126 ± 0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.4	0.252
M	0.25 $\begin{smallmatrix} +0.10 \\ -0.05 \end{smallmatrix}$	0.010 $\begin{smallmatrix} +0.004 \\ -0.003 \end{smallmatrix}$
N	0.25	0.01
P	1.0 MIN.	0.039 MIN.

μPD6451AGT-101, μPD6451AGT-301

20-pin plastic SOP (375 mil)



P20GM-50-375B-1

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	13.00 MAX.	0.512 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40 ^{+0.10} _{-0.05}	0.016 ^{+0.004} _{-0.003}
E	0.1 ^{+0.2} _{-0.1}	0.004 ^{+0.008} _{-0.004}
F	2.9 MAX.	0.115 MAX.
G	2.50	0.098
H	10.3 ^{±0.3}	0.406 ^{+0.012} _{-0.013}
I	7.2	0.283
J	1.6	0.063
K	0.15 ^{+0.10} _{-0.05}	0.006 ^{+0.004} _{-0.002}
L	0.8 ^{±0.2}	0.031 ^{+0.009} _{-0.008}
M	0.12	0.005

[MEMO]

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Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

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