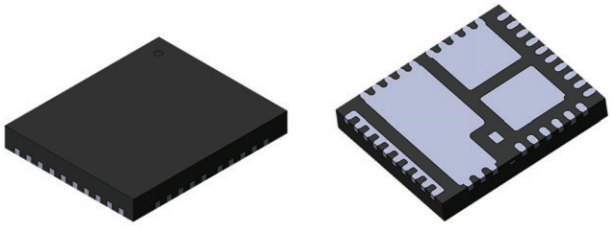
SiC810, 80 A VRPower®, Smart Power Stage With Current Sensing and Temperature Monitor



DESCRIPTION

The SiC810 is an integrated power stage solution optimized for synchronous buck applications to offer high current, high efficiency, and high power density performance. Packaged in Vishay's proprietary 5 mm x 6 mm MLP package, SiC810 enables voltage regulator design to deliver in excess of 80 A per phase current.

The internal power MOSFETs utilize Vishay's state-of-the-art TrenchFET® Gen IV technology that delivers industry bench mark performance to significantly reduce switching and conduction losses.

The SiC810 incorporates an advanced MOSFET gate driver IC that features high current driving capability, adaptive dead-time control, and integrated bootstrap switch, a thermal monitor that alerts the system of excessive junction temperature. This driver is also compatible with wide range of PWM controllers with the support of both 3.3 V and 5 V PWM logic with tri-state. Diode emulation mode can be enabled at light loads through the use of GLCTRL signal. The device also integrates a current monitor to provide a real time scale down of inductor current (I_{MON}). A temperature monitor provides the system an indication of the power stage internal temperature (T_{MON}) and can be used to throttle the system operation down to a safer level if needed. The device also integrates fault alerts such as HS FET overcurrent, over temperature and HS MOSFET short failures.

FEATURES

- Thermally enhanced PowerPAK® MLP39-65 package
- Optimize MOSFET switching performance with integrated Schottky diode in LS MOSFET
- Up to 80 A continuous current
- High frequency operation up to 2 MHz
- Power MOSFETs optimized for 12 V input stage and 10 % to 15 % duty cycle operation
- 3.3 V / 5 V PWM logic with tri-state and hold-off
- PWM minimum controllable on time of 30 ns
- Diode emulation mode at light loads for high efficiency over the full load range using GLCTRL pin
- Low PWM propagation delay (< 20 ns)
- Current sense monitor (I_{MON})
- Temperature monitor (T_{MON})
- Over temperature alert
- HS MOSFET over-current and short alert
- Under voltage lockout for V_{DRV}
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- Synchronous buck converters
- Multi-phase VRDs for CPU, GPU, and memory
- DC/DC VR modules

EFFICIENCY

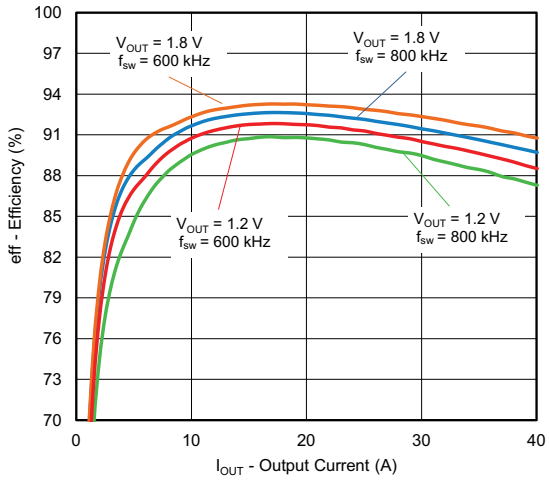


Fig. 1 - Efficiency vs. Output Current
(V_{IN} = 12 V, L = 150 nH, V_{CC} = V_{DRV} = 5 V)

TYPICAL APPLICATION CIRCUIT

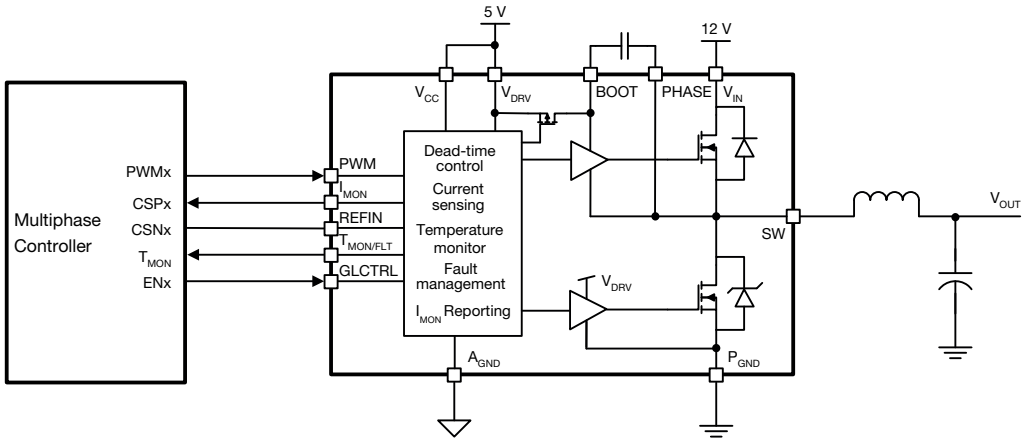


Fig. 2 - Application Diagram

PIN CONFIGURATION

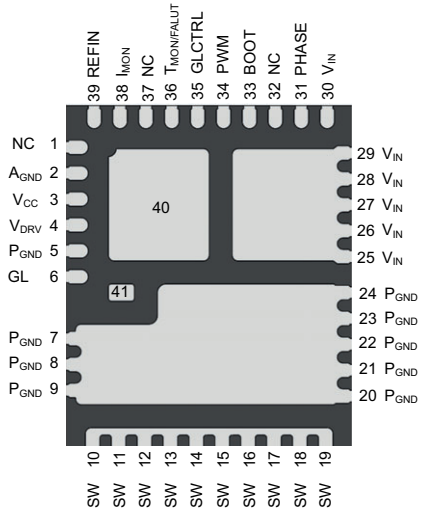


Fig. 3 - Pin Configuration - Top Transparent View

PIN DESCRIPTION		
PIN NUMBER	**SYMBOL**	**DESCRIPTION**
1, 32, 37	NC	This pin can be left floating or connected to A_{GND}
2	A_{GND}	Ground for internal circuitry (not a ground for the drivers)
3	V_{CC}	Supply voltage for internal circuitry (does not power the drivers)
4	V_{DRV}	Supply voltage for internal gate drive
5, 7 to 9, 20 to 24, 40	P_{GND}	Power ground (note: pin 5 is intended to be used as a Kelvin pickup of the P_{GND} for I_{MON} sensing)
6, 41	GATEL (GL)	Low side MOSFET gate signal for observation purposes - do not connect externally
10 to 19	SW	Switch node of the power stage. Connect directly to output inductor
25 to 30	V_{IN}	Power stage input voltage. Drain of high side MOSFET
31	PHASE	Return path of HS gate driver and the boot capacitor. Connected internally to the SW node. Do not connect this pin to the switch node externally
33	BOOT	High side driver bootstrap voltage. Connect a 0.1 µF to 1 µF capacitor between BOOT and PHASE pins
34	PWM	PWM input logic. tri-state PWM input signal means both HS and LS MOSFETs are turned off
35	GLCTRL	Enables the low side switching FET. Logic low turns off LS FET
36	$T_{MON/FAULT}$	Temperature monitor with a conversion factor of 8 mV/°C with 0.8 V offset / catastrophic fault pin
38	I_{MON}	Output voltage representative of the inductor current with a ratio of 5 mV/A
39	REFIN	Internal reference voltage for I_{OUT}, but can be overdriven externally if desired

ORDERING INFORMATION			
PART NUMBER	**PWM**	**PACKAGE**	**MARKING CODE**
SiC810ED-T1-GE3	5 V	PowerPAK MLP39-65	810
SiC810AED-T1-GE3	3.3 V	PowerPAK MLP39-65	810A
SiC810DB	5 V	Reference board	
SiC810ADB	3.3 V	Reference board	

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)			
ELECTRICAL PARAMETER	**SYMBOL**	**LIMITS**	**UNIT**
Input voltage	V_{IN}	-0.3 to +25	V
Control input voltage	V_{CC}	-0.3 to +6.5	
Drive input voltage	V_{DRV}	-0.3 to +6.5	
Switch node (DC)	V_{SW}	-0.3 to +25	
Switch node (AC) (1)		-8 to +30	
BOOT voltage (V_{BOOT_GND})	V_{BS}	-0.3 to +32	
BOOT to switching node (DC voltage)	V_{BS_SW}	-0.3 to +6.5	
All logic inputs and outputs (PWM, EN, ZCD, I_{OUT_REF} and $T_{OUT/FAULT}$)		-0.3 to V_{CC} + 0.3	
Max. operating junction temperature	T_J	150	°C
Ambient temperature	T_A	-40 to +125	
Storage temperature	T_{stg}	-65 to +150	
ESD / HBM		2000	V
ESD / CDM		500	

Note

(1) The specification values indicated “AC” is V_{SW} to P_{GND} -8 V (< 20 ns, 10 µJ), min. and 30 V (< 50 ns), max.

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating/conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS				
ELECTRICAL PARAMETER	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Input voltage (V_{IN})	4.5	12	16	V
Drive input voltage (V_{DRV})	4.5	5	5.5	
Control input voltage (V_{CC})	4.5	5	5.5	
Switching node (LX, DC voltage)	-	-	25	
BOOT-SW	4.5	5	5.5	
Switching frequency	300	-	1200	kHz
Thermal Resistance				
Thermal resistance from junction to case (to P3 PAD “VSWH”)	-	2.5	-	°C/W
Thermal resistance from junction to PCB	-	5	-	

ELECTRICAL SPECIFICATIONS (EN = 5 V, V_{IN} = 12 V, V_{DRV} and V_{CC} = 5 V, T_A = 25 °C)
min./max. values are V_{IN} = 12 V, V_{CC} = V_{DRV} = 5 V ± 10 % and T_J = T_A = -40 to 125 °C unless otherwise specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power Supplies						
Quiescent current	I_Q	I_Q = I_{VCC} + I_{VDRV}, GATEL = high, non-switching	-	5.5	10	mA
Driver current	I_{VDRV_300kHz}	f_{sw} = 300 kHz, D = 0.2	-	16	25	
	I_{VDRV_1MHz}	f_{sw} = 1 MHz, D = 0.2	-	60	-	
Bootstrap Supply						
Bootstrap switch forward voltage	V_F	V_{CC} = 5 V, forward bias current 2 mA from BOOST to GND GL = high (PWM = low)	-	-	0.4	V
Bootstrap switch breakdown voltage	$BOOT_{BV}$		30	-	-	
Bootstrap level-shifter forced refresh voltage	$V_{BOOT\_REFRESH}$	Minimum V_{BOOT} voltage with respect to V_{DRV} before recharge initiated. PWM is tri-state	-	2.7	-	
Bootstrap level-shifter minimum drive voltage (rising)	V_{BM}	Minimum boot voltage before recharge initiated	2.95	3.05	3.15	
Bootstrap refresh comparator hysteresis	V_{BM_HYS}	Hysteresis of boot refresh comparator	-	250	-	mV
PWM Control Input						
PWM low level voltage	$V_{PWM\_L\_3p3}$	With manufacturing option of 3.3 V logic interface	-	-	0.8	V
PWM high level voltage	$V_{PWM\_H\_3p3}$		2.2	-	-	
Tri-state voltage window low level	$V_{TRI\_L\_3p3}$		1.2	-	-	
Tri-state voltage window high level	$V_{TRI\_H\_3p3}$		-	-	1.8	
Tri-state open voltage	$V_{TRI\_HIZ\_3p3}$	Floating PWM input, with manufacturing option of 3.3 V logic interface	1.3	1.5	1.7	
Sink impedance (3.3 V option)	PWM_{SNK_3p3}	With manufacturing option of 3.3 V logic interface	-	50	-	kΩ
Source impedance (3.3 V option)	PWM_{SRC_3p3}		-	20	-	
PWM low level voltage	$V_{PWM\_L\_5p0}$	With manufacturing option of 5 V logic interface	-	-	0.8	V
PWM high level voltage	$V_{PWM\_H\_5p0}$		3.8	-	-	
Tri-state voltage window low level	$V_{TRI\_L\_5p0}$		1.2	-	-	
Tri-state voltage window high level	$V_{TRI\_H\_5p0}$		-	-	3.1	
Tri-state open voltage	$V_{TRI\_HIZ\_5p0}$	Floating PWM input, with manufacturing option of 5 V logic interface	2.1	2.5	2.9	
Sink impedance (5 V option)	PWM_{SNK_5p0}	With manufacturing option of 5 V logic interface	-	21	-	kΩ
Source impedance (5 V option)	PWM_{SRC_5p0}		-	21	-	

ELECTRICAL SPECIFICATIONS (EN = 5 V, V_{IN} = 12 V, V_{DRV} and V_{CC} = 5 V, T_A = 25 °C)
min./max. values are V_{IN} = 12 V, V_{CC} = V_{DRV} = 5 V ± 10 % and T_J = T_A = -40 to 125 °C unless otherwise specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
PWM INPUT TIMING SPECIFICATIONS						
PWM minimum controllable on-time	$T_{PWM\_ON\_MIN.}$	Defined as measured 90 % to 90 % voltage level on SW node. Tested at 25 °C and V_{CC} = 5 V	26	32	38	ns
		Defined as measured 90 % to 90 % voltage level on SW node. Over full temperature range and supply	40	-	-	
Tri-state to GH rising propagation delay	$T_{PD\_R\_Tri}$	No load, see Fig. 4. Result is time measured from PWM voltage leaving tri-state (P_{WMTH_R}) to LX rising by 1 V (above tri-state LX voltage)	-	-	36	
Tri-state to GL rising propagation delay	$T_{PD\_L\_Tri}$	No load, see Fig. 4. Result is time measured from PWM voltage leaving tri-state (P_{WMTH_F}) to GL rising to 1 V	-	-	30	
Tri-state hold-off time (from PWM low)	T_{TSHO_R}	Tri-state is entered if the PWM input signal enters this mode for at least this amount of time. Time measured from voltage of PWM rising past $P_{WM\_Tri\_R}$ to GL falling to 90 %	-	40	60	
Tri-state hold-off time (from PWM high)	T_{TSHO_F}	Tri-state is entered if the PWM input signal enters this mode for at least this amount of time. Time measured from voltage of PWM falling past $P_{WM\_Tri\_F}$ to LX falling to 90 %	-	40	60	
GH - turn off propagation delay	$T_{PD\_OFF\_GH}$	Condition: inductor PEAK current = 3 A. Result is time measured from PWM falling below 0.8 V to LX falling to 90 % of V_{IN}. PWM input pulse is longer than 30 ns	24	34	44	
GH - turn on propagation delay (dead time rising)	$T_{PD\_ON\_GH}$	Condition: inductor VALLEY current = 1 A, result is time from GL falling below 1 V to LX rising above -0.05 V	-	10	-	
GL - turn off propagation delay	$T_{PD\_OFF\_GL}$	Time from PWM transitioning above 2.2 V to GL falling below 1 V	-	28	38	
GL - turn on propagation delay (dead time falling)	$T_{PD\_ON\_GL}$	Condition: inductor PEAK current = 3 A. Result is the time measured from LX falling below 90 % V_{IN} to GL rising above 1 V	-	18	-	
$T_{MON/\ FAULT}$						
Gain	$TMON_{GAIN}$		-	8	-	mV/°C
Offset voltage at 25 °C	$TMON_{25°C}$		0.784	0.8	0.816	V
T_{MON} range 150 °C (temp. reporting)	$TMON_{150°C}$		1.764	-	1.836	
FAULT mode	$FAULT_{HIGH}$		2.4	-	3.6	
FAULT drive current	$FAULT_{DRV}$		5	-	-	mA
Protection						
Under voltage lockout	V_{UVLO}	V_{CC} rising	3.7	3.8	4.1	V
Under voltage lockout hysteresis	V_{UVLO_HYS}		-	380	-	mV
UVLO delay	T_{UVLO_DLY}	V_{CC} UVLO rising to internal PWM enable. Test condition: input supply abruptly turned on from 0 V to 4.5 V	-	-	20	us
Positive over current alert	I_{POS_OC}	Triggered when over current condition lasts for >10x consecutive cycles	-	120	-	A
Negative over current alert	I_{NEG_OC}		-	-120	-	

ELECTRICAL SPECIFICATIONS (EN = 5 V, V_{IN} = 12 V, V_{DRV} and V_{CC} = 5 V, T_A = 25 °C)
min./max. values are V_{IN} = 12 V, V_{CC} = V_{DRV} = 5 V ± 10 % and T_J = T_A = -40 to 125 °C unless otherwise specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{MON}						
I_{MON_REF} common mode	$IMON_{REF\_CM}$	Allowable user provided reference	1.15	1.5	2	V
Current sense output	$IMON_{GAIN}$		-	5	-	mV/A
Current sense inaccuracy	$I_{ACCURACY}$	15 A to 50 A inductor current measured over a 200 µs moving average window of time Note: this accuracy applies for temperatures -10 °C < T_J < 85 °C	-	± 2	± 3	%
		5 A to 15 A inductor current measured over a 200 µs moving average window of time Note: this accuracy applies for temperatures -10 °C < T_J < 85 °C	-	± 3	± 4	
		2 A to 5 A inductor current measured over a 200 µs moving average window of time Note: this accuracy applies for temperatures -10 °C < T_J < 85 °C	-	± 8	± 10	
I_{MON} dynamic range	$IMON_{RANGE}$		-50	-	100	A
I_{MON} output buffer latency	$IMON_{LATENCY}$	$C_{IMON\text{-}IMON\_REF}$ < 100 pF Not tested. Guaranteed by design	-	-	50	ns
I_{MON} output buffer bandwidth	$IMON_{BW}$	$C_{IMON\text{-}IMON\_REF}$ < 100 pF Not tested. Guaranteed by design	10	-	-	MHz
I_{MON} calibration time	I_{MONCAL}	PWM cycles required after GLCTRL and UVLO transition to active. I_{MON} is not reported during this time. I_{MON} = I_{MON_REF} during this time	-	-	1024	cycles
GLCTRL INPUT						
GLCTRL logic input high threshold	V_{DSBL_HIGH}		2	-	-	V
GLCTRL logic input low threshold	V_{DSBL_LOW}		-	-	0.8	
GLCTRL pull down resistance	R_{PLD_GATEL}		-	240	-	kΩ
GLCTRL high to GL rising propagation delay	$T_{PD\_R\_GATEL}$	Note: the GLCTRL pin enables / disables the low side FET. It does not disable the rest of the IC when low	-	10	-	ns
GLCTRL low to GL falling propagation delay	$T_{PD\_F\_GATEL}$		-	12	-	

DETAILED OPERATIONAL DESCRIPTION

PWM Input with Tri-state Function

The PWM input receives the PWM control signal from the VR controller IC. The PWM input is designed to be compatible with standard controllers using two state logic (H and L) and advanced controllers that incorporate tri-state logic (H, L, and tri-state) on the PWM output. For two state logic, the PWM input operates as follows. When PWM is high, the low side is turned OFF and the high side is turned ON. When PWM input is driven low, the high side turns off and the low side turns on. For tri-state logic, the PWM input operates as above for driving the MOSFETs. However, there is a third state that is entered into as the PWM output of the tri-state compatible controller enters its high impedance state during shut-down. The high impedance state of the controller's PWM output allows the SiC810 to pull the PWM input into the tri-state region (see the tri-state voltage threshold diagram below). If the PWM input stays in this region for the tri-state hold-off period, t_{TSHO}, both high side and low side MOSFETs are turned off. This function allows the VR phase to be disabled without negative output voltage swing caused by inductor ringing and saves a Schottky diode clamp. The PWM and tri-state regions are separated by hysteresis to prevent false triggering. The SiC810A incorporates PWM voltage thresholds that are compatible with 3.3 V logic while the SiC810 incorporates PWM voltage thresholds that are compatible with 5 V logic.

$T_{MON/FAULT}$

The $T_{MON/\ FAULT}$ signal is a dual function pin:

1. It is a voltage signal proportional to the internal temperature of the power stage device with a conversion factor of 8 mV/°C. In a multi-phase solution, all $T_{MON/FAULT}$ signals are “wired-or” connected to the PWM controller and will indicate the temperature of the highest device
2. It indicates a catastrophic fault condition in the power stage by pulling the signal to logic high (3.3 V logic compatible). The catastrophic fault conditions are:
   a. HS FET over-current for 10 consecutive cycles
   b. OT trip for the device maximum junction temperature
   c. High side MOSFET drain to source short

$T_{MON/FAULT}$ pin provides an 8 mV/°C output providing monitoring of the junction temperature. In the event of a fault, the power stage will pull $T_{MON/FAULT}$ pin high.

GLCTRL

The GLCTRL pin provides a means to keep the LS MOSFET disabled regardless of the PWM signal. When pulled low, the low side MOSFET is kept in the off state.

Voltage Input (V_{IN})

This is the power input to the drain of the high side power MOSFET. This pin is connected to the high power intermediate BUS rail.

Switch Node (SW and PHASE)

The switch node (SW) is the circuit PWM regulated output. This is the output applied to the filter circuit to deliver the regulated high output for the buck converter. The PHASE pin is internally connected to the switch node (SW). This pin (PHASE) is to be used exclusively as the return pin for the BOOT capacitor. A 20.2 kΩ resistor is connected between GH and PHASE to provide a discharge path for the HS MOSFET in the event that V_{DRV} goes to zero while V_{IN} is still applied.

Ground Connections (A_{GND} and P_{GND})

Internal to the SiC810, the A_{GND} is shorted to the P_{GND} through the lead frame. To avoid parasitic ground loops, the A_{GND} for each individual instantiation of the SiC810 on the PCB should be derived from the P_{GND} of the same SiC810. It is not advised to connect all of the A_{GND} connections at the system level together. If decoupling capacitance to A_{GND} is used for each SiC810 I_{MON_REF} pin, it should be tied to the local A_{GND}. Further, if possible, it is recommended to use the provided I_{MON_REF} signal from each SiC810 to accompany the I_{MON} signal to provide a true differential output and avoid ground coupled cross-talk between I_{MON} channels. A_{GND} decoupling capacitance to V_{CC} should be kept as close as possible to the SiC810. Typically, a 1 Ω//1 µF capacitor decoupling capacitor network on V_{CC} to A_{GND} should be used. The 1 Ω resistor feeding V_{CC} is connected to V_{DRV} for its unfiltered voltage. V_{DRV} should have its own 1 µF capacitor to A_{GND}.

Control and Drive Supply Voltage Input (V_{DRV}, V_{CC})

V_{CC} is the bias supply for the gate drive control IC. V_{DRV} is the bias supply for the gate drivers. It is recommended to separate these pins through a 1 Ω resistor with 1 µF//10 nF decoupling capacitance. This creates a low pass filtering effect to avoid coupling of high frequency gate drive noise into the IC’s sensitive analog circuits.

Bootstrap Circuit (BOOT)

The internal bootstrap switch and an external bootstrap capacitor form a charge pump that supplies voltage to the BOOT pin. An integrated bootstrap diode is incorporated so that only an external capacitor is necessary to complete the bootstrap circuit. Connect a boot strap capacitor with one leg tied to BOOT pin and the other tied to PHASE pin.

I_{MON}

A current sense circuit monitors the low side MOSFET and reproduces a real-time representative signal for the entire switching period. The I_{MON} pin is a voltage source output signal that duplicates the real-time waveform of inductor current proportional to the load current by a ratio of 5 mV/A and is differentially referenced to I_{MON_REF} voltage which is provided internally (1.5 V), but can be driven externally.

I_{MON_REF}

Internal 1.5 V (with 1 kΩ impedance) reference provided by SiC810 but can be over-driven externally on PCB or from controller. The I_{MON} signal is referenced to this signal. Capacitance from I_{MON_REF} (and I_{MON}) to A_{GND} and P_{GND} should be minimized if multiple channels have their I_{MON_REF} tied together to avoid crosstalk.

Shoot-Through Protection and Adaptive Dead Time

The SiC810 has an internal adaptive logic to avoid shoot through and optimize dead time. The shoot through protection ensures that both high side and low side MOSFET are not turned on the same time. The adaptive dead time control operates as follows. The HS and LS gate voltages are monitored to prevent the one turning on until the other's gate voltage is sufficiently low (1 V), that and built in delays ensure each power MOS is turned off before the other turns on. This feature helps to adjust dead time as gate transitions change with respect to output current and temperature.

Under Voltage Lockout (UVLO)

During the start up cycle, the UVLO disables the gate drive holding high side and low side MOSFET gate low until the input voltage rail has reached a point at which the logic circuitry can be safely activated. The SiC810 also incorporates logic to clamp the gate drive signals to zero when the UVLO falling edge triggers the shutdown of the device. As an added precaution, a 20.2 kΩ resistor is connected between GH and PHASE to provide a discharge path for the HS MOSFET. Additionally, there is a UVLO that monitors the BOOT voltage. If the BOOT voltage droops low, the low side drive will be momentarily activated to recharge the BOOT capacitor.

FUNCTIONAL BLOCK DIAGRAM

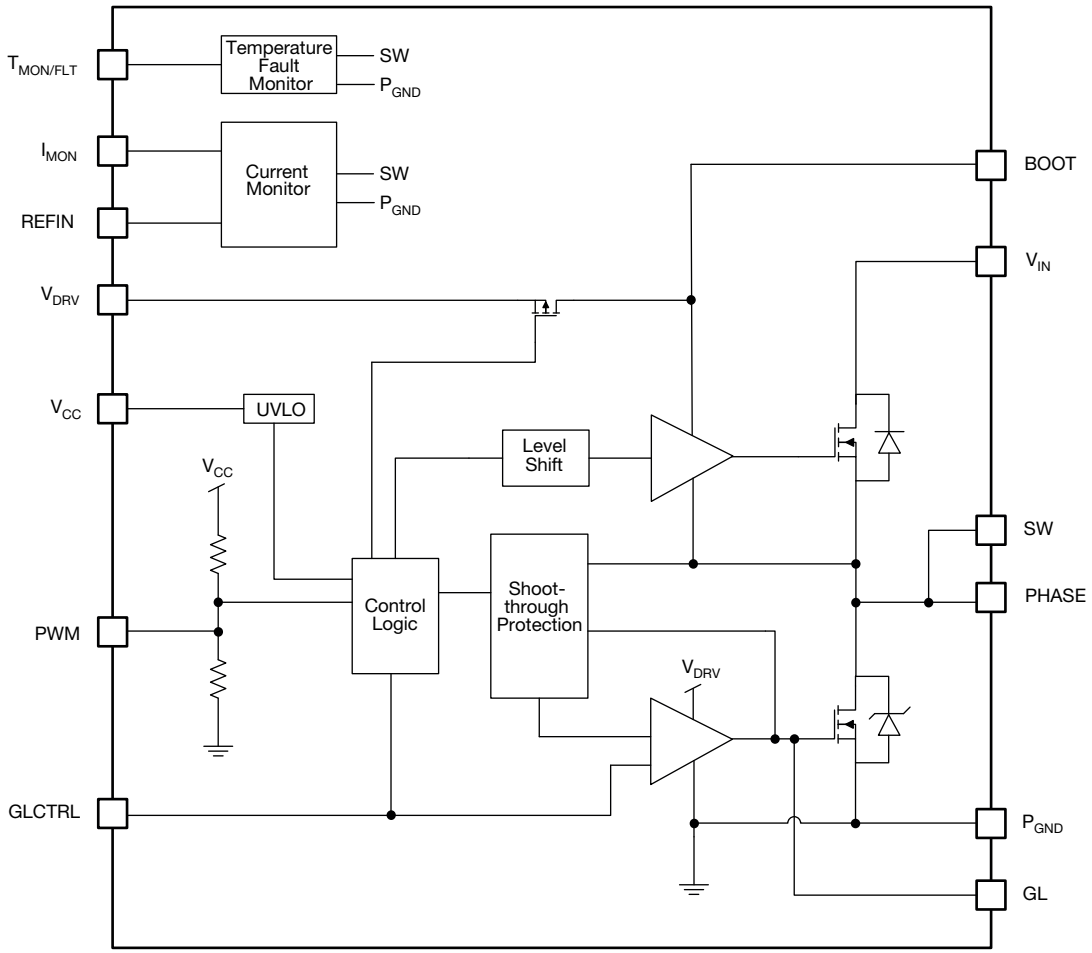


Fig. 4 - Functional Block Diagram

PWM TIMING DIAGRAM

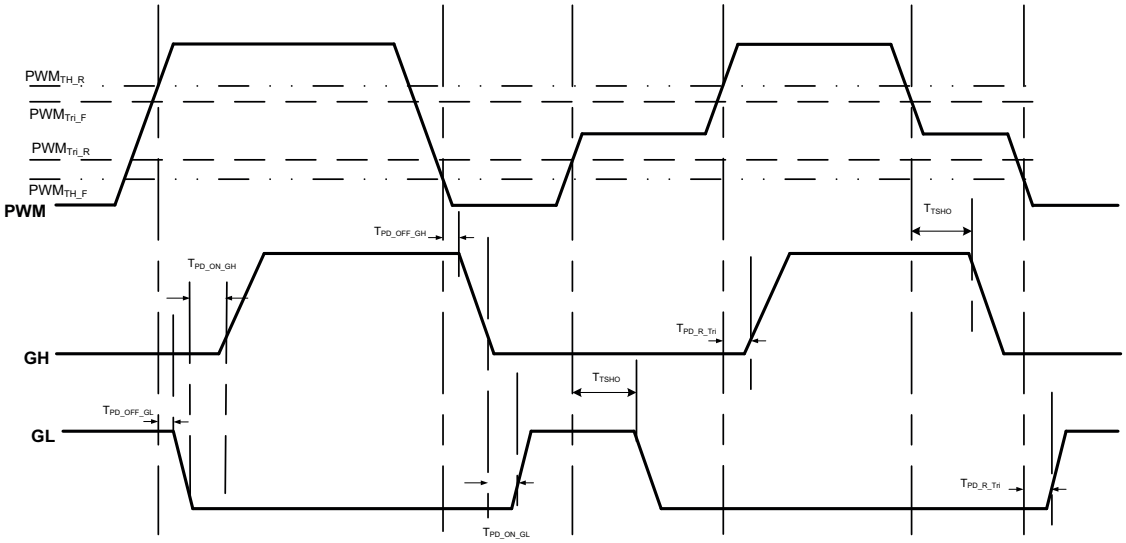


Fig. 5 - Definition of PWM Logic and Tri-state

ELECTRICAL CHARACTERISTICS (V_{IN} = 12 V, V_{DRV} = V_{CC} = 5 V, L_{OUT} = 150 nH. Power loss includes inductor loss, driver and controller loss unless otherwise stated)

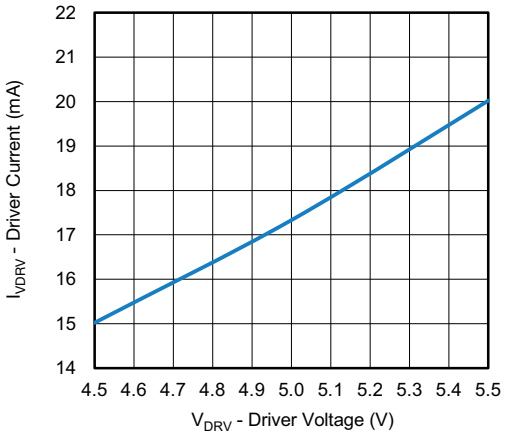


Fig. 6 - Driver Current vs. Driver Voltage

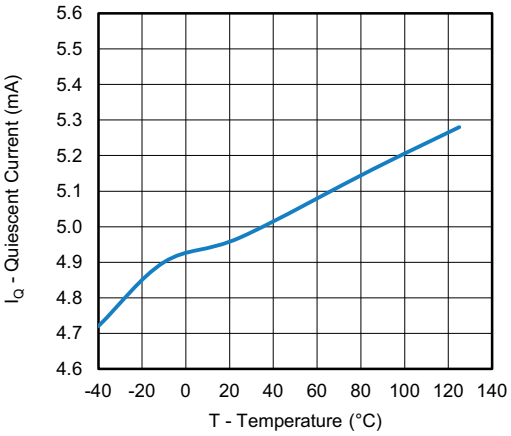


Fig. 9 - Quiescent Current vs. Temperature

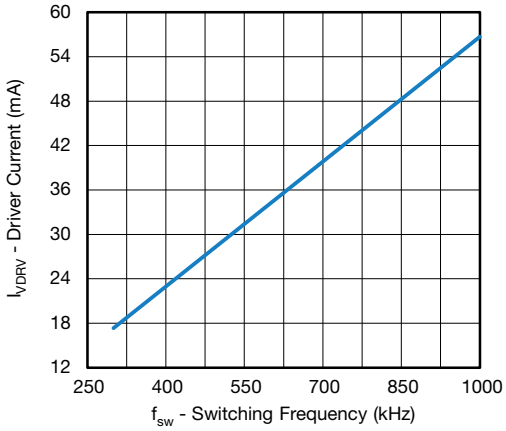


Fig. 7 - Driver Current vs. Switching Frequency

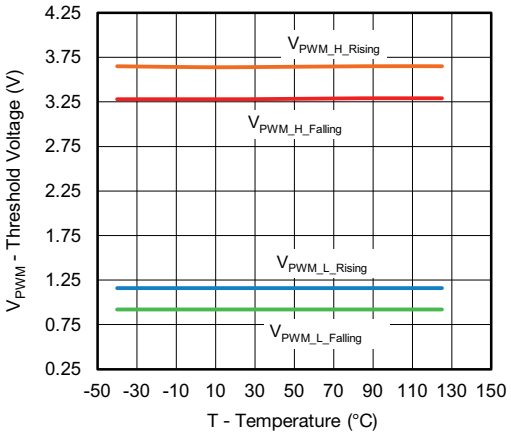


Fig. 10 - Threshold Voltage vs. Temperature

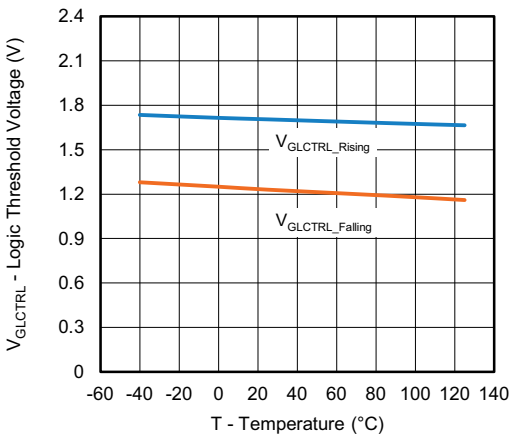


Fig. 8 - Threshold Voltage vs. Temperature

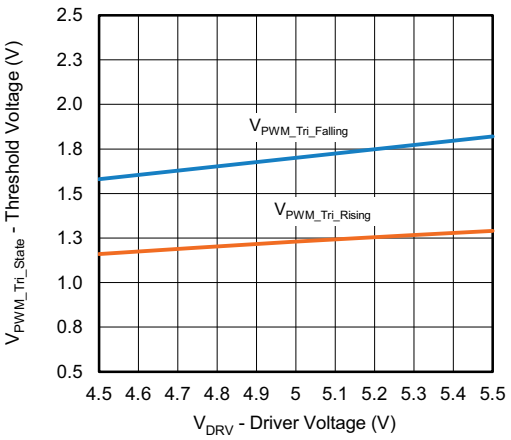


Fig. 11 - Threshold Voltage vs. Driver Voltage

ELECTRICAL CHARACTERISTICS (V_{IN} = 12 V, V_{DRV} = V_{CC} = 5 V, L_{OUT} = 150 nH. Power loss includes inductor loss, driver and controller loss unless otherwise stated)

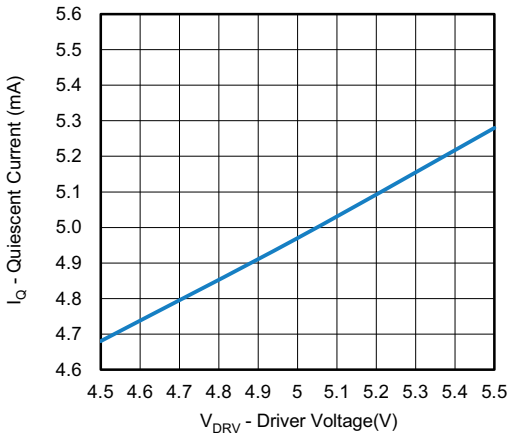


Fig. 12 - Quiescent Current vs. Driver Voltage

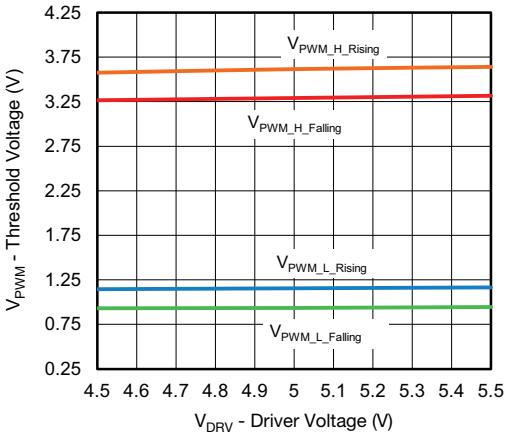


Fig. 13 - Threshold Voltage vs. Driver Voltage

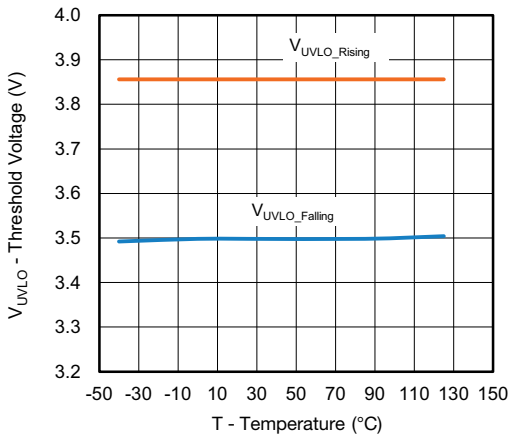


Fig. 14 - Threshold Voltage vs. Temperature

PCB LAYOUT RECOMNDATIONS

Step 1: V_{IN}/GND Planes and Decoupling

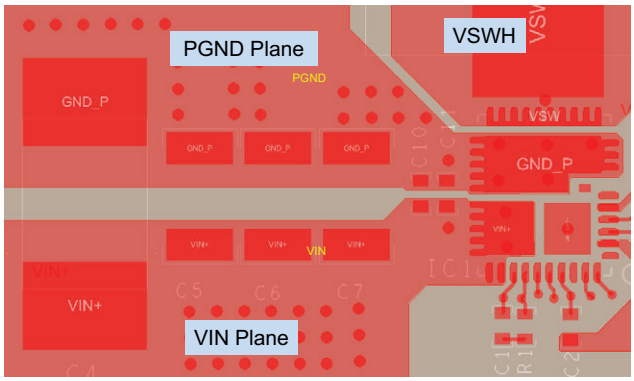


Fig. 15

1. Layout V_{IN} and P_{GND} planes as shown above
2. Ceramic capacitors should be placed right between V_{IN} and P_{GND}, and very close to the device for best decoupling effect to reduce the high current power loop inductance and input current ripple induced by the MOSFET switching operation
3. Difference values / packages of ceramic capacitors should be used to cover entire decoupling spectrum e.g. 1210, 0805, 0603, and 0402
4. Smaller capacitance value, closer to device V_{IN} pin (s) - better high frequency noise absorbing

Step 2: VSWH Plane

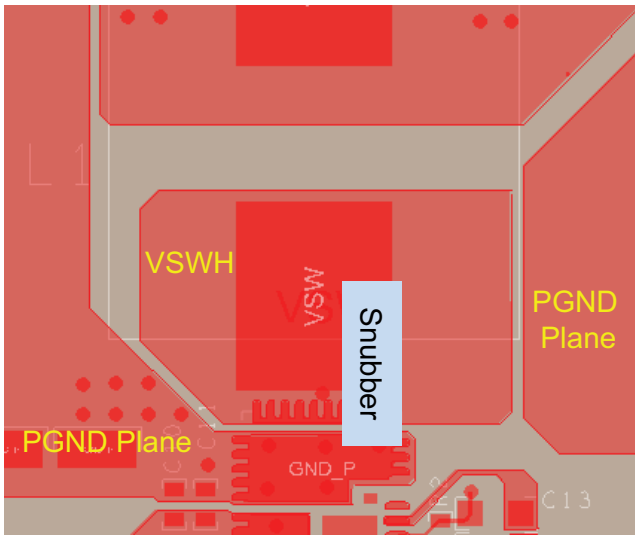


Fig. 16

1. Connect output inductor to DrMOS with large plane to lower the resistance and minimize the conduction loss due to the PCB trace. GND plane can be placed next to VSWH plane to shield the switching noise
2. If any snubber network is required, place the components as shown above and the network can be placed at bottom

Step 3: V_{CIN}/V_{DRV} Input Filter

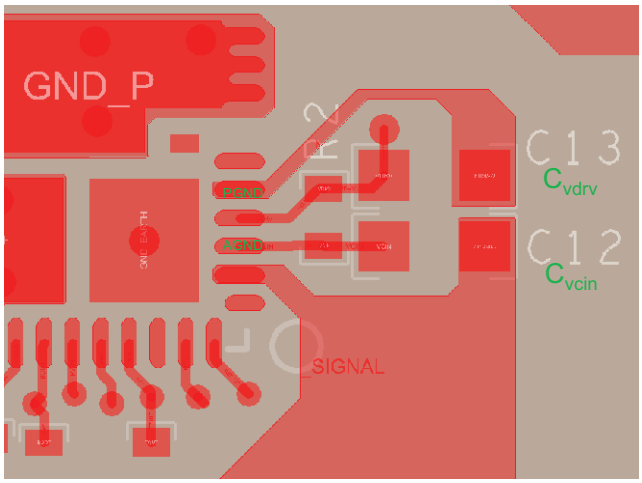


Fig. 17

1. The V_{CIN}/V_{DRV} input filter ceramic cap should be placed very close to DrMOS. It's recommended to connect two caps separately with one resistor in between
2. C_{VCIN} cap should be placed between pin 3 and pin 2 (A_{GND} of driver IC) to achieve best noise filtering
3. C_{VDRV} cap should be placed between pin 5 (P_{GND} of driver IC) and pin 4 to provide maximum instantaneous driver current for low side MOSFET during switching cycle
4. For connecting C_{VCIN} analog ground, it is recommended to use large plane to reduce parasitic inductance

Step 4: BOOT Resistor and Capacitor Placement

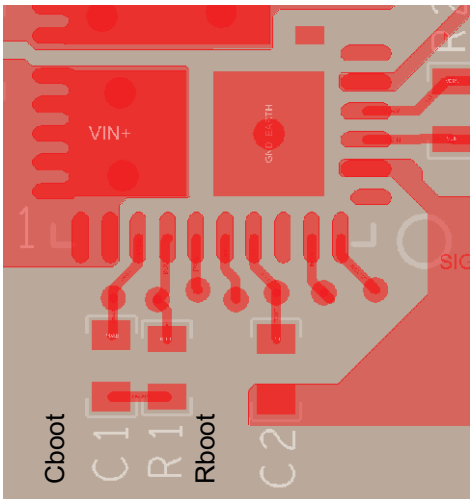


Fig. 18

1. These components need to be placed very close to DrMOS, right between PHASE (pin 32) and BOOT (pin 33)
2. To reduce parasitic inductance, chip size 0402 can be used

Step 5: Signal Routing

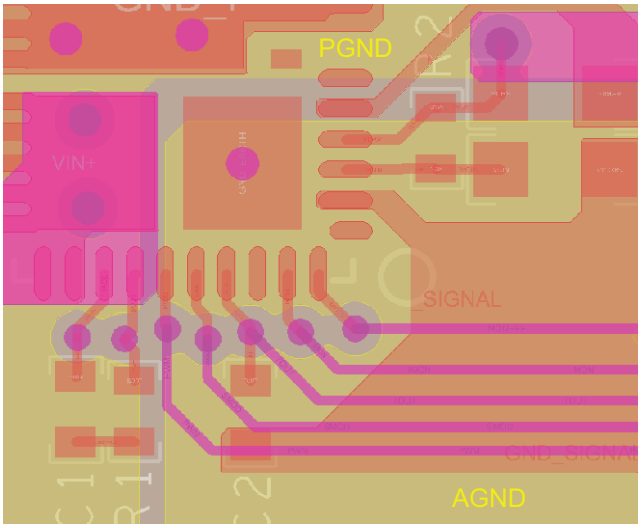


Fig. 19

1. Route the PWM/Tout/Imon/Imonref/GLCTRL signal traces out of the bottom right corner next DrMOS pin 1
2. These signals are sensitive. Both signal and return traces need to pay special attention of not letting this trace cross any power nodes on any layer
3. A small cap can be placed between Tout and A_{GND} to absorb the noise if necessary
4. It is best to “shield” them with GND island form power switching nodes, e.g. VSWH, to improve signal integrity
5. GL (pin 6) has been connected with GL pad (pin 41) internally and does not need to connect externally

Step 6: Adding Thermal Relief Vias

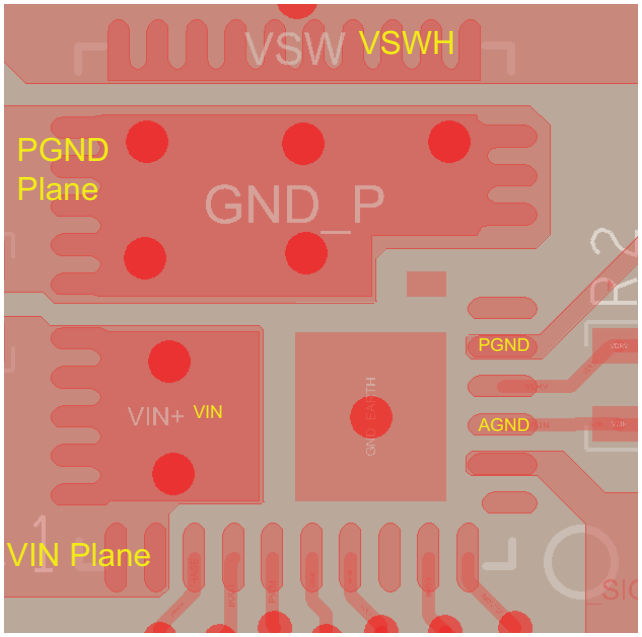


Fig. 20

1. Thermal relief Vias can be added on the V_{IN} and GND pads to utilize inner layers for high current and thermal dissipation
2. To achieve better thermal performance, additional Vias can be put on V_{IN} plane and P_{GND} plane
3. VSWH pad is a noise source and not recommended to put Vias on this plane
4. 8 mil drill for pads and 10 mils drill for plane can be the optional Via size. The Vias on pad may drain solder during assembly and cause assembly issue. Please consult with the assembly house for guideline

Step 7: Ground Connection

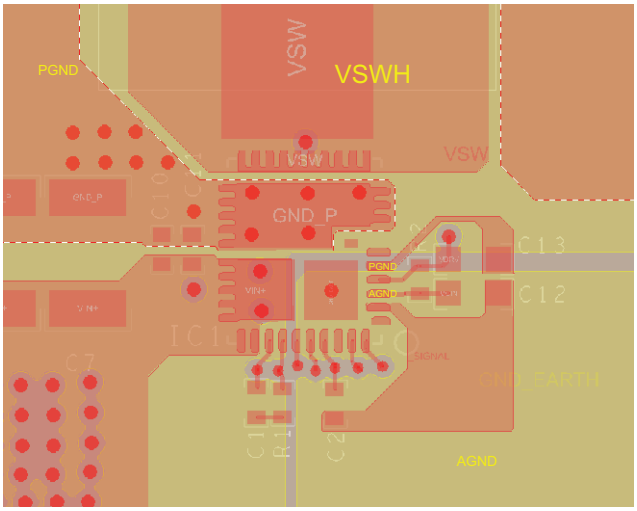


Fig. 21

1. Pin 2 A_{GND}; pin 5 P_{GND}; pin 40 GND PAD and P_{GND} PAD have been connected internally already. Do NOT connect them externally in order to avoid GND loop
2. It is recommended to make the whole inner 1 layer (next to top layer) ground plane and separate them into A_{GND} and P_{GND} plane
3. These ground planes provide shielding between noise source on top layer and signal trace on bottom layer

PRODUCT SUMMARY	
Part number	SiC810
Description	80 A smart power stage with current sensing and temperature monitor
Input voltage min. (V)	4.5
Input voltage max. (V)	16
Current rating (A)	80
Switch frequency max. (kHz)	2000
Enable (yes / no)	No
Monitoring features	I_{MON}, T_{MON}
Protection	LS-UVLO, OTP
Light load mode	None
Peak efficiency (%)	
Pulse-width modulation (V)	5
Package type	MLP39-65
Package size (W, L, H) (mm)	5 x 6 x 0.75
Status code	1
Product type	VRPower (DrMOS)
Applications	Multiphase V_{CORE}

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