Micro Linear

ML6311

3V/5V Read Channel Back-end Processor

GENERAL DESCRIPTION

The ML6311 is a BiCMOS Read Channel Back-end Processor IC which is one half of the disk read channel chipset from Micro Linear, intended for the next generation of smaller form factor (1.8" & 1.3") disk drives, operating on 3V and 5V supplies. It works in conjunction with the ML6310 Read Channel Front-end Processor to form a complete solution for the low voltage/low power disk read/write channel. It incorporates a full function data synchronizer with a 3:1 operating range, a full function frequency synthesizer with onboard M&N dividers, (1,7) RLL encoder/decoder and write precompensation circuitry. The most critical blocks on this chip are the three VCOs, one for the data synchronizer PLL, one for the frequency synthesizer PLL and the third VCO is used to generate the tracking 1/3 cell delay for (1,7) RLL data synchronization. Careful design considerations have been incorporated to minimize the noise coupling and crosstalk among the VCOs. The system noise is highly minimized as the VCO operates at only 1.5X the data rate.

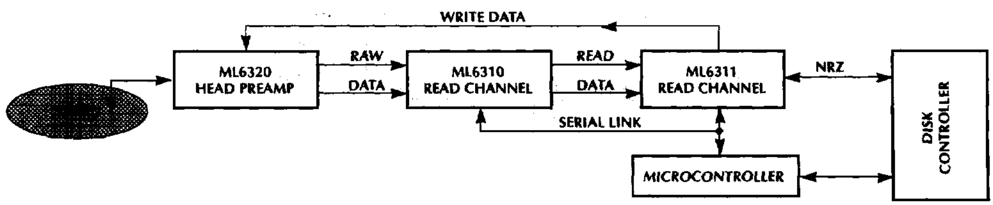
It provides 40-bits for user programmability of a number of features through a serial microprocessor interface and a bank of internal control registers. The center frequency of the VCO, window centering, M & N dividers and power management options are programmable. Independent early and late write precompensation programmability is provided through a 6-bit decoder array. The ML6311 requires two external components besides the two loop filters for the PLL's.

The ML6311 supports six power down modes. An external hardware pin is also provided to implement real time power management. The operating power dissipation is targeted to be less than 170mW, while it will dissipate less than 100µW in the sleep mode.

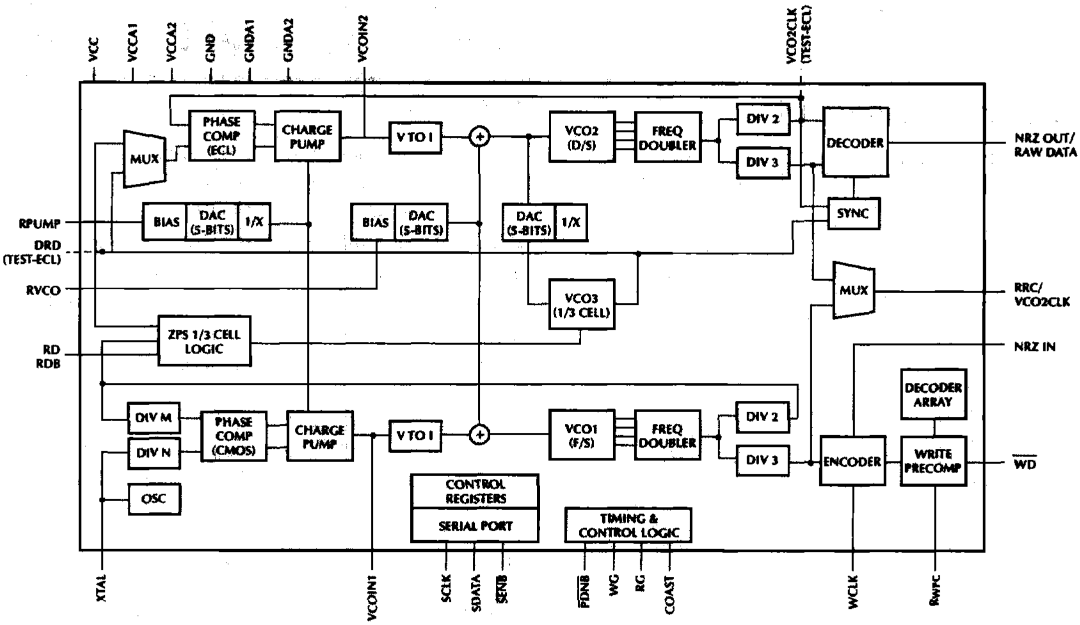
FEATURES

- Operating supply range 2.7V to 3.6V or 4.5V to 5.5V
- Very Low Power dissipation at 3V
  P_{SLEEP} < 100µW, P_{OPR} < 170mW
- Low profile, small area, 32-pin TQFP package
- 3:1 Disk data rate range — 11 to 32 Mbits/s
- Fast acquisition PLL with zero phase start capability
- 3:1 VCO tuning range with 48 Mbits/s 1,7RLL code rate
- Onboard (1, 7) RLL encoder/decoder
- Tracking 1/3 cell delay for internal 1,7 RLL Endec and 1/4 cell delay for external 2, 7 RLL Endec
- Programmable VCO center frequency and window centering adjustment (75% to 125% in steps of 1.6%)
- PLL based frequency synthesizer with reference crystal oscillator and M (7-bit) & N (7-bit) dividers
- Programmable independent early and late write precompensation.
- High speed (20MHz) three wire serial microprocessor interface with double buffered data latches
- Programmable six levels of power management control with external power down pin support
- CMOS, TTL compatible I/O interface for lower power

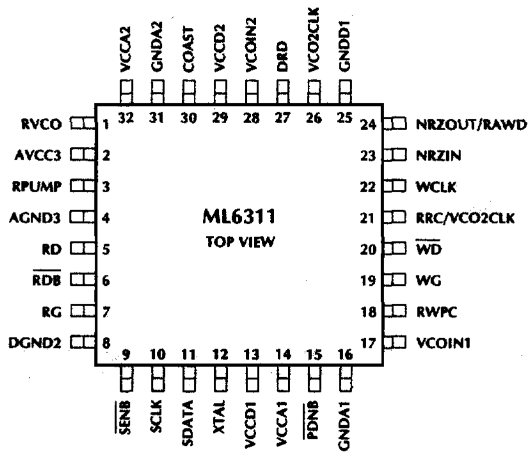
SYSTEM BLOCK DIAGRAM



BLOCK DIAGRAM



PIN CONNECTION



PIN DESCRIPTION

PIN	NAME	FUNCTION
ECL Level Logic Inputs		
5	RD	Encoded read data from the disk drive read channel front-end chip ML6310. The rising edges of RD represent the flux changes on the disk. (differential "+" input)
6	$\overline{RDB}$	Encoded read data from the disk drive read channel front-end chip ML6310. The falling edges of RDB represent the flux changes on the disk. (differential "–" input)
ECL Level Logic Outputs		
(Note: These are test outputs for characterization purposes. External current sources are necessary to provide driving capability for these signals and the ECL buffer needs to be enabled from Control Register #7)		
27	DRD	Delayed read data output after the 1/3rd cell delay. This signal is used for 1/3rd cell delay characterization and window margin test.
26	VCO2CLK	Test point for Data seperator VCO clock output.
CMOS Level Logic Inputs		
7	RG	Read Gate signal from the disk controller. Active high signal indicates read mode. This input selects the phase detector input, switches the RRC output, initiates the data separator PLL acquisition and enables the (1, 7) RLL decoder.
19	WG	Write Gate signal from the disk controller. Active high signal indicates write mode. This input enables the (1, 7) RLL encoder and write precompensation circuits.
30	COAST	A high level on this pin disables phase detector/charge pump of the data separator PLL and allows the VCO to coast.
15	$\overline{PDNB}$	Power Down Control. A low level input on this pin puts the chip in the power down (SLEEP) mode with a power dissipation of less than 100μW.
12	XTAL	A parallel resonant crystal with low parasitic capacitance is connected between this pin and ground as the master clock source. If a crystal oscillator is not desired, an external clock can be forced onto this pin.

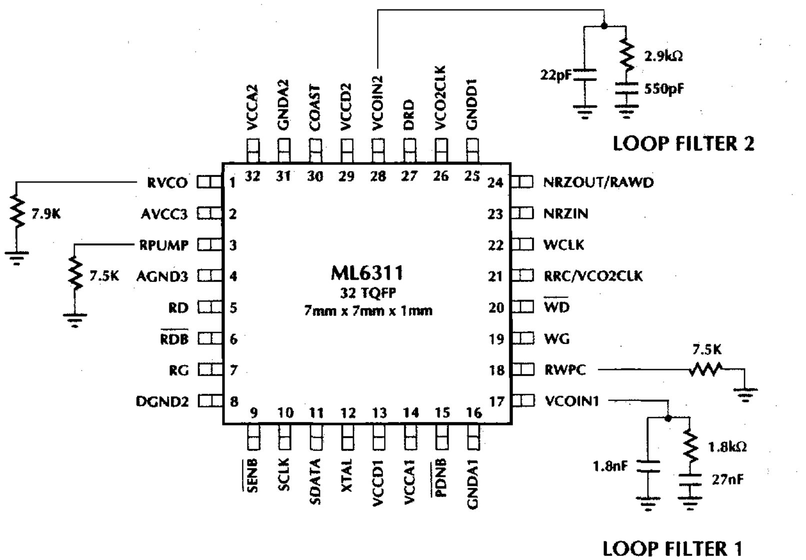
PIN	NAME	FUNCTION
CMOS Level Logic Inputs (continued)		
22	WCLK	Write data clock from disk controller. This is the data rate clock synchronized to the RRC. If minimum cable delay is desired, WCLK pin can be shorted to RRC.
23	NRZIN	Non-return to zero write data input from disk controller. In write mode, NRZIN is clocked into the chip on the rising edges of the WCLK.
9	$\overline{SENB}$	Active low CMOS input — Control Register Enable. A logic low input on this pin allows the SCLK input to clock the SDATA into the control Register and a logic high on this input, latches the control register contents.
10	SCLK	This is a CMOS input which clocks the Control Register. Internally this pin is gated with the $\overline{SENB}$ signal. While $\overline{SENB}$ is low, address and programming data are clocked in at the chip on the falling edges of SCLK.
11	SDATA	Control Register Data, CMOS input, clocked by SCLK.
CMOS Level Logic Outputs		
24	NRZOUT	Non-return to zero read data output. This is the synchronized and decoded data from the disk drive. In the read mode, NRZOUT is clocked out of the chip on the falling edges of RRC. In the external Endec mode (selected through the control register #6 RAW bit), this pin provides the synchronized encoded data output.
21	RRC	Read/Reference clock. In the write mode, this pin outputs 1X (data rate) clock derived from the frequency synthesizer VCO clock. In the read mode, it switches to 1X clock derived from the data separator VCO clock after detecting 19 pulses on the RD line. In the external Endec mode (selected through the control register #6 RAW bit), this pin outputs 1.5X clock (1, 7RLL) and 2X clock (2, 7RLL), derived from the data separator VCO2.
20	$\overline{WD}$	(1, 7) RLL encoded write data output.

PIN DESCRIPTION

PIN	NAME	FUNCTION
Analog Pins		
18	RWPC	A 1% timing resistor for write precompensation delay setting.
4	RVCO	A 1% resistor connected between this pin and GNDA3 sets the current level for data rate programmability.
3	RPUMP	1% resistor connected between this pin and GNDA3 sets the charge pump current for the two PLL's and the bias current for miscellaneous blocks.
17	VCOIN1	Frequency synthesizer PLL charge pump output and VCO input pin. A lowpass filter is connected between this pin and GNDA1.
28	VCOIN2	Data separator PLL charge pump output and VCO input pin. A lowpass filter is connected between this pin and GNDA2.

PIN	NAME	FUNCTION
Power Supplies		
13	VCCD1	2.7V to 5.5V digital supply
29	VCCD2	2.7V to 5.5V digital supply
14	VCCA1	2.7V to 3.6V analog supply for frequency synthesizer. This pin should be left open for 5V operation.
32	VCCA2	2.7V to 3.6V analog supply for data separator. This pin should be left open for 5V operation.
2	VCCA3	2.7V to 3.6V analog supply for miscellaneous functions. This pin should be left open for 5V operation.
25	GNDD1	Digital Ground
8	GNDD2	Digital Ground
16	GNDA1	Analog ground for frequency synthesizer
31	GNDA2	Analog ground for data separator
1	GNDA3	Analog ground for miscellaneous functions

TYPICAL EXTERNAL COMPONENTS



ASSUMPTIONS

$T_S = 1\mu s$ @ $F_{VCO} = 48MHz$

Change pump current = 3X

$K_O = 2400A/S/V$

$\theta_{e,f} = 15\%\ \theta_{e,i}$

$\xi = 0.95,\ \omega_n T = 1.2$

ASSUMPTIONS

$F_{XTAL} = 20MHz$

N + 1 = 20, M + 1 + 48

$K_O = 800A/S/V$

$T_S = 200\mu s$

$\omega_n T = 5$

$\theta_{e,f}$ = 1% of $\theta_{e,i}$

$\xi = 0.6$

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage (VCCA & VCCD) .... –0.3 to +7V
Analog & Digital Inputs/Outputs ...... –0.3 to VCCA + 0.3V
Input Current per Pin .... –25 to +25mA
Storage Temperature .... –65 to +150°C
Maximum Junction Temperature .... 125°C

RECOMMENDED OPERATING CONDITIONS

DC Supply Voltage Range .... 2.7V to 3.6V or 4.5V to 5.5V
For 5V Operation ...... VCCA is left open, VCCD is at 5V
For 3V Operation .... VCCA and VCCD are tied to 3V
Operating Temperature Range .... 0°C to +70°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, VCCA = VCCD = 2.7 to 3.6 volts or 4.5 to 5.5 volts and T_A = 0 to 70°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Dissipation					
Analog Vcc (VCCA)	Left open for 5V operation	2.7		3.6	V
Digital Vcc (VCCD)	Connected for both 3V & 5V	2.7		5.5	V
Analog Supply Current	VCCA = 3.6V, Data Rate = 32 Mbps				
Normal Mode	All circuits operational		37	40	mA
Read Mode	Encoder & WPrecomp OFF		36	39	mA
Write Mode	Data separator and decoder OFF		15	17	mA
PLLFS Mode	Data separator, endec, WPrecomp OFF		14	16	mA
Idle Mode	Only bias circuits & serial interface ON		5	5.5	mA
Sleep Mode	All circuits OFF, register contents retained			10	µA
Digital Supply Current	VCCD = 3.6V, Data Rate = 32 Mbps, C_L < 15pF				
Normal Mode	All circuits operational		16	20	mA
Read Mode	Encoder & WPrecomp OFF		16	20	mA
Write Mode	Data separator and decoder OFF		15	20	mA
PLLFS Mode	Data separator, endec, WPrecomp OFF		9	11	mA
Idle Mode	Only bias circuits & serial interface ON		1.5	2	mA
Sleep Mode	All circuits OFF, register contents retained			10	µA
Digital Supply Current	VCCA = open, VCCD = 4.5V to 5.5V, Data Rate = 32 Mbps, C_L < 15pF				
Normal Mode	All circuits operational			60	mA
Read Mode	Encoder & WPrecomp OFF			59	mA
Write Mode	Data separator and decoder OFF			37	mA
PLLFS Mode	Data separator, endec, WPrecomp OFF			27	mA
Idle Mode	Only bias circuits & serial interface ON			7.5	mA
Sleep Mode	All circuits OFF, register contents retained			20	µA
Digital I/O Specifications					
High level input voltage		VCCD – 0.5		VCCD	V
Low level input voltage		GNDD		0.5	V
High level input current	V_{IN} = VCC			0.1	µA
Low level input current	V_{IN} = GND			0.1	µA
High level output voltage	$\|I_{OUT}\|$ = 2mA	VCCD – 0.5		VCCD	V
Low level output voltage	$\|I_{OUT}\|$ = 2mA			0.4	V
High impedance output current	@ V_{IN} = 100mV & VCC – 100mV	–0.5		0.5	µA

ELECTRICAL CHARACTERISTICS (continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC Characteristics					
Differential Input voltage swing	On ECL input pins RD & RDB	0.8		1.6	V_{P-P}
Psuedo ECL low level output voltage	@ I_{OUT} = 3 mA DRD & VCO2CLK pins	VCCA – 2.05		VCCA – 1.45	V
Psuedo ECL high level output voltage	@ I_{OUT} = 3 mA DRD & VCO2CLK pins	VCC – 1.7		VCC – 1.3	V
Psuedo ECL output swing		0.15	0.25	0.35	V
Low level input current (Psuedo ECL)	Diff V_{IN} = 0V & VCC – 0.7V (RD & RDB inputs)	0.8	1.0	1.3	mA
High level input current (Psuedo ECL)	Diff V_{IN} = VCC – 0.7V & 0V (RD & RDB inputs)	0.8	1.0	1.3	mA
$V_{RD/RDB}$ common mode	Note 1		VCCA – V_{BE}		V
RPUMP bias voltage	RPUMP = 7.5 Kohms (1%)		0.75		V
RWPC bias voltage	RWPC = 15 Kohms (1%) RWPC = 7.87 Kohms (1%)	1.25 0.63	1.5 0.78	1.75 0.92	V V
RVCO resistor	7.87KΩ (1%) recommended	0.6	0.78	0.9	KΩ
Frequency Synthesizer					
Xtal or input frequency	Parallel resonant type with minimum capacitance loading	5		20	MHz
M divider register		1		127	Decimal
N divider register		1		127	Decimal
VCO center frequency dynamic range (f_O)	Measure f_H @ VCOIN1 = 0.7V Measure f_L @ VCOIN1 = 2.3V Dynamic range = $(f_H - f_L)/f_O$	±17	±20		%
VCO gain	$\omega_O = 2 \times \pi \times f_O$, $K_{VCO} = \pi \times (f_1 - f_2)/100mV$ f_1 @ VCOIN1 @ f_O + 100 mV f_2 @ VCOIN1 @ f_O – 100 mV	0.3	0.35	0.4	rad/s-V
Pump current resistor	for setting pump current		7.5		Kohms
Pump current	@ f_O = 48MHz, $I_O = 0.75V/(2 \times R_{PUMP})$	$0.85I_O$	I_O	$1.15I_O$	µA
Phase detector gain	$Kd = (I_O \times 48MHz) / (2 \times \pi \times f_O)$	0.85Kd	Kd	1.15Kd	A/rad
PLL loop gain	$G_O = 3.6 \times 106 / R_{PUMP}$	$0.75G_O$	G_O	$1.25G_O$	A/s x V
PLLFS jitter	RG active, 5V mode, Note 1 RG active, 3V mode, Note 1		200 120	TBD TBD	ps ps

ELECTRICAL CHARACTERISTICS (continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Read Mode and Data Synchronizer					
VCO center frequency dynamic range (f_O)	Measure f_H @ VCOIN2 = 0.7V Measure f_L @ VCOIN2 = 2.3V Dynamic range = $(f_H - f_L)/f_O$	±17	±20		%
VCO gain	$\omega_O = 2 \times \pi \times f_O$, $K_{VCO} = \pi \times (f_1 - f_2)/100mV$ f_1 @ VCOIN1 @ f_O + 100 mV f_2 @ VCOIN1 @ f_O – 100 mV	0.3	0.35	0.4	rad/s – V
Read mode pump current during preamble	@ f_O = 48 MHz, $I_O = (2 \times 0.75V)/R_{PUMP}$ if CPG bit = 0	$0.64I_O$	$0.75I_O$	$0.86I_O$	µA
Normal pump current	@ f_O = 48 MHz, $I_O = (2 \times 0.75V)/R_{PUMP}$ if CPG bit = 0	$0.21I_O$	$0.25I_O$	$0.29I_O$	A
Phase detector gain	$Kd = (I_O \times 48MHz) / (2 \times \pi \times f_O)$	0.85Kd	Kd	1.15Kd	A/rad
PLL loop gain	$G_O = 2.9 \times 106/R_{PUMP}$ (during preamble)	$0.75G_O$	G_O	$1.25G_O$	A/s x V
VCO ZPS error	(zero phase start)	–0.02T – 2		+0.02T + 2	ns
1/3 cell delay accuracy	relative to T/2			±5	%
1/4 cell delay accuracy	relative to T/2, RAW bit = 1 (Reg #6)			±5	%
Decode window centering accuracy				±1	ns
RD input pulse width	t_{WRD}	15		30	ns
RRC duty cycle	WG = 0, RG = 1	40		60	%
PLLDS jitter	Input = 8MHz, sine wave $100mV_{P-P}$, 48MHz encoded clock rate (1 sigma) 5V mode 3V mode		 300 200	 TBD TBD	 ps ps
RRC to NRZout delay	t_{DNRZ1}			5	ns
RG to valid NRZout delay	t_{DNRZ2}		6TRRC		ns
Write Mode and Write Precompensation					
Write precomp accuracy	$t_E = (R_{WPC} \times C \times E/10)$ $0 < E < 7$ $t_L = (R_{WPC} \times C \times L/10)$ $0 < L < 7$ $7.5K < R_{WPC} < 15K$ & C(int) = 0.67pF	$0.8t_E$ $0.8t_L$		$1.2t_E$ $1.2t_L$	ns ns
WD pulse width	$T = 1/f_O$ t_{WWD}	0.6T		1.4T	ns
RRC duty cycle	WG = 1	40		60	%
WCLK to NRZin Hold time	t_{HNRZ}	5			ns
NRZin to WCLK setup time	t_{SNRZ}	5			ns
Serial Microprocessor Interface					
Serial clock (SCLK) frequency		0.01		20	MHz
SCLK pulse width	t_{PW}	40			ns
SCLK to SDATA hold time	t_{HSD}	10			ns
SDATA to SCLK setup time	t_{SSD}	10			ns
SENB to SCLK setup time	t_{SSEN}	10			ns

Note 1. These parameters are guaranteed by design and verified by characterization only and are not part of the production test program, hence only the typical values are indicated for system designer's reference.

TIMING DIAGRAMS

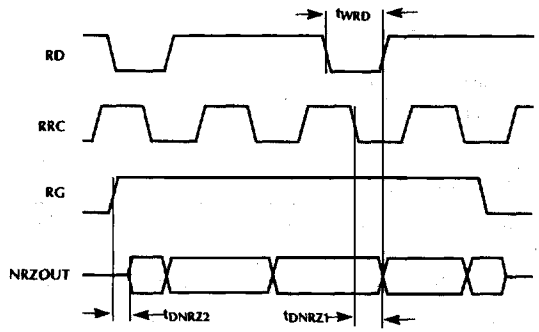


Figure 1. Read Mode Timing

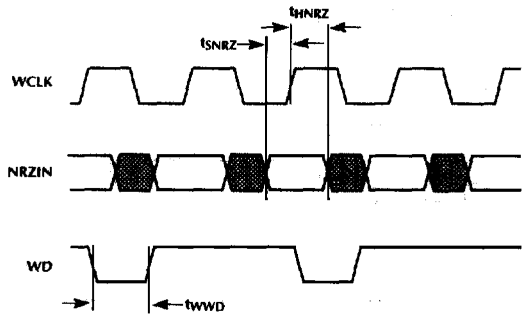


Figure 2. Write Mode Timing

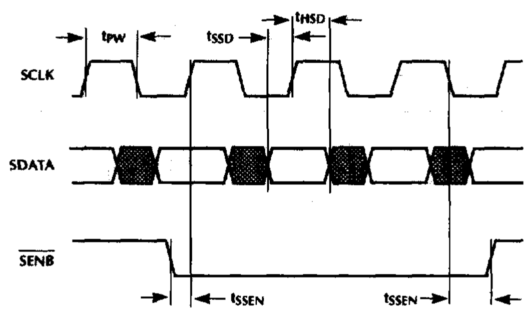


Figure 3. Serial Port Timing

FUNCTIONAL DESCRIPTION

The ML6311 is a BiCMOS Read Channel Back-end Processor IC which is one half of the disk read channel chipset from Micro Linear, intended for the next generation of smaller form factor (1.8" & 1.3") disk drives, operating on 3V and 5V supplies. Fabricated in Micro Linear's BiCMOS process (1.5μ CMOS, 4 GHz ft bipolar), it works in conjunction with the ML6310 Read Channel Front-end Processor to form a complete solution for the low voltage/low power disk read/write channel. It incorporates a full function data synchronizer with a 3:1 operating range, a full function frequency synthesizer with onboard M&N dividers, (1, 7) RLL encoder/decoder and write precompensation circuitry. Bidirectional NRZ I/O can be realized by tying the NRZ Out & NRZ In pins.

The most critical blocks on this chip are the three VCOs, one for the data synchronizer PLL, one for the frequency synthesizer PLL and the third VCO is used to generate the tracking 1/3 cell delay for (1, 7) RLL data synchronization. It also supports a tracking 1/4 cell delay for (2, 7) RLL data synchronization, with an external endec. Careful design considerations have been incorporated to minimize the noise coupling and crosstalk among the VCOs. The highlights of the ML6311 VCO architecture are that it is a fully differential, high speed circuit with built-in switching. It provides a constant amplitude across the frequency span with on-chip timing capacitors. The system noise is highly minimized as the VCO operates at only 1.5X the data rate.

It provides 40-bits for user programmability of a number of features through a serial microprocessor interface and a bank of internal control registers. The control registers come up in an undetermined state on physical power-up and hence need to be initialized, to setup the ML6311 in a known state, on power-up. The control registers will retain their contents in all the power down modes, until power is physically switched off to the chip. The center frequency of the frequency synthesizer VCO is programmed with a 5-bit current DAC. The program information can be provided by the user, or it can be derived from the M & N information. The VCO control current results from the summation of this DAC based coarse control and PLL based fine control. The center frequency of the data separator VCO is programmed by duplicating the control current in the frequency synthesizer VCO as the coarse control. This leaves only the data rate variation to be fine tuned by the PLL, hence implying lower sensitivity and better jitter performance. The VCO3 period is programmed from a 5-bit current DAC, which is in turn referenced to the VCO2 control current. This will vary the 1/2 cycle of VCO3 for the required window centering programmability. Independent early and late write precompensation programmability is provided through a 6-bit decoder array. The external resistor is used to set the time delay for the precompensation.

The ML6311 supports six power down modes for implementation of intelligent power management schemes. An external hardware pin is also provided to implement real time power management. The operating power dissipation is targeted to be less than 170mW, while it will dissipate less than 100μW in the sleep mode. In this mode all sections are powered down except the serial microprocessor interface.

The ML6311 accepts the raw data in a pseudo ECL voltage level, as generated by the ML6310 and provides the synchronized data and clock outputs for the disk controller. Please refer to the block diagram of the ML6311 for the details.

VCO ARCHITECTURE

The most critical circuit blocks in the ML6311 are the three VCOs. The first VCO is used in the frequency synthesizer PLL, the second VCO is used in the data separator PLL and the third VCO is used to generate the tracking 1/3 cell delay for (1, 7) RLL data synchronization or a tracking 1/4 cell delay for (2, 7)RLL data synchronization.

The VCO architecture is optimized to minimize noise coupling from the digital sections of the chip and also the cross talk among the VCOs. The highlights of the VCO architecture are:

- High speed operation with built-in switching mechanism for optimized performance.
- Fully differential circuit configuration to achieve high level of noise immunity.
- On chip timing capacitors to control accuracy and for better noise immunity.
- Constant amplitude across frequency span.
- Symmetrical waveform (~50% duty cycle).

The operating frequency of the VCO is controlled by the tail current of the VCO which consists of two components — a fixed but programmable current (coarse), generated from a DAC which is controlled by the control register #3 and a variable current generated from the PLL. The coarse setting sets the center frequency of the VCO near the operating frequency and the negative feedback around the PLL is used to tune the VCO into the target operating frequency. To minimize the dependence on process and temperature variations the DAC current is derived using an external 1% resistor R_{VCO}. The center frequency is given by the equation:

$$f_O = \frac{m+17}{(16 \times R_{VCO} \times C)}$$

where m = 0 to 31 from control register #3

C = internal capacitor

R_{VCO} = 7.87 kOhms, 1% (recommended)

The architecture of the VCOs is such that they are running at 1.5X the data rate, as opposed to the 3X data rate in the conventional designs used for (1, 7) RLL data streams. This reduces the speed requirements of the circuits and also helps in minimizing crosstalk between the VCOs, thus contributing towards overall system noise immunity. The output of the VCO is sent to a frequency doubler to generate the 3X frequency locally which is then divided by 2 or 3 to generate the synchronized 1.5X and 1X clocks. Zero phase start of the data separator VCO is supported for initial phase alignment.

PLL ARCHITECTURE

There are two PLLs implemented to realize the data separation (for data and clock recovery) and frequency synthesis function (required to support a zoned bit recording (ZBR) implementation). Shown below is a block diagram of the PLL which requires a first order loop filter.

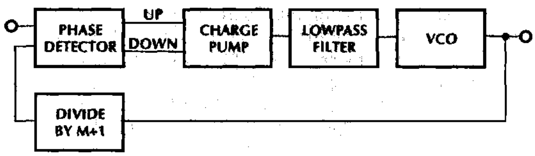


Figure 4. Block Diagram of PLL.

To design the PLL response with a well controlled loop gain value, an external 1% resistor (R_{PUMP}) is used to set the charge pump current according to the bandgap reference voltage generated on chip. The recommended value for Rpump is 7.5kOhms. The capacitor in series with the resistor in the loop filter is chosen so that typically it is 10 times the other capacitor. The resistor is chosen to yield a damping factor between 0.5 and 1 for the acquisition performance of the PLL. The recommended loop filter values are shown in the typical external component diagram.

FREQUENCY SYNTHESIZER PLL

In a ZBR implementation, the disk is divided into a number of zones and the data rate varies from zone to zone. In order to support a ZBR implementation the appropriate frequencies need to be synthesized. VCO1 is used in the ML6311 frequency synthesizer to generate a clock with frequency f_{VCO1}. This is given by the formula:

$$f_{VCO1} = \frac{(M+1) \times f_{XTAL}}{(N+1)}$$

where M and N are 7-bit dividers, programmable through control registers #6, 5, 4. M and N should be at least 1 so that the divide ratio in both the forward and feedback paths are no less than 2, as that 50% duty cycle is guaranteed for the phase compared clocks. In a typical application the users keeps the N at a fixed value and reprograms M from zone to zone to synthesize the required frequency. A 2.5:1 span is required for most applications. The synthesized VCO1 clock is used to derive the encoder clock and the RRC (read/reference clock) for the write operation in ZBR applications. The VCO1 clock is also used to train VCO2 PLL during the non-read mode.

PLL LOOP FILTER DESIGN FOR FREQUENCY SYNTHESIZER

To select the components for the loop filter, two parameters, ξ (damping factor) and ω_n (natural frequency) of the loop characteristic need to be specified.

It is desirable to have the damping factor ξ between 0.5 and 1 to prevent locking to harmonics while maintaining an acceptable lock time. For a high gain, second-order loop this results in minimum noise bandwidth.

The desired natural frequency ω_n of the loop is determined by satisfying the acquisition time (1% maximum phase error after phase acquisition) which is less than the minimum track-to-track seek time. This yields a settling time of approximately $t_S = 5/\omega_n$.

The formulae for the filter components are shown in equations (1) and (2).

$$C_1 = \frac{\frac{K_O}{(M+1)}}{\omega_n^2} \quad (1)$$

$$R = \frac{2\xi\omega_n(M+1)}{K_O} \quad (2)$$

where $K_O = K_D K_{VCO}$ (open loop gain)

The operating frequency F_{VCO} (code rate) is programmed by M&N registers. Equation (3) shows the programming relationship.

$$F_{VCO} = \frac{(M+1)}{(N+1)} F_{XTAL} \quad (3)$$

The value of N should be fixed in the above equation and allow only the M to change for desired operating frequency.

Loop Filter Design Example:

NRZ data rate = 12 to 24 Mbps (1:2 ratio)
Code rate, F_{VCO} = 24 to 48MHz
(assumes (2, 7) RLL code)
F_{XTAL} = 20MHz
Choose N = 19, ⇒ M = 23 to 47
$K_D K_{VCO}$ = 800 A/S/V

Let the loop damping factor, ξ = 0.9 at F_{VCO} = 24MHz to allow ξ to drop at higher frequencies. Let ω_n = 50Krad/s (relatively low frequency, in the order of tens Krad/s for better jitter performance). This value produces a loop settling time = 100µs.

from eqn. (3) M + 1 = 24
from eqn. (1) C_1 = 13.3nF ⇒ $C_2 = C_1/15$ = 880pF
from eqn. (2) R = 2.7KΩ

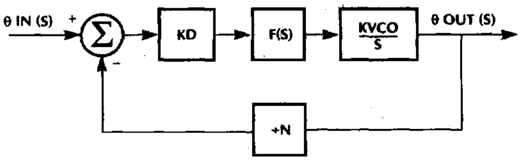
At F_{VCO} = 48MHz, M+1 = 48 which yields ξ = 0.64, and ω_n = 35Krad/s.

DATA SEPARATOR PLL

The center frequency of VCO2 is programmed by duplicating the control current in the VCO1 as the coarse control (control register #3). VCOIN2 thus has to do the fine tuning due to data rate variations (less than several percent), thus implying low sensitivity and good jitter performance. This is an important factor because the data separator PLL has higher bandwidth (of the order of 200KHz) to track the data rate variations and is hence more susceptible to noise induced jitter.

The charge pump has two modes of operation. During the non-read mode, the VCO clock is compared to the frequency synthesizer clock in every cycle, hence the charge pump operates in the low speed mode. After Read Gate is asserted, the charge pump is switched to the high speed mode with (3X CPG = 0) gain and VCO clock is compared to the preamble data on every third clock (assuming 3T preamble pattern for (1, 7) RLL code).

The overall block diagram for the PLL can be described as:



where N = The ratio of the VCO frequency to the input frequency

To select the components for the loop filter, the user needs to consider the following loop requirements:

1. Residual phase error at the end of the preamble should be less than 4% of the total synchronization window (i.e. $\theta_e < 1$ns for $F_{VCO} = 48$MHz or $T_W = 20.8$ns). This implies a large loop bandwidth so that it can quickly obtain lock within a predetermined length of the preamble field.
2. The lock-in range $\Delta\omega_L$ must larger than the expected frequency step change due to variations in disk rotational velocity. In today's technology, the disk rotational velocity can be well controlled within ±1%.
3. The natural frequency ω_n and the damp factor ξ of the loop must be minimized to achieve maximum jitter rejection in the data field. The minimum value for the damping factor ξ will be 0.5 for adequate stability.
4. Re-lock time to the reference clock (frequency synthesizer) must be less than the minimum track-to-track seek time.

It is generally valid to assume the minimum value of wn is dominated by the bandwidth needed during preamble from requirement #1. This assumption will be checked in the design example.

The following loop filter design example assumes:

a. (2, 7) RLL code

b. The PLL encounters a phase offset instead of a frequency offset of the incoming data at the initial lock acquisition. The zero phase start function minimizes the initial phase offset to ±(0.2T + 2)ns where T = synchronization window.

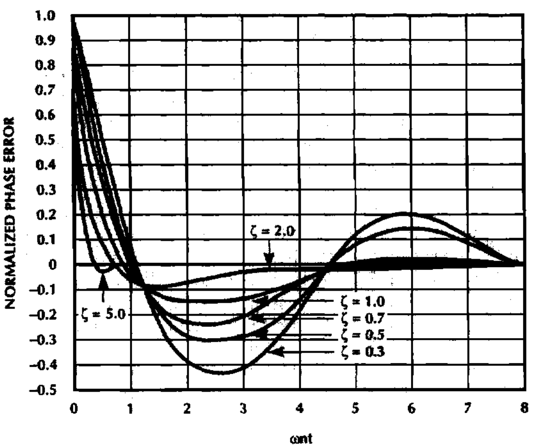


Figure 4. Transient Phase Error $\theta_e(t)$ Due to Step in Phase $\Delta\theta$.

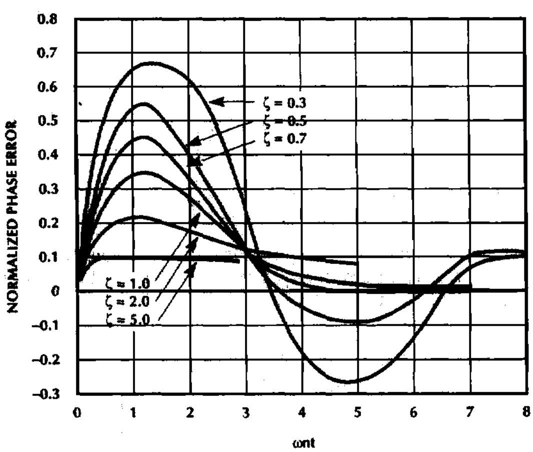


Figure 5. Transient Phase Error $\theta_e(t)$ Due to Step in Frequency $\Delta\omega$.

Since the highest data rate yields the minimum amount of time that the PLL has to settle before decoding data, the settling time is calculated based on the highest data rate.

Loop Filter Design Example:

NRZ data rate = 24MHz
Code rate, F_{VCO} = 48MHz
N_{MIN} = 3 (during preamble, highest recorded frequency)
N_{MAX} = 8 (lowest recorded frequency)
Preamble length = 24 of 3T (100) pattern
TS (settling time of PLL) = 3 x 24 ÷ 48MHz = 1.5µs
Initial phase error $\theta_{e,i}$ = 3ns
Final phase error (after TS) $\theta_{e,f} < 20\%$ of $\theta_{e,i}$
K_O = 3200 A/S/V during preamble

It is desirable to have the damping factor ξ between 0.5 and 1 during acquisition. For a high gain, second-order loop this results in minimum noise bandwidth.

Let the loop damping factor $\xi = 0.8$ to allow ξ to drop at $N \neq 3$
As shown in figure 4, with $\xi = 0.8$, choosing $\omega_n T = 2.4$ the phase error will be at most 20% of the initial phase error. Since $T_S = 1.5\mu s$, $\omega_n = 1.6$Mrad/s.

If the previous assumption is correct, $\omega_n = 1.6$Mrad/s should meet the loop requirements 2 and 4. First, examining requirement #2:

Let the maximum frequency step $\Delta f = \pm 1\%$ of the preamble frequency
$\Delta f = \pm 0.01 \times 48\text{MHz} \div 3 = \pm 160\text{KHz}$
Lock-in range is given by
$\Delta\omega_L = 2\xi\omega_n = 2 \times 0.8 \times 1.6\text{Mrad/s} = 2.56\text{ Mrad/s}$

Thu, Δf_L = 407KHz > 160KHz and requirement #2 is met.

User is encouraged to check that ω_n =1.6Mrad/s durnig preamble does meet the requirement #4.

Recall the equations for determining the filter components:

$$C_1 = \frac{\frac{K_O}{N}}{\omega_n^2} \qquad (4)$$

$$R = \frac{2\xi\omega_n N}{K_O} \qquad (5)$$

from eqn. (4) $C_1 = 417\text{pF} \Rightarrow C_2 = C_1/15 = 28\text{pF}$
from eqn. (2) $R = 2.4\text{K}\Omega$

The above analysis is only shown as an example. The calculated values for filter components are most likely not optimized for all systems using the same data rate, code and preamble.

The coarse center frequency of the frequency synthesizer VCO is programmed with a 5-bit current DAC in conjunction with control register #3. This speeds up the frequency acquisition and also minimizes the VCO sensitivity to V_{VCOIN1} and improves the jitter performance. The synthesized frequency is tuned using the M & N divider information and the crystal frequency, as given by the equation above.

1/3 CELL DELAY & SYNCHRONIZER

The synchronizer circuits align the encoded read data pulses to the data separator VCO clock for the proper decoding of read data. The encoded read data comes in at ECL levels with the timing information embedded in its falling edges. On each rising edge of the encoded read data, the VCO3 is enabled for half of a cycle to generate a DRD (delayed read data) pulse. The falling edges of the DRD pulse enable the phase detector, which operates in phase only mode during read operation, so that the falling edges of the DRD will be phase compared to the rising edges of the VCO2 clock. The falling edges of the DRD are aligned to the rising edges of the VCO2 clock by the negative feedback around the PLL. The rising edges of DRD set the output of the internal data register to a 1, so that the following rising edge of the VCO2 clock will clock it into the synchronizer. After the 1 is clocked into the synchronizer, the internal data register is reset to a 0 and the following VCO2 clocks will clock in 0's to the synchronizer until the data register is set by another read pulse. The VCO3 period is programmed from a 5-bit DAC which is in turn referenced to the VCO2 control current. This will vary the 1/2 cycle of VCO3 for the required window centering programmability (control register #2), while performing a window margin test.

When the RAW bit in control register #6 is set, then this becomes a 1/4 cell delay and the endec is disabled, thus allowing the handling of (2, 7)RLL data. The synchronized data and 2X clock outputs are made available on the NRZOUT and RRC pins.

READ MODE OPERATION OF THE ML6311

When Read Gate (RG) is inactive low, the data separator PLL is locked to the VCO1 clock with the phase detector operating in the phase/frequency mode. The internal multiplexer selects the 1X clock derived from VCO1 clock and outputs it as the RRC (read/reference clock).

When Read Gate (RG) goes active high, the chip enters the read mode. In the read mode the decoder circuits and the NRZOUT signal are enabled. The internal counter starts counting the number of pulses received on the RD/$\overline{\text{RDB}}$ input. After 3 pulses the VCO2 is stopped. VCO2 will restart at the next input transition. The zero phase start circuit eliminates the initial misalignment and speeds up the PLL acquisition. When VCO2 restarts, the phase detector is switched to phase only mode with the input connected to DRD (delayed read data). The phase detector gain is also increased by 3X to ensure that the PLL has enough bandwidth to lock within 16 preamble bytes. After 16 more RD pulses the PLL acquisition is assumed complete. The multiplexer now selects the 1X clock derived from VCO2 clock and outputs it as the RRC (read/reference clock). The decoder then recovers the NRZ data from the RD input and outputs it onto the NRZOUT pin. The data on NRZOUT is clocked out on the falling edges of RRC.

The end of the read operation is signalled by Read Gate going inactive low, which then returns the NRZOUT pin to high impedance and also switches the phase detector input to the VCO1 clock with low gain. VCO2 is stopped again and is restarted, synchronized with VCO1. Circuitry is implemented to ensure a glitchless transition of the clock frequencies on the RRC output.

WRITE MODE OPERATION OF THE ML6311 WRITE PRECOMPENSATION CIRCUITRY

When Write Gate (WG) is asserted active high, the chip enters the write mode. During this mode it clocks in the data on the NRZIN input on the rising edges of WCLK and puts out the (1, 7)RLL encoded write data ($\overline{WD}$). The width of the $\overline{WD}$ pulse is made to track the data rate. Write precompensation can be achieved on this write data if desired. Write precompensation can be bypassed by setting the appropriate bit in control register #0. Write precompensation is implemented through a decoder array and the precompensation current is set through an external resistor, R_{WPC}. The recommended values of R_{WPC} are 7.5KOhm or 15KOhm. The early and late shift values are independently programmed through control registers #1 & #0. Table 1 shows the (1, 7) RLL code mapping table used in the ML6311 and Table 2 shows the write precompensation algorithim.

Table 1: (1, 7) RLL Code Mapping table

NRZ DATA				(1, 7) RLL CODE					
X0	X1	X2	X3	Y1	Y2	Y3	Y4	Y5	Y6
0	0	*	*	X	0	1			
0	1	*	*	0	1	0			
1	0	*	*	X	0	0			
1	1	0	0	0	1	0	0	0	1
1	1	0	1	X	0	0	0	0	0
1	1	1	0	X	0	0	0	0	1
1	1	1	1	0	1	0	0	0	0

Note: X is the complement of the previous code bit

Table 2: Write Precompensation Algorithm

BIT n-1	BIT n-2	BIT n	BIT n+1	BIT n+2	COMPENSATION BIT n
1	0	1	0	1	None
0	0	1	0	0	None
1	0	1	0	0	Early
0	0	1	0	1	Late

Late: Bit n is time shited (delayed) from its nominal time position towards the bit n+1 time position.

Early: Bit n is time shited (advanced) from its nominal time position towards the bit n-1 time position.

POWER MANAGEMENT

The ML6311 provides a hardware pin (PDNB) and three bits in control register #7 for seven levels of micro power management control.

1	1	1	CPG	BUF	PM2	PM1	PM0

The major circuit blocks in the ML6311 comprises of the regulator, the serial interface, VCO1 & frequency synthesizer PLL, VCO2 & data separator PLL, VCO3, synchronizer, decoder, encoder, precompensation circuits, bias circuits and I/O circuits. The PDNB pin in conjunction with the 3 bits in control register #7 can be used to selectively turn off a combination of these blocks depending on the mode of operation. This allows the system designer to turn off sections of the chip that are not in use during a particular sequence of events, thus minimizing power dissipation at a micro management level. Table 3 shows these seven different power down modes and the circuit blocks affected in these different modes. Total typical power dissipation has two components — analog power dissipation which is more or less constant and digital power dissipation which varies with operating data rate.

Table 3: Power down modes in the ML6311 with typical power dissipation

POWER DOWN MODE	SLEEP	IDLE	PLLFS	READ	WRITE	NORMAL	PDWN
PDNB pin	high	high	high	high	high	high	low
Bits PM2,PM1,PM0	000	010	011	100	101	110	XXX
VCO1 and PLLFS	off	off	on	on	on	on	off
VCO2 and PLLDS	off	off	off	on	off	on	off
VCO3, Synchronizer and Decoder	off	off	off	on	off	on	off
Encode & WPrecomp	off	off	off	off	on	on	off
Bias and I/O circuits	off	on	on	on	on	on	off
Serial Interface	on	on	on	on	on	on	on
Typical analog power dissipation @ 2.7V	25µW	14mW	40mW	97mW	41mW	100mW	25µW

SERIAL MICROPROCESSOR INTERFACE

The serial microprocessor interface consists of a simple three-wire serial port. Data is shifted serially into the ML6311 on the SDATA line on the falling edges of the serial shift clock, SCLK, provided the $\overline{SENB}$ pin is active (low). The data is shifted in blocks of eight bits with MSBit first. The internal registers are organized in blocks of eight bits, with the three most significant bits denoting the address, followed by the five data bits. This addressing scheme thus allows for a register bank of eight registers. When the chip is physically powered-up, the control registers come up in an undetermined state and hence they need to be initialized to some preset configuration, so that the behavior of the chip is predictable. The control registers retain their programmed information in all the power-down modes, except when the chip is physically powered-down. When the $\overline{SENB}$ pin goes inactive (high), the SDATA and SCLK pins are ignored and the previously shifted information is latched on the rising edge of the $\overline{SENB}$, into the appropriate register bank based on the address bits. It is recommended that the SCLK input be kept inactive low till such time when it is in use. The SCLK input is capable of handling speeds up to 20MHz.

CONTROL REGISTER DEFINITIONS

The control register bank consists of eight registers with addresses from 0 through 7. Outlined below are the detailed bit by bit definitions of the control registers 0 through 7.

CONTROL REGISTER #0

Write Precompensation Late control

MSB

A2	A1	A0	D4	D3	D2	D1	D0
0	0	0	L2	L1	L0	BYP	REG

BYP = 0 Do not bypass the write precompensation circuitry

BYP = 1 Bypass the write precompensation circuitry

REG = 0 implies regulator is ON (5V Mode)

REG = 1 implies regulator is OFF (3V Mode)

The REG bit applies only in the 3V operating mode, where the regulator should be switched OFF, to minimize power dissipation, as it is not needed. This bit must be set to 0 in the 5V operating mode.

L2	L1	L0	R_{WPC} = 7.5K	R_{WPC} = 15K
0	0	0	0 ns	0 ns
0	0	1	0.5 ns	1.0 ns
0	1	0	1.0 ns	2.0 ns
0	1	1	1.5 ns	3.0 ns
1	0	0	2.0 ns	4.0 ns
1	0	1	2.5 ns	5.0 ns
1	1	0	3.0 ns	6.0 ns
1	1	1	3.5 ns	7.0 ns

CONTROL REGISTER #1

Write Precompensation Early control

MSB

A2	A1	A0	D4	D3	D2	D1	D0
0	0	1	E2	E1	E0	RSVD	RSVD

RSVD = 1 Reserved, must be programmed as a 1, all the time, to ensure proper operation of the chip.

E2	E1	E0	R_{WPC} = 7.5K	R_{WPC} = 15K
0	0	0	0 ns	0 ns
0	0	1	0.5 ns	1.0 ns
0	1	0	1.0 ns	2.0 ns
0	1	1	1.5 ns	3.0 ns
1	0	0	2.0 ns	4.0 ns
1	0	1	2.5 ns	5.0 ns
1	1	0	3.0 ns	6.0 ns
1	1	1	3.5 ns	7.0 ns

CONTROL REGISTER #2

Data separator PLL window centering control

MSB

A2	A1	A0	D4	D3	D2	D1	D0
0	1	0	WC4	WC3	WC2	WC1	WC0

WC4	WC3	WC2	WC1	WC0	VALUE
0	0	0	0	0	–24.0 %
0	0	0	0	1	–22.4 %
0	0	0	1	0	–20.8 %
0	0	0	1	1	–19.2 %
0	0	1	0	0	–17.6 %
0	0	1	0	1	–16.0 %
0	0	1	1	0	–14.4 %
0	0	1	1	1	–12.8 %
0	1	0	0	0	–11.2 %
0	1	0	0	1	–9.6 %
0	1	0	1	0	–8.0 %
0	1	0	1	1	–6.4 %
0	1	1	0	0	–4.8 %
0	1	1	0	1	–3.2 %
0	1	1	1	0	–1.6 %
0	1	1	1	1	0 % (center)
1	0	0	0	0	+1.6 %
1	0	0	0	1	+3.2 %
1	0	0	1	0	+4.8 %
1	0	0	1	1	+6.4 %
1	0	1	0	0	+8.0 %
1	0	1	0	1	+9.6 %
1	0	1	1	0	+11.2 %
1	0	1	1	1	+12.8 %
1	1	0	0	0	+14.4 %
1	1	0	0	1	+16.0 %
1	1	0	1	0	+17.6 %
1	1	0	1	1	+19.2 %
1	1	1	0	0	+20.8 %
1	1	1	0	1	+22.4 %
1	1	1	1	0	+24.0 %
1	1	1	1	1	+25.6 %

CONTROL REGISTER #3

VCO Coarse Center Frequency Control

MSB

A2	A1	A0	D4	D3	D2	D1	D0
0	1	1	CF4	CF3	CF2	CF1	CF0

CF4	CF3	CF2	CF1	CF0	F_O MHZ
0	0	0	0	0	17 MHz
0	0	0	0	1	18 MHz
0	0	0	1	0	19 MHz
0	0	0	1	1	20 MHz
0	0	1	0	0	21 MHz
0	0	1	0	1	22 MHz
0	0	1	1	0	23 MHz
0	0	1	1	1	24 MHz
0	1	0	0	0	25 MHz
0	1	0	0	1	26 MHz
0	1	0	1	0	27 MHz
0	1	0	1	1	28 MHz
0	1	1	0	0	29 MHz
0	1	1	0	1	30 MHz
0	1	1	1	0	31 MHz
0	1	1	1	1	31 MHz
1	0	0	0	0	33 MHz
1	0	0	0	1	34 MHz
1	0	0	1	0	35 MHz
1	0	0	1	1	36 MHz
1	0	1	0	0	37 MHz
1	0	1	0	1	38 MHz
1	0	1	1	0	39 MHz
1	0	1	1	1	40 MHz
1	1	0	0	0	41 MHz
1	1	0	0	1	42 MHz
1	1	0	1	0	43 MHz
1	1	0	1	1	44 MHz
1	1	1	0	0	45 MHz
1	1	1	0	1	46 MHz
1	1	1	1	0	47 MHz
1	1	1	1	1	48 MHz

CONTROL REGISTER #4

Divide by N Control

MSB

A2	A1	A0	D4	D3	D2	D1	D0
1	0	0	N6	N5	N4	N3	N2

CONTROL REGISTER #5

Divide by M Control

MSB

A2	A1	A0	D4	D3	D2	D1	D0
1	0	1	M6	M5	M4	M3	M2

CONTROL REGISTER #6

Divide by M & N and endec control

MSB

A2	A1	A0	D4	D3	D2	D1	D0
1	1	0	RAW	M1	M0	N1	N0

RAW = 0 Onboard (1, 7)RLL endec enabled NRZ data output on NRZOUT and 1X clock output on RRC pins.

RAW = 1 Onboard (1, 7) RLL endec is disabled. Encoded synchronized data on NRZOUT pin and VCO clock output (2X clock) is available on the RRC pin for (2, 7)RLL code.

M & N are given by :

$M = M6 \times 2^6 + M5 \times 2^5 + M4 \times 2^4 + M3 \times 2^3 + M2 \times 2^2 + M1 \times 2^1 + 1$

or

$M = 64 \times M6 + 32 \times M5 + 16 \times M4 + 8 \times M3 + 4 \times M2 + 2 \times M1 + 1$

and

$N = N6 \times 2^6 + N5 \times 2^5 + N4 \times 2^4 + N3 \times 2^3 + N2 \times 2^2 + N1 \times 2^1 + 1$

or

$N = 64 \times N6 + 32 \times N5 + 16 \times N4 + 8 \times N3 + 4 \times N2 + 2 \times N1 + 1$

Note: The 7-bit M & N values are updated (latched) internally only when the most significant bit (M6 or N6) is written to, irrespective of changes in any other bits.

CONTROL REGISTER #7

Power Down Control

MSB

A2	A1	A0	D4	D3	D2	D1	D0
1	1	1	CPG	BUF	PM2	PM1	PM0

BUF = 1 This bit enables the ECL output buffers so that the test signals DRD and VCO2CLK are made available to the user.

BUF = 0 This disables the ECL output buffer. The two pins (ECL output buffer) must be left open for zero power consumption.

CPG = 0 Implies PLLDS Charge Pump Gain is 1X in training mode and 3X in the read mode.

CPG = 1 Implies PLLDS (Data Separator) Charge Pump Gain is 2X in training mode and 4X in the read mode.

Bit configuration for power down modes

PDNB	PM2	PM1	PM0	MODE
1	0	0	0	SLEEP
1	0	0	1	Reserved
1	0	1	0	IDLE
1	0	1	1	PLLFS
1	1	0	0	READ
1	1	0	1	WRITE
1	1	1	0	NORMAL
1	1	1	1	Reserved
0	X	X	X	PDOWN

Note: PDOWN dissipation is the same as SLEEP mode

ORDERING INFORMATION

PART NUMBER	VCC RANGE	TEMPERATURE RANGE	PACKAGE
ML6311 CH2	2.7V to 3.3V	0°C to 70°C	32-pin TQFP (H32)
ML6311 CH3	3.0V to 3.6	0°C to 70°C	32-pin TQFP (H32)
ML6311 CH5	4.5V to 5.5V	0°C to 70°C	32-pin TQFP (H32)